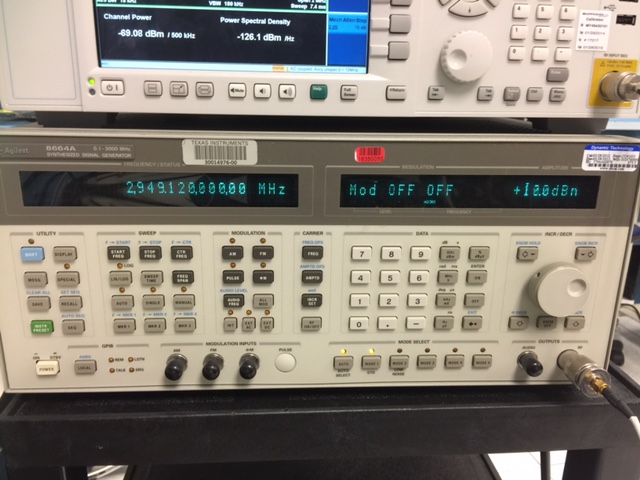
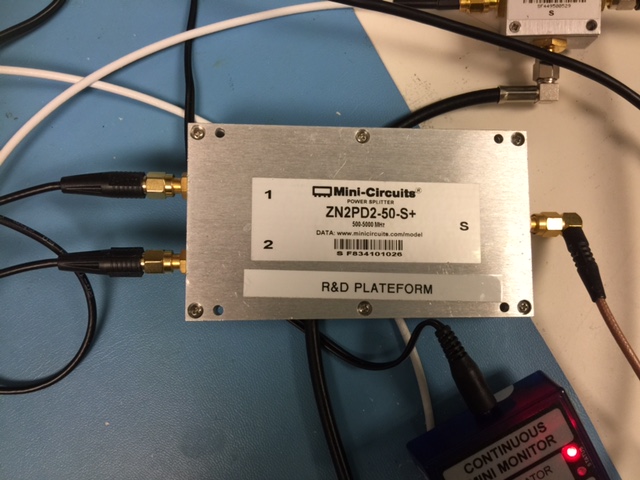
Using external clock for ADC32RF80

For demo4, ADC32RF80EVM requires two synced clock resource to connector J5 and J7 inputs. The clock power level is desired to be 5dBm. DLC which provides clock through J15/J16 SMA connectors give power of -4dBm. Although it works on our system, using external clock from signal generator will exclude the clock power deficiency issue when things are not working.

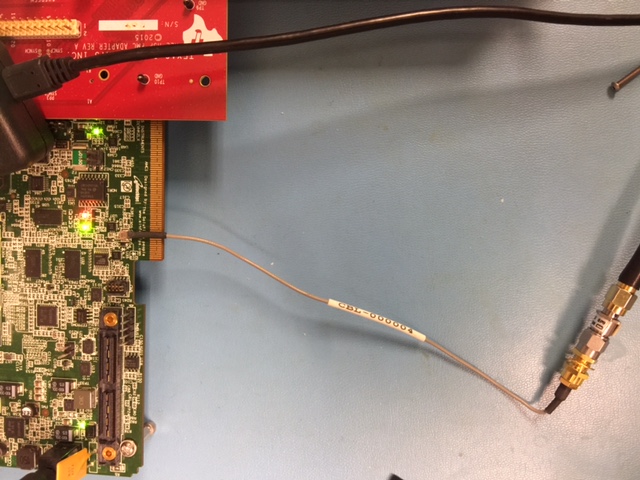
The hardware connection update based on demo4 GSG:

Use signal generator, set freq to 2949.12MHz and power to 10dBm. Connector signal generator output to the S port of power splitter. Connect the power splitter port 1 and 2 to J5 and J7 of ADC32RF80 EVM.





10MHz output (located at the back of the signal generator): connect the 10MHz signal to CN7 of Lamarr EVM. This connection requires U.FL to SMA cable, SMA cable, SMA-BNC connector. Make sure to measure and adjust the power level before connecting to CN7, or it may damage the device on board. On rev3 Lamarr EVM, the resistors are set so that Vref of U37 is 1.2V. A 6dB attenuator is used so that the 10MHz from signal generator reference out is attenuated to +-1Vpp (10dBm).



The rest hardware connection remains the same.

The BMC terminal is used to set the CDC register so that it’s taking 10MHz external clock instead of 19.2MHz onboard clock. The commands are:

>hwdbg cmd show

clkreg 1.1 0x0060

clkreg 1.2 0x05FF

clkreg 1.4 0x208C

To verify that the reference clock is indeed locked, use a splitter at signal generator reference output, one goes into Lamarr EVM, and the other goes into oscilloscope (10MHz\_ref). The 2nd CDC on Lamarr EVM can be programmed to generate 10MHz on CN18/19 (10MHz\_out). The program commands are:

>hwdbg cmd show

clkreg 2.0 0x01B9

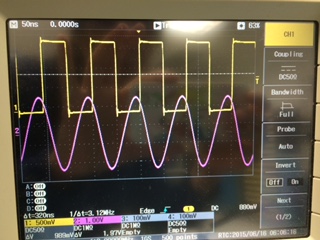
clkreg 2.1 0x017C

clkreg 2.2 0x187C

clkreg 2.4 0x20EC

clkreg 2.18 0x00D3

The 10MHz\_out signal is also sent to oscilloscope. Then both clocks are locked.



The rest of the operation remains the same as GSG.