AM6421 Gateway

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Revision Number

REV	D
VER	1.3

D-Note:-

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

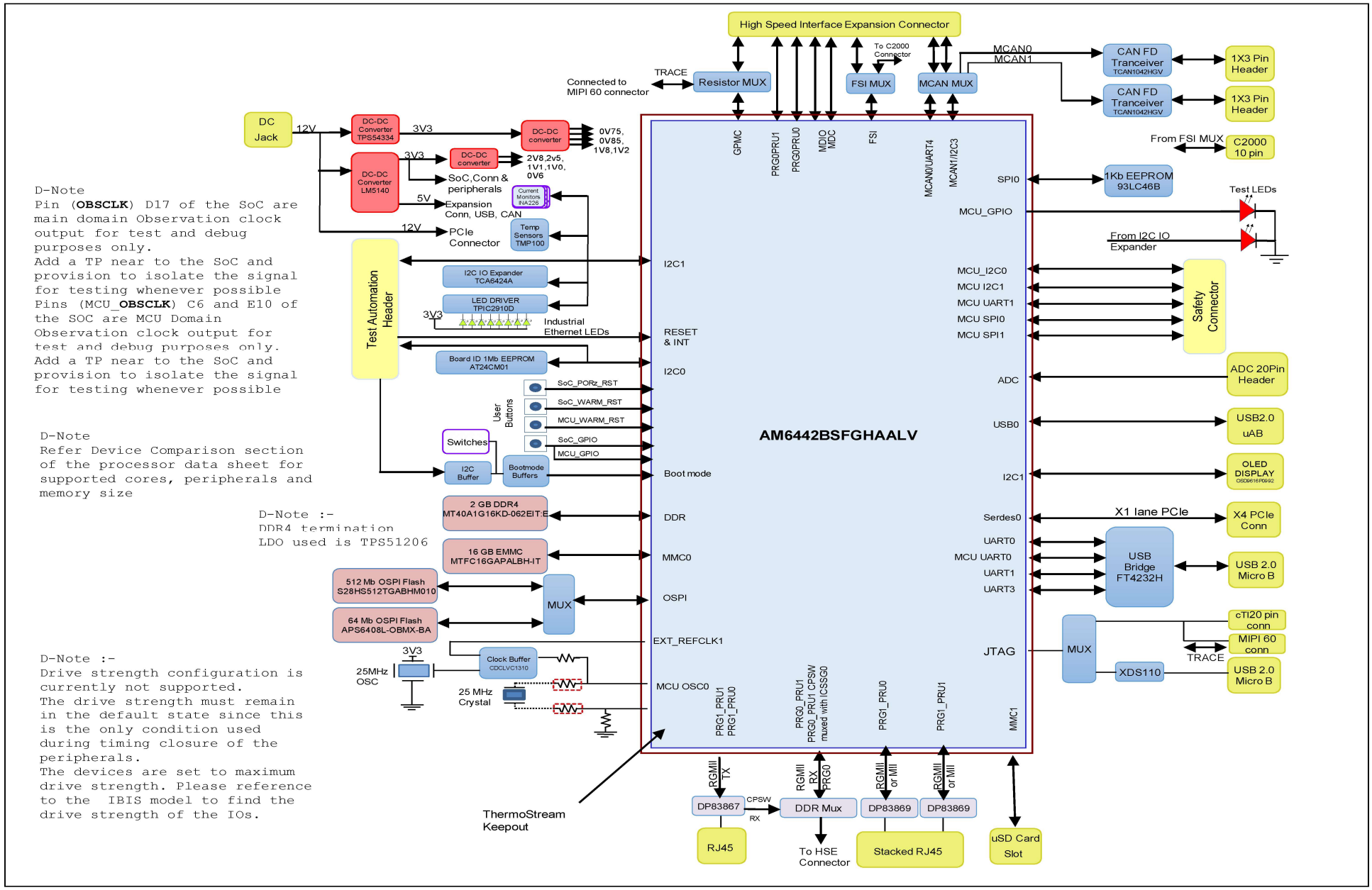
R-Note:-

* Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of board design before board assembly.
* A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor.
* Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details)

KEY LINKS TO COLLATERALS

Hardware Design Guide : https://www.ti.com/lit/an/sprad67a/sprad67a.pdf
Schematic Design and Review Checklist : https://www.ti.com/lit/an/spracu5c/spracu5c.pdf
DDR Board Design and Layout Guidelines : https://www.ti.com/lit/an/spracu1a/spracu1a.pdf
PMIC Power Solutions application note - > Powering the AM64x with the TPS65220 or TPS65219 PMIC https://www.ti.com/lit/pdf/slvafe9
Using LP8733xx and TPS65218xx PMICs to Power AM64x and AM243x Sitara Processors https://www.ti.com/lit/pdf/slda059
EVM/SKs (Starter Kits) for reference : TMDS64EVM, SK-AM64B

BLOCK DIAGRAM_AM64x_EVM



D-Note
Pin (**OBSCLK**) D17 of the SoC are main domain Observation clock output for test and debug purposes only.
Add a TP near to the SoC and provision to isolate the signal for testing whenever possible
Pins (MCU_**OBSCLK**) C6 and E10 of the SOC are MCU Domain Observation clock output for test and debug purposes only.
Add a TP near to the SoC and provision to isolate the signal for testing whenever possible

D-Note
Refer Device Comparison section of the processor data sheet for supported cores, peripherals and memory size

D-Note :-
DDR4 termination
LDO used is TPS51206

D-Note :-
Drive strength configuration is currently not supported.
The drive strength must remain in the default state since this is the only condition used during timing closure of the peripherals.
The devices are set to maximum drive strength. Please reference to the IBIS model to find the drive strength of the IOs.

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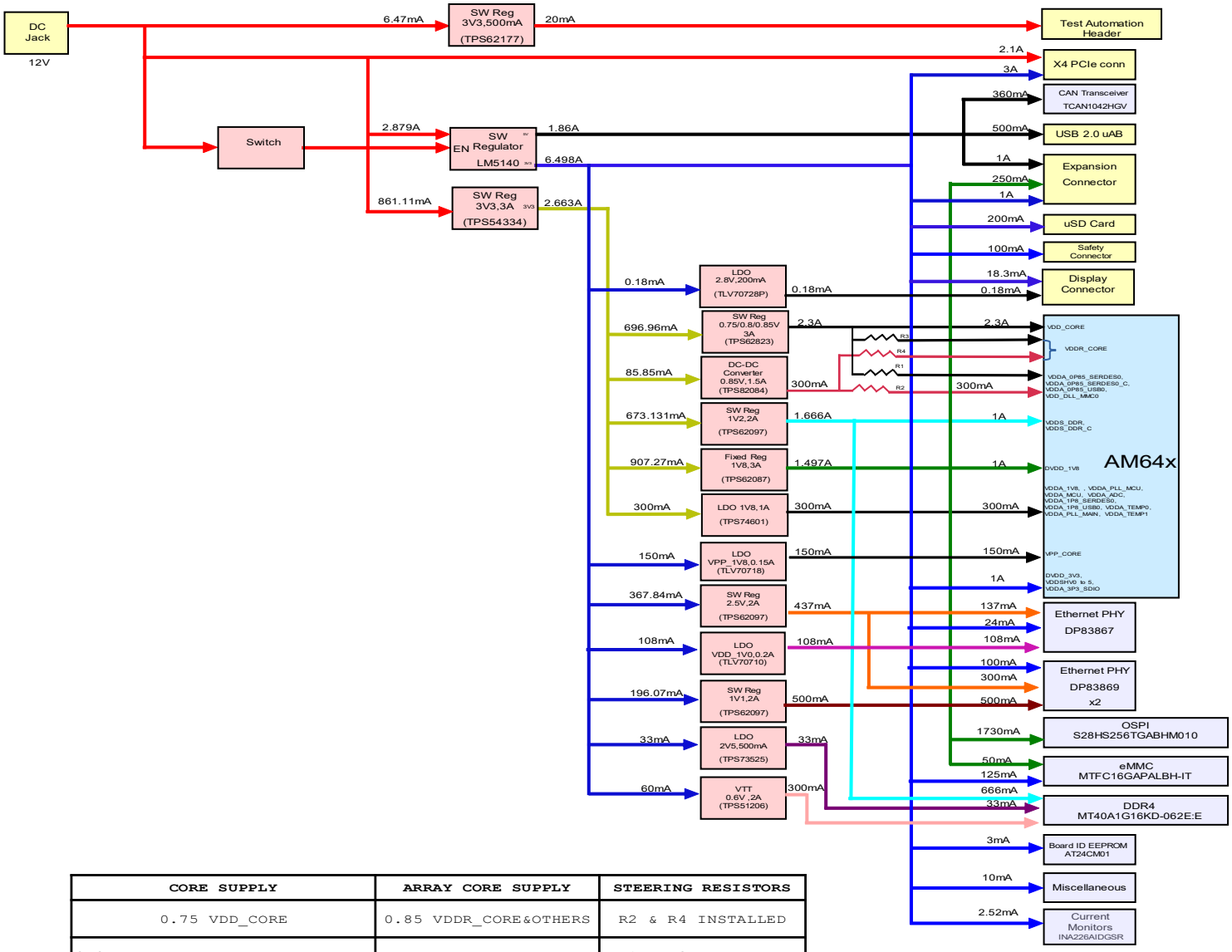
POWER FLOW DIAGRAM



CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

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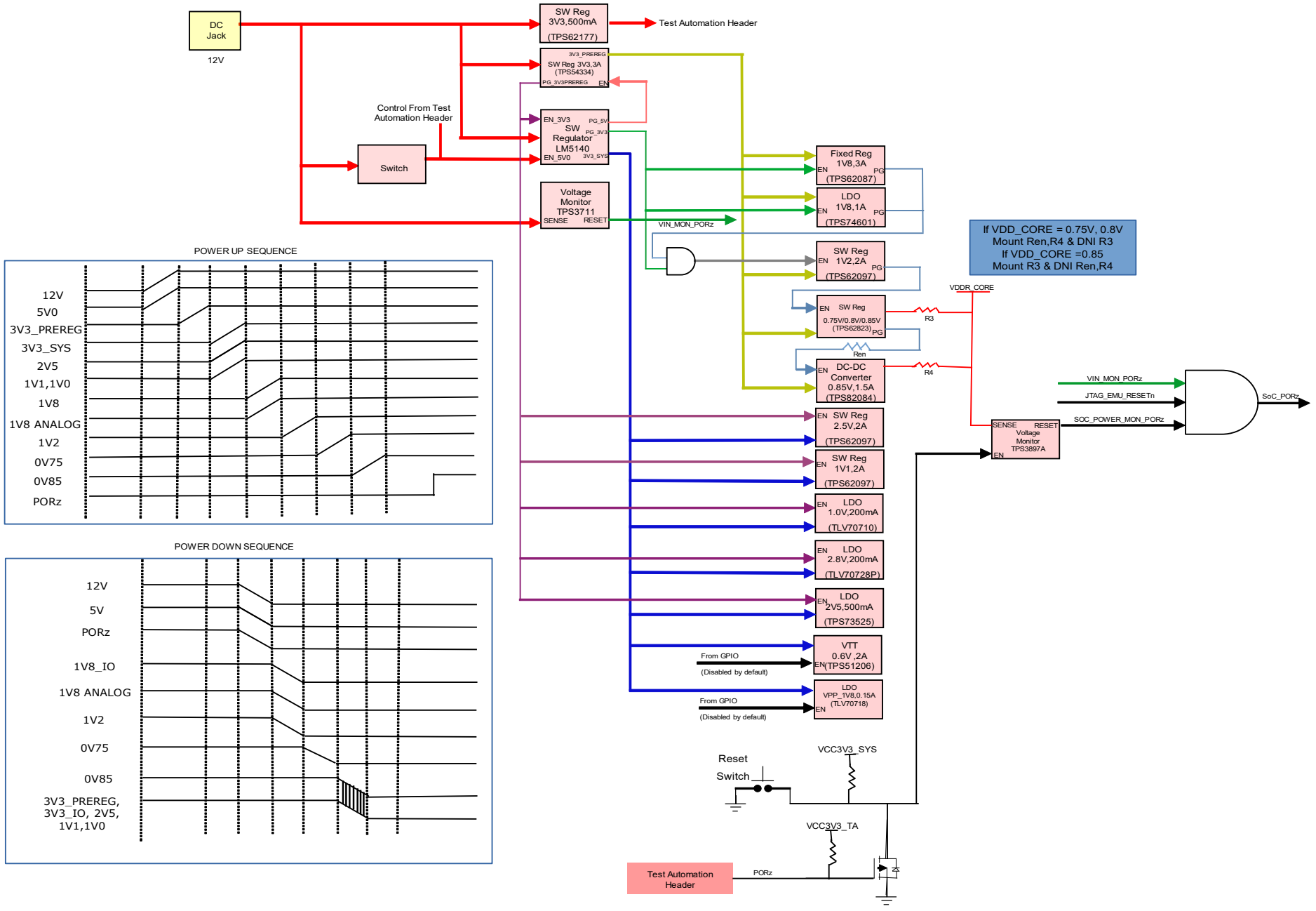
POWER SEQUENCE



POWER UP SEQUENCE

POWER DOWN SEQUENCE

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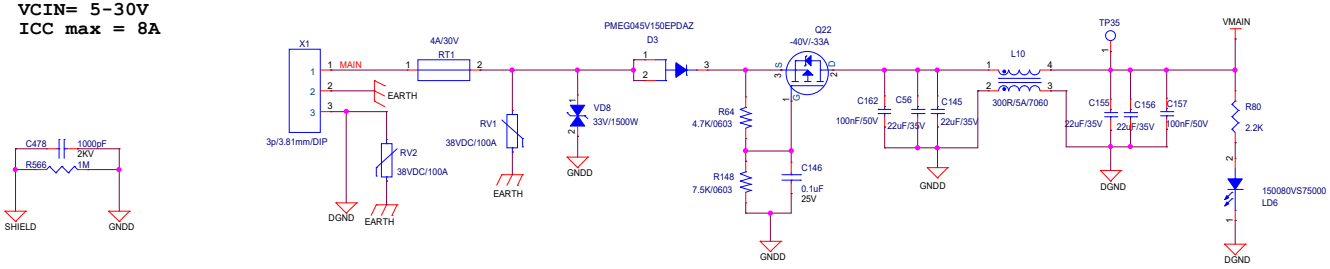
GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPI0_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via 0E res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2Interrupt			Interrupt			INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPI0_PCIe_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Seleection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN tranceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN tranceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Seleection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
18	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPI0_CSn1	OUTPUT	LOW	HIGH
19	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPI0_CS1	INPUT	HIGH	LOW
20	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
21	OLED Display RESET GPIO	GPIO_OLED_RESETn	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
22	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
23	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 01.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
24	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Seleection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
25	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
26	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH
27	One GPIO to enable the PCIe Clock generator outputs	CDC_OE1/E4	GP EVM	Clock output enable	IO EXPANDER- P21		OUTPUT	HIGH	HIGH

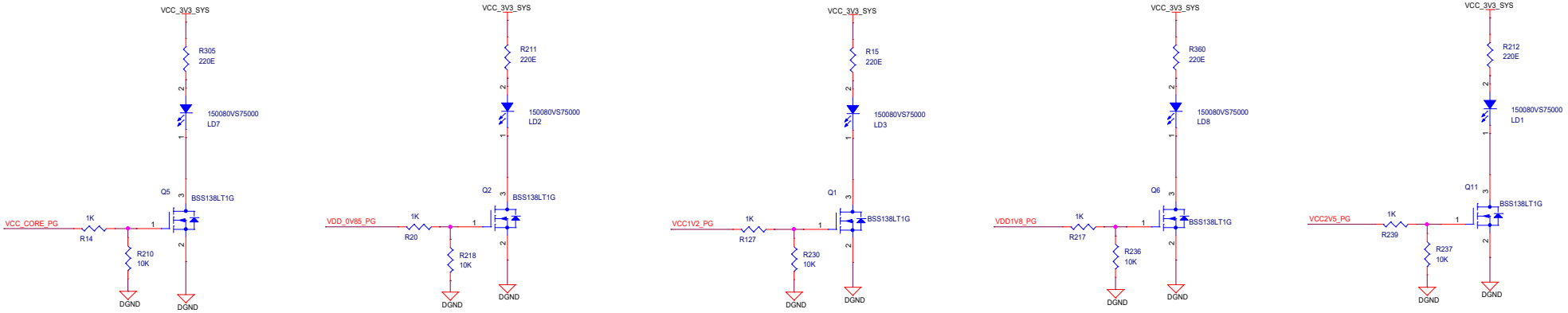
MAIN INPUT 5-30VDC

VCIN= 5-30V
ICC max = 8A



Condition	LED Status(LD1)
Reverse Voltage	ON

POWER INDICATION LED's



Ground test points

Off Page Connections

VCC_CORE_PG
VDD_0V85_PG
VCC1V2_PG
VDD1V8_PG
VCC2V5_PG

VCC_CORE_PG {7,10}
VDD_0V85_PG {10}
VCC1V2_PG {10}
VDD1V8_PG {10}
VCC2V5_PG {8}

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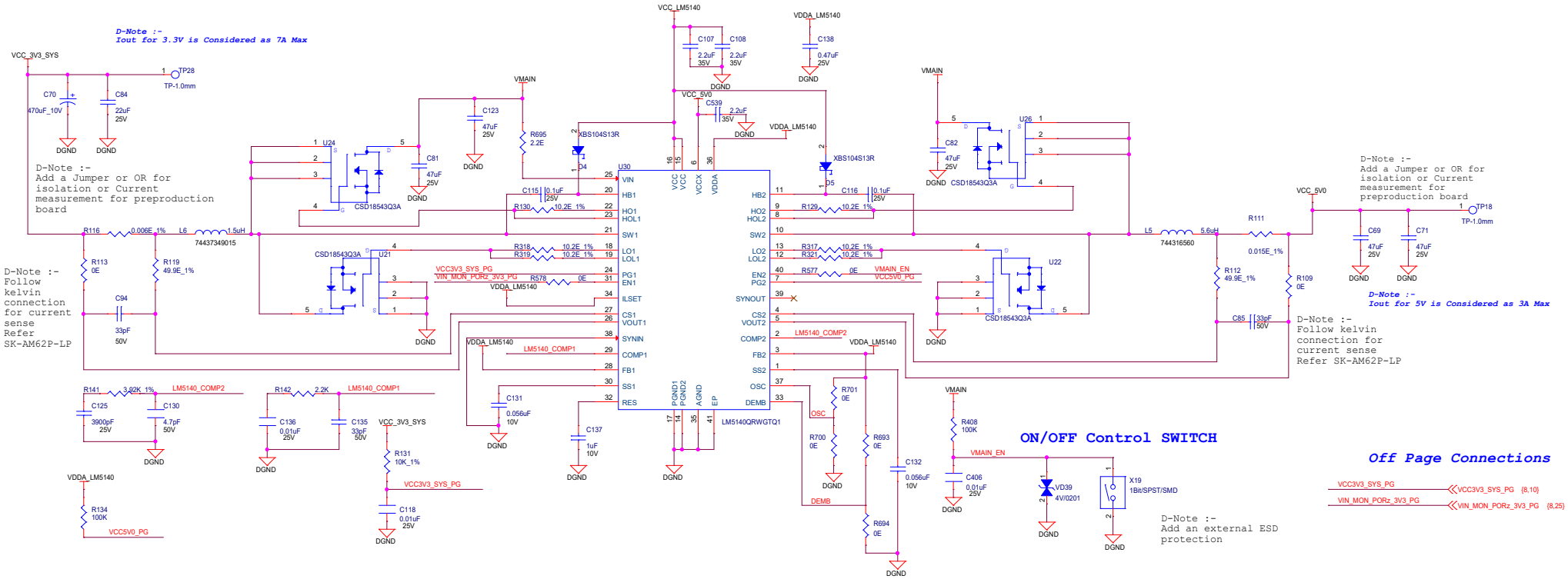
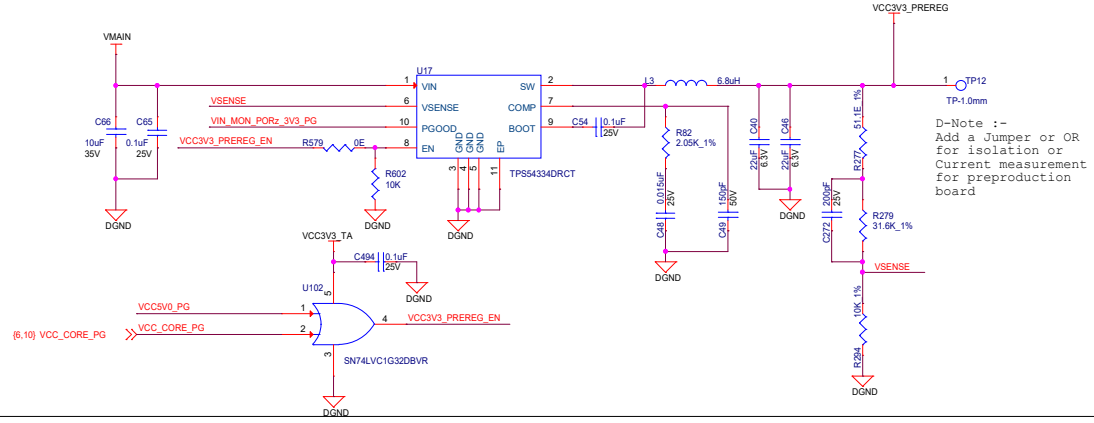
VCC3V3_SYS & VCC_5V0 POWER SUPPLY

5V,3A and 3.3V,7A Dual SUPPLY



PREREG 3.3V, 3.0AMPS SUPPLY



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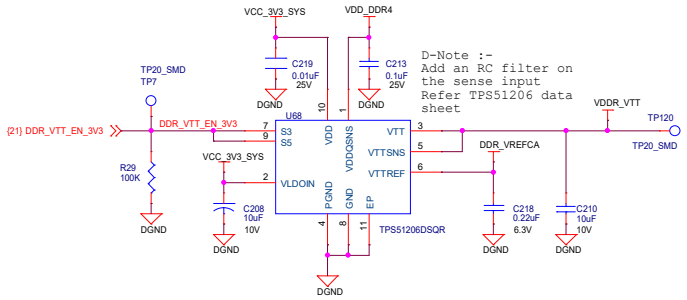
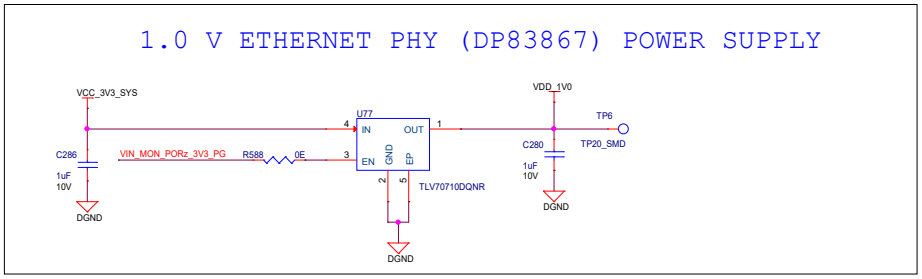
PERIPHERAL POWER SUPPLIES

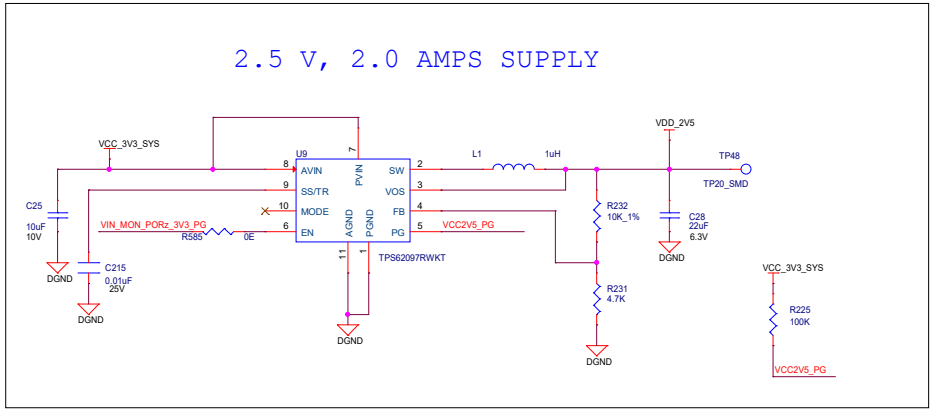
VTT SUPPLY FOR DDR4



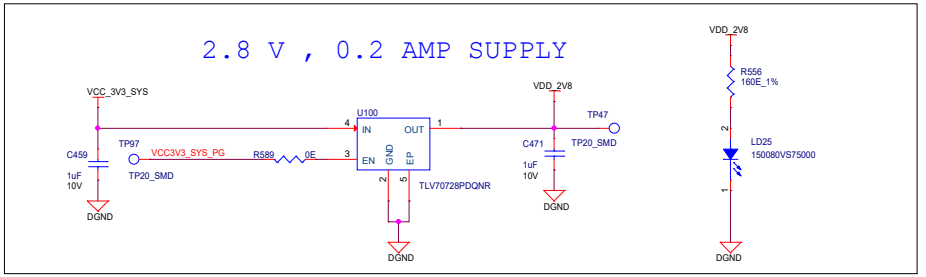
1.0 V ETHERNET PHY (DP83867) POWER SUPPLY



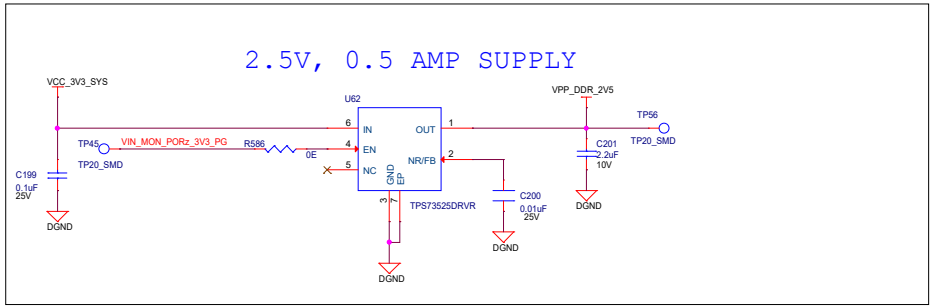
2.5 V, 2.0 AMPS SUPPLY



2.8 V , 0.2 AMP SUPPLY



2.5V, 0.5 AMP SUPPLY



Off Page Connections

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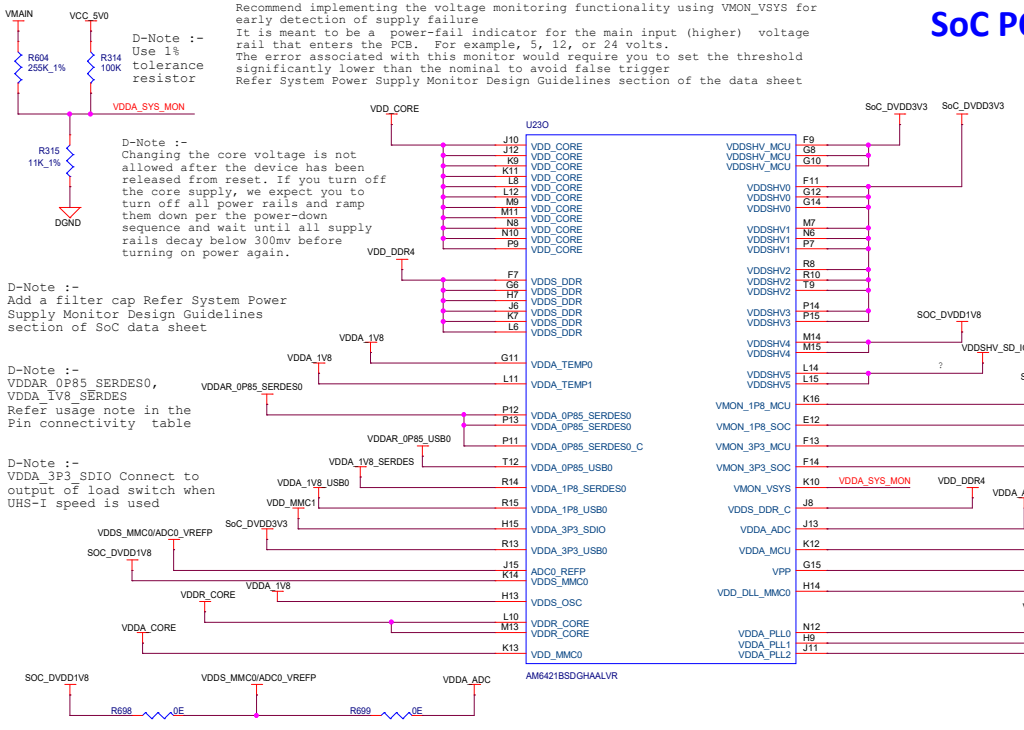
SoC POWER

D-Note :-
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure
It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts.
The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid false trigger
Refer System Power Supply Monitor Design Guidelines section of the data sheet



D-Note :-
Use 1% tolerance resistor

D-Note :-
Changing the core voltage is not allowed after the device has been released from reset. If you turn off the core supply, we expect you to turn off all power rails and ramp them down per the power-down sequence and wait until all supply rails decay below 300mv before turning on power again.

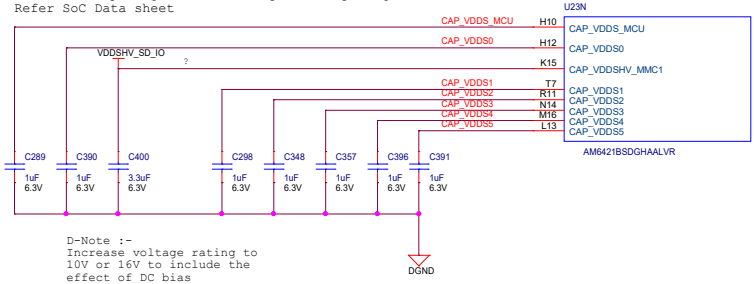
D-Note :-
Add a filter cap Refer System Power Supply Monitor Design Guidelines section of SoC data sheet

D-Note :-
VDDAR_0P85_SERDES0, VDDA_1V8_SERDES
Refer usage note in the Pin connectivity table

D-Note :-
VDDA_3P3_SDIO Connect to output of load switch when UHS-I speed is used

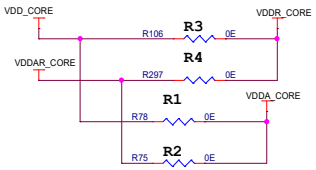
D-Note :-
VDDSHV_SD_IO
Refer pin connectivity table when SD card interface is not used

D-Note :-
Select a capacitor with ESR < 1 O.
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package
Refer SoC Data sheet



D-Note :-
Increase voltage rating to 10V or 16V to include the effect of DC bias

R-Note
Connecting 1.8V supply source directly to VPP continuously is not allowed



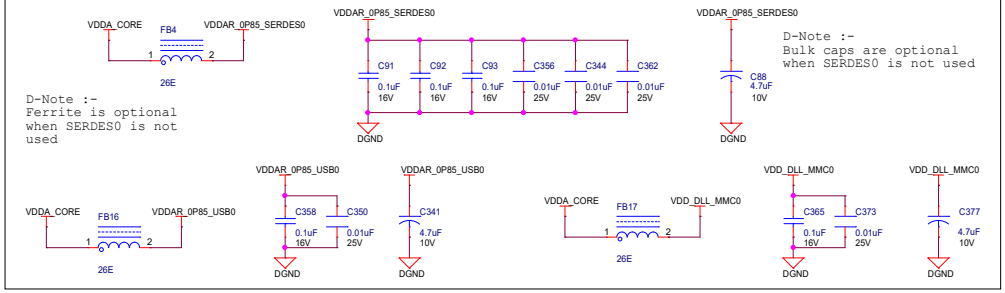
CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

D Note :-
Mount R699 and DNI R698 when SR2.0 Device is used
Mount R698 and DNI R699 when SR1.0 Device is used
Currently shipped device are SR2.0

D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

D-Note :-
A Trace connected to SOC is effectively an antenna that will pick up noise.
A potential will be generated on the signal when noise couples into the antenna.
This potential will be largest on the highest impedance end of the signal.
By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

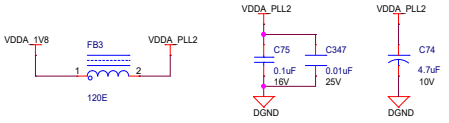
CORE SUPPLY



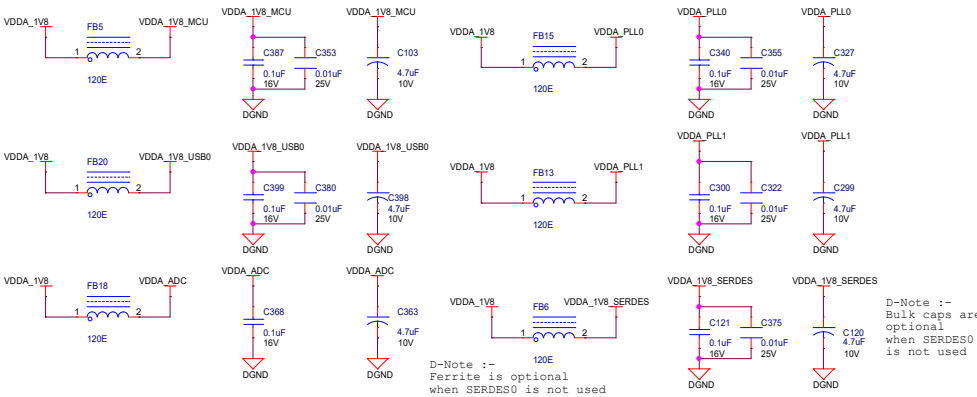
D-Note :-
Ferrite is optional when SERDES0 is not used

D-Note :-
Bulk caps are optional when SERDES0 is not used

1.8V Analog SUPPLY



1.8V Analog SUPPLY



D-Note :-
Ferrite is optional when SERDES0 is not used

D-Note :-
Bulk caps are optional when SERDES0 is not used

D-Note :-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IOs
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

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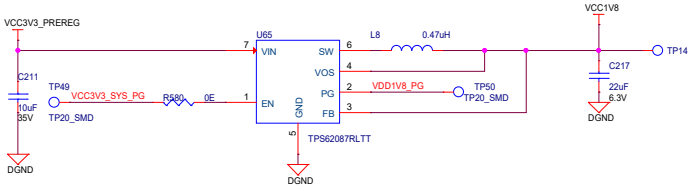
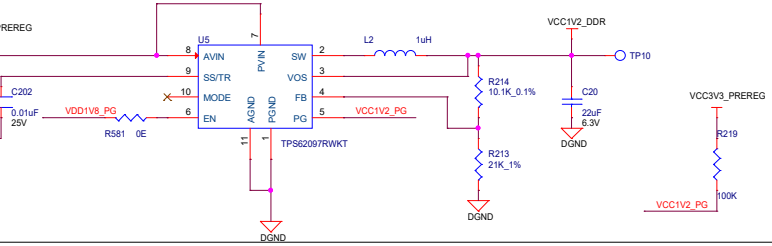
SoC POWER SUPPLIES

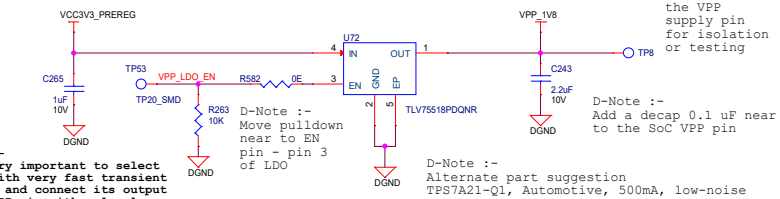
1.8V IO, 3.0 AMPS SUPPLY



1.2V, 2.0 AMPS SUPPLY



1.8V VPP, 0.5 AMP SUPPLY



D-Note :-
Add a series resistor to the VPP supply pin for isolation or testing

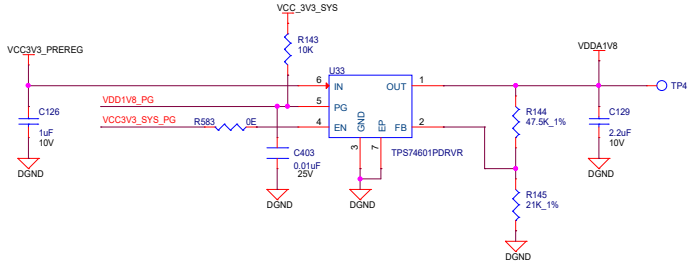
D-Note :-
Move pulldown near to EN pin - pin 3 of LDO

D-Note :-
Add a decap 0.1 uF near to the SoC VPP pin

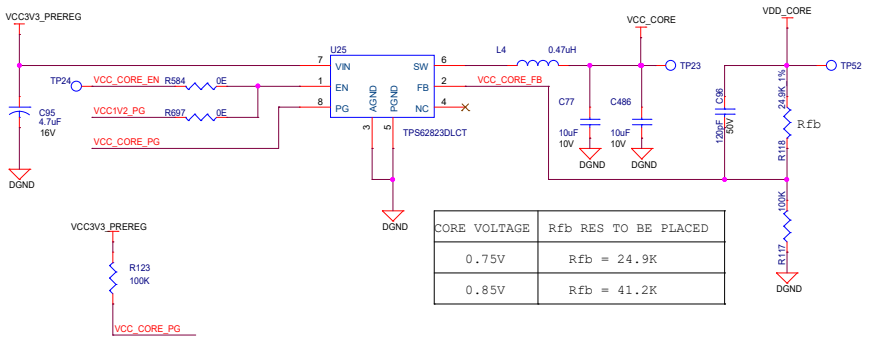
D-Note :-
It is very important to select an LDO with very fast transient response and connect its output to the VPP pin with a low loop inductance path to ensure it is able to source the high transient load, where the VPP pin never drops below the minimum operating voltage.

D-Note :-
Alternate part suggestion
TPS7A21-Q1, Automotive, 500mA, low-noise ultra-low-IQ high-PSRR low-dropout (LDO) voltage regulator

1.8V Analog , 1 AMP SUPPLY

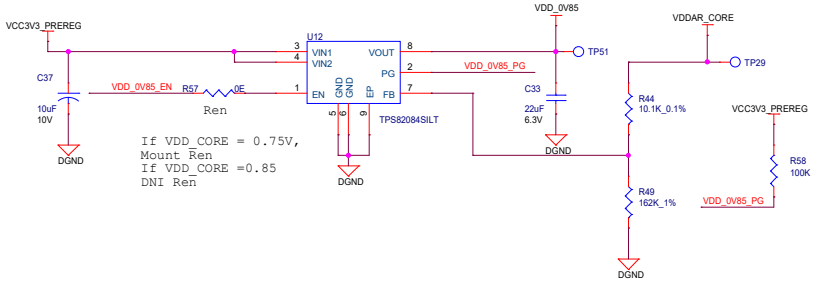


0.75 /0.85V, 3.0 AMPS SUPPLY



CORE VOLTAGE	Rfb RES TO BE PLACED
0.75V	Rfb = 24.9K
0.85V	Rfb = 41.2K

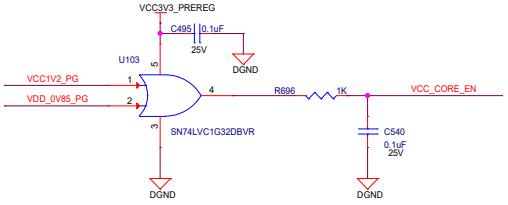
0.85 V, 1.5 AMPS SUPPLY

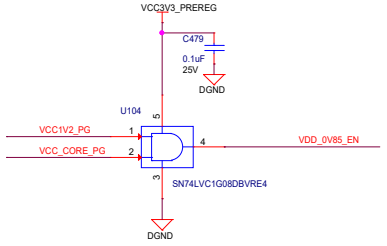


If VDD_CORE = 0.75V,
Mount Ren
If VDD_CORE =0.85
DNI Ren

D-Note :-
An alternative way to source the VPP is to use an external supply. The required caps and termination/Discharge resistor are recommended to be placed near to the SoC VPP pin.
SOC GPIO output can be used to control or time the external power supply output

D-Note :-
Given the transient current requirement during eFuse programming, using load switch or FET switch may not be a recommended approach,
It is recommended to use an LDO. A load or FET switch is likely to have too much voltage drop that can't be compensated like when using an LDO.





Off Page Connections

{6,7} VCC_CORE_PG
{6} VDD_0V85_PG
{6} VCC1V2_PG
{6} VDD1V8_PG
{21} VPP_LDO_EN
{7,8,25} VIN_MON_PORz_3V3_PG
{7,8} VCC3V3_SYS_PG

VCC_CORE_PG
VDD_0V85_PG
VCC1V2_PG
VDD1V8_PG
VPP_LDO_EN
VIN_MON_PORz_3V3_PG
VCC3V3_SYS_PG

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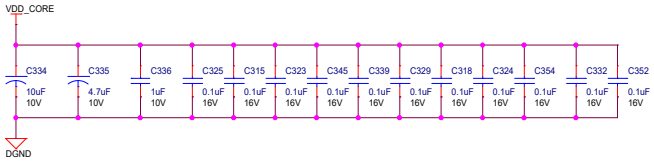
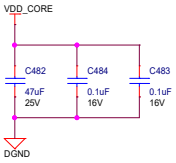
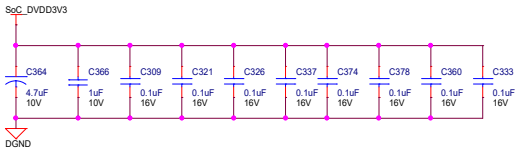
SOC POWER SUPPLIES - DECAPS



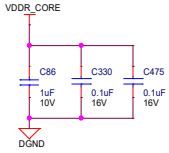
Cad Note :- Place 0.1 uF caps near to SoC pins

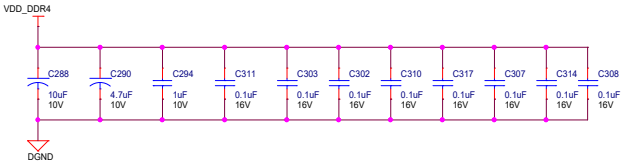


Cad Note :-
To place after current sense resistor on VDD_CORE plane

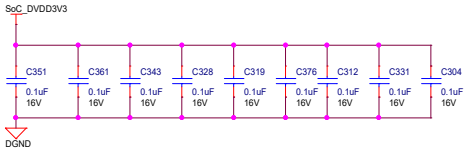


Cad Note :- Place 0.1 uF caps near to SoC pins

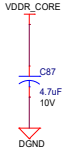




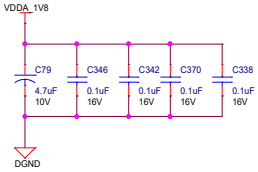
Cad Note :- Place 0.1 uF caps near to SoC pins



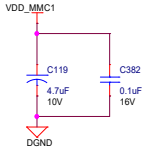
Cad Note :- Place 0.1 uF caps near to SoC pins



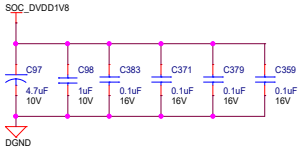
VDD ARRAY CORE

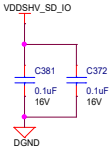


VDDA_3P3_SDIO



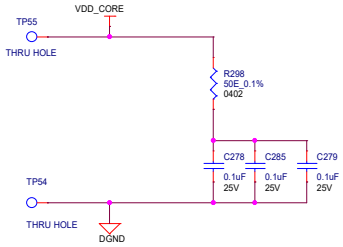
Cad Note :- Place 0.1 uF caps near to SoC pins

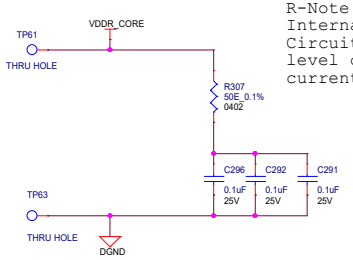




Cad Note :- Place 0.1 uF caps near to SoC pins

Core & Array Core Supply Kelvin Sensing

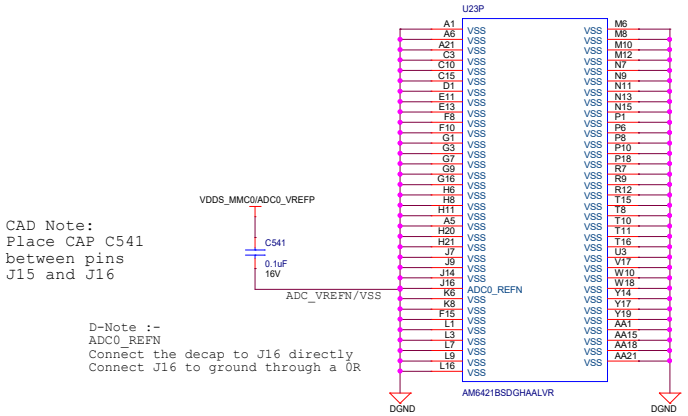




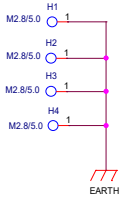
R-Note :-
Internal testing
Circuit for testing of noise level on the low voltage/high current power rails

Uniqgrid	Size: C	CAGE Code: <Cage Code>	DWG NO: <Doc>
	Rev: A		
Scale:		Sheet: 11 of 33	

SoC POWER - VSS

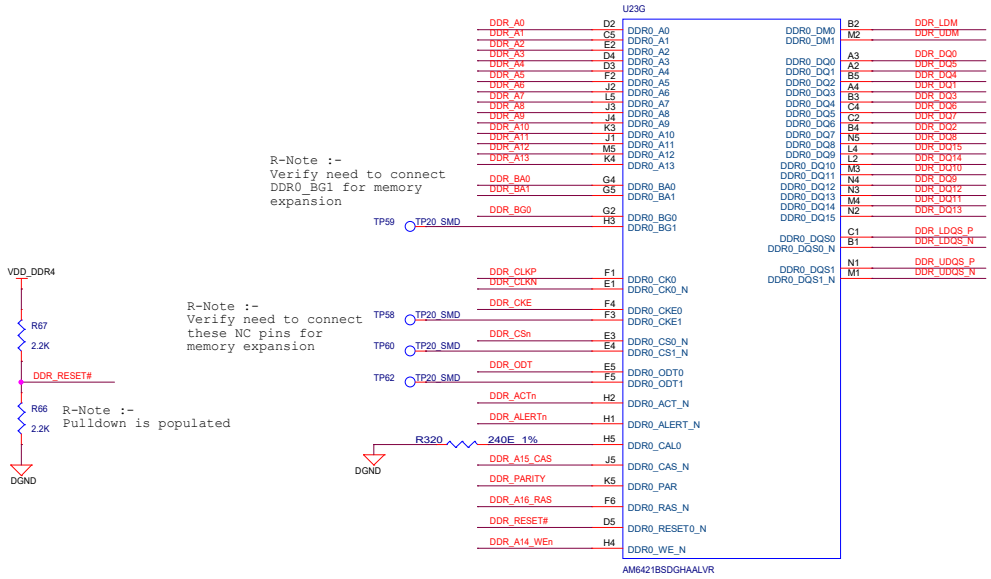


Positioning Hole



Size C	CAGE Code <Cage Code>	DWG NO <Doc>	Rev A
Scale		Sheet 12 of 33	

SoC DDR INTERFACE



R-Note :-
Verify need to connect
DDR0_BG1 for memory
expansion

TP59 TP20_SMD

R-Note :-
Verify need to connect
these NC pins for
memory expansion

TP58 TP20_SMD
TP60 TP20_SMD
TP62 TP20_SMD

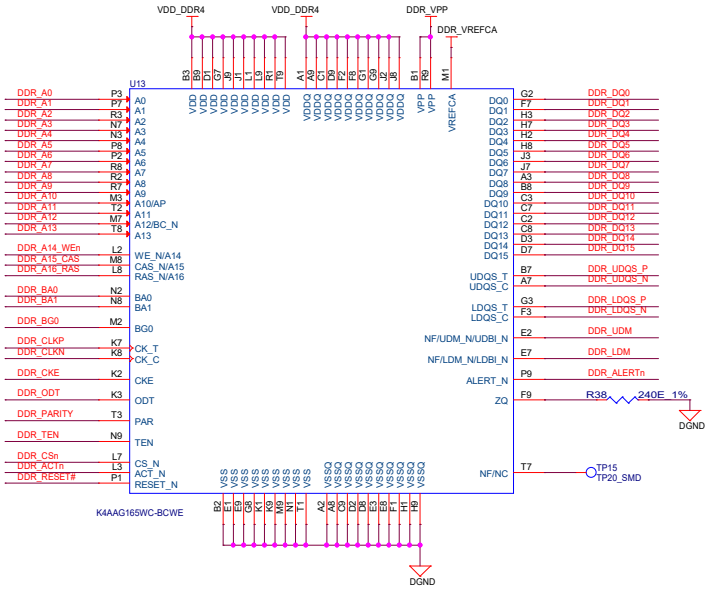
R320 240E 1%

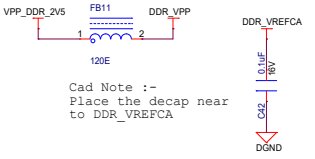
VDD_DDR4
R67 2.2K
DDR_RESET#
R66 2.2K
DGND

R-Note :-
Pulldown is populated

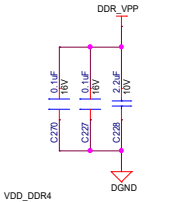
D-Note :-
DDR DQ Lines Swapped With Data Byte

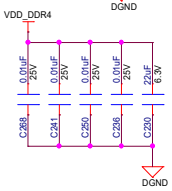
DDR4 DEVICE OK

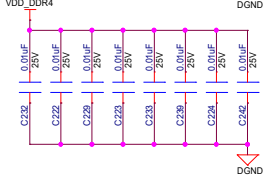




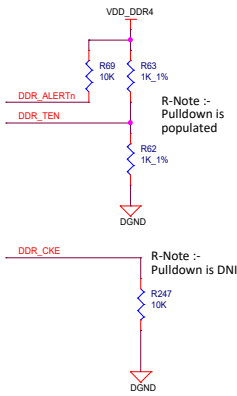
Cad Note :-
Place the decap near
to DDR_VREFCA





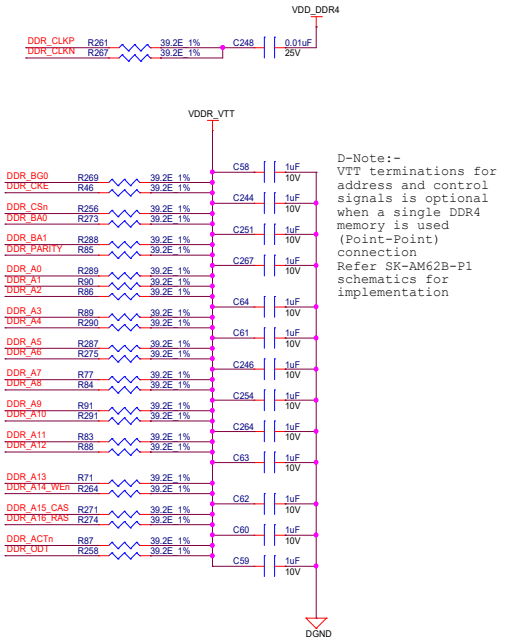


DDR TERMINATION



R-Note :-
Pulldown is populated

R-Note :-
Pulldown is DNI

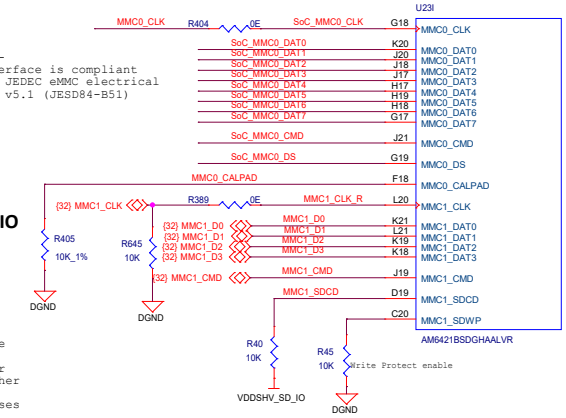


D-Note:-
VTT terminations for address and control signals is optional when a single DDR4 memory is used (Point-Point) connection
Refer SK-AM62B-P1 schematics for implementation

Uniqgrid	Size: C	CAGE Code: <Cage Code>	DWG NO: <Doc>
	Rev: A	Scale:	Sheet: 13 of 33

eMMC FLASH OK

SOC - MMC INTERFACE



D-Note :-
0E provision on MMC0_CLK
Helps improve signal integrity

D-Note :-
MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)

MMC1 used as SDIO (WIFI5 module)

R-Note :-
What is the reason we selected pulldown instead of pullup for EMMC, SD card or other peripherals?
Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

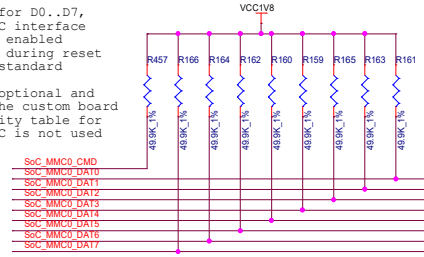
CAD Note :-
Place SOC clock output pulldown resistor near to the clock input pin of the attached (memory) device

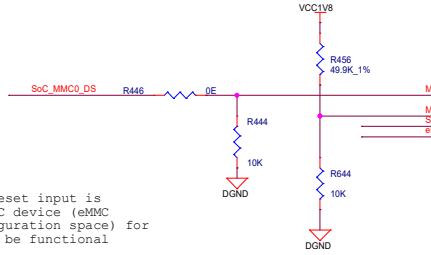
D-Note :-
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or OLDI0 or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

D-Note :-
You could eliminate the GPIO option and only use the reset output (Warm or Cold), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.

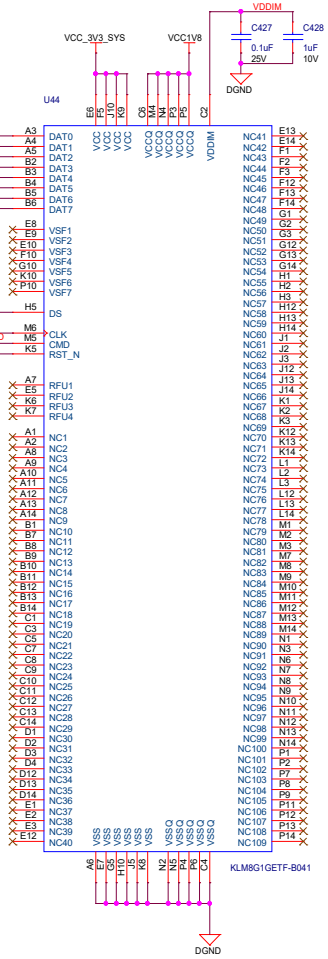
D-Note :-
This family of processor implements a hard and dedicated PHY for eMMC interface.
The pull required for D0..D7, Clock and other eMMC interface control signals are enabled internal to the SOC during reset
Refer pin connectivity table for guidelines when eMMC is not used

D-Note :-
The pulls required for D0..D7, Clock and other eMMC interface control signals are enabled internal to the SOC during reset and are eMMC JEDEC standard compliant
External pullup is optional and can be deleted on the custom board
Refer pin connectivity table for guidelines when eMMC is not used

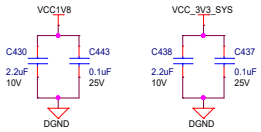




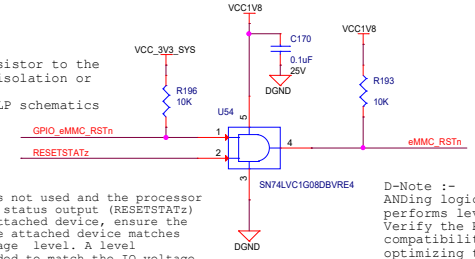
D-Note :-
Ensure eMMC_RSTn Reset input is enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional



D-Note :-
Add additional decaps as required
Refer SK-AM62P-LP schematics



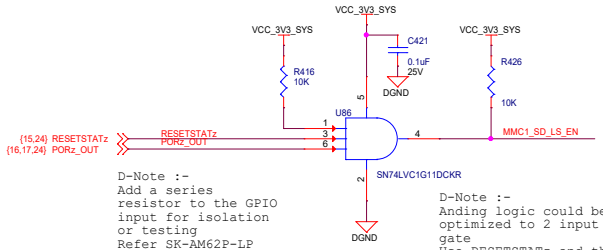
eMMC FLASH RESET



D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

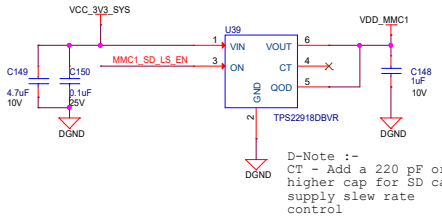
D-Note :-
In case ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is selected. If too high the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If too low it will cause the AM62x to source too much steady-state current during normal operation.

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation



D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

D-Note :-
Anding logic could be optimized to 2 input AND gate
Use RESETSTATz and the SoC IO as inputs



D-Note :-
CT - Add a 220 pF or higher cap for SD card supply slew rate control

Off Page Connections

From & To IO Expander

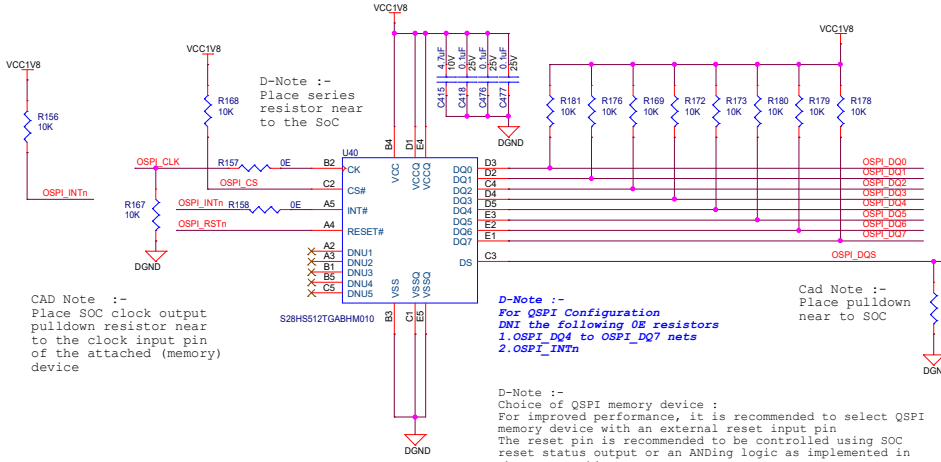
{21} GPIO_eMMC_RSTn >> GPIO_eMMC_RSTn

Size	CAGE Code	DWG NO	Rev
C	<Cage Code>	<Doc>	A
Scale		Sheet	14 of 33

512Mb OSPI NORFLASH

SOC OSPI INTERFACE

R-Note :-
SOC IO buffers are off during power-up. A pullup is recommended near to the attached device, to hold the attached device IOs in a known state.
Use of Pullups are attached device dependent



CAD Note :-
Place SOC clock output pulldown resistor near to the clock input pin of the attached (memory) device

D-Note :-
For QSPI Configuration
DNI the following 0E resistors
1.OSPI_DQ4 to OSPI_DQ7 nets
2.OSPI_INTn

Cad Note :-
Place pulldown near to SOC

R-Note :-
DQS pulldown is enabled
Place pulldown closer to the SoC

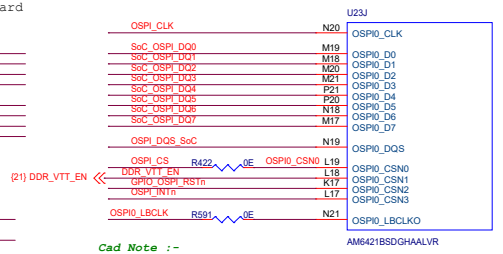
CAD Note :-
Place R600 close to the memory to avoid stub

D-Note :-
Choice of QSPI memory device :
For improved performance, it is recommended to select QSPI memory device with an external reset input pin
The reset pin is recommended to be controlled using SOC reset status output or an ANDing logic as implemented in the starter kit

D-Note :-
These 0R resistors are used for configuring QSPI and OSPI
This is optional during custom board design

Cad Note :-
Place series resistor close to the Memory

D-Note :-
Connecting OSPI interface to multiple devices is not recommended or supported



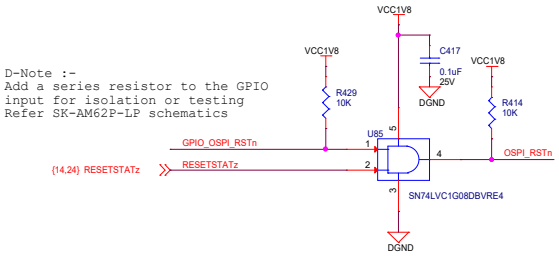
Cad Note :-

Place R591 close to the ball with as little trace as possible

D-Note :-
External loopback clock series resistors are DNI when DQS is connected

To Route DQS to LBCLK0	To Route DQS to SOC's DQS
Mount R591 & R600	DNI R591 & R600

OSPI FLASH RESET

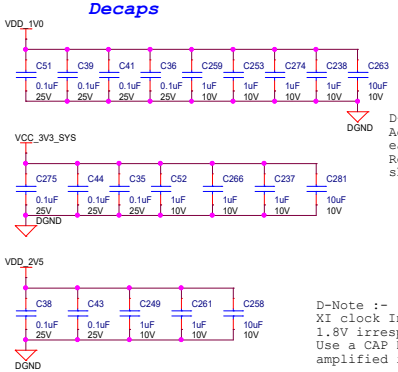


D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

Uniqgrid	Size C	CAGE Code <Cage Code>	DWG NO <Doc> Rev A
	Scale		Sheet 15 of 33

CPSW3G RGMII 1 - ETHERNET PHY

Decaps



D-Note :-
The caps and values used are as per the EPHY data sheet recommendations

D-Note :-
Add 10 nF cap for each supply rail Refer EPHY data sheet

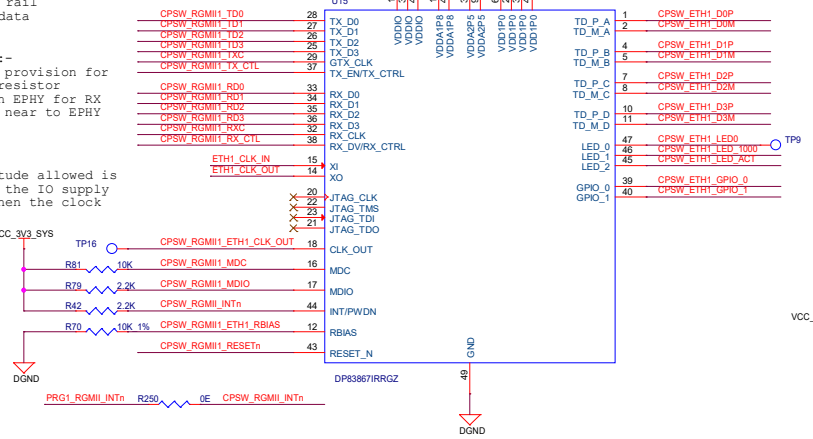
D-Note :-
Provide provision for Series resistor based on EPHY for RX signals near to EPHY

D-Note :-
XI clock Input amplitude allowed is 1.8V irrespective of the IO supply Use a CAP DIVIDER when the clock amplified is 3.3V

D-Note :-
Add a parallel 22 pF cap These changes are for Ethernet compliance test performance improvement

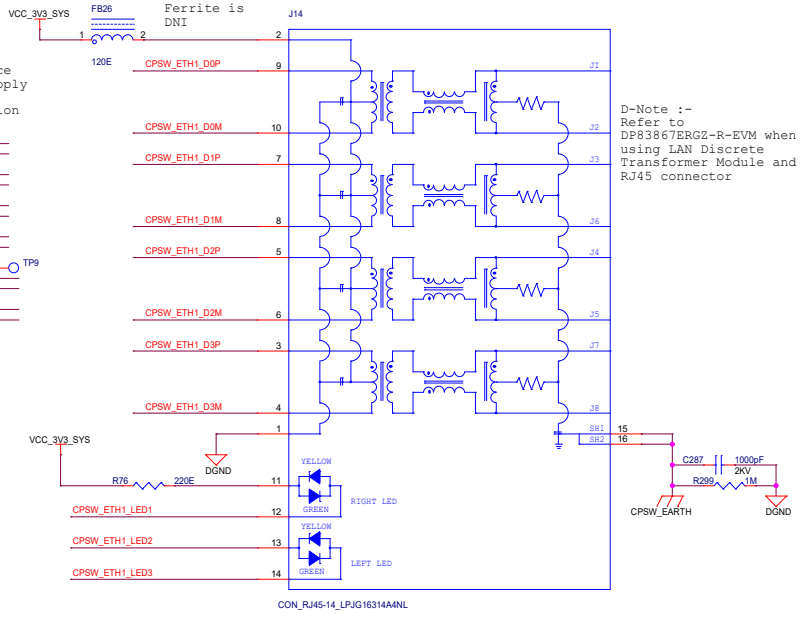
D-Note :-
VDDA1P8 These are LDO outputs Do not short. Add individual TPs for testing

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration



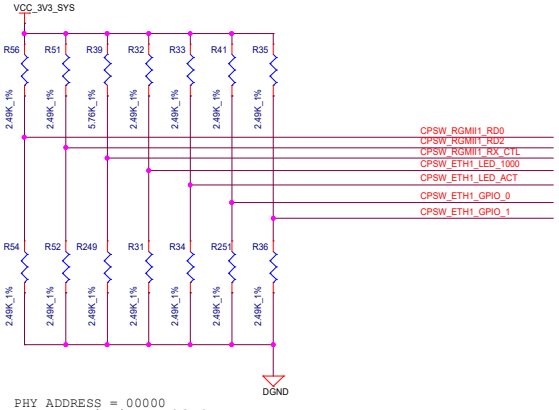
RJ45 with Integrated Mangnetics

R-Note :-
Ferrite is DNI

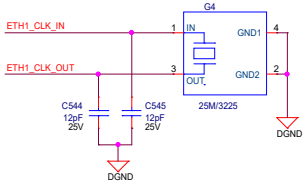


D-Note :-
Refer to DP83867ERGZ-R-EVM when using LAN Discrete Transformer Module and RJ45 connector

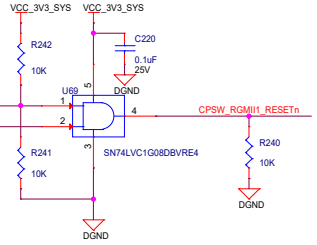
STRAPPING RESISTORS



PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx & Rx Clock Skew = 2.0ns



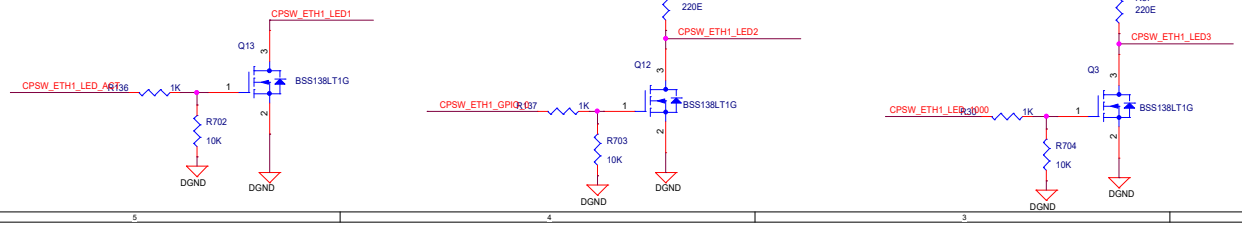
CPSW3G EPHY - 1 RESET



D-Note :-
Add an isolation resistor (0R) to SoC GPIO for debug and testing

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch could cause supply leakage and affect SOC operation

CPSW_ETHERNET PHY- 1 SPEED & ACTIVITY LED 's DRIVERS



Off Page Connections

From Processor

{22} CPSW_RGMII1_RD0 → CPSW_RGMII1_RD0
{22} CPSW_RGMII1_RD1 → CPSW_RGMII1_RD1
{22} CPSW_RGMII1_RD2 → CPSW_RGMII1_RD2
{22} CPSW_RGMII1_RD3 → CPSW_RGMII1_RD3
{22} CPSW_RGMII1_RX_CTL → CPSW_RGMII1_RX_CTL
{22} CPSW_RGMII1_RXC → CPSW_RGMII1_RXC

From Processor

{22} CPSW_RGMII1_TD0 → CPSW_RGMII1_TD0
{22} CPSW_RGMII1_TD1 → CPSW_RGMII1_TD1
{22} CPSW_RGMII1_TD2 → CPSW_RGMII1_TD2
{22} CPSW_RGMII1_TD3 → CPSW_RGMII1_TD3
{22} CPSW_RGMII1_TX_CTL → CPSW_RGMII1_TX_CTL
{22} CPSW_RGMII1_TXC → CPSW_RGMII1_TXC

{14,17,24} PORz_OUT → PORz_OUT
{17,24} PRG1_RGMII_INTn → PRG1_RGMII_INTn

From IO Expander

{16,21} GPIO_CPSW1_RST → GPIO_CPSW1_RST

From Clock Buffer

From Processor

{22} CPSW_RGMII1_MDIO → CPSW_RGMII1_MDIO
{22} CPSW_RGMII1_MDC → CPSW_RGMII1_MDC

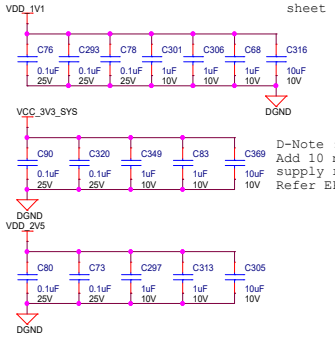
Size C	CAGE Code <Cage Code>	DWG NO <Doc>	Rev A
Scale		Sheet 16 of 33	

ICSSG RGMII 1 - ETHERNET PHY

Dual RJ45 CON With Integrated Magnetics

Decaps

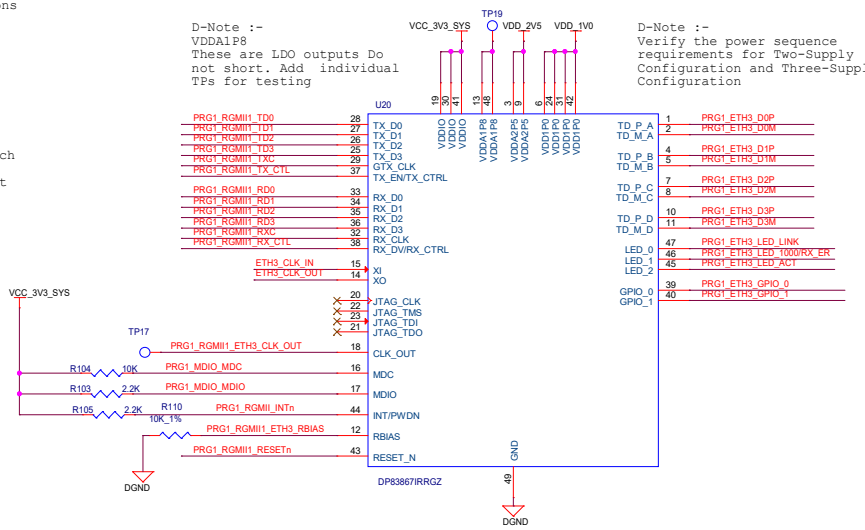
D-Note :-
The caps and values used are as per the EPHY data sheet recommendations



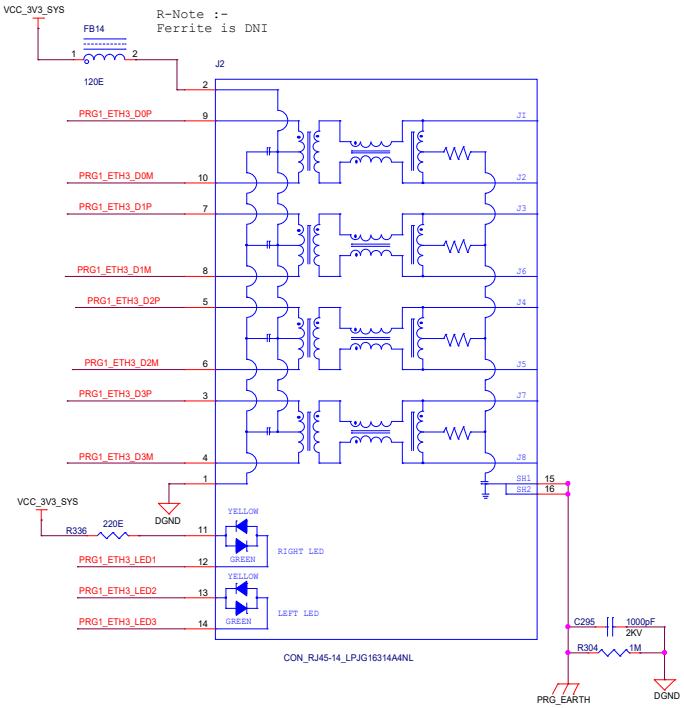
D-Note :-
Add 10 nF cap for each supply rail
Refer EPHY data sheet

D-Note :-
VDDA1P8
These are LDO outputs Do not short. Add individual TPs for testing

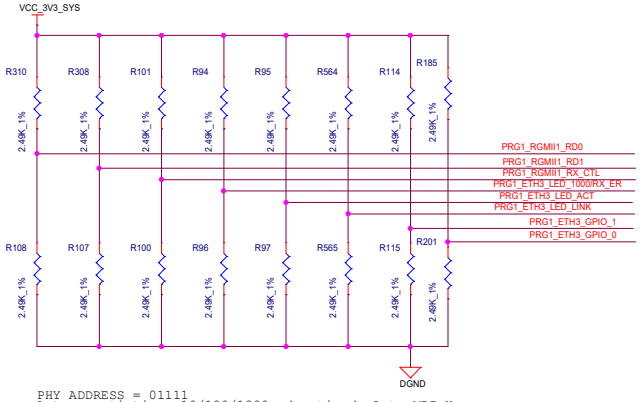
D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration



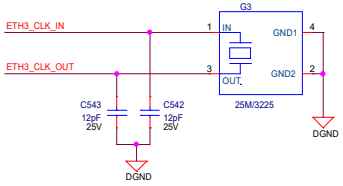
R-Note :-
Ferrite is DNI



STRAPPING RESISTORS



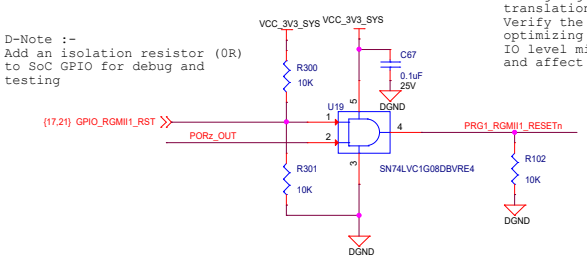
PHY ADDRESS = 01111
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000BaseT/100Base-TX/10Base-Te)



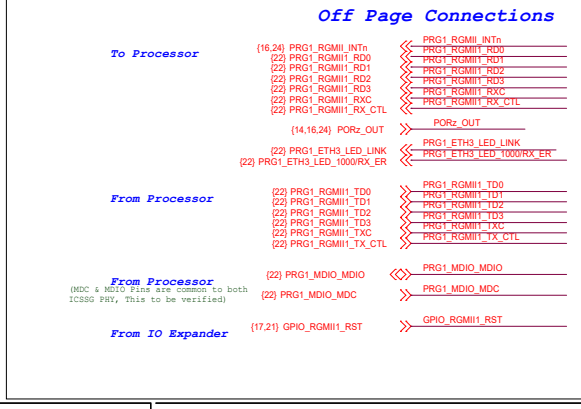
PRG1 (ICSSG) ETH1 RESET

D-Note :-
Add an isolation resistor (0R) to SoC GPIO for debug and testing

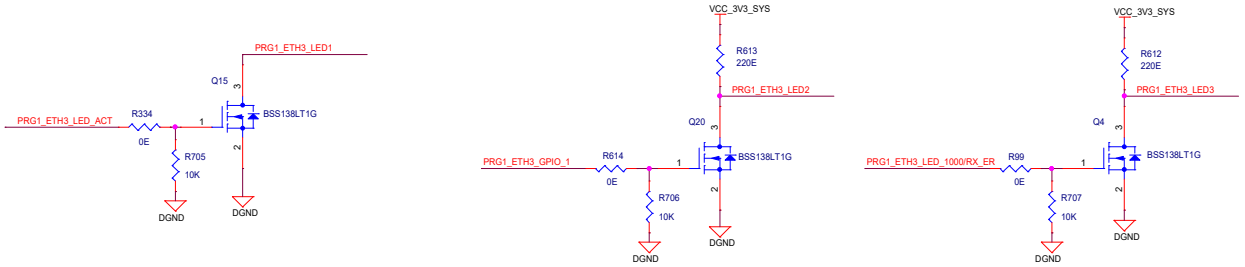
D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation



Off Page Connections



PRG1_ETHERNET - 3 SPEED & ACTIVITY LED 's DRIVERS



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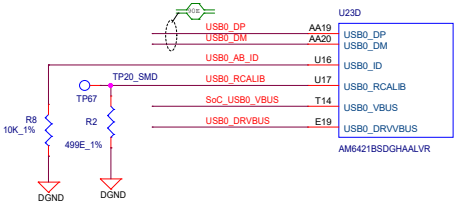
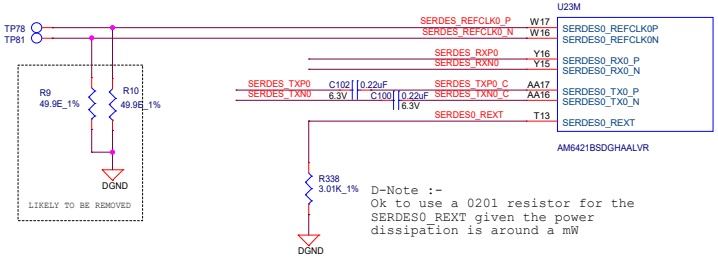
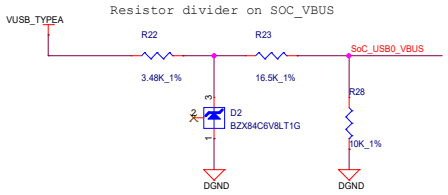
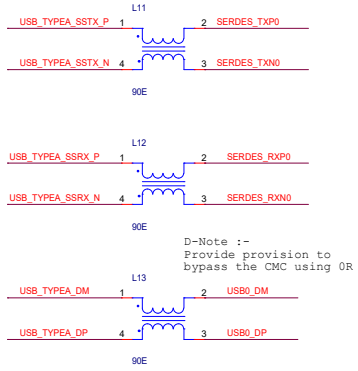
Scale		Sheet	17 of 33



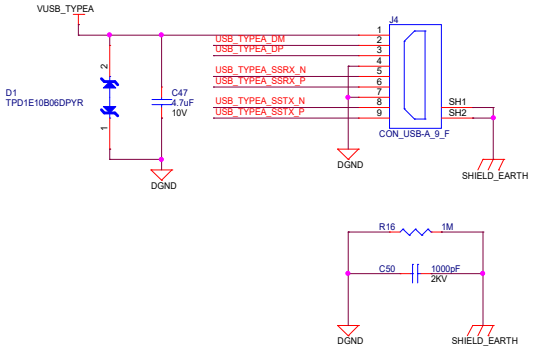




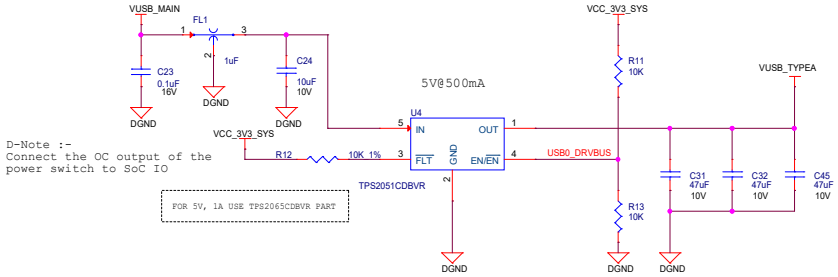
CHOKE



Type-A Connector



5V Power switch for USB 3.0 Device



Off Page Connections

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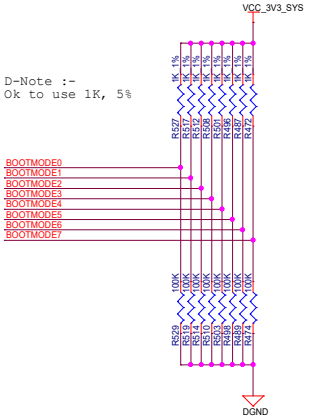
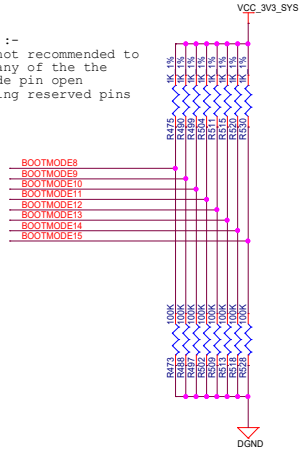
	Rev: A	Scale:	Sheet: 18 of 33

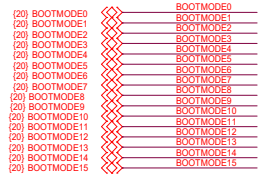
BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES





Off Page Connections

From Processor



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. CPSW Ethernet Slave
5. USB Host
6. USB Device
7. UART
8. Ethernet

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GPMC

D-Note :-
SOC IO buffers for signals used for GPMC interface are disabled during reset
The required pulls for the interfaced signals are provided on the GPMC interface card

D-Note :-
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot
Shorting the bootmode pins directly to VCC or ground directly is not recommended
Connect each of the bootmode pins through separate resistor
Choose the bootmode resistor value based on the use case (10K or similar)

D-Note :-
Add a series resistor 0R when used as GPMC0_CLK

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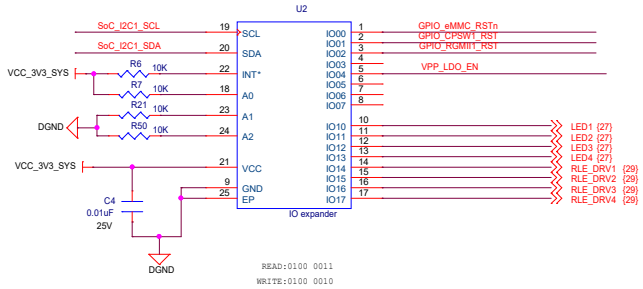
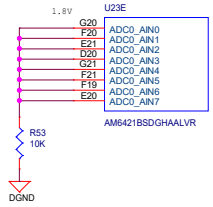
	Rev: A		
	Scale:		Sheet: 20 of 33

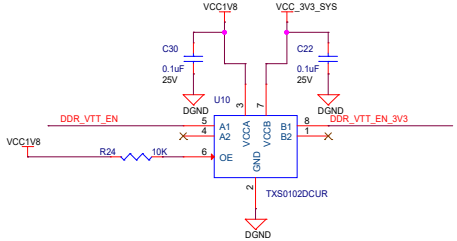
IO EXPANDER



ADC



LEVEL TRANSLATOR



Off Page Connections

GPIO_eMMC_RSTn → GPIO_eMMC_RSTn {14}

GPIO_CPSW1_RST → GPIO_CPSW1_RST {16}

GPIO_RGMII1_RST → GPIO_RGMII1_RST {17}

VPP_LDO_EN → VPP_LDO_EN {10}

RESETSTATz ← RESETSTATz {14,15,24}

SoC_I2C1_SDA ↔ SoC_I2C1_SDA {26,27,28}

SoC_I2C1_SCL ↔ SoC_I2C1_SCL {26,27,28}

SoC_I2C0_SDA ↔ SoC_I2C0_SDA {26,28,30}

SoC_I2C0_SCL ↔ SoC_I2C0_SCL {26,28,30}

From Safety Connector

From SoC OSPI Section

To Processor

To VTT Reg

DDR_VTT_EN ← DDR_VTT_EN {15}

DDR_VTT_EN_3V3 → DDR_VTT_EN_3V3 {8}

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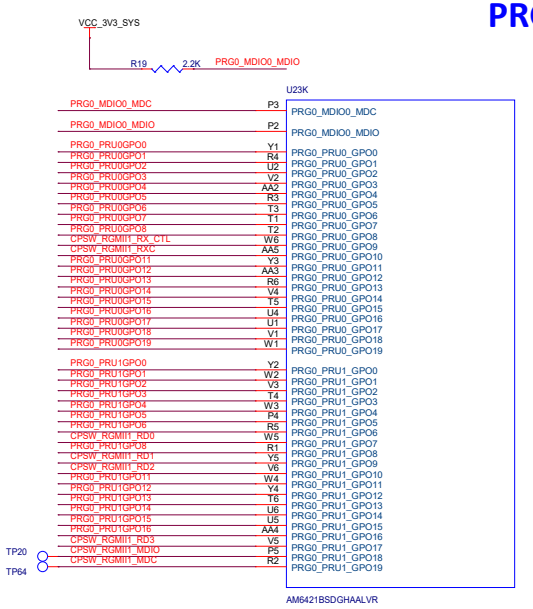
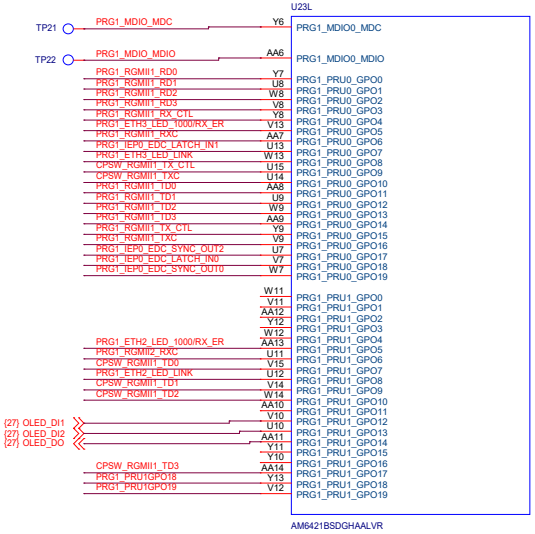
PRG0 & PRG1





D-Note :-
Add series resistors 22 R on the
Ethernet interface TX (TDx) signals
near to the SoC

From Processor

{24,25} MCU_RESETz — MCU_RESETz

{26,28,30} SoC_I2C0_SCL — SoC_I2C0_SCL

{26,28,30} SoC_I2C0_SDA — SoC_I2C0_SDA

To Processor

{16,17,24} PRG1_RGMII_INTn — PRG1_RGMII_INTn

To and from ICSSG2 RGMII 1 Ethernet PHY

{17} PRG1_MDIO_MDIO — PRG1_MDIO_MDIO
{17} PRG1_MDIO_MDC — PRG1_MDIO_MDC
{17} PRG1_ETH3_LED_LINK — PRG1_ETH3_LED_LINK
{17} PRG1_RGMII1_RD0 — PRG1_RGMII1_RD0
{17} PRG1_RGMII1_RD1 — PRG1_RGMII1_RD1
{17} PRG1_RGMII1_RD2 — PRG1_RGMII1_RD2
{17} PRG1_RGMII1_RD3 — PRG1_RGMII1_RD3
{17} PRG1_RGMII1_RXC — PRG1_RGMII1_RXC
{17} PRG1_RGMII1_RX_CTL — PRG1_RGMII1_RX_CTL
{17} PRG1_ETH3_LED_1000/RX_ER — PRG1_ETH3_LED_1000/RX_ER
{17} PRG1_RGMII1_TD0 — PRG1_RGMII1_TD0
{17} PRG1_RGMII1_TD1 — PRG1_RGMII1_TD1
{17} PRG1_RGMII1_TD2 — PRG1_RGMII1_TD2
{17} PRG1_RGMII1_TD3 — PRG1_RGMII1_TD3
{17} PRG1_RGMII1_TXC — PRG1_RGMII1_TXC
{17} PRG1_RGMII1_TX_CTL — PRG1_RGMII1_TX_CTL

SYNC TP

TP36 — PRG1_IEP0_EDC_SYNC_OUT0
TP37 — PRG1_IEP0_EDC_LATCH_IN0
TP38 — PRG1_IEP0_EDC_SYNC_OUT2
TP69 — PRG1_IEP0_EDC_LATCH_IN1

To MUX From SoC

{16} CPSW_RGMII1_MDIO — CPSW_RGMII1_MDIO
{16} CPSW_RGMII1_MDC — CPSW_RGMII1_MDC
{16} CPSW_RGMII1_RD0 — CPSW_RGMII1_RD0
{16} CPSW_RGMII1_RD1 — CPSW_RGMII1_RD1
{16} CPSW_RGMII1_RD2 — CPSW_RGMII1_RD2
{16} CPSW_RGMII1_RD3 — CPSW_RGMII1_RD3
{16} CPSW_RGMII1_RX_CTL — CPSW_RGMII1_RX_CTL
{16} CPSW_RGMII1_RXC — CPSW_RGMII1_RXC

From CPSW RGMII 1 PHY

{16} CPSW_RGMII1_TD0 — CPSW_RGMII1_TD0
{16} CPSW_RGMII1_TD1 — CPSW_RGMII1_TD1
{16} CPSW_RGMII1_TD2 — CPSW_RGMII1_TD2
{16} CPSW_RGMII1_TD3 — CPSW_RGMII1_TD3
{16} CPSW_RGMII1_TX_CTL — CPSW_RGMII1_TX_CTL
{16} CPSW_RGMII1_TXC — CPSW_RGMII1_TXC

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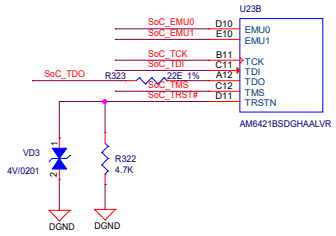
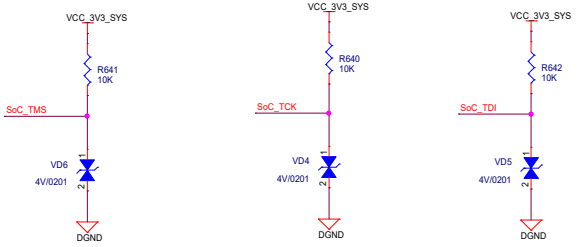
JTAG SoC SECTION

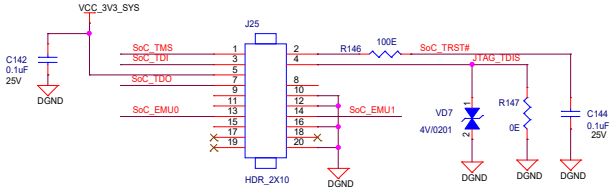


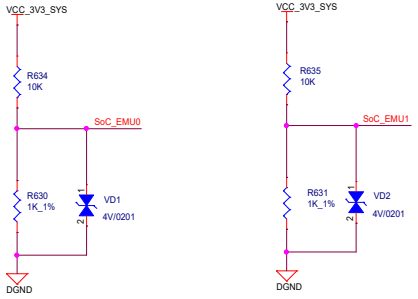
D-Note :-
Place pulls on JTAG
signals near to the SoC
Refer AM62P schematics



JTAG 20 PIN cTI CONNECTOR

D-Note :-
Place pulls on the JTAG signals near to the SoC
Refer SoC data sheet for Pin Connectivity
Requirements





D-Note :-
Add an external ESD protection to provide system
level ESD protection
when external connector is used for debug
Follow the connectivity table for connecting the
required pulls for the SOC JTAG interface
Add Test points, and external ESD protection when
JTAG connector is not used

D-Note :-
TRSTn is the reset to the JTAG logic. For normal operation,
this is pulled low, and thus the JTAG remains in reset as it is
not being used. When a JTAG pod is connected, the pod will
eventually drive this signal high to release the JTAG logic from
reset and enable a JTAG connection.

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JTAG

Size	CAGE Code	DWG NO	Rev
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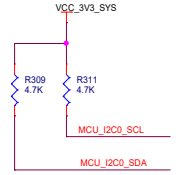
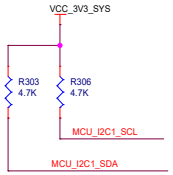
SOC-MCU_GENERAL



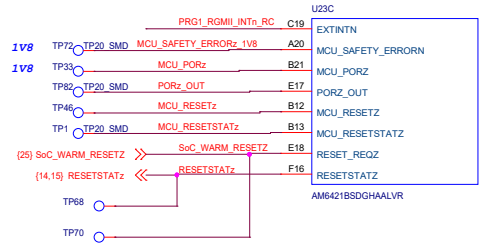
D-Note :-
RC for Open drain output type I2C slew rate control



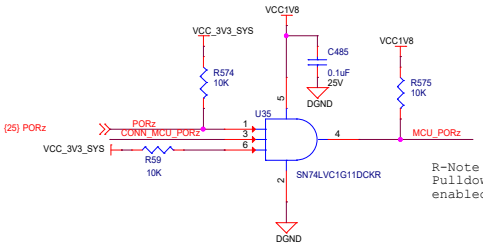
D-Note :-
Add a series resistor 22R to the SPI1 clock output near to the SoC

D-Note :-
MCU_SAFETY_ERRORz_1V8
Provision for a pulldown
Populate when attached
device is connected
Refer SOC data sheet pin
connectivity requirements

SOC RESET

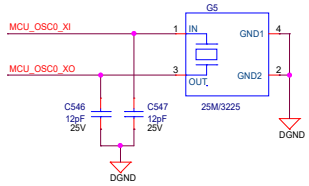


D-Note :-
It is recommended to connect the output from logic gate or discrete buffer (with fast rise time) as MCU_PORz input rather than slow rising open drain output (could glitch internally).

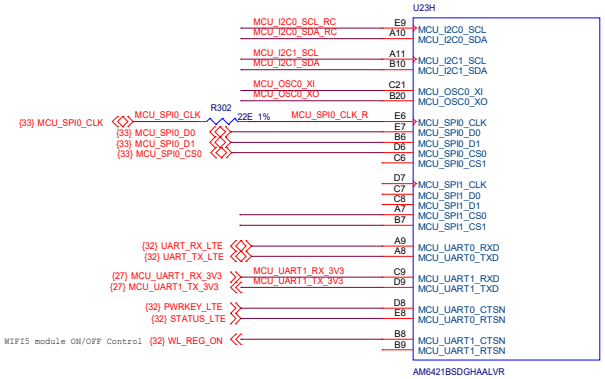


R-Note :-
Pulldown is enabled

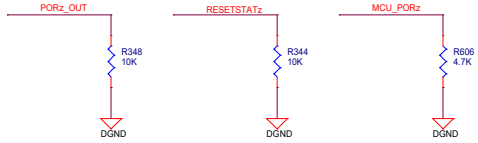
D-Note :-
Not connecting a valid MCU_PORz could cause unpredictable and probably random behavior, since the device is not getting a valid reset, internal circuits would be in random states. Slow rising reset signal could cause glitches internal to the SOC reset circuit. Use a discrete buffer and have the fast rising output of the buffer drive the MCU_PORz is recommended



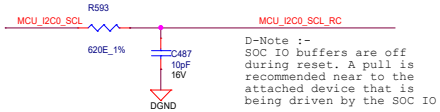
D-Note :-
Refer Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:
Clock Routing Guidelines
Oscillator Routing



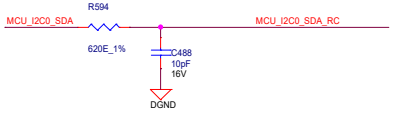
D-Note :-
MCU_PORz pulldown is used to hold the SOC in reset during power-up

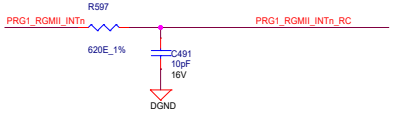


D-Note :-
Pull-down resistors on PORz_OUT and RESETSTATz are provided to keep the signal low until the processor is released from reset during the power-up sequence



D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO





Off Page Connections

To level translator
From Level Translator

To Boot Mode Section

From ICSSG Phy1&2

MCU_RESETz → MCU_RESETz {25}

PORz_OUT → PORz_OUT {14,16,17}

PRG1_RGMII_INTn ← PRG1_RGMII_INTn {16,17}

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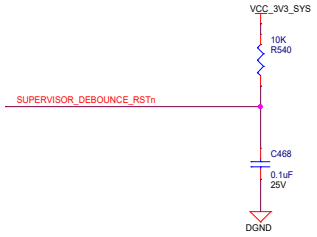
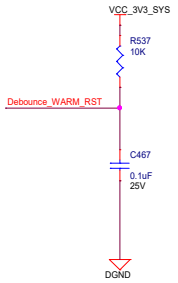
SoC POR_RST

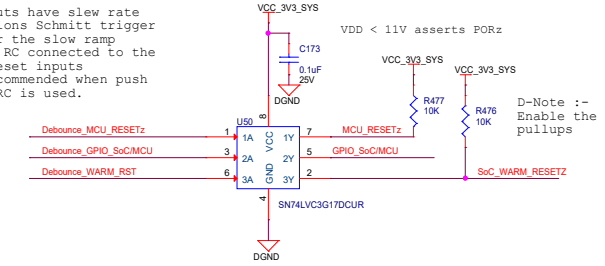


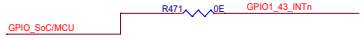
SoC WARM_RST



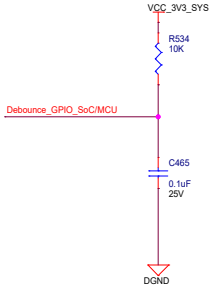
DEBOUNCE CIRCUIT

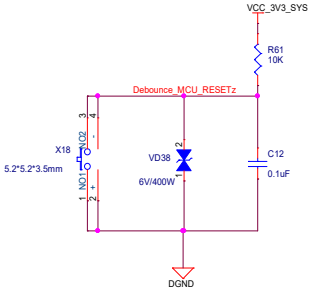
D-Note:-
LVCMOS inputs have slew rate specifications Schmitt trigger is used for the slow ramp pushbutton RC connected to the SoC warm reset inputs
This is recommended when push button or RC is used.

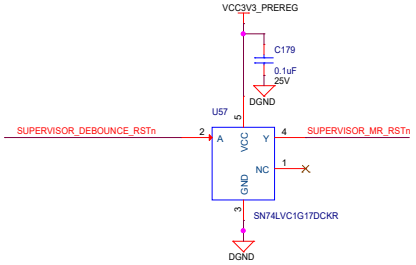




MCU WARM RESET



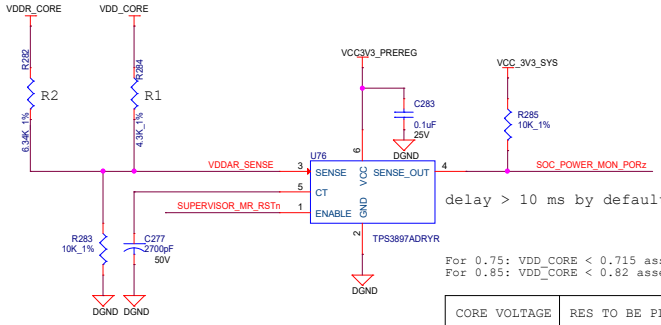




Off Page Connections

VOLTAGE SUPERVISOR

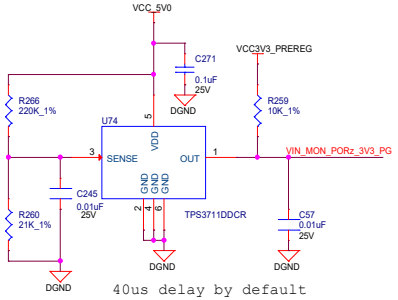
Core Voltage Monitor (VDDAR_CORE/VDD_CORE)



For 0.75: VDD_CORE < 0.715 assert PORz
For 0.85: VDD_CORE < 0.82 asserts PORz

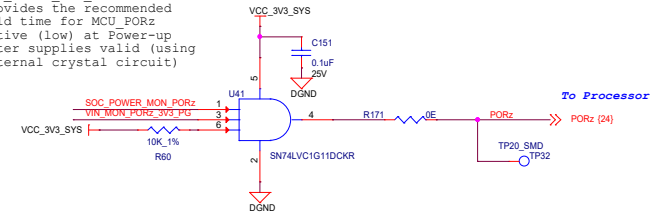
CORE VOLTAGE	RES TO BE PLACED
0.75V	R1 = 4.3K
0.85V	R2 = 6.34K

5V OUTPUT MONITOR (VCC_5V0)



40us delay by default
VDD < 4.6 asserts PORz

D-Note :-
SOC_POWER_MON_PORz (TPS3897) provides the recommended Hold time for MCU_PORz active (low) at Power-up after supplies valid (using external crystal circuit)



D-Note :-
MCU_PORz input have a maximum rise/fall time requirements when PMIC_POWERGOOD or similar signal is connected to the MCU_PORz. Adjust the pullup to minimize the rise time (100..200 ns) when using open drain output.
MCU_PORz is fail-safe and 3.3v tolerant. Therefore, you can pull the MCU_PORz signal to 1.8V or 3.3V.

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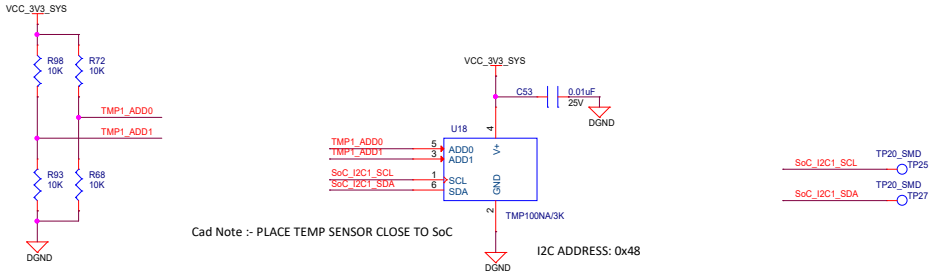
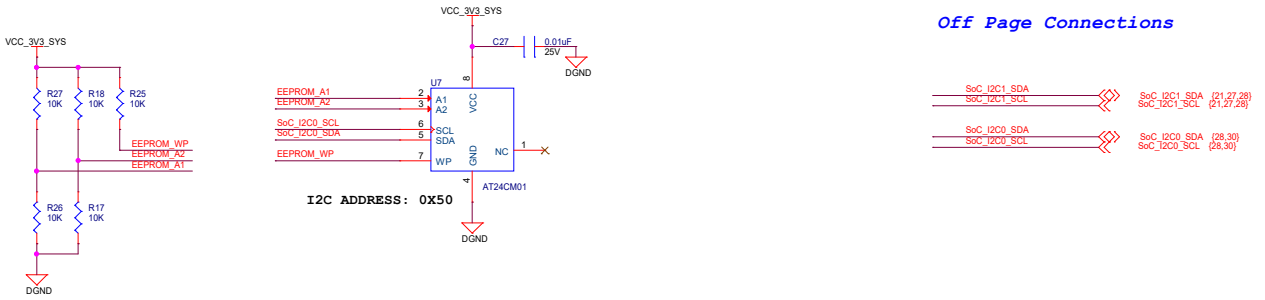
DIGITAL TEMPERATURE SENSOR



Cad Note :- PLACE TEMP SENSOR CLOSE TO SoC

I2C ADDRESS: 0x48

BOARD ID EEPROM



I2C ADDRESS: 0X50

Off Page Connections

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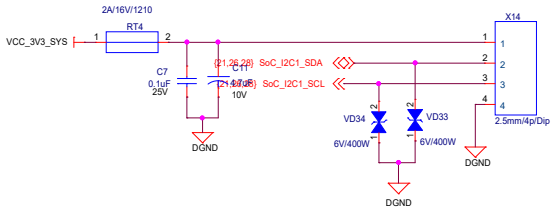
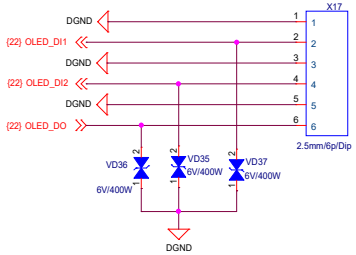
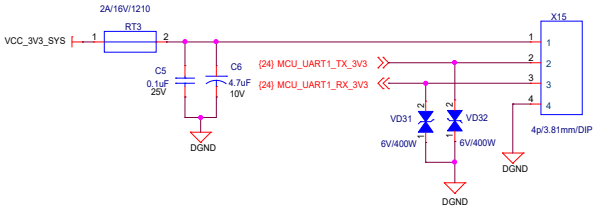
OLED INTERFACE

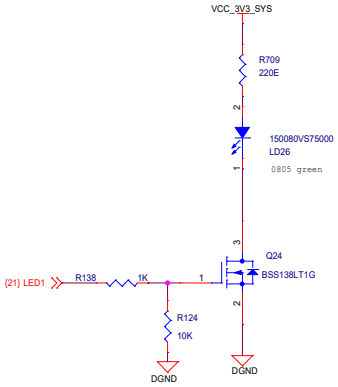


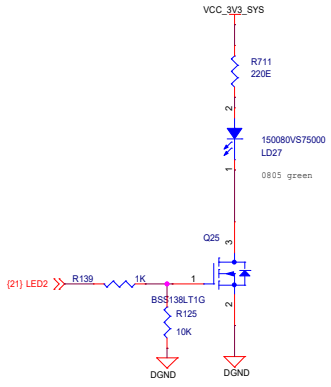


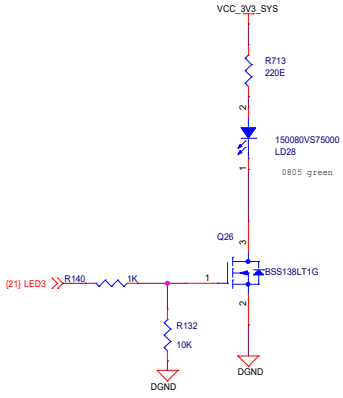
Additional UART

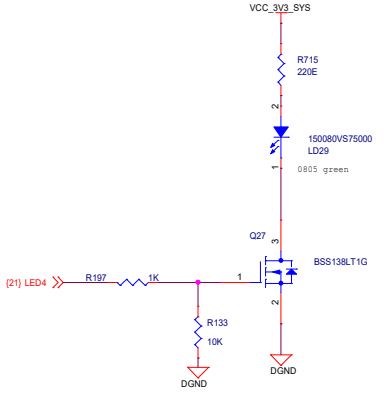


INDICATOR LIGHTS

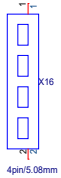








Light Pipe



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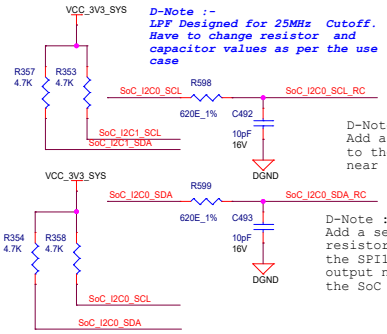
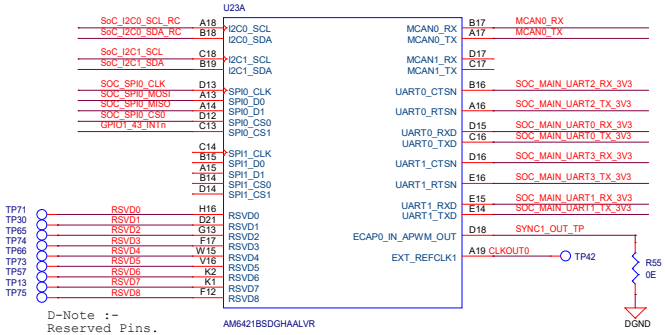


D-Note :-
SOC IO buffers are off
during reset. A pull is
recommended near to the
attached device that is
being driven by the SOC
IO

D-Note :-
RC for Open drain
output type I2C
interface for slew
rate control when
pulled to 3.3V
Refer SOC Data sheet

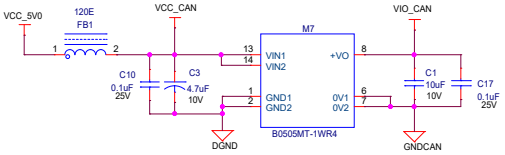
D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V. An RC is recommended for slew rate control. Refer SK-AM62P-LP schematics



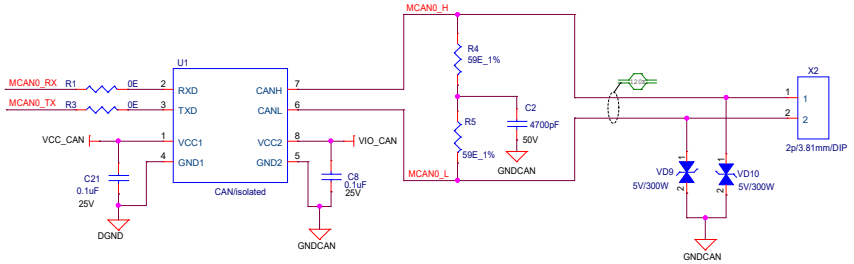
D-Note :-
Reserved Pins.
Leave unconnected

D-Note :-
Ext_Refclk1 used as Clkout0
A clock signal should always be connected point to point without any branches. When connecting Clkout0 to more than one (multiple) clock inputs, use a buffer with one input and multiple outputs.

5V To 5V Isolated

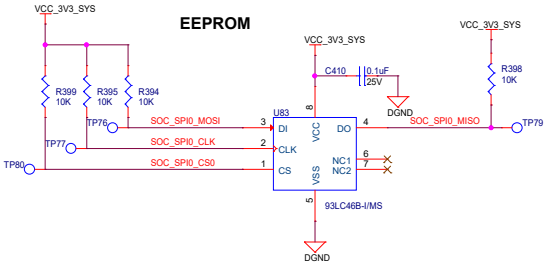


CAN INTERFACE OK



D-Note :-
An external ESD protection is required when connecting the SOC signals directly to external input

SPI EEPROM



Off Page Connections

From Debounce Circuit
GPIO1_43_INTn → GPIO1_43_INTn {25}

To Clock Buffer
SoC_I2C0_SCL → SoC_I2C0_SCL {26,30}
SoC_I2C0_SDA → SoC_I2C0_SDA {26,30}
SoC_I2C1_SCL → SoC_I2C1_SCL {21,26,27}
SoC_I2C1_SDA → SoC_I2C1_SDA {21,26,27}

To RS232/485
SOC_MAIN_UART0_TX_3V3 → SOC_MAIN_UART0_TX_3V3 {31}
SOC_MAIN_UART0_RX_3V3 → SOC_MAIN_UART0_RX_3V3 {31}
SOC_MAIN_UART2_RX_3V3 → SOC_MAIN_UART2_RX_3V3 {31}
SOC_MAIN_UART2_TX_3V3 → SOC_MAIN_UART2_TX_3V3 {31}
SOC_MAIN_UART1_TX_3V3 → SOC_MAIN_UART1_TX_3V3 {31}
SOC_MAIN_UART1_RX_3V3 → SOC_MAIN_UART1_RX_3V3 {31}
SOC_MAIN_UART3_RX_3V3 → SOC_MAIN_UART3_RX_3V3 {30}
SOC_MAIN_UART3_TX_3V3 → SOC_MAIN_UART3_TX_3V3 {30}

Uniqgrid

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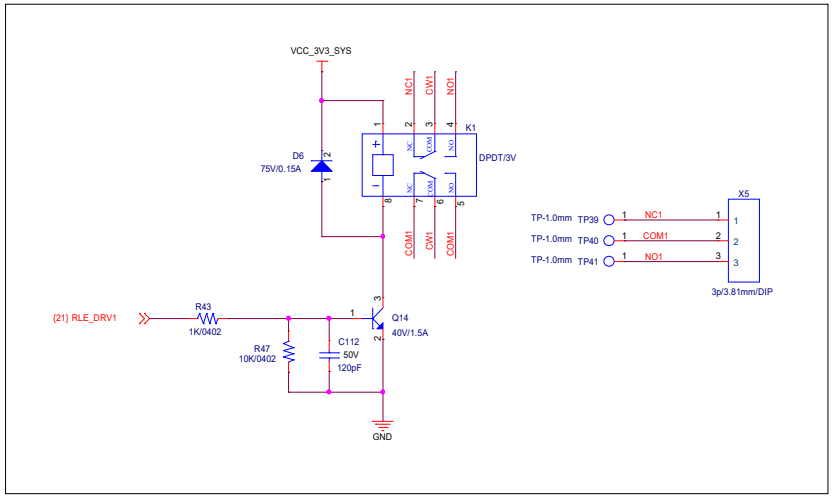
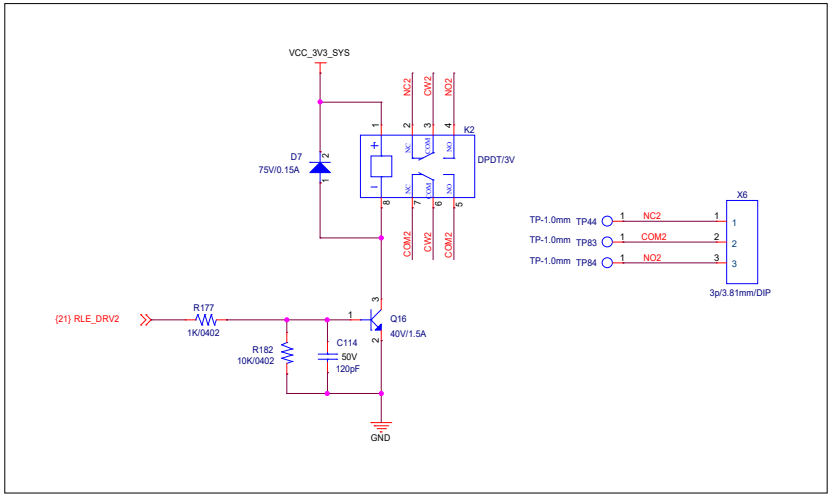
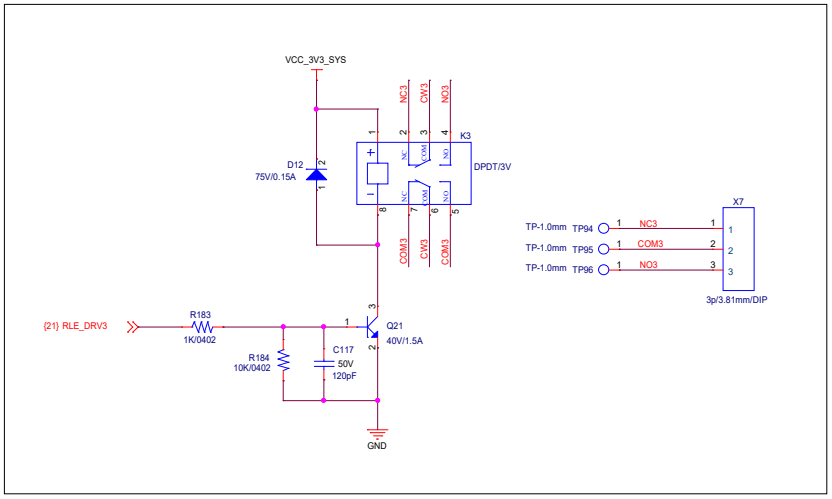
RELAY INTERFACE 1



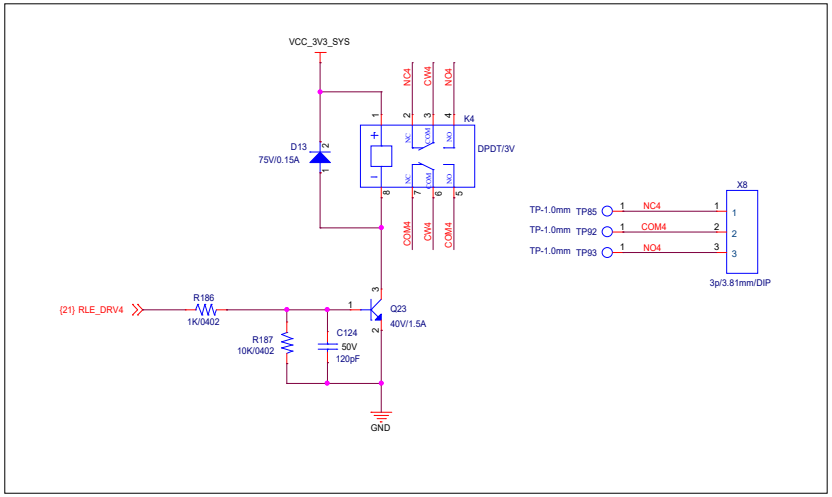
RELAY INTERFACE 2



RELAY INTERFACE 3



RELAY INTERFACE 4



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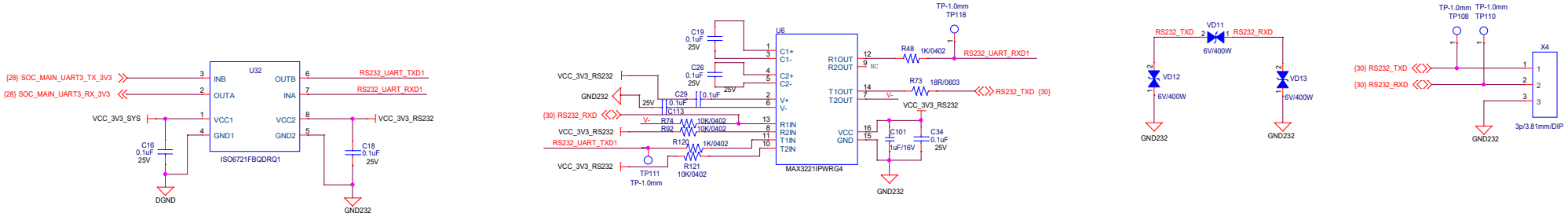
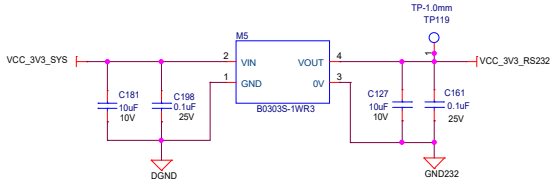
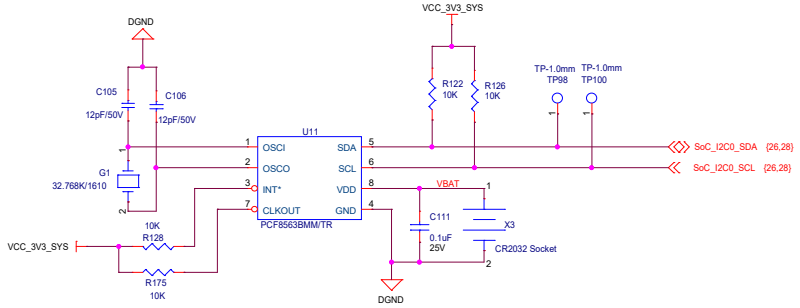
RS232 Isolated INTERFACE



3.3V To 3.3V Isolated



RTC



Address:Read:A3h; Write:A2h

400KHz max.

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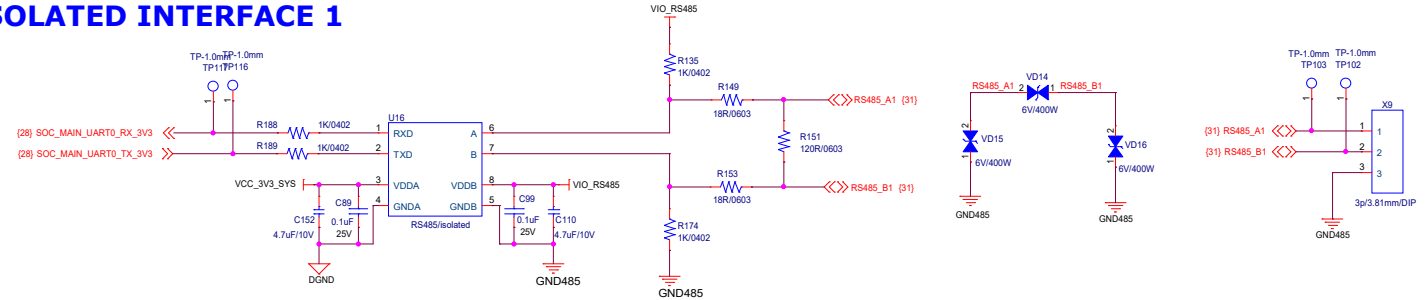
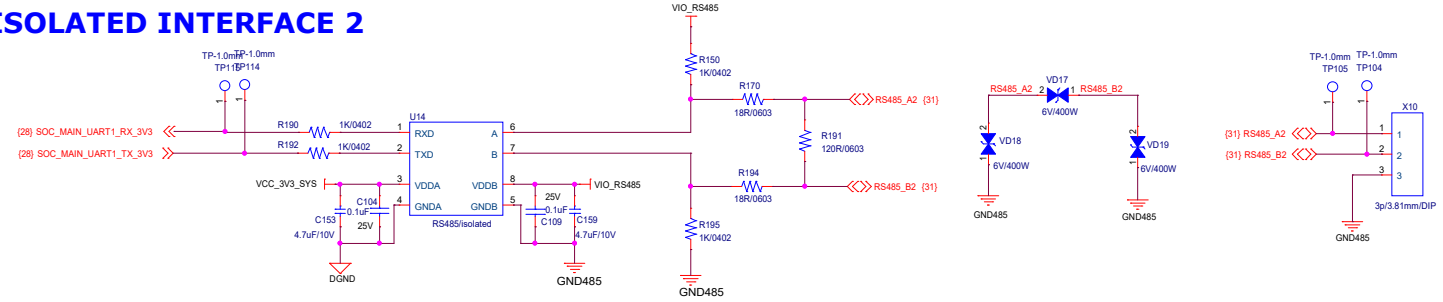
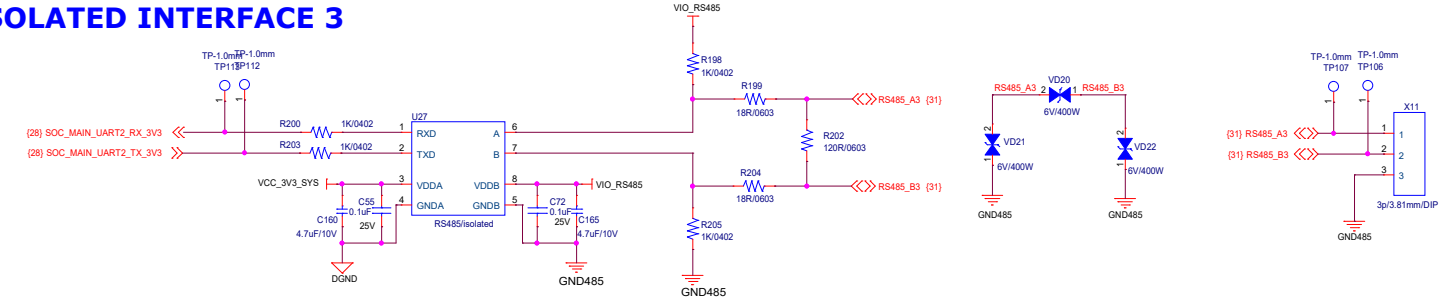
RS485 ISOLATED INTERFACE 1



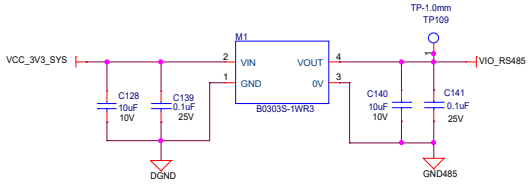
RS485 ISOLATED INTERFACE 2



RS485 ISOLATED INTERFACE 3



3.3V To 3.3V Isolated



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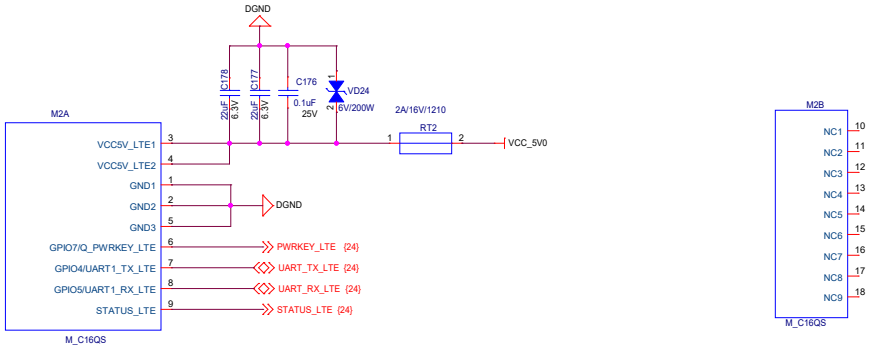
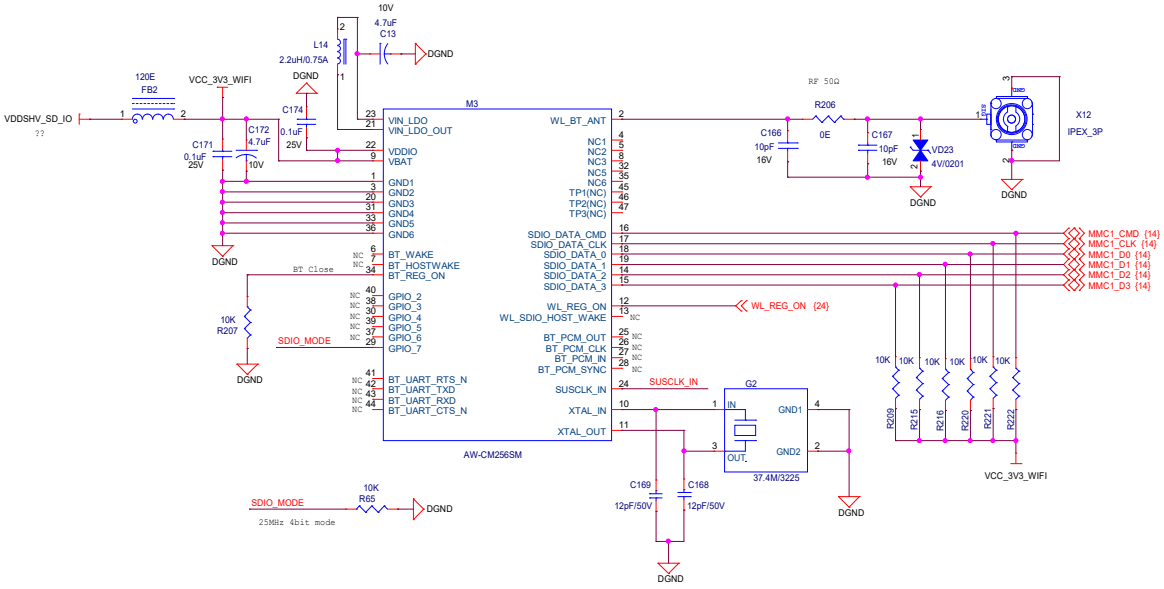
4G module



WIFI5 module



SDIO Interface

<Variant Name>

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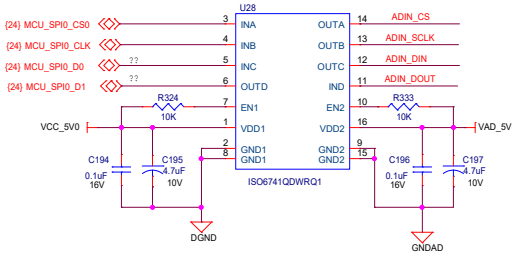
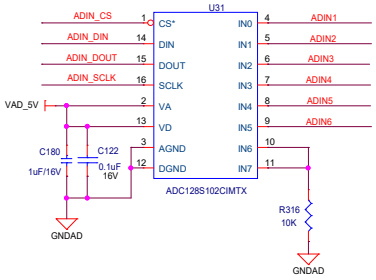
6 Channels Analog and digital signal inputs

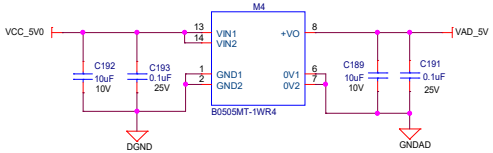
SPI Isolated

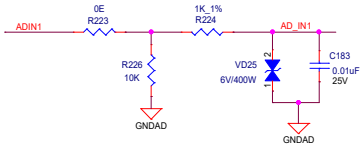


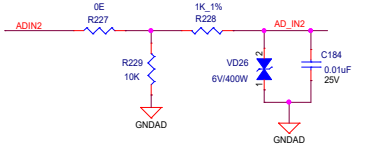
6*AD Input To SPI

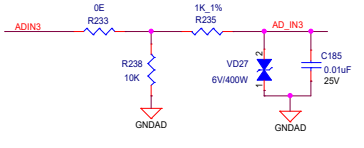


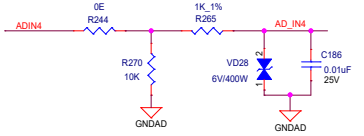
5V To 5V Isolated

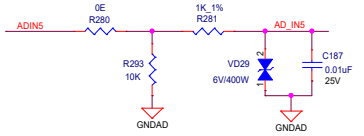


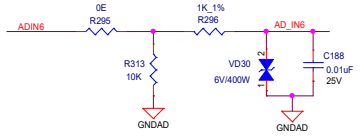


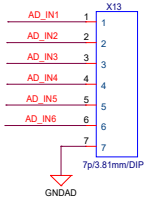












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