J6/TDA2-Plus Ref Study PCB Power Integrity Analysis

Alec Schott, Bill McCracken

Date	Revision	History
03/19/2018	1.0	Added Power Caps LL

Power Integrity Parameters of Interest

- **Effective Resistance (Reff)**
  - Static/DC Analysis Parameter
  - Voltage/IR Drop (IRd) of power rail from power source to load component

  Reff = PCB Trace Resistance (Rt) + Series Element Resistance (Rs)

  Reff = Rt + Rs

  IRd = Imax * Reff (where Imax is for maximum power Use Case)
- **Loop Inductance (LL)**
  - Dynamic/AC Analysis Parameter
  - Spreading loop inductance from a component's power inputs to local decoupling caps
  - Evaluated over 30-70Mhz freq range with inductance at 50MHz reported
- **Target Impedance (Tz)**
  - Dynamic/AC Analysis Parameter
  - Changing impedance of power rail as a function of frequency
  - Evaluated over 1-200Mhz range with impedance at critical frequencies typically reported

8-Layer PCB, J6P/TDA2P Ref Study PIA Summary

- PCB Filename: 518711study_0112a_gpu.brd
- PI Simulation CAD Tool: Sentinel PSI v14.2.1.p3

Rail / Domain Priority[1]	Rail / Domain Name	Power Rail Effective Resistance (Reff) [mΩ] SMPS to SoC	Power Rail Loop Inductance (LL) [nH] @ 50MHz	Dcap Loop Inductance (LL) [nH] @ 50MHz Min and max	Target Impedance (Tz) w/ Optimized Dcap Scheme [mΩ] @ [MHz]
1	VDD_MPU_AVS	4.1	C169 = 0.85	0.45 – 0.83	24.2
	VDD_MPU(1.8GHz)[2]	18	C170 = 1.31	< 1.5	< 22 @ 20
2	VDD_DSPEVE_AVS	5.1	C148 = 1.24	0.19 – 1.16	45.5
	VDD_DSPEVE[2]	22	C158 = 1.15	< 1.6	< 40 @ 30
3	VDD_GPU_AVS	7.4	C153 = 1.56	0.18 - 1.01	54.6
	VDD_GPU[2]	22	C154 = 1.47	< 2.1	< 48 @ 30
4	VDD_CORE	12.6	C146 = 2.48	0.96 – 1.32	40.5
	VDD[2]	32		< 1.6	<43 @ 30
5	VDD_IVA_AVS	27	C143 = 6.02	1.15 – 2.37	169
	VDD_IVA[2]	48		< 2.1	< 179 @ 30
6	VCAP_xxx	NA		1.17 – 1.61	NA
	VCAP_xxx[2]	NA		< 6	NA
7	VDDR_MEM_1v35	4.5		0.80 – 1.35	104
	VDDR[2]	18		< 1.5	< 130 @ 100

[1]PCB Guideline targets given in J6Plus/DRA7xxP/TDA2Px DM, Table 7-3
[2]Priority is based on Current Draw for EVM Superset

10-Layer PCB, J6P/TDA2P Ref Study PIA Summary

- PCB Filename: 518711study_0122a_gpu.brd
- PI Simulation CAD Tool: Sentinel PSI v14.2.1.p3

Rail / Domain Priority[1]	Rail / Domain Name	Power Rail Effective Resistance (Reff) [mΩ] SMPS to SoC	Power Rail Loop Inductance (LL) [nH] @ 50MHz	Dcap Loop Inductance (LL) [nH] @ 50MHz Min and max	Target Impedance (Tz) w/ Optimized Dcap Scheme [mΩ] @ [MHz]
1	VDD_MPU_AVS	3.3	C169 = 0.528	0.309 – 0.745	18.7
	VDD_MPU(1.8GHz)[2]	18	C170 = 0.873	< 1.5	< 22 @ 20
2	VDD_DSPEVE_AVS	3.8	C148 = 0.816	0.332 – 0.921	32.1
	VDD_DSPEVE[2]	22	C158 = 0.720	< 1.6	< 40 @ 30
3	VDD_GPU_AVS	5.1	C153 = 0.84	0.36 – 0.91	38.4
	VDD_GPU[2]	22	C154 = 0.75	< 2.1	< 48 @ 30
4	VDD_CORE	7.6	C146 = 1.076	0.52 – 1.36	29.4
	VDD[2]	32		< 1.6	<43 @ 30
5	VDD_IVA_AVS	15.1	C143 = 3.23	1.16 – 2.00	143.3
	VDD_IVA[2]	48		< 2.1	< 179 @ 30
6	VCAP_xxx	NA		1.20 – 1.63	NA
	VCAP_xxx[2]	NA		< 6	NA
7	VDDR_MEM_1v35	2.7		0.55 – 1.46	71.8
	VDDR[2]	18		< 1.5	< 130 @ 100

[1]PCB Guideline targets given in J6Plus/DRA7xxP/TDA2Px DM, Table 7-3
[2]Priority is based on Current Draw for EVM Superset

8 LAYER PCB - J6P/TDA2P REF STUDY PIA

8-Layer PCB Stack-up

Layout Cross Section

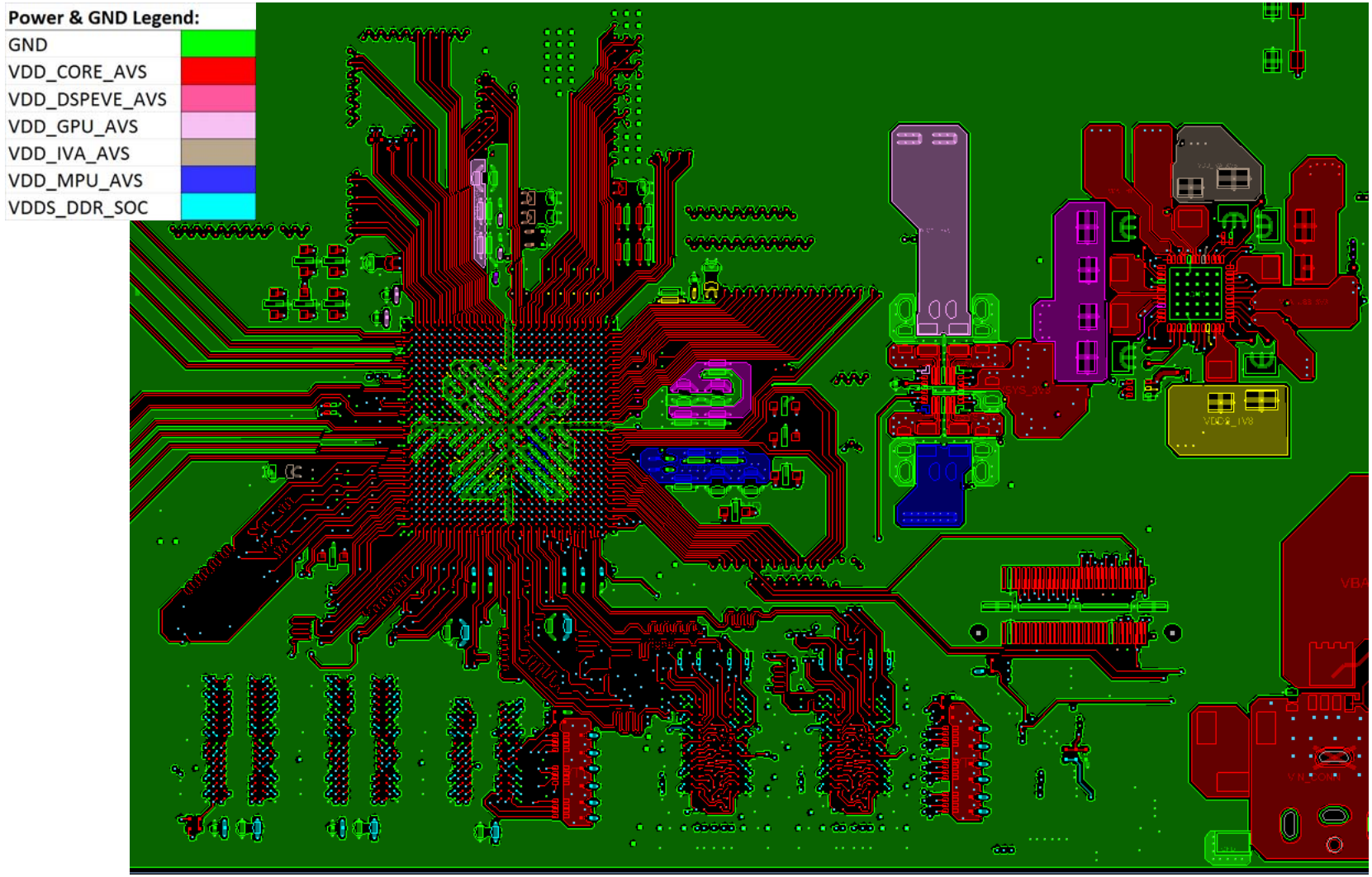
	Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MIL)	Impedance (ohm)
1		SURFACE	SOLDER_MASK			3.5	0.033				
2		DIELECTRIC	SOLDER_MASK	0.5	0	2.55	0.0019				
3	TOP	CONDUCTOR	COPPER	1.7	595900	2.55	0	☐		5.50	49.367
4		DIELECTRIC	FR-4	3.6	0	4.37	0.021				
5	L2-GND	PLANE	COPPER	1.2	595900	4.37	0	☐	☒		
6		DIELECTRIC	FR-4	6	0	4.33	0.021				
7	L3-SIG	CONDUCTOR	COPPER	0.6	595900	4.14	0	☐		4.30	48.647
8		DIELECTRIC	FR-4	4.3	0	4.14	0.021				
9	L4-VCC	PLANE	COPPER	0.6	595900	4.14	0	☐	☒		
10		DIELECTRIC	FR-4	23	0	4.57	0.019				
11	L5-VCC	PLANE	COPPER	0.6	595900	4.12	0	☐	☒		
12		DIELECTRIC	FR-4	4.2	0	4.16	0.021				
13	L6-SIG	CONDUCTOR	COPPER	0.6	595900	4.16	0	☐		4.30	48.2
14		DIELECTRIC	FR-4	6	0	4.33	0.021				
15	L7-GND	PLANE	COPPER	1.2	595900	4.37	0	☐	☒		
16		DIELECTRIC	FR-4	3.6	0	4.37	0.021				
17	BOTTOM	CONDUCTOR	COPPER	1.7	595900	2.55	0	☐		5.50	49.367
18		DIELECTRIC	SOLDER_MASK	0.5	0	2.55	0.0019				
19		SURFACE	SOLDER_MASK			3.5	0.033				

Total Thickness: 59.9 MIL

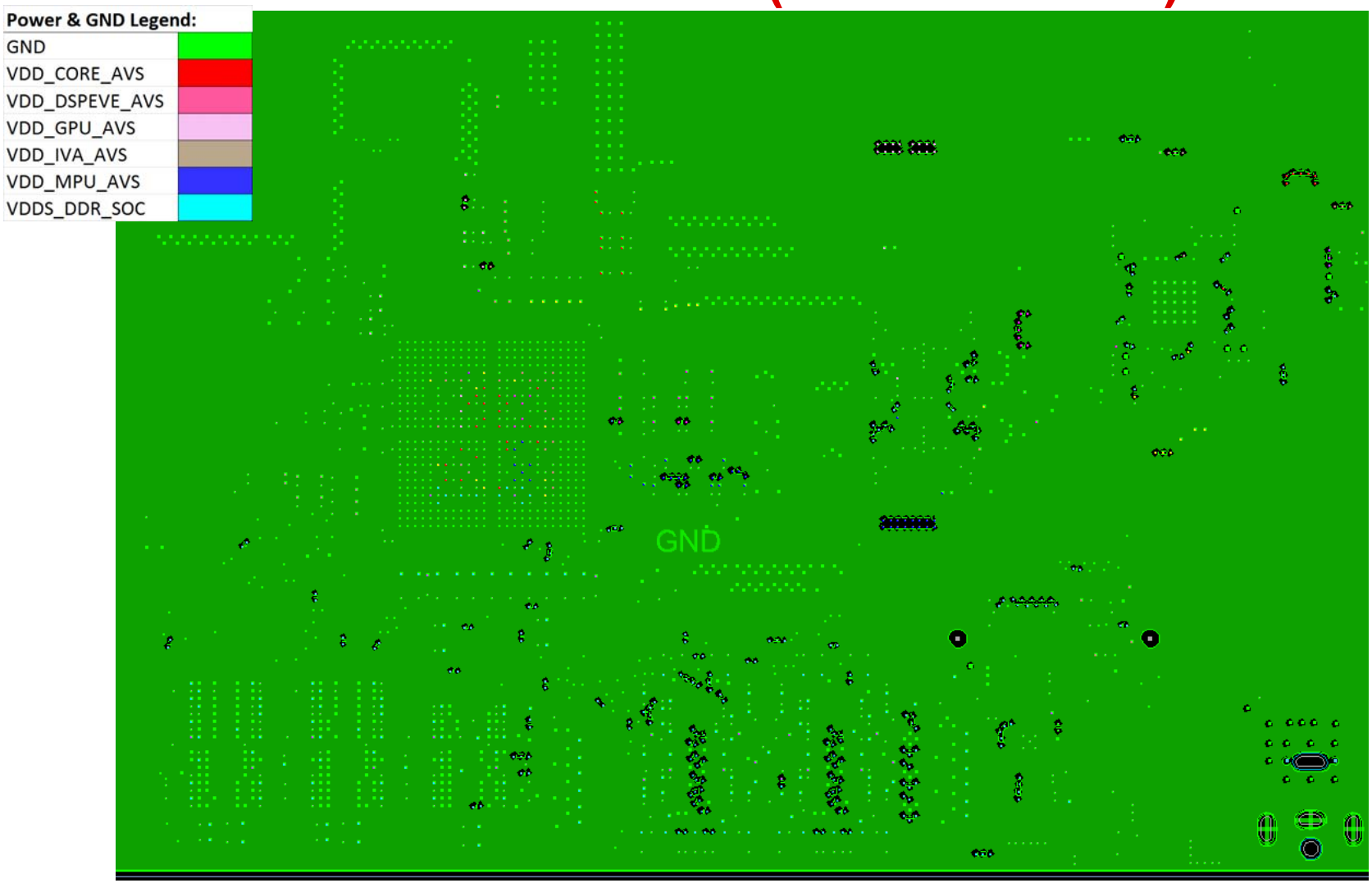
Layer Type ALL | **Material** ALL | **Field to Set** Thickness | **Value to Set** | Update Fields

☑ Show Single Impedance
☐ Show Diff Impedance

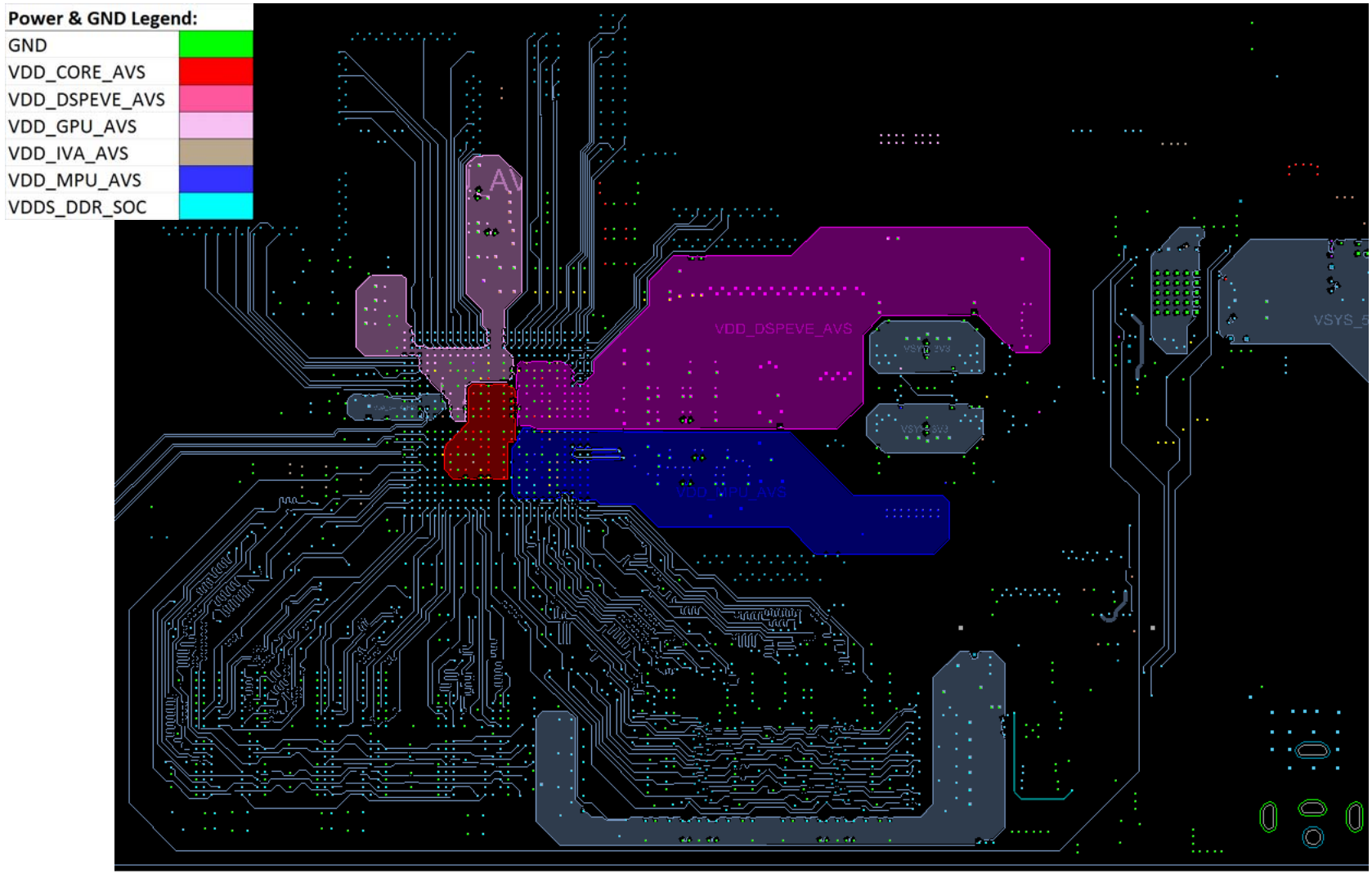
8-Layer PDN Overview – Lyr 1/Top (Signal-1)



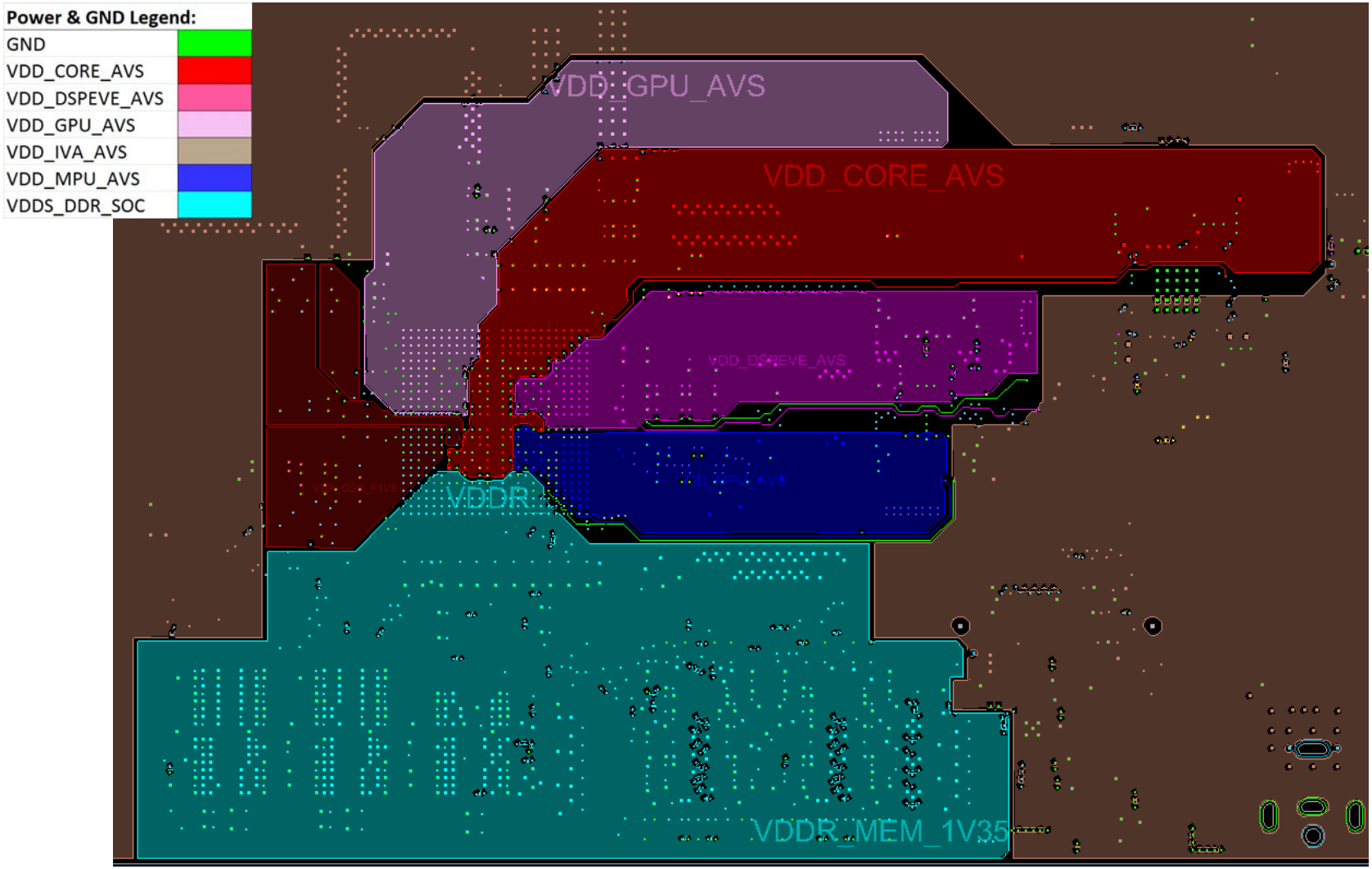
8-Layer PDN Overview – Lyrs-2 & 7
Gnd net (Planes–1 & 4)



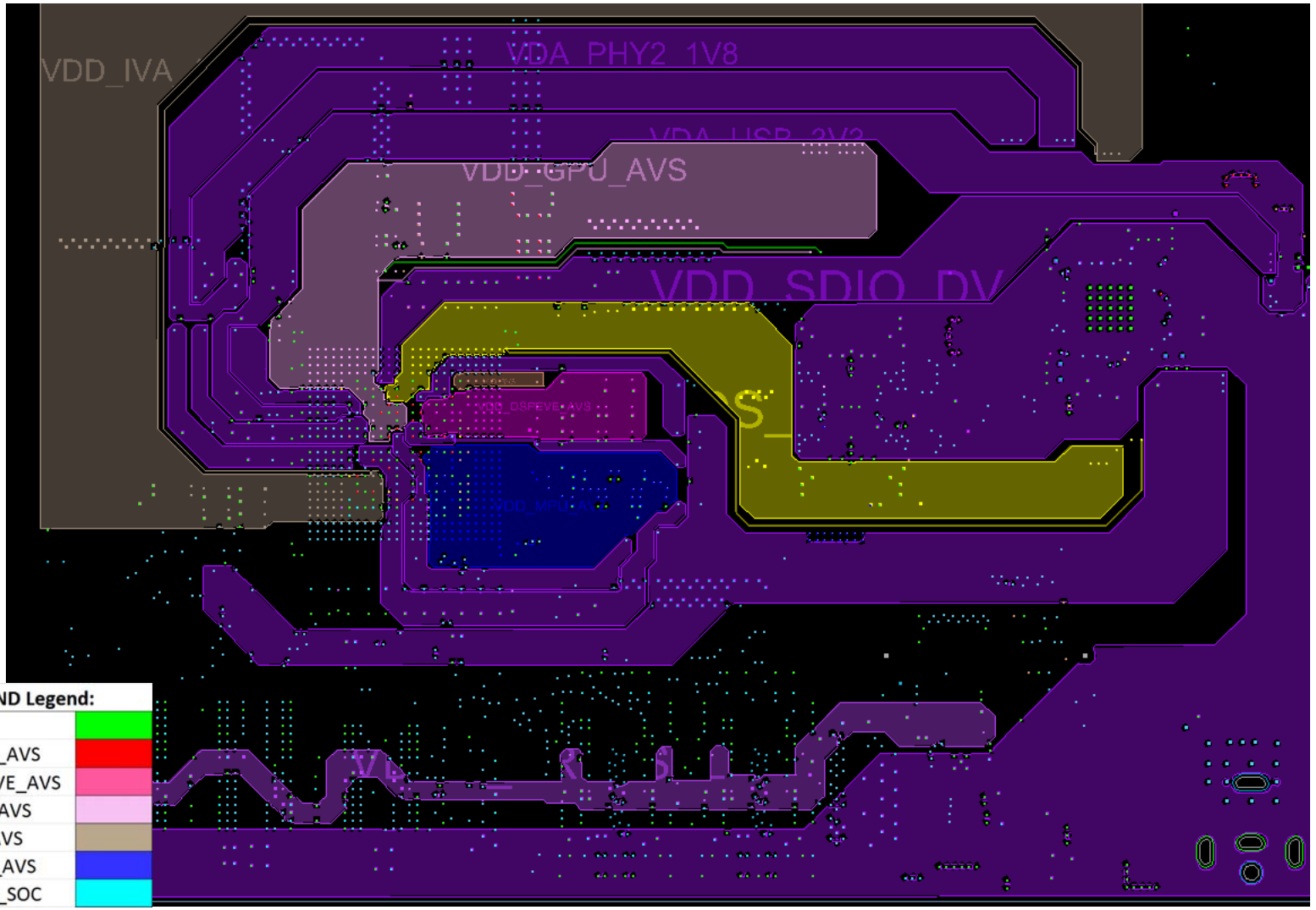
8-Layer PDN Overview – Lyr 3 (Signal-2)



8-Layer PDN Overview – Lyr 4 (Plane-2)

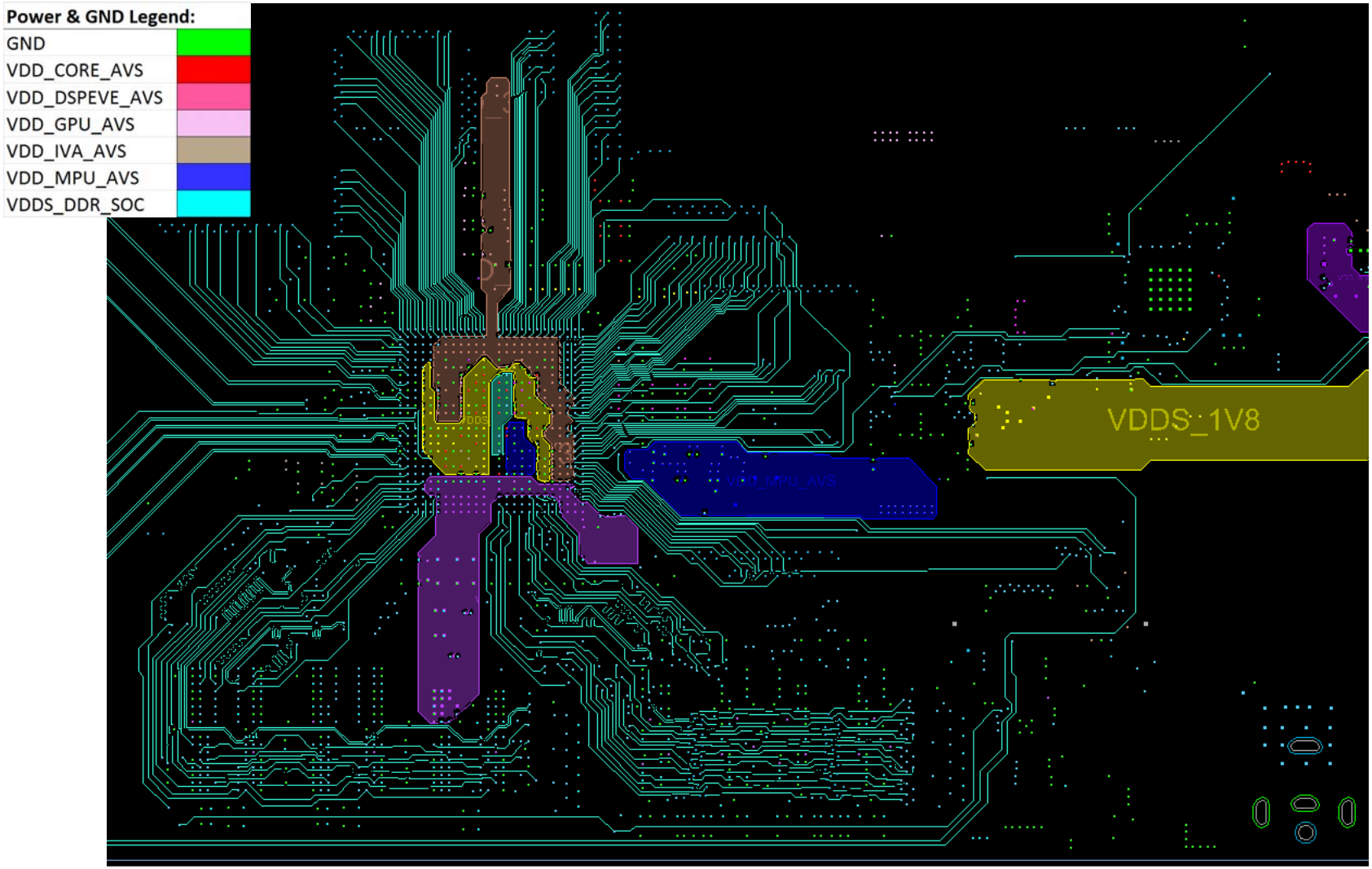


8-Layer PDN Overview – Lyr 5 (Plane-3)

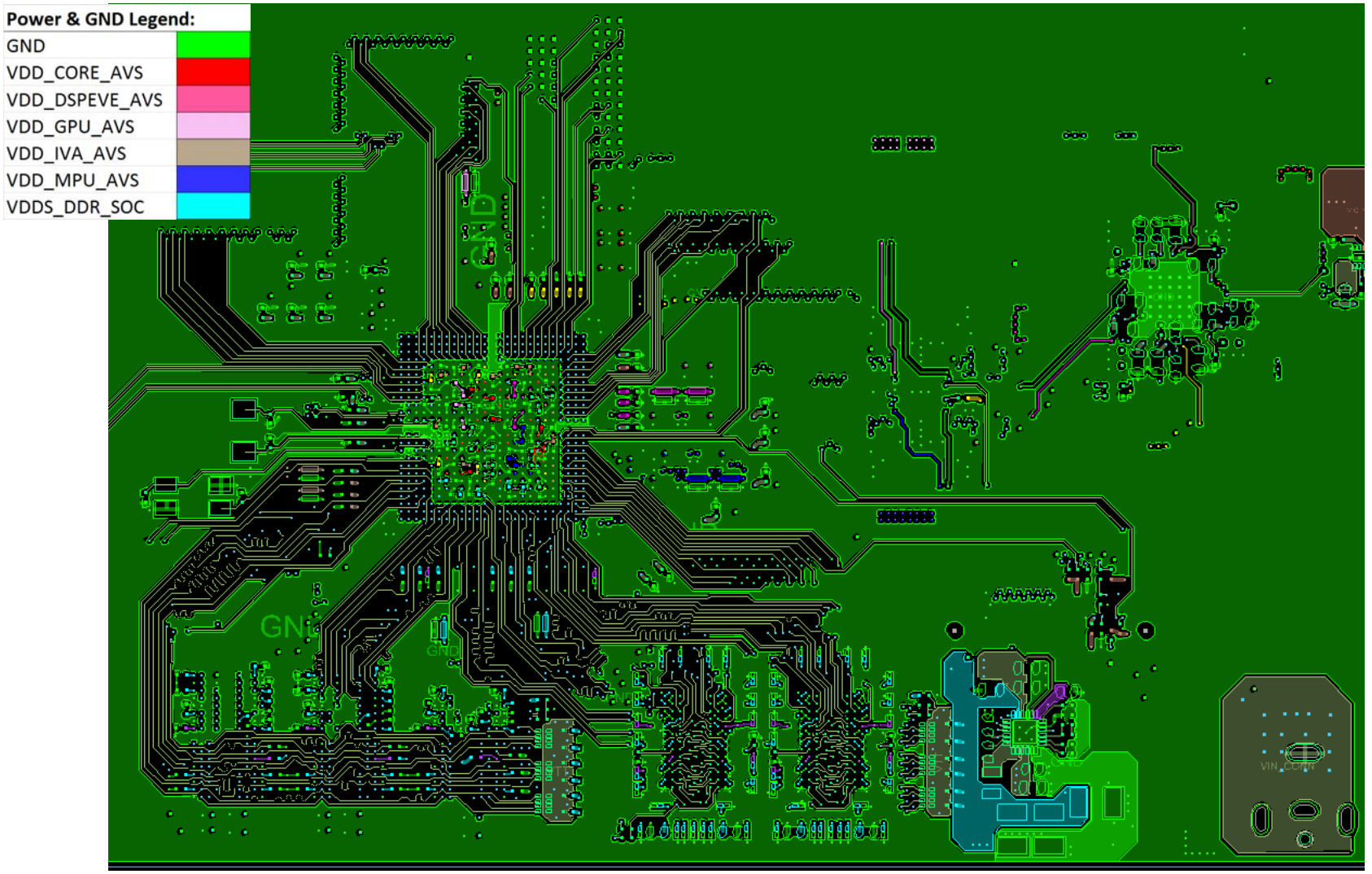


Power & GND Legend:
GND
VDD_CORE_AVS
VDD_DSPEVE_AVS
VDD_GPU_AVS
VDD_IVA_AVS
VDD_MPU_AVS
VDDS_DDR_SOC

8-Layer PDN Overview – Lyr 6 (Signal-3)



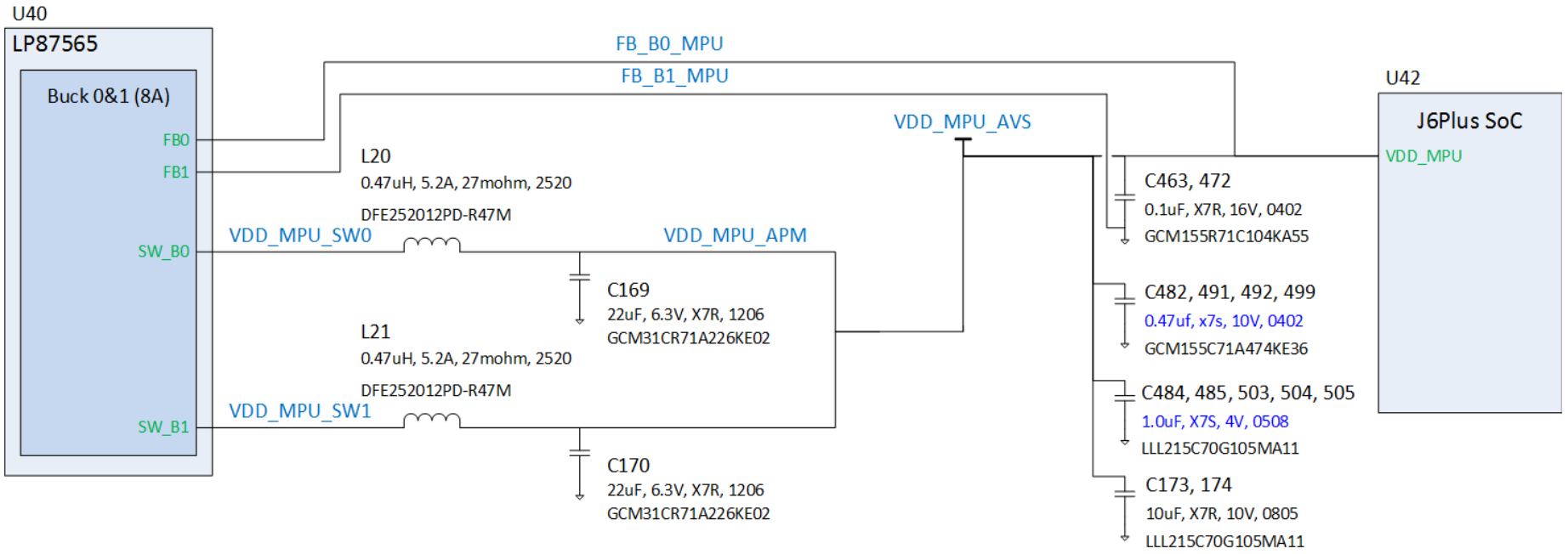
8-Layer PDN Overview – Lyr 8/Bottom (Signal-4)



VDD_MPU_AVS POWER DOMAIN

VDD_MPU_AVS - Simplified Power SCH

J6Plus Ref – VDD_MPU_AVS Power Rail Model

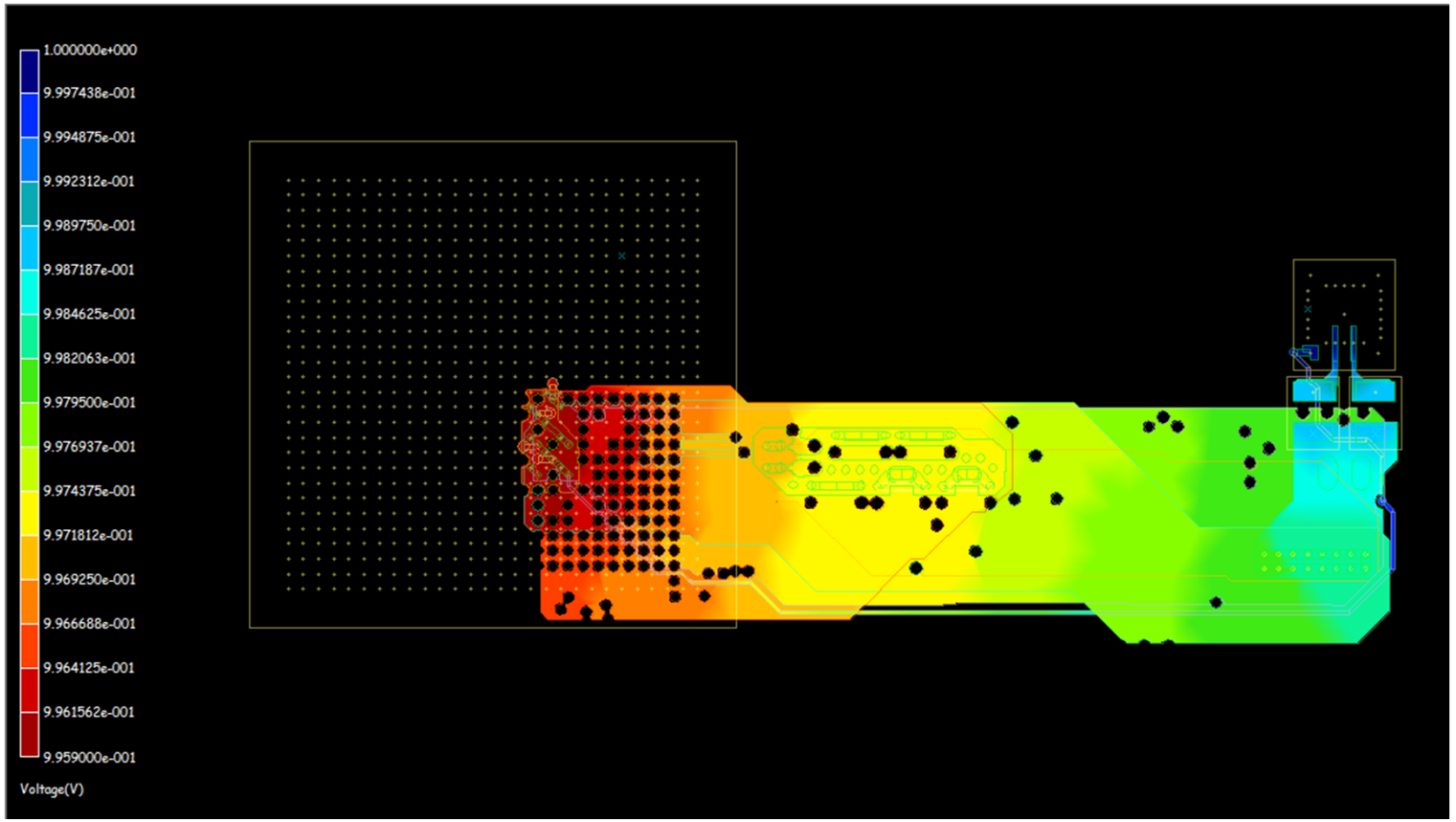


Recommended Dcap Scheme Optimized for PCB Design						Power Rail: VDD_MPU_AVS		
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C173, 174	10	2	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C484, 485, 503, 504, 505	1.0	5	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C482, 491, 492, 499	0.47	4	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
C463, 472	0.1	2	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155R71C104KA55	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B1X7R1C104K050BC
Totals	27.1	13	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDD_MPU_AVS

Derived from: Vdrop Analysis						
Name	Vin [V]	Vout [V]	Vdrop [V]	Current [A]	Reff [Ohms]	Target [mohms]
VDD_MPU_AVS	1.0000					
		0.9959	0.0041	1	0.0041	18.0

Routed on Layers
1
3
4
5
6



Dcap Loop Inductance: VDD_MPU_AVS

- Decoupling Cap's Loop Inductance (LL) Range: 0.453 – 0.830 nH (@ 50 MHz)

Capacitor Footprints (FP)	Footprint Types	Inductance	Code
	2-via, skinny-end exit	Highest	2vSEE
	2-via, wide-end exit		2vWEE
	2-via, wide-side exit		2vWSE
	4-via, wide-side exit		4vWSE
	via in-pad	Lowest	vIP

Cap Ref Des	v0112 8Lyr Ref PCB Loop Inductance @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Pwr Ball-Field (ref ball =K18) [mils]	Value [uF]	Size
C463	0.83	2vWSE	Bottom, Under BGA	111	0.1	0402
C472	0.778	2vWSE	Bottom, Under BGA	54	0.1	0402
C482	0.697	2vWSE	Bottom, Under BGA	79	0.47	0402
C491	0.73	2vWEE	Top	458	0.47	0402
C492	0.827	2vWSE	Bottom, Under BGA	65	0.47	0402
C499	0.685	2vWEE	Top	462	0.47	0402
C484	0.485	4vWSE	Top	758	1.0	0508
C485	0.456	4vWSE	Top	623	1.0	0508
C503	0.724	4vWSE	Bottom	849	1.0	0508
C504	0.685	4vWSE	Bottom	715	1.0	0508
C505	0.453	4vWSE	Top	582	1.0	0508
C173	0.691	4vWSE	Top	712	10	0805
C174	0.729	4vWSE	Top	846	10	0805
Min	0.453					
Max	0.830					
Average:	0.675					

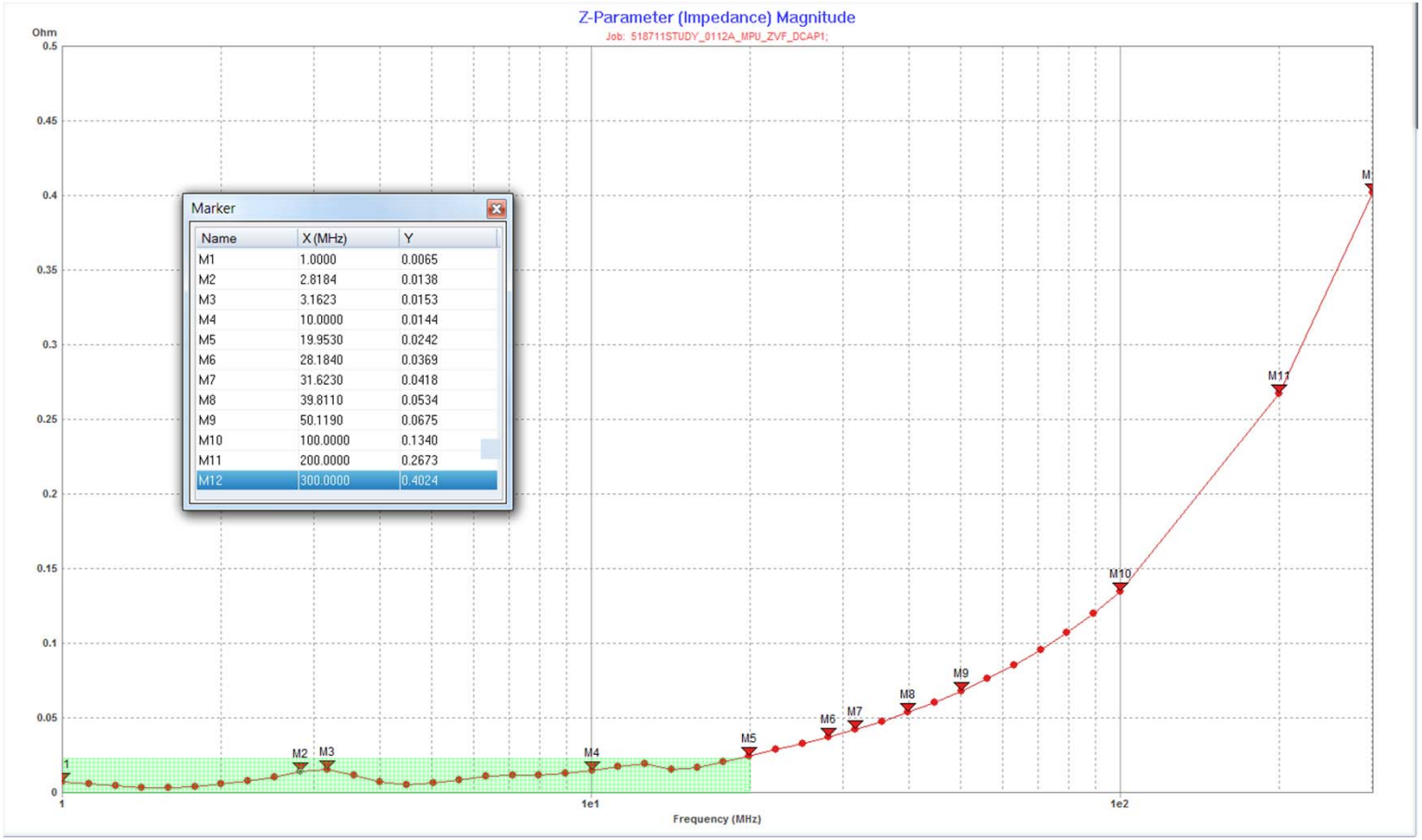
Notes:

1) Distances are wrt "middle of Ball Field", Ref pt between: U42-K18 to middle of Dcap's power pad unless specified

Power Rail Loop Inductance

Item #	Cap Ref Des	v0112 8 LyrRef PCB Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Pwr Ball-Field (ref ball =K18) [mils]	Value [uF]	Size
14	C169	0.85	Power Cap	Top	1594.9	22	1206
15	C170	1.311	Power Cap	Top	1664.8	22	1206

Target Impedance: VDD_MPU_AVS

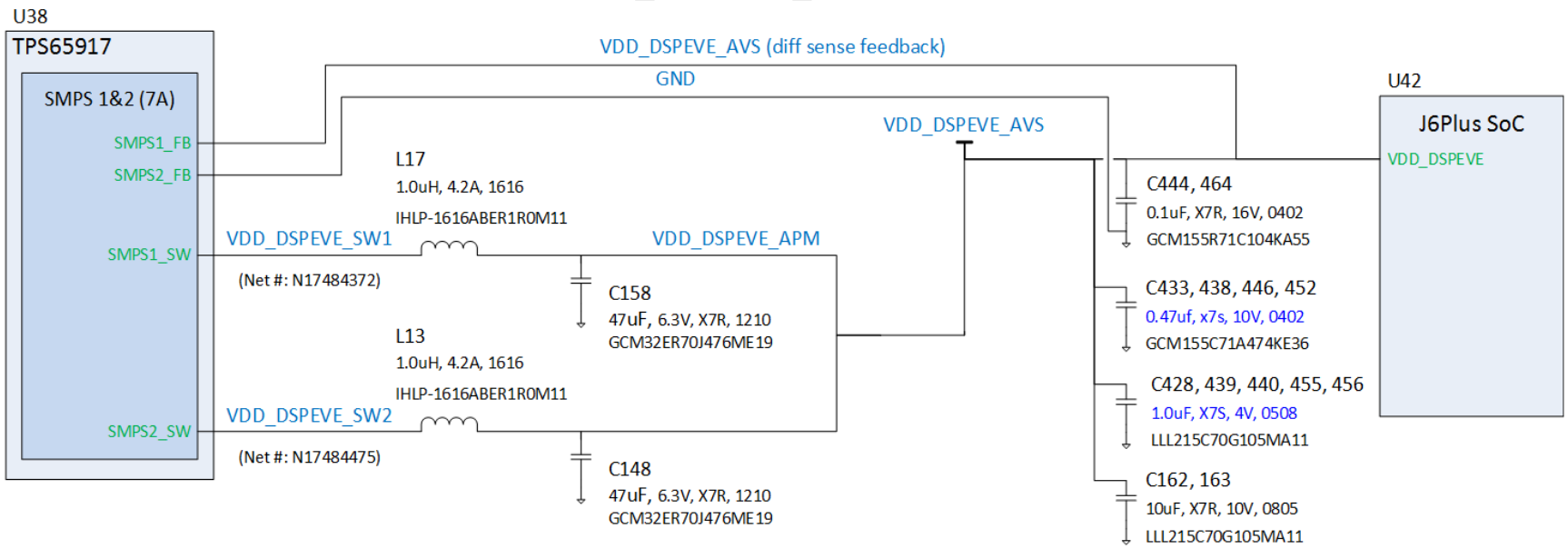


Green box = Power rail's Max Target Impedance of 22mOhm up to "Freq of Interest" 20 MHz

VDD_DSPEVE_AVS POWER DOMAIN

VDD_DSPEVE_AVS – Simplified Power SCH

J6Plus Ref – VDD_DSPEVE_AVS Power Rail Model

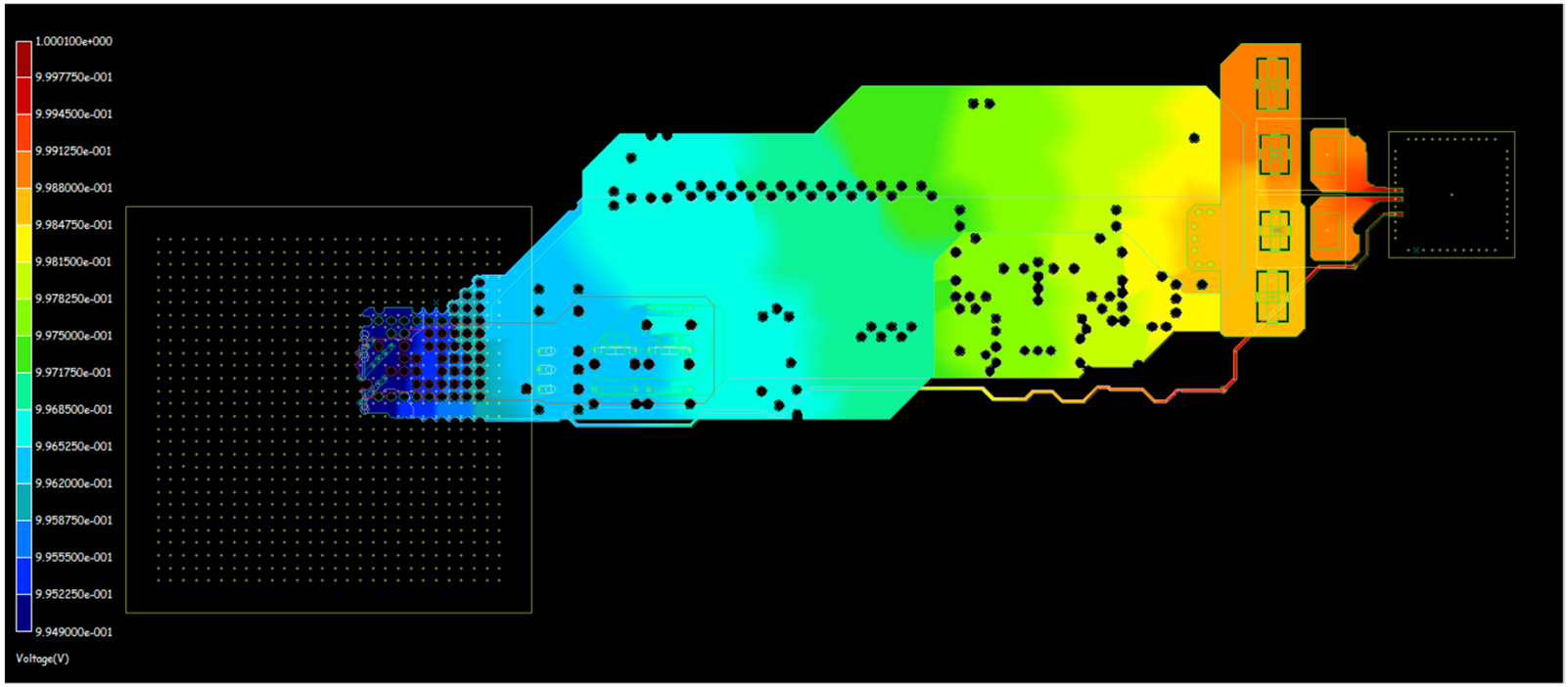


Recommended Dcap Scheme Optimized for PCB Design						Power Rail: VDD_DSPEVE_AVS		
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C162, 163	10	2	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C428, 439, 440, 455, 456	1.0	5	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C433, 438, 446, 452	0.47	4	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
C444, 464	0.1	2	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155R71C104KA55	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B1X7R1C104K050BC
Totals	27.1	13	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDD_DSPEVE_AVS

Derived from: Vdrop Analysis						
Name	Vin [V]	Vout [V]	Vdrop [V]	Current [A]	Reff [Ohms]	Target [mohms]
VDD_DSP_AVS	1.0000					
		0.9949	0.0051	1	0.0051	22.0

Routed on Layers
1
3
4
5



Dcap Loop Inductance: VDD_DSPEVE_AVS

- Decoupling Cap's Loop Inductance (LL) Range: 0.192 – 1.160 nH (@ 50 MHz)

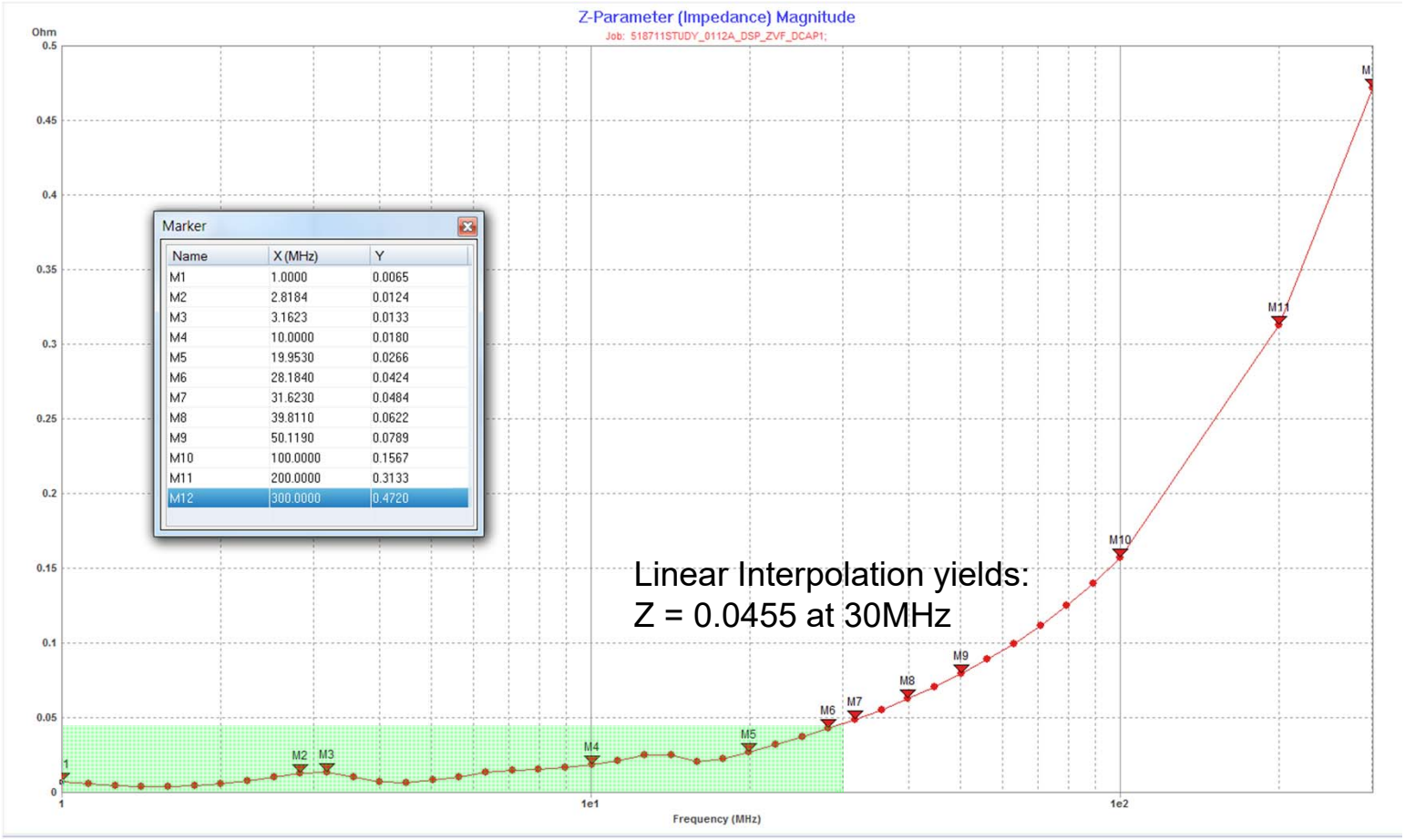
Capacitor Footprints (FP)	Footprint Types	Inductance	Code
	2-via, skinny-end exit	Highest	2vSEE
	2-via, wide-end exit		2vWEE
	2-via, wide-side exit		2vWSE
	4-via, wide-side exit		4vWSE
	via in-pad	Lowest	vIP

Port #	Cap Ref Des	v0112a Ref Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field K10 [mils]	Value [uF]	Size
1	C162	0.597	4vWSE	Top	574	10	0805
2	C163	0.606	4vWSE	Top	708	10	0805
3	C428	0.520	4vWSE	Top	716	1	0508
4	C433	0.611	2vWSE	Bottom, Under BGA	67	0.47	0402
5	C438	1.160	2vWEE	Bottom	413	0.47	0402
6	C439	0.776	4vWSE	Bottom	708	1.0	0508
7	C440	0.735	4vWSE	Bottom	573	1.0	0508
8	C446	1.130	2vWEE	Bottom	415	0.47	0402
9	C452	1.150	2vWEE	Bottom	423	0.47	0402
10	C455	0.637	4vWSE	Top	714	1	0508
11	C456	0.537	4vWSE	Top	580	1	0508
12	C444	0.201	2vWSE	Bottom, Under BGA	53	0.1	0402
13	C464	0.192	2vWSE	Bottom, Under BGA	150	0.1	0402
	Min	0.192					
	Max	1.160					
	Average	0.681					

Power Rail Loop Inductance

Port #	Cap Ref Des	v0112 8 LyrRef Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field K10 [mils]	Value [uF]	Size
14	C148	1.240	Power cap	Top	2311	47	1210
15	C158	1.150	Power cap	Top	2216.6	47	1210

Target Impedance: VDD_DSPEVE_AVS

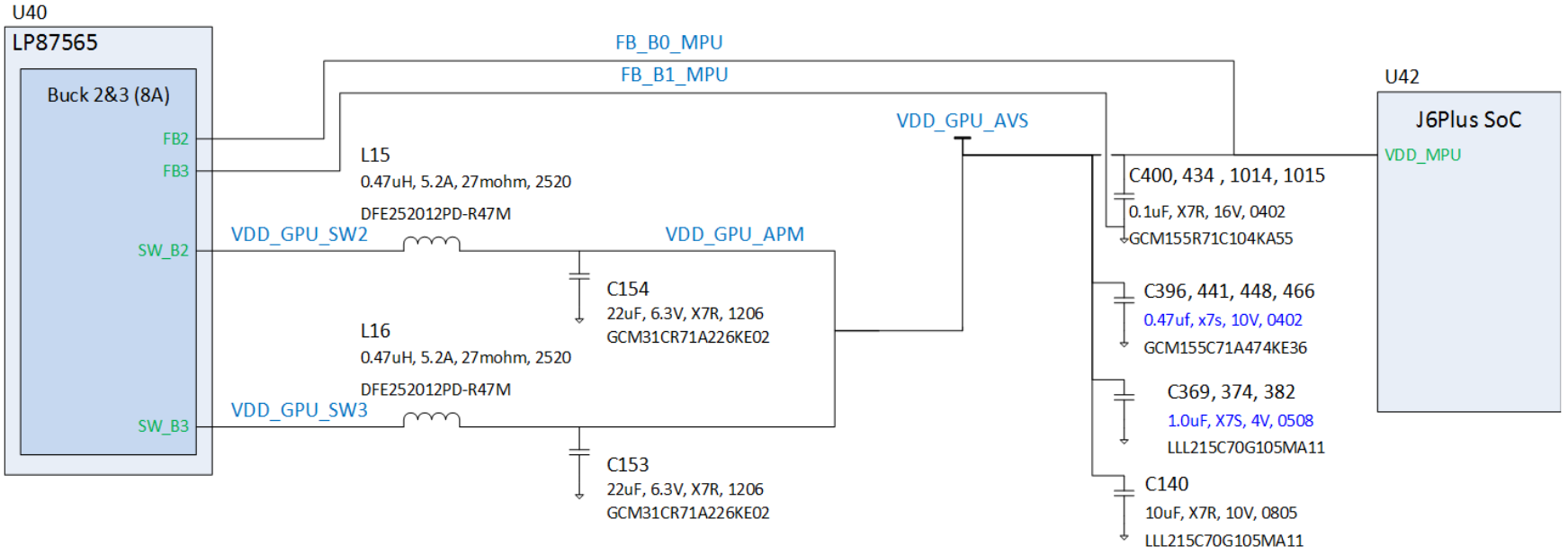


Green box = Power rail's Max Target Impedance of 40mOhm up to "Freq of Interest" 30 MHz

VDD_GPU_AVS POWER DOMAIN

VDD_GPU_AVS – Simplified Power SCH

J6Plus Ref – VDD_GPU_AVS Power Rail Model

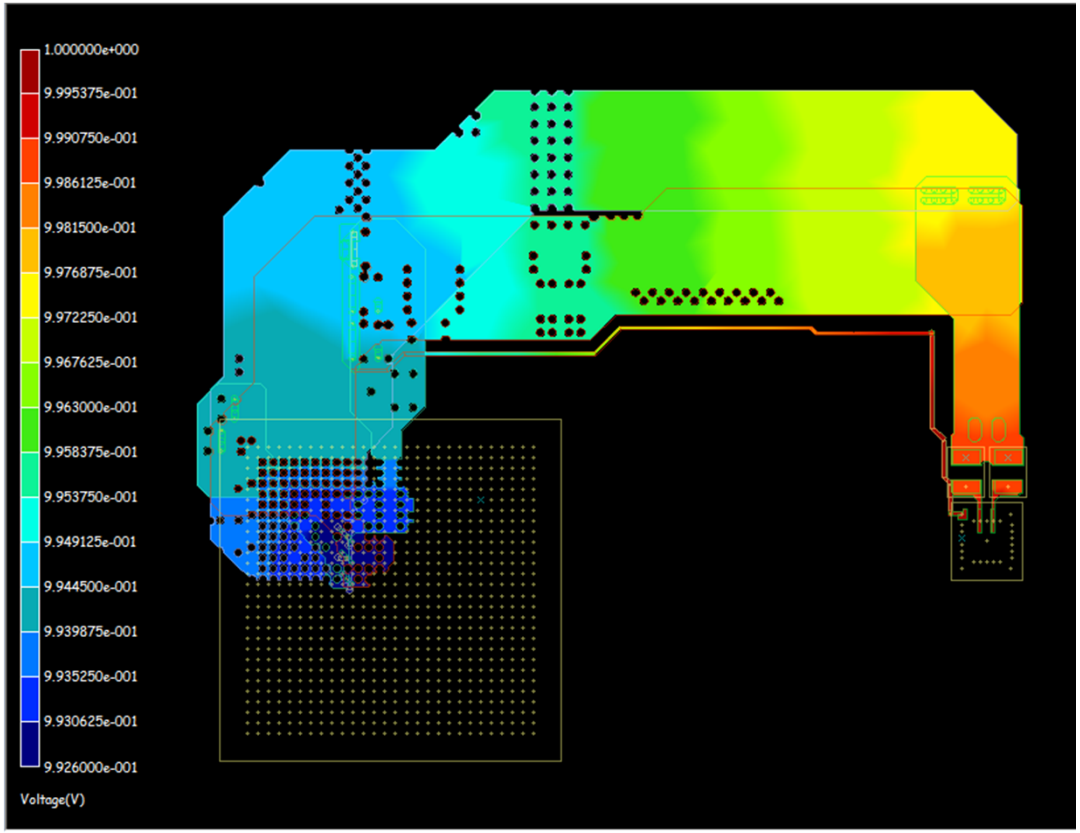


Recommended Dcap Scheme Optimized for PCB Design					Power Rail: VDD_GPU_AVS			
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C140	10	1	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C369, 374, 382	1.0	3	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C396, 441, 448, 466	0.47	4	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
C400, 434, 1014, 1015	0.1	4	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155R71C104KA55	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B1X7R1C104K050BC
Totals	18.9	12	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDD_GPU_AVS

Derived from: Vdrop Analysis						
Name	Vin [V]	Vout [V]	Vdrop [V]	Current [A]	Reff [Ohms]	Target [mohms]
VDD_GPU_AVS	1.0000					
		0.9926	0.0074	1	0.0074	13.0

Routed on Layers
1
3
4
5



Dcap Loop Inductance: VDD_GPU_AVS

- Decoupling Cap's Loop Inductance (LL) Range: 0.18 – 1.01 nH (@ 50 MHz)

Capacitor Footprints (FP)	Footprint Types	Inductance	Code
	2-via, skinny-end exit	Highest	2vSEE
	2-via, wide-end exit		2vWEE
	2-via, wide-side exit		2vWSE
	4-via, wide-side exit		4vWSE
	via in-pad	Lowest	vIP

Item #	Cap Ref Des	v0112a 8Lyr opt Ref PCB Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Pwr Ball-Field (ref ball =V10) [mils]	Value [uF]	Size
1	C140	0.522	4vWSE	Top	868	10	0805
2	C369	0.731	4vWSE	Bottom	868	1	0805
3	C374	0.39	4vWSE	Top	734	1	0402
4	C382	0.378	2vWEE	Top	594	1	0402
5	C396	0.763	2vWEE	Top	529	0.47	0402
6	C400	0.202	2vWEE	Top	470	0.1	0508
7	C434	0.2	2vWSE	Bottom, Under BGA	61	0.1	0508
8	C441	0.534	2vWSE	Bottom, Under BGA	15	0.47	0402
9	C448	0.852	2vWSE	Bottom, Under BGA	64	0.47	0402
10	C466	1.01	2vWSE	Bottom, Under BGA	142	0.47	0402
11	C1014	0.184	4vWSE	Top	491	0.1	0402
12	C1015	0.184	4vWSE	Top	526	0.1	0402

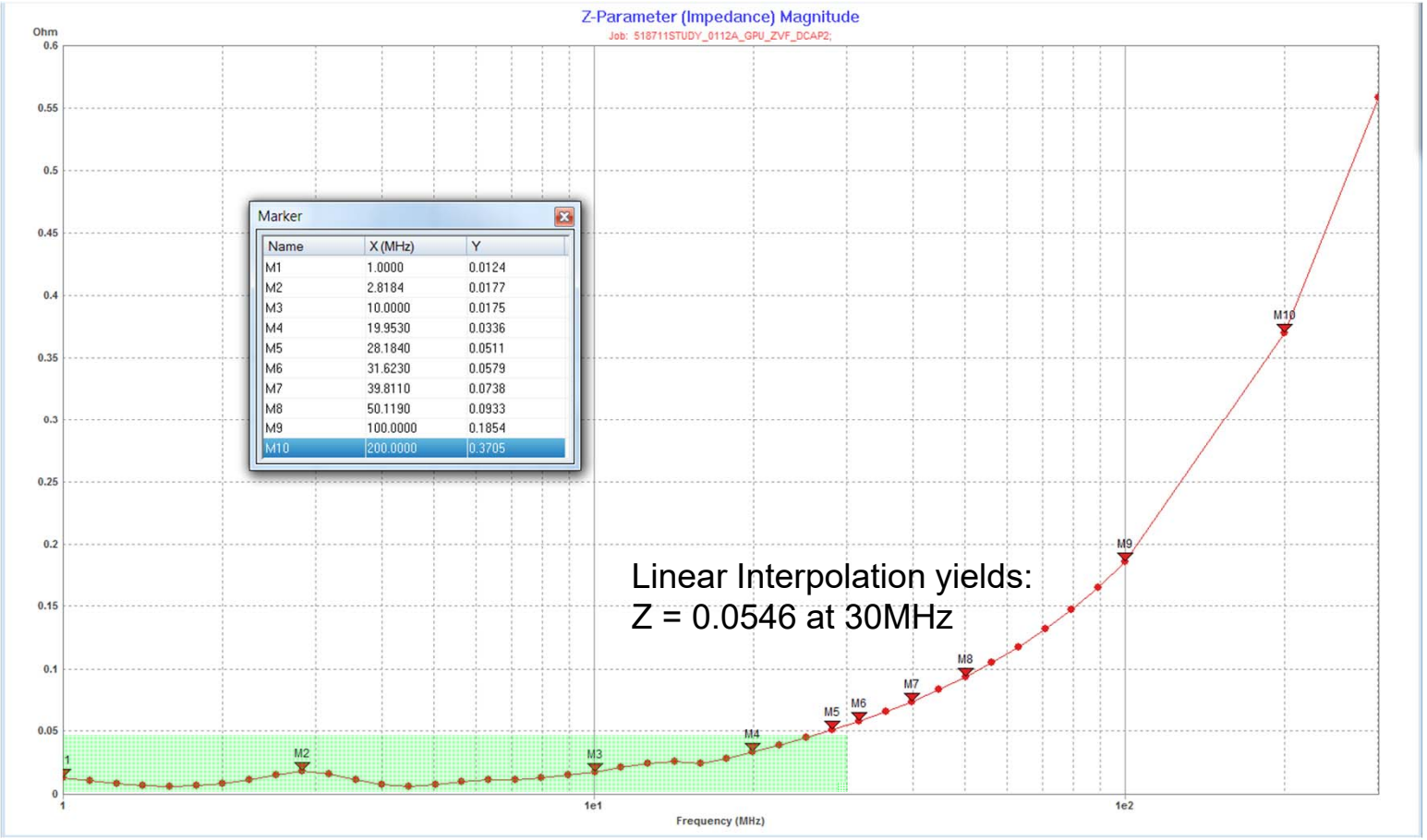
Min	0.18
Max	1.01
Average:	0.50

Notes:
1) Distances are wrt "middle of Ball Field", Ref pt between: U42-V10 to middle of Dcap's power pad unless specifed

Power Rail Loop Inductance

Item #	Cap Ref Des	v0112 Ref 8Lyr PCB Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Pwr Ball-Field (ref ball =V10) [mils]	Value [uF]	Size
13	C153	1.56	Power Cap	Top	1875.3	22	1206
14	C154	1.47	Power Cap	Top	1944.2	22	1206

Target Impedance: VDD_GPU_AVS

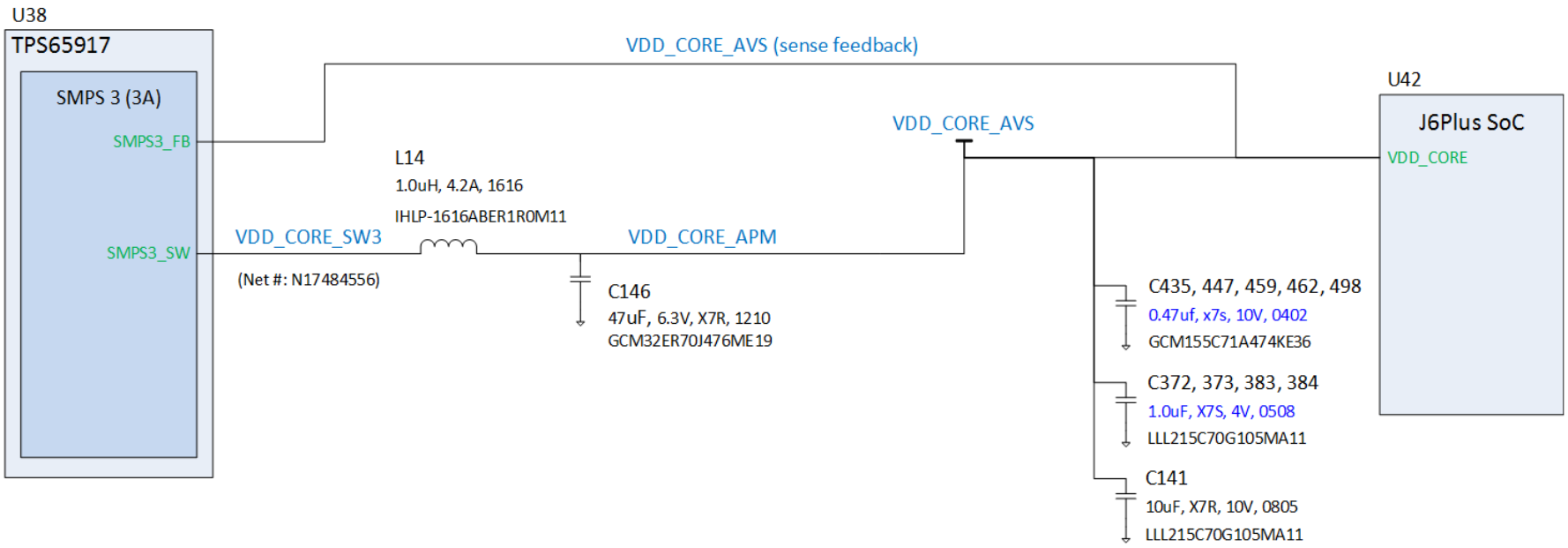


Green box = Power rail's Max Target Impedance of 48mOhm up to "Freq of Interest" 30 MHz

VDD_CORE_AVS POWER DOMAIN

VDD_CORE_AVS – Simplified Power SCH

J6Plus Ref – VDD_CORE_AVS Power Rail Model



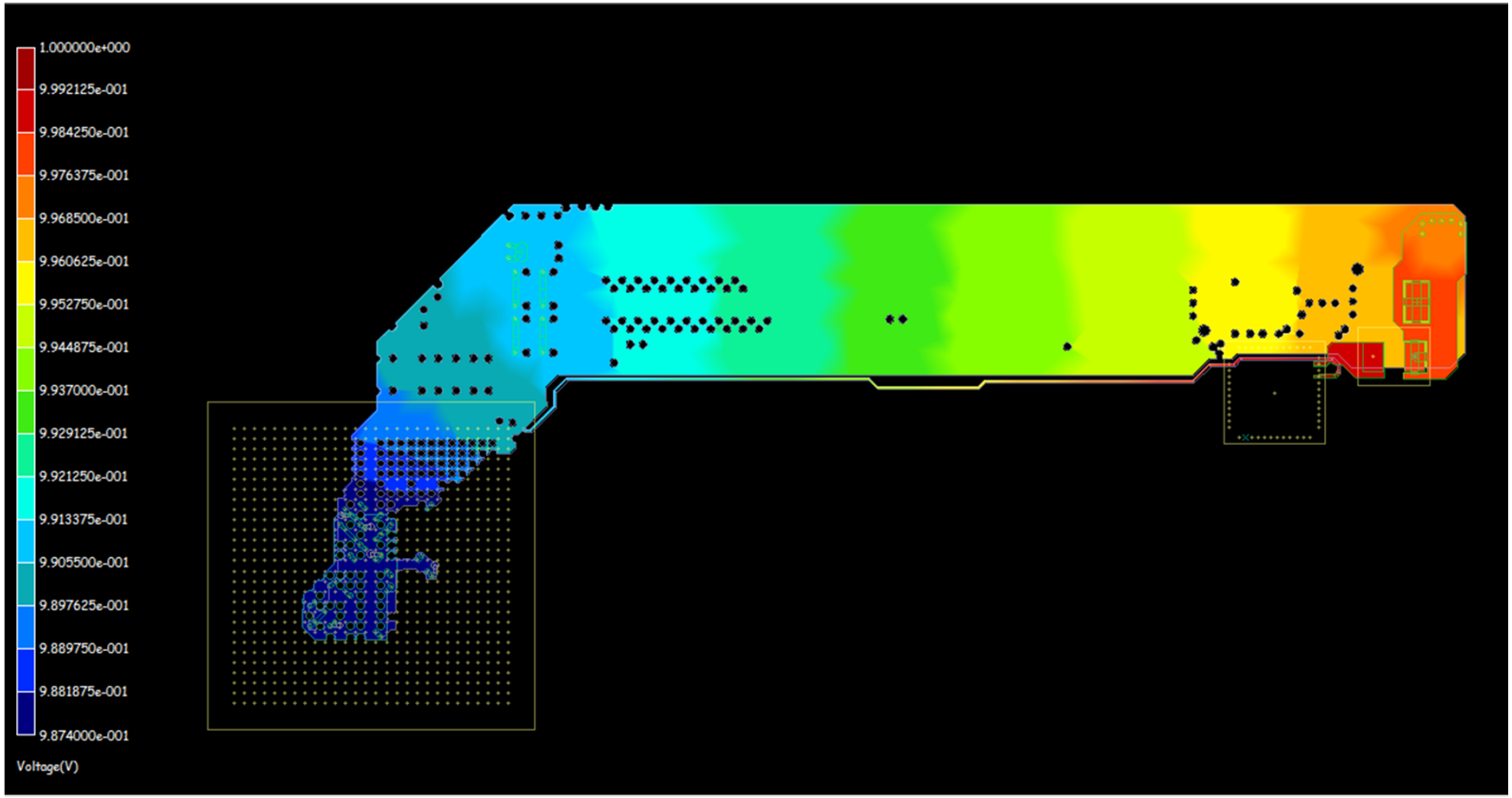
Recommended Dcap Scheme Optimized for PCB Design					Power Rail: VDD_CORE_AVS			
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C141	10	1	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C372, 373, 383, 384	1.0	4	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C435, 447, 459, 462, 498	0.47	5	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
Totals	16.4	10	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDD_CORE_AVS

Derived from: Vdrop Analysis

Name	Vin [V]	Vout [V]	Reff [Ohms]	Target [mohms]
VDD_CORE_AVS	1.0000			
		0.9874	0.0126	32.0

Routed on Layers
1
3
4



Dcap Loop Inductance: VDD_CORE_AVS

- Decoupling Cap's Loop Inductance (LL) Range: 0.960 – 1.32 nH (@ 50 MHz)

Capacitor Footprints (FP)		Footprint Types	Inductance	Code
		2-via, skinny-end exit	Highest	2vSEE
		2-via, wide-end exit		2vWEE
		2-via, wide-side exit		2vWSE
		4-via, wide-side exit		4vWSE
		via in-pad	Lowest	vIP

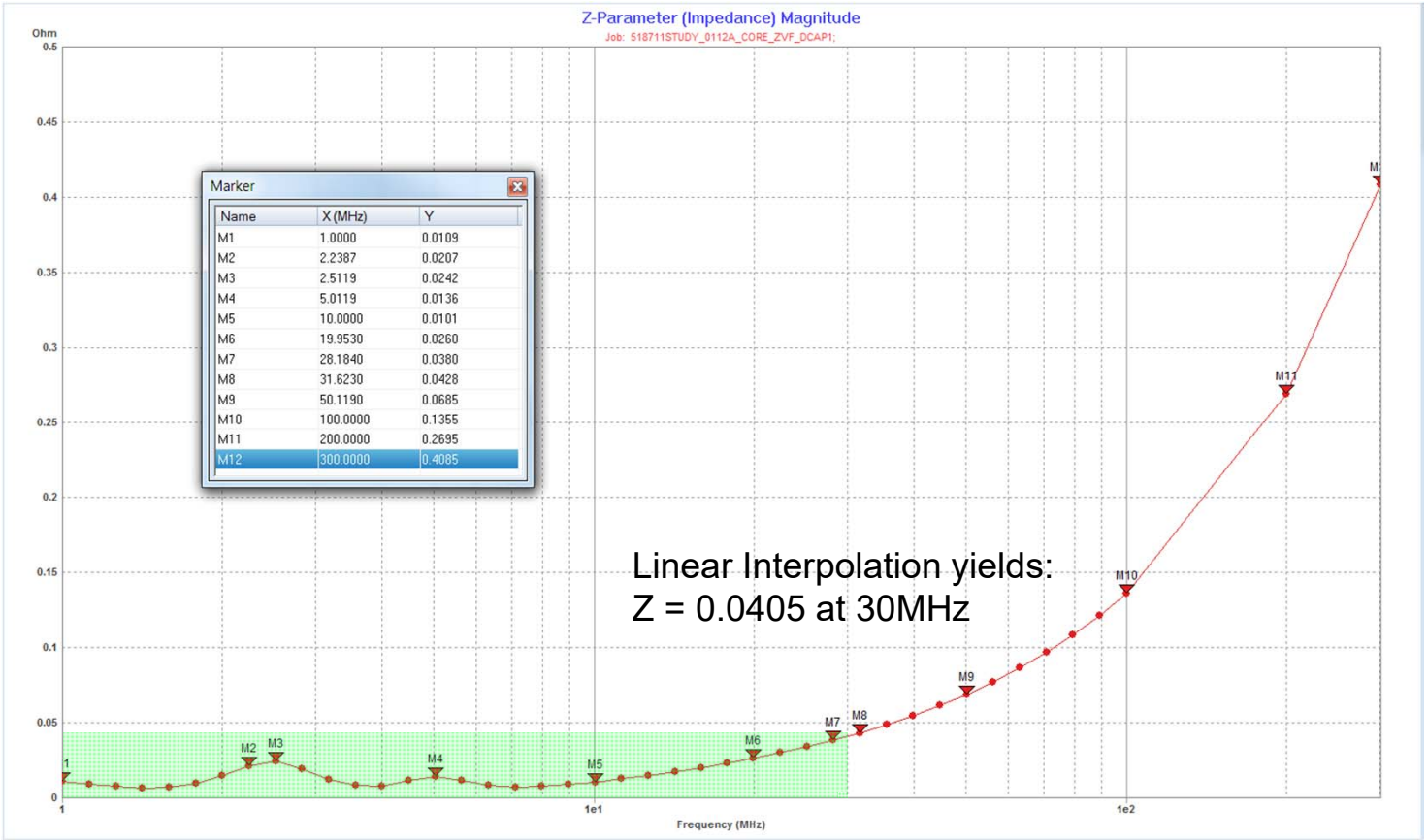
Item #	Cap Ref Des	v0112 8 lyr PCB Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field R13 [mils]	Value [uF]	Size
1	C141	1.269	4vWSE	Top	1041	10	0805
2	C372	0.957	4vWSE	Top	931	1	0508
3	C373	0.993	4vWSE	Top	976	1	0508
4	C383	0.979	4vWSE	Top	808	1	0508
5	C384	1.022	4vWSE	Top	860	1	0508
6	C498	1.150	2vWSE	Bottom, Under BGA	245	0.47	0402
7	C435	1.083	2vWSE	Bottom, Under BGA	129	0.47	0402
8	C447	1.067	2vWSE	Bottom, Under BGA	74	0.47	0402
9	C459	1.098	2vWSE	Bottom, Under BGA	20	0.47	0402
10	C462	1.317	2vWSE	Bottom, Under BGA	220	0.47	0402
	Min	0.96					
	Max	1.32					
	Average:	1.09					

Notes:
1) Distances are wrt "middle of Ball Field", Ref pt between: U42-R13 to middle of Dcap's power pad unless specifed

Power Rail Loop Inductance

Item #	Cap Ref Des	v0112 8 lyr Ref Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field R13 [mils]	Value [uF]	Size
11	C146	2.480	Power Cap	Top	3346.3	47.00	1210

Target Impedance: VDD_CORE_AVS

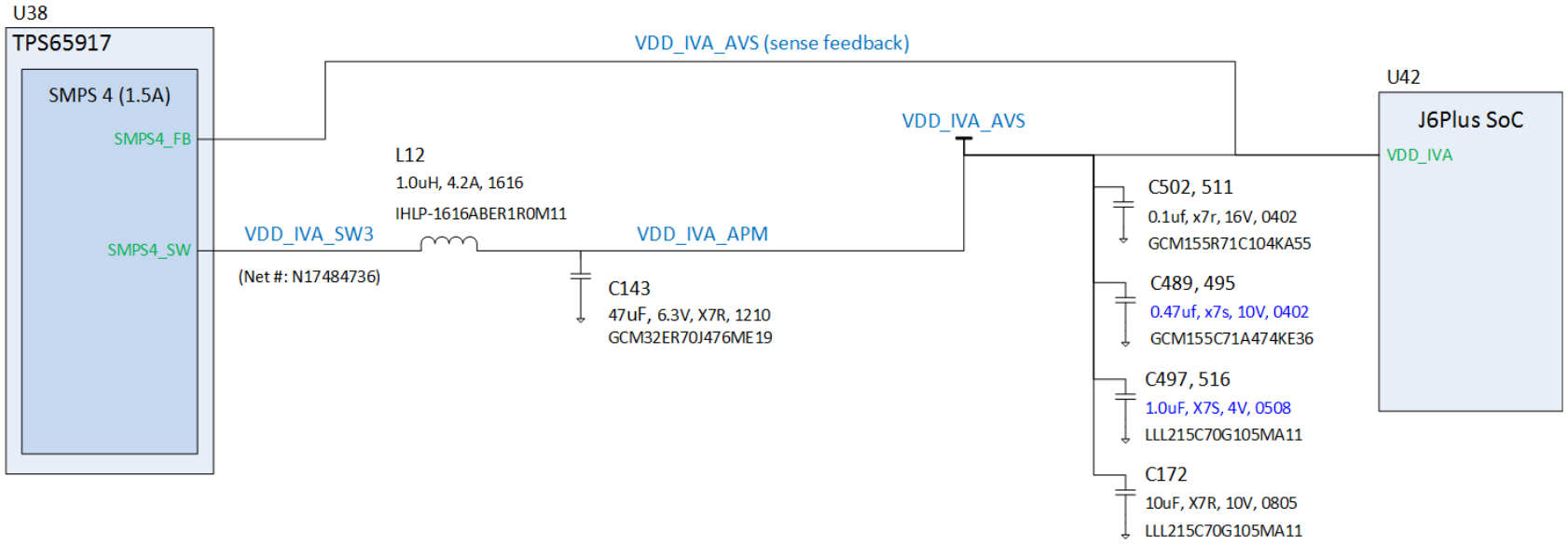


Green box = Power rail's Max Target Impedance of 40mOhm up to "Freq of Interest" 30 MHz

VDD_IVA_AVS POWER DOMAIN

VDD_IVA_AVS – Simplified Power SCH

J6Plus Ref – VDD_IVA_AVS Power Rail Model



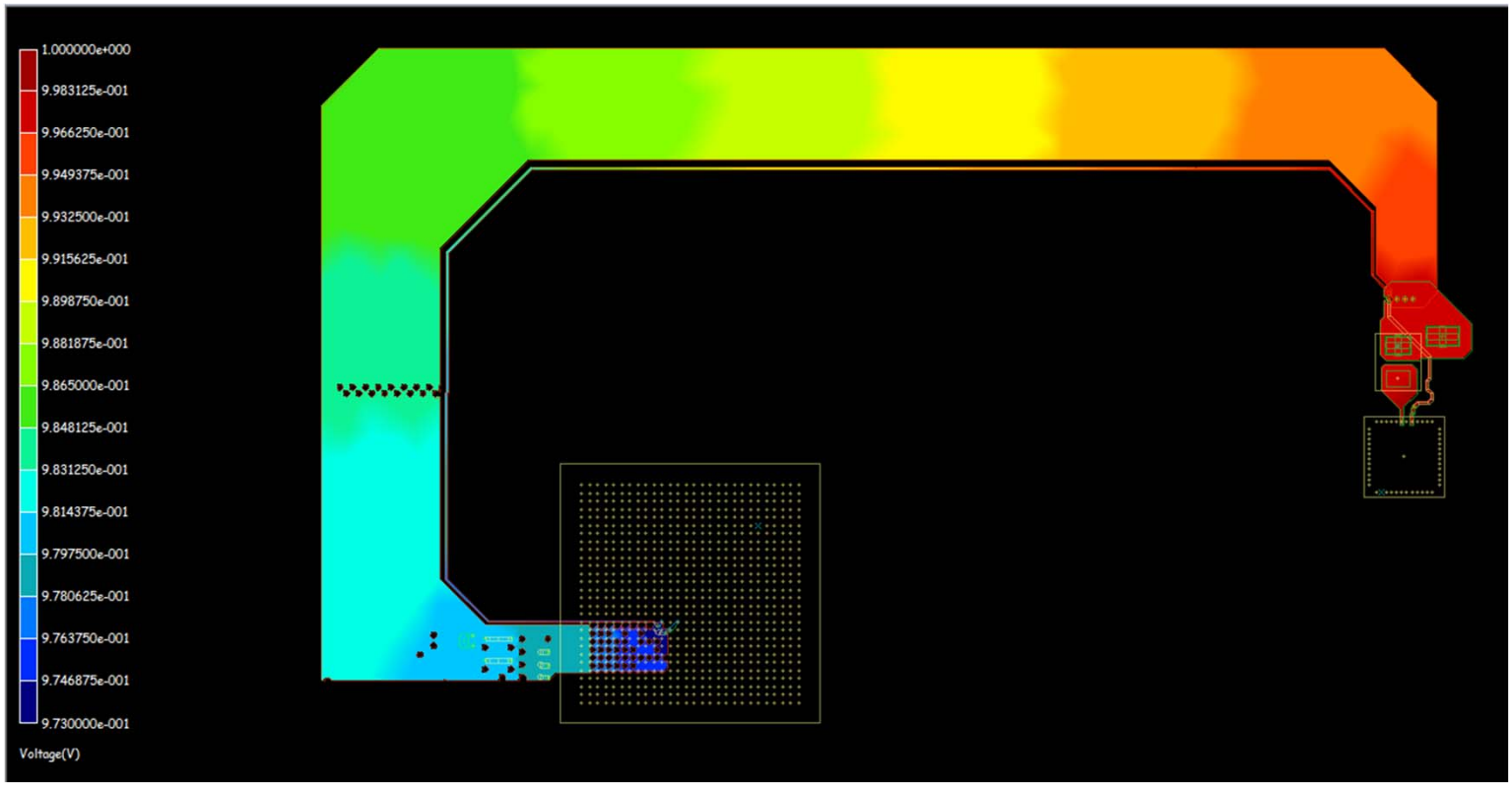
Recommended Dcap Scheme Power Rail: VDD_IVA_AVS

Ref Des	Vaule [uF]	Qty	Description #1	Manufacturer #1	Manf #1 P/N	Description #2	Manufacturer #2	Manf #2 P/N
C172	10	1	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C497, 516	1.0	2	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C489, 495	0.47	2	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
C502, 511	0.1	2	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155R71C104KA55	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B1X7R1C104K050BC
Totals	13.14	7	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDD_IVA_AVS

Derived from: Vdrop Analysis						
Name	**Vin [V]**	**Vout [V]**	**Vdrop [V]**	**Current [A]**	**Reff [Ohms]**	**Target [mohms]**
VDD_IVA_AVS	1.0000					
		0.9730	0.0270	1	0.027	48.0

Routed on Layers
1
5



Dcap Loop Inductance: VDD_IVA_AVS

- Decoupling Cap's Loop Inductance (LL) Range: 1.15 – 2.37 nH (@ 50 MHz)

Capacitor Footprints (FP)	Footprint Types	Inductance	Code
	2-via, skinny-end exit	Highest	2vSEE
	2-via, wide-end exit		2vWEE
	2-via, wide-side exit		2vWSE
	4-via, wide-side exit		4vWSE
	via in-pad	Lowest	vIP

Item #	Cap Ref Des	v0112a Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field(U19) [mils]	Value [uF]	Size
1	C172	2.37	4vWSE	Top	809	10	0805
2	C497	1.72	4vWSE	Bottom	672	1	0508
3	C516	1.73	4vWSE	Bottom	681	1	0508
4	C489	1.15	2vWEE	Bottom, Under BGA	43	0.47	0402
5	C495	1.78	2vWEE	Bottom	513	0.47	0402
6	C511	1.89	2vWEE	Bottom	524	0.1	0402
7	C502	1.82	2vWEE	Bottom	540	0.1	0402

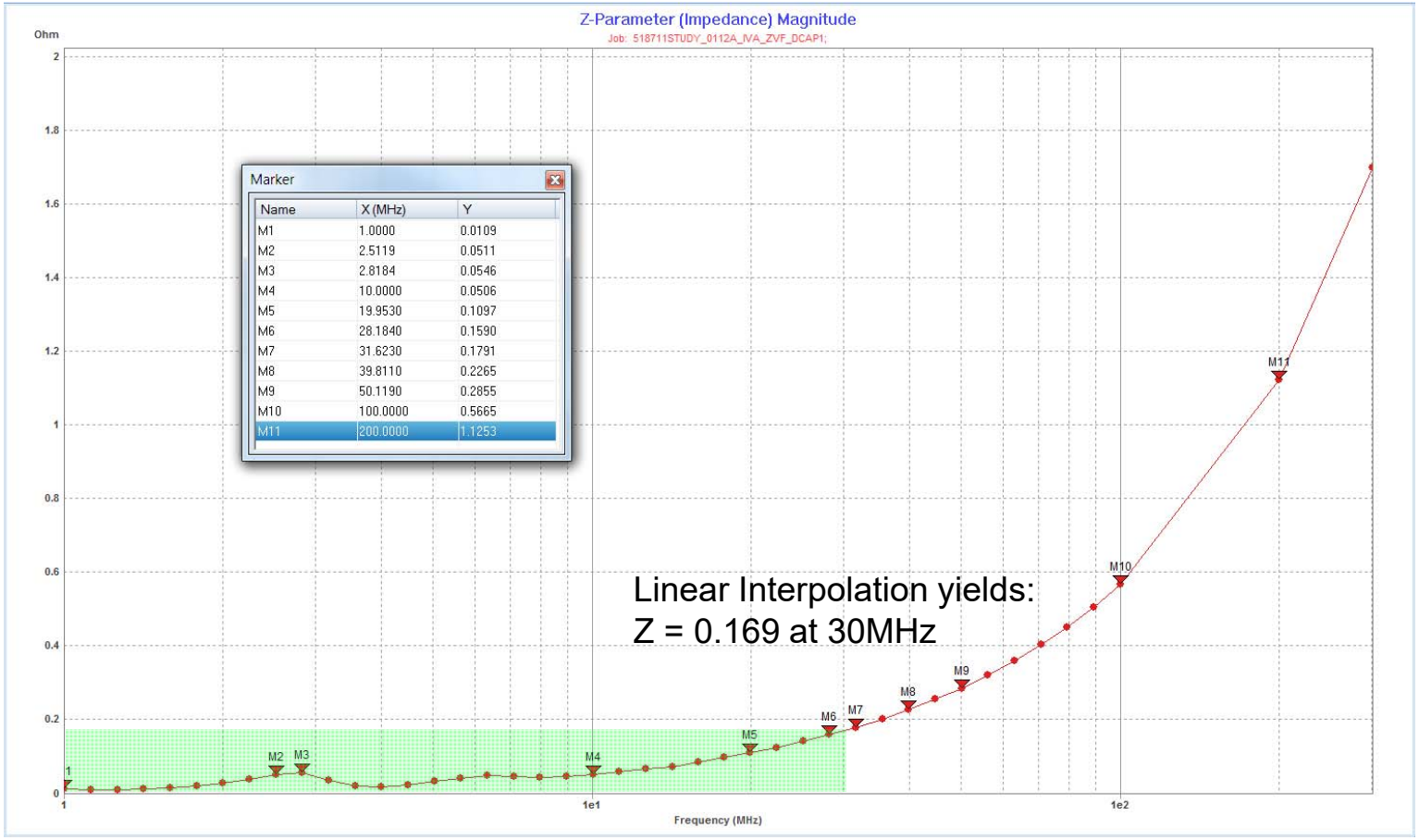
Min	1.15
Max	2.37
Average	1.78

Notes:
1) Distances are wrt "middle of Ball Field", Ref pt between: U42-U19 to middle of Dcap's power pad unless specifed

Power Rail Loop Inductance

Item #	Cap Ref Des	v0112a 8 lyr Loop Inductacne 1@ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field(U19) [mils]	Value [uF]	Size
8	C143	6.02	Power Cap	Top	3239.3	47.0	1210

Target Impedance: VDD_IVA_AVS

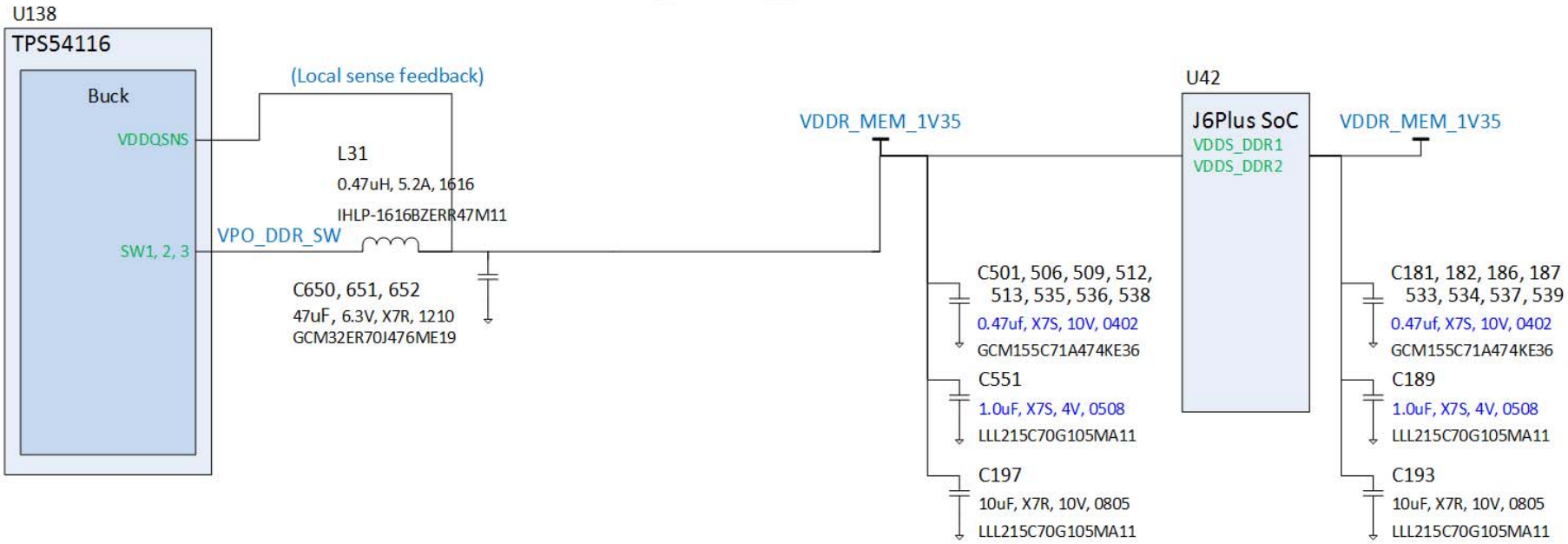


Green box = Power rail's Max Target Impedance of 179mOhm up to "Freq of Interest" 30 MHz

VDDR_MEM_1V35 POWER DOMAIN

VDDR_MEM_1V35 – Simplified Power SCH

J6Plus Ref – VDDR_MEM_1V35 Power Rail Model

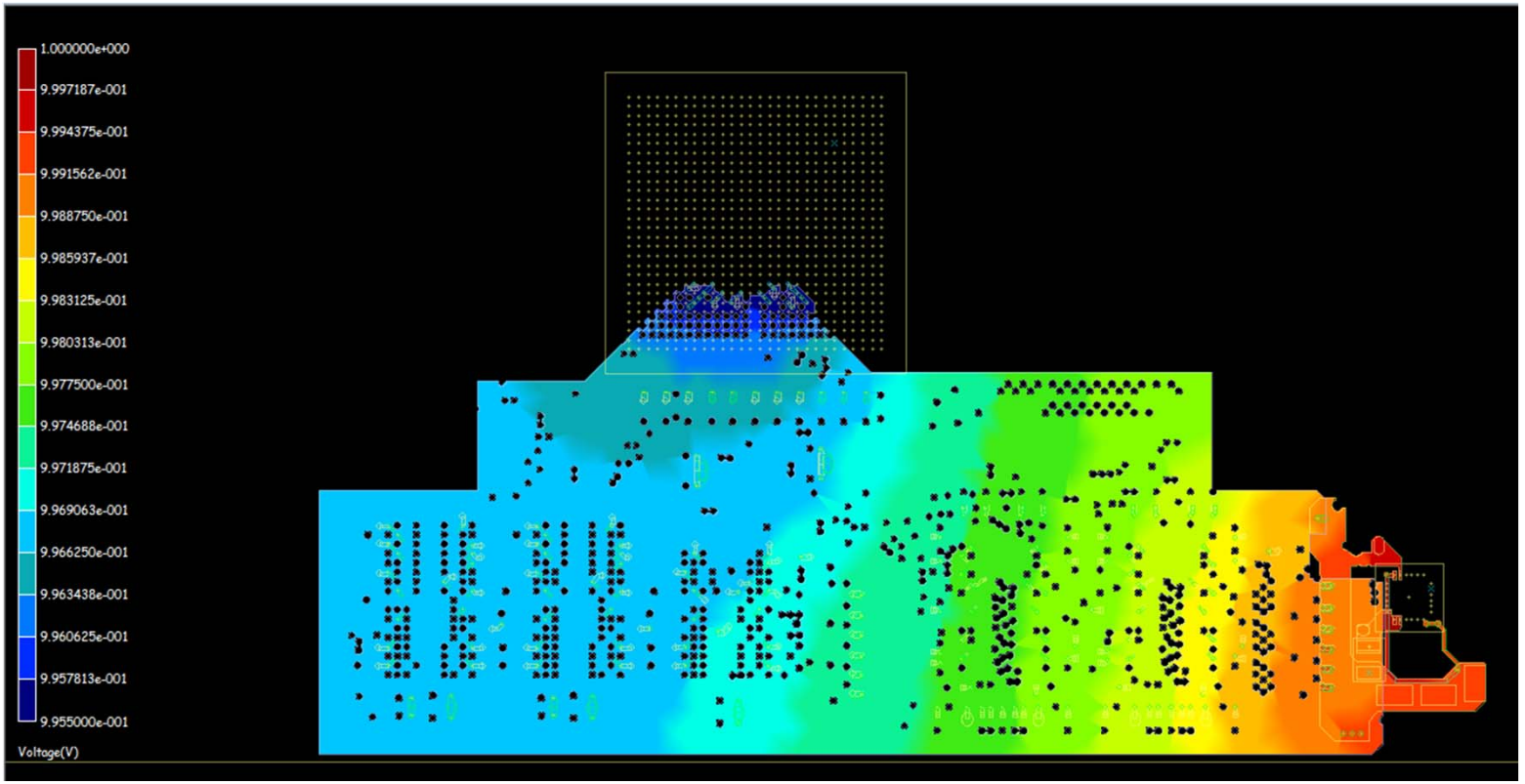


Recommended Dcap Scheme Optimized for PCB Design					Power Rail:	VDDR_MEM_1V35			
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C193, 197	10	2	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C189, 551	1.0	2	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C181, 182, 186, 187, 533, 534, 537, 539, 501, 506, 509, 512, 513, 535, 536, 538	0.47	16	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
Totals	29.5	20	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDDR_MEM_1V35

Derived from: Vdrop Analysis						
Name	Vin [V]	Vout [V]	Vdrop [V]	Current [A]	Reff [Ohms]	Target [mohms]
VDDR_MEM_1V35	1.0000					
0		0.9955	0.0045	1	0.0045	18.0

Routed on Layers
4
8



Loop Inductance: VDDR_MEM_1V35

- Decoupling Cap's Loop Inductance (LL) Range: 0.80 – 1.35 nH (@ 50 MHz)

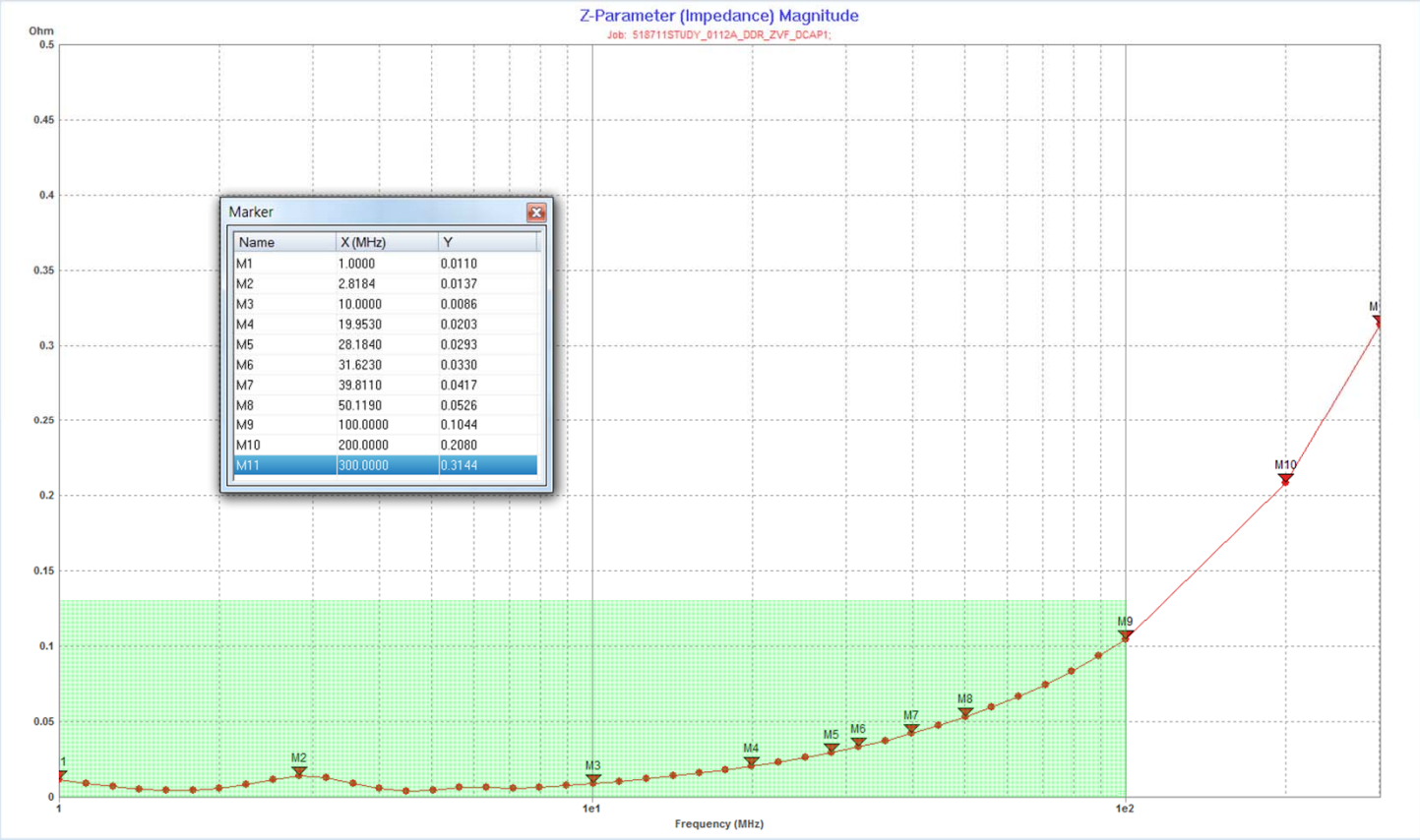
Capacitor Footprints (FP)	Footprint Types	Inductance	Code
	2-via, skinny-end exit	Highest	2vSEE
	2-via, wide-end exit		2vWEE
	2-via, wide-side exit		2vWSE
	4-via, wide-side exit		4vWSE
	via in-pad	Lowest	vIP

Item #	Cap Ref Des	v0112a Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field [mils]	Value [uF]	Size
1	C181	1.32	2vWEE	Bottom	408	0.47	0402
2	C182	1.29	2vWEE	Bottom	370	0.47	0402
3	C186	1.02	2vWEE	Top	559	0.47	0402
4	C187	1.31	2vWEE	Bottom	417	0.47	0402
5	C189	0.96	4vWSE	Bottom	621	1.0	0508
6	C193	0.89	4vWSE	Top	616	10	0805
7	C197	0.80	4vWSE	Top	646	10	0805
8	C501	1.26	2vWEE	Bottom, Under BGA	107	0.47	0402
9	C506	1.35	2vWEE	Bottom, Under BGA	173	0.47	0402
10	C509	1.30	2vWEE	Bottom, Under BGA	112	0.47	0402
11	C512	1.16	2vWSE	Bottom, Under BGA	45	0.47	0402
12	C513	1.09	2vWSE	Bottom, Under BGA	97	0.47	0402
13	C533	0.92	2vWEE	Top	380	0.47	0402
14	C534	1.34	2vWEE	Bottom	446	0.47	0402
15	C535	1.31	2vWEE	Bottom	492	0.47	0402
16	C536	0.81	2vWEE	Top	368	0.47	0402
17	C537	0.91	2vWEE	Top	505	0.47	0402
18	C538	0.87	2vWEE	Top	457	0.47	0402
19	C539	1.29	2vWEE	Bottom	387	0.47	0402
20	C551	0.91	4vWSE	Bottom	638	1.0	0508

Min	0.80
Max	1.35
Average	1.11

Notes:
1) Distances are wrt "middle of Ball Field", Ref pt between: U5000-N10 to middle of Dcap's power pad unless specifed

Target Impedance: VDDR_MEM_1V35

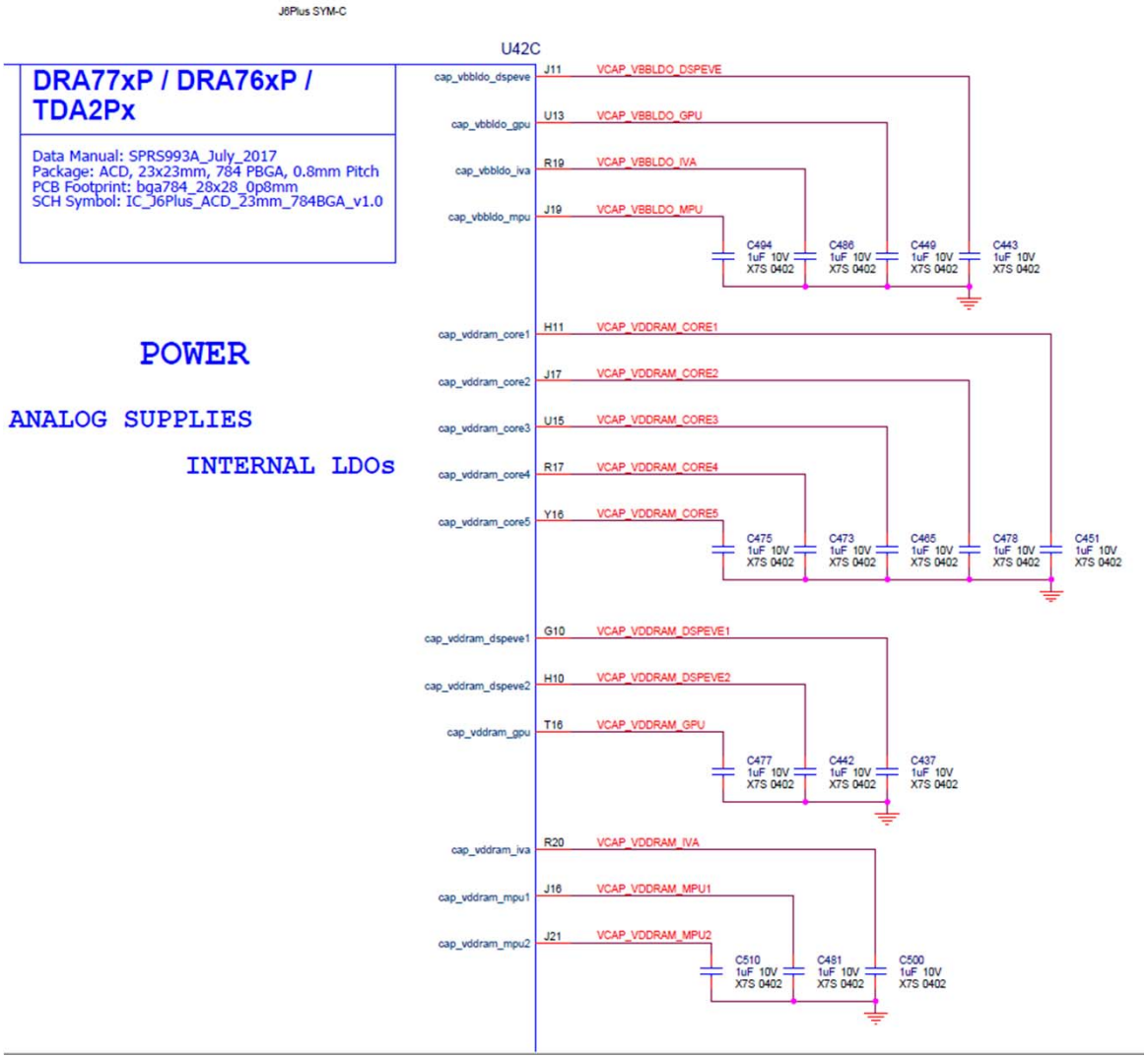


Green box = Power rail's Max Target Impedance of 130mOhm up to "Freq of Interest" 100 MHz

VCAP_XXX
POWER DOMAIN

Recommended Dcap Scheme Optimized for PCB Design				Power Rail:	VCAP_xxx			
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C494, 486, 449, 443, 475, 473, 465, 478, 451, 477, 442, 437, 510, 481, 500	1.0	15	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
Totals	15.0	15	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

VCAP_xxx – Simplified SCH



Loop Inductance – VCAP_xxx

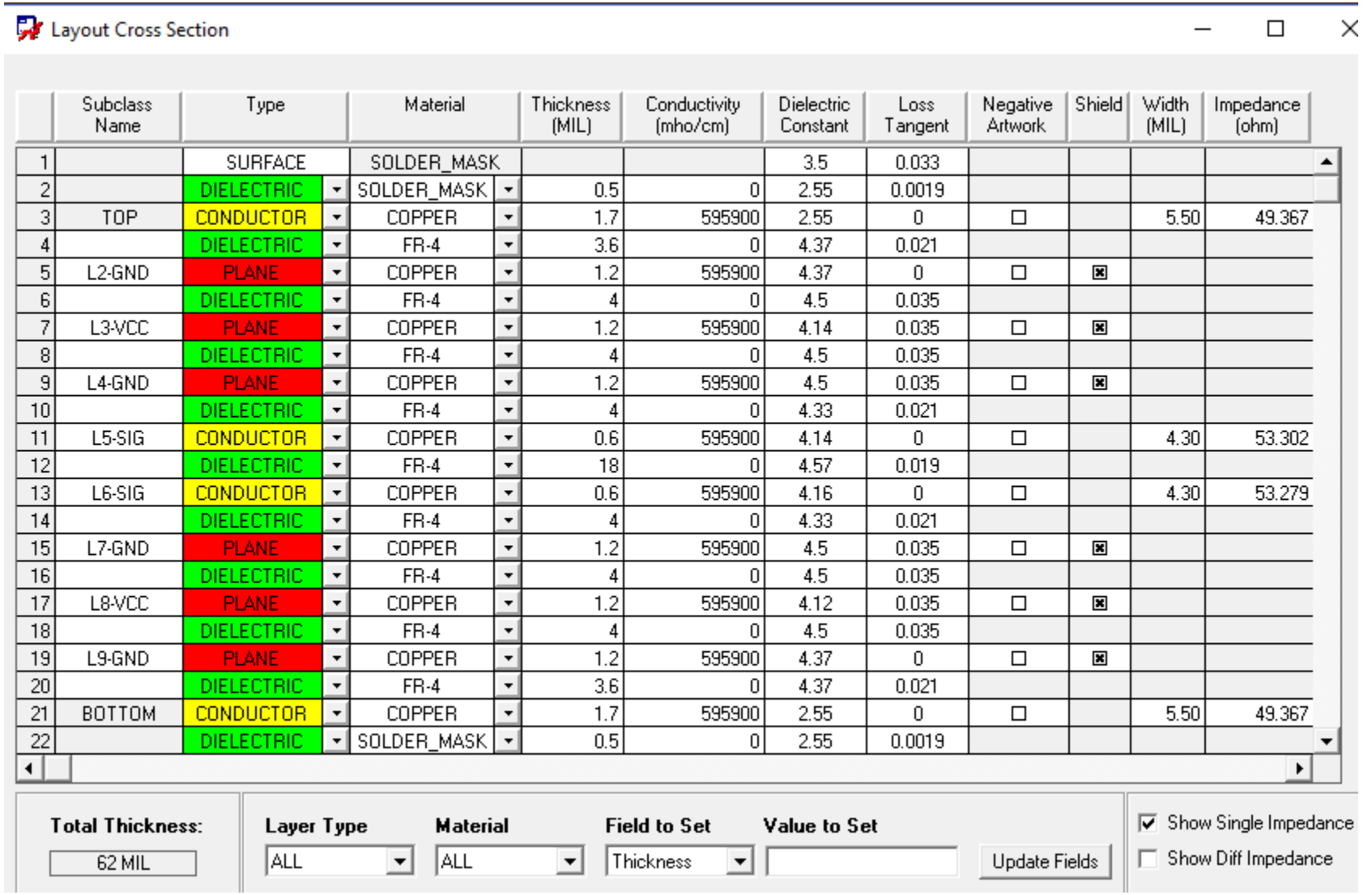
- Decoupling Cap's Loop Inductance (LL) Range: 1.17 – 1.61 nH (@ 50 MHz)

Capacitor Footprints (FP)		Footprint Types	Inductance	Code
		2-via, skinny-end exit	Highest	2vSEE
		2-via, wide-end exit		2vWEE
		2-via, wide-side exit		2vWSE
		4-via, wide-side exit		4vWSE
		via in-pad	Lowest	vIP

Item #	Cap Ref Des	Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Value [uF]	Size
1	C437	1.532	2vWEE	Bottom, Under BGA	1	0402
2	C442	1.606	2vWEE	Bottom, Under BGA	1	0402
3	C443	1.61	2vWEE	Bottom, Under BGA	1	0402
4	C449	1.366	2vWEE	Bottom, Under BGA	1	0402
5	C451	1.39	2vWEE	Bottom, Under BGA	1	0402
6	C465	1.17	2vWEE	Bottom, Under BGA	1	0402
7	C473	1.386	2vWEE	Bottom, Under BGA	1	0402
8	C475	1.409	2vWEE	Bottom, Under BGA	1	0402
9	C477	1.49	2vWEE	Bottom, Under BGA	1	0402
10	C478	1.52	2vWEE	Bottom, Under BGA	1	0402
11	C481	1.495	2vWEE	Bottom, Under BGA	1	0402
12	C486	1.41	2vWEE	Bottom, Under BGA	1	0402
13	C494	1.4333	2vWEE	Bottom, Under BGA	1	0402
14	C500	1.535	2vWEE	Bottom, Under BGA	1	0402
15	C510	1.49	2vWEE	Bottom, Under BGA	1	0402
	Min	1.17				
	Max	1.61				

10 LAYER PCB - J6P/TDA2P REF STUDY PIA

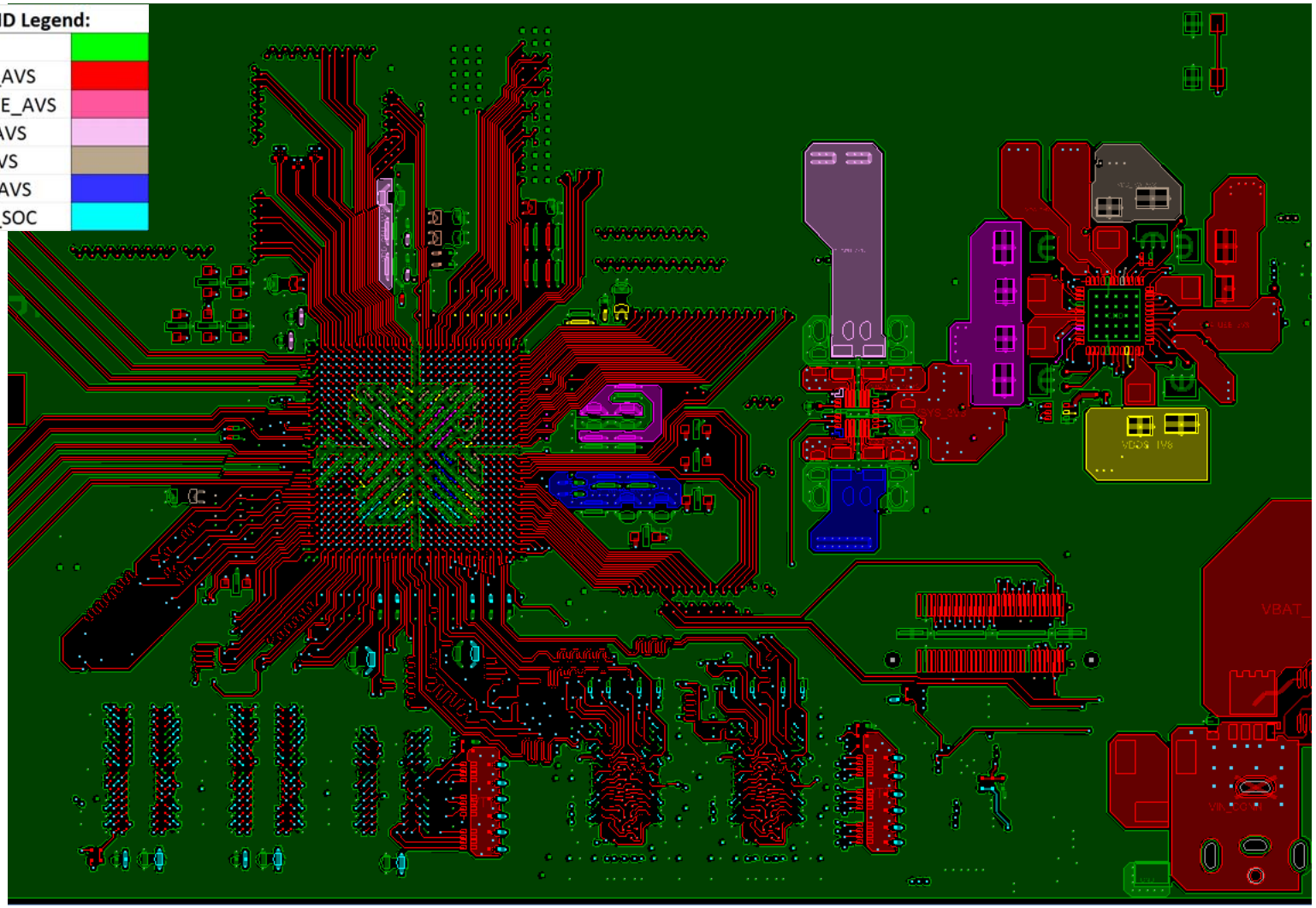
10-Layer PCB Stack-up



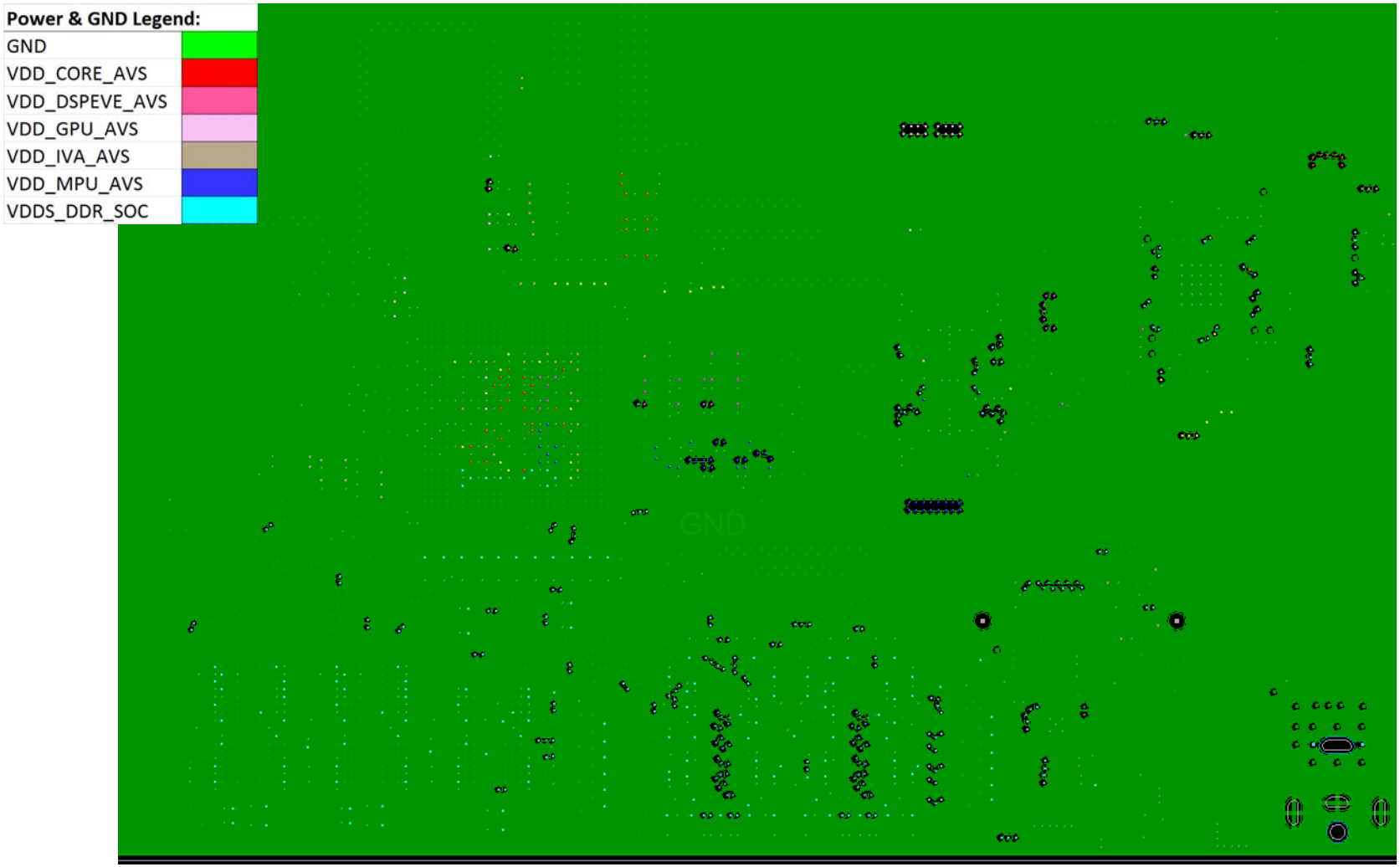
	Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MIL)	Impedance (ohm)
1		SURFACE	SOLDER_MASK			3.5	0.033				
2		DIELECTRIC	SOLDER_MASK	0.5	0	2.55	0.0019				
3	TOP	CONDUCTOR	COPPER	1.7	595900	2.55	0	☐		5.50	49.367
4		DIELECTRIC	FR-4	3.6	0	4.37	0.021				
5	L2-GND	PLANE	COPPER	1.2	595900	4.37	0	☐	☒		
6		DIELECTRIC	FR-4	4	0	4.5	0.035				
7	L3-VCC	PLANE	COPPER	1.2	595900	4.14	0.035	☐	☒		
8		DIELECTRIC	FR-4	4	0	4.5	0.035				
9	L4-GND	PLANE	COPPER	1.2	595900	4.5	0.035	☐	☒		
10		DIELECTRIC	FR-4	4	0	4.33	0.021				
11	L5-SIG	CONDUCTOR	COPPER	0.6	595900	4.14	0	☐		4.30	53.302
12		DIELECTRIC	FR-4	18	0	4.57	0.019				
13	L6-SIG	CONDUCTOR	COPPER	0.6	595900	4.16	0	☐		4.30	53.279
14		DIELECTRIC	FR-4	4	0	4.33	0.021				
15	L7-GND	PLANE	COPPER	1.2	595900	4.5	0.035	☐	☒		
16		DIELECTRIC	FR-4	4	0	4.5	0.035				
17	L8-VCC	PLANE	COPPER	1.2	595900	4.12	0.035	☐	☒		
18		DIELECTRIC	FR-4	4	0	4.5	0.035				
19	L9-GND	PLANE	COPPER	1.2	595900	4.37	0	☐	☒		
20		DIELECTRIC	FR-4	3.6	0	4.37	0.021				
21	BOTTOM	CONDUCTOR	COPPER	1.7	595900	2.55	0	☐		5.50	49.367
22		DIELECTRIC	SOLDER_MASK	0.5	0	2.55	0.0019				

10-Layer PDN Overview – Lyr 1/Top (Signal-1)

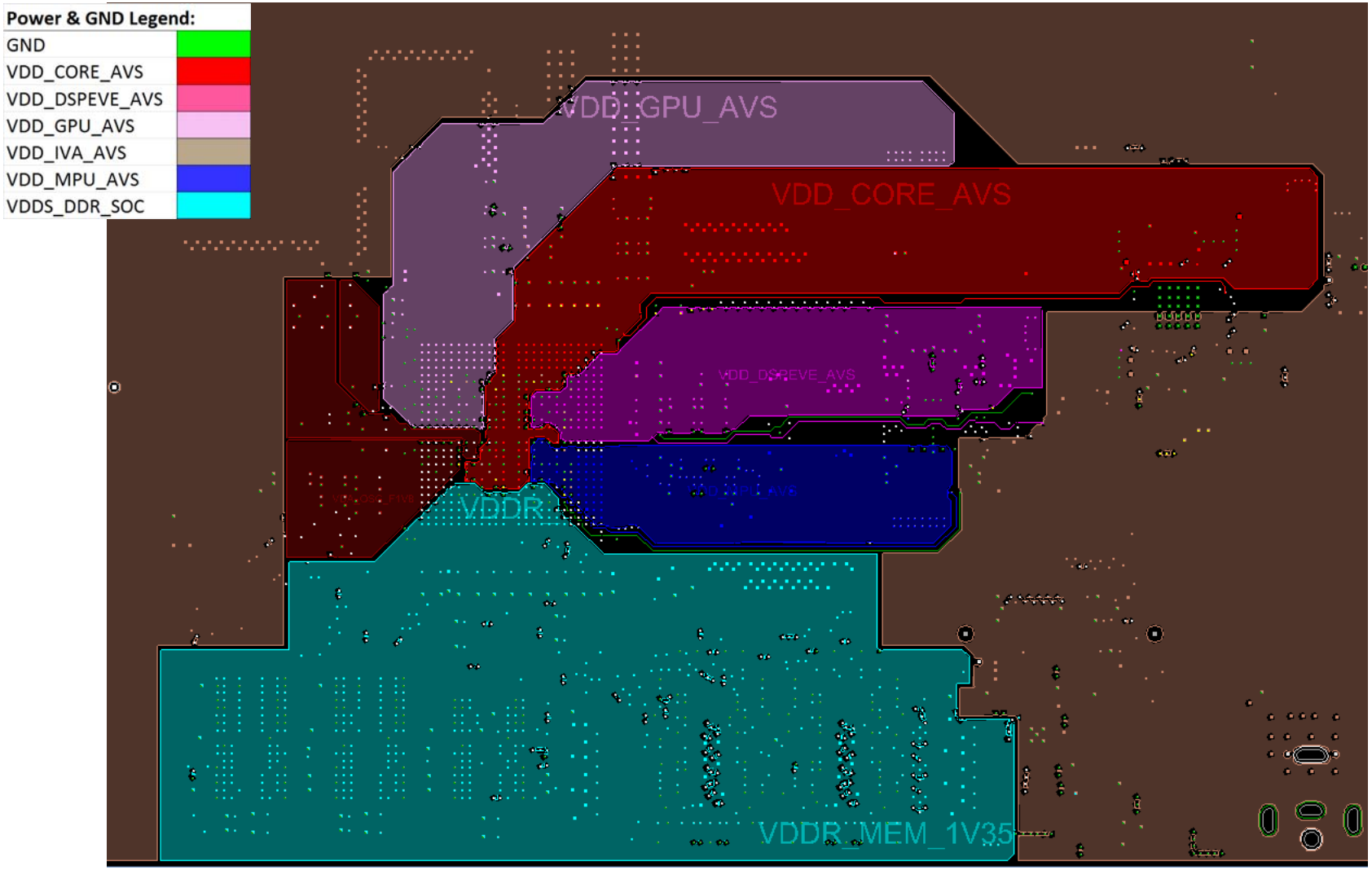
Power & GND Legend:	
GND	
VDD_CORE_AVS	
VDD_DSPEVE_AVS	
VDD_GPU_AVS	
VDD_IVA_AVS	
VDD_MPU_AVS	
VDDS_DDR_SOC	



10-Layer PDN Overview – Lyrs-2, 4, 7 & 9 Gnd net (Planes–1, 3, 4 & 6)

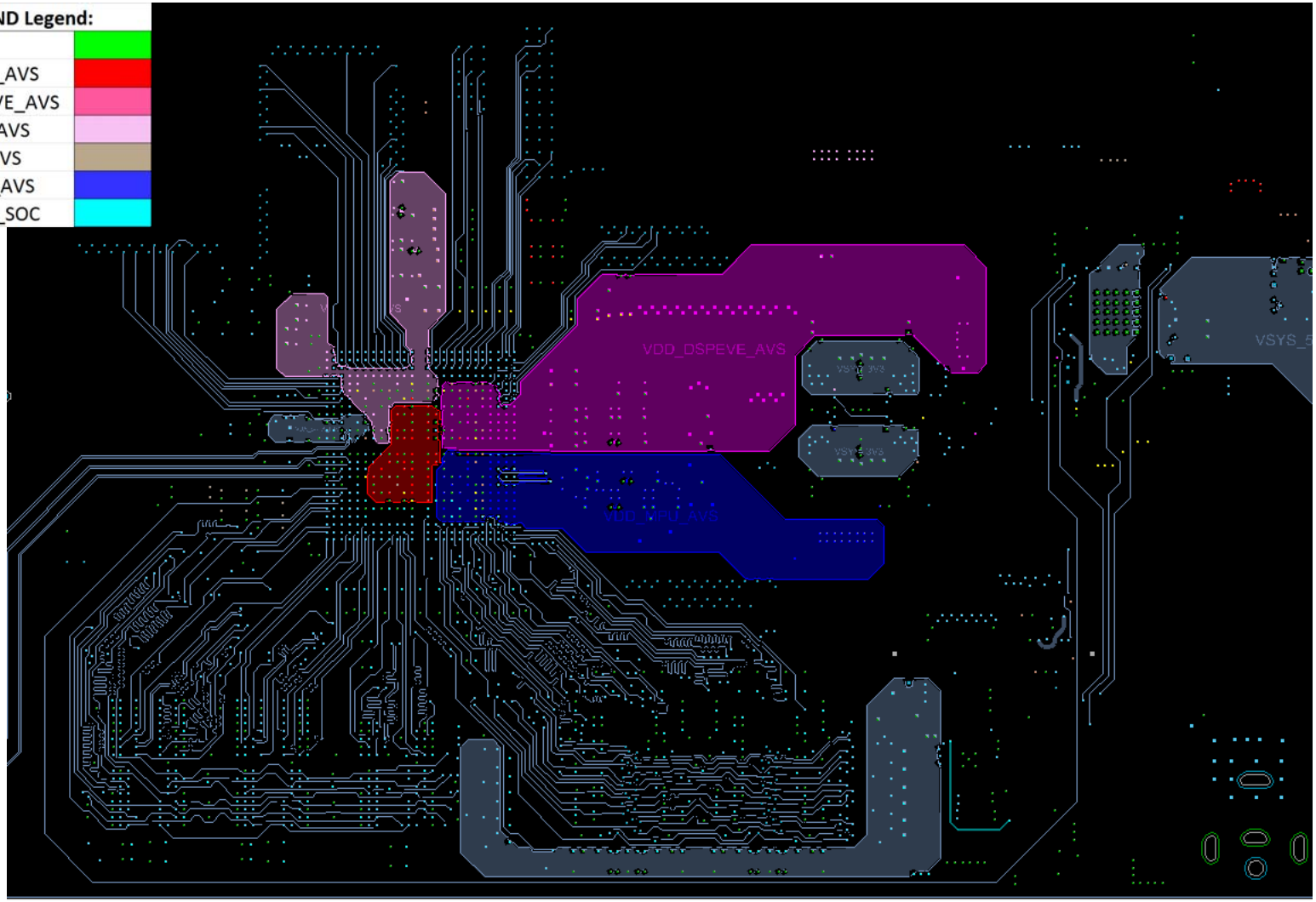


10-Layer PDN Overview – Lyr 3 (Plane-2)

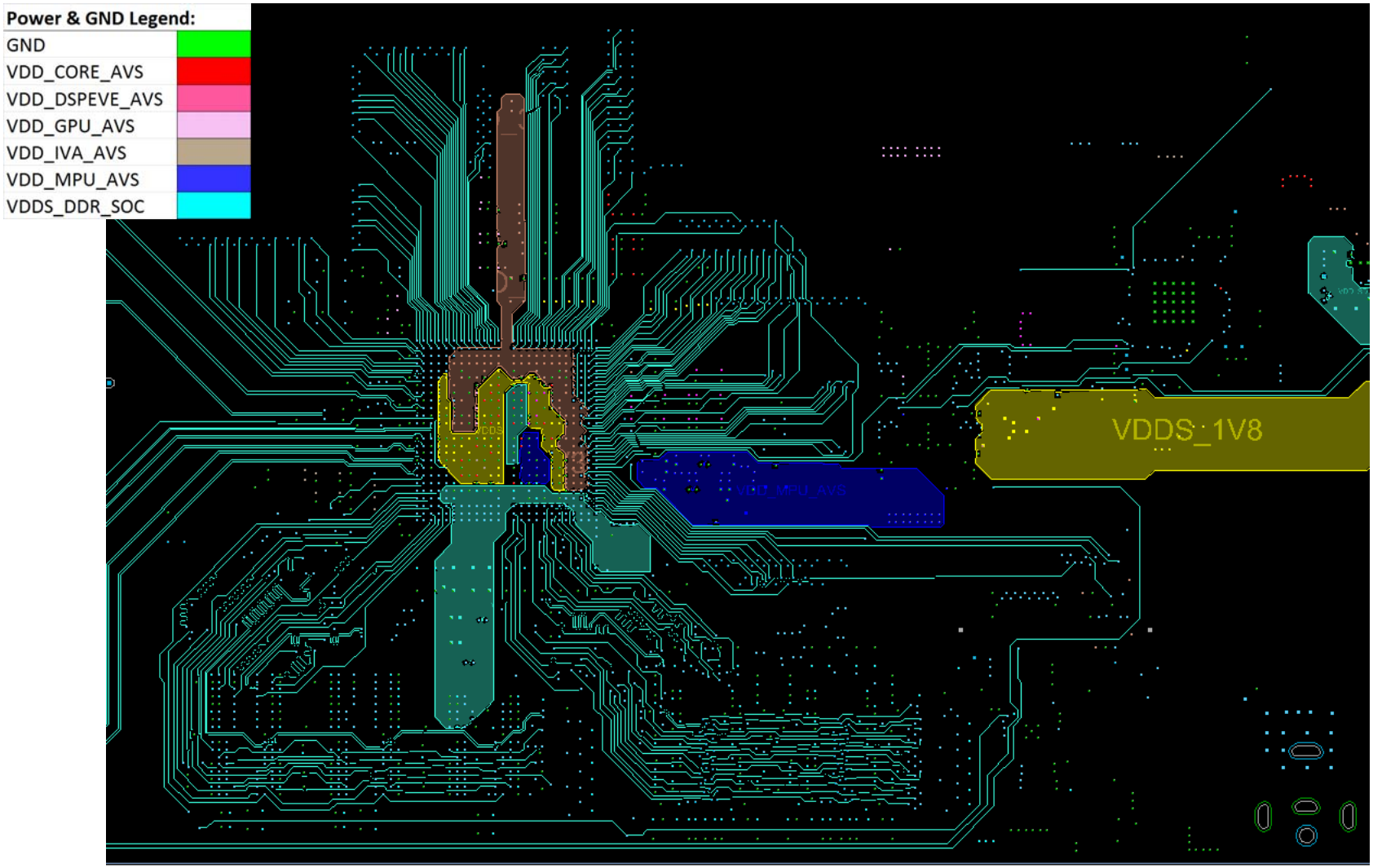


10-Layer PDN Overview – Lyr 5 (Signal-2)

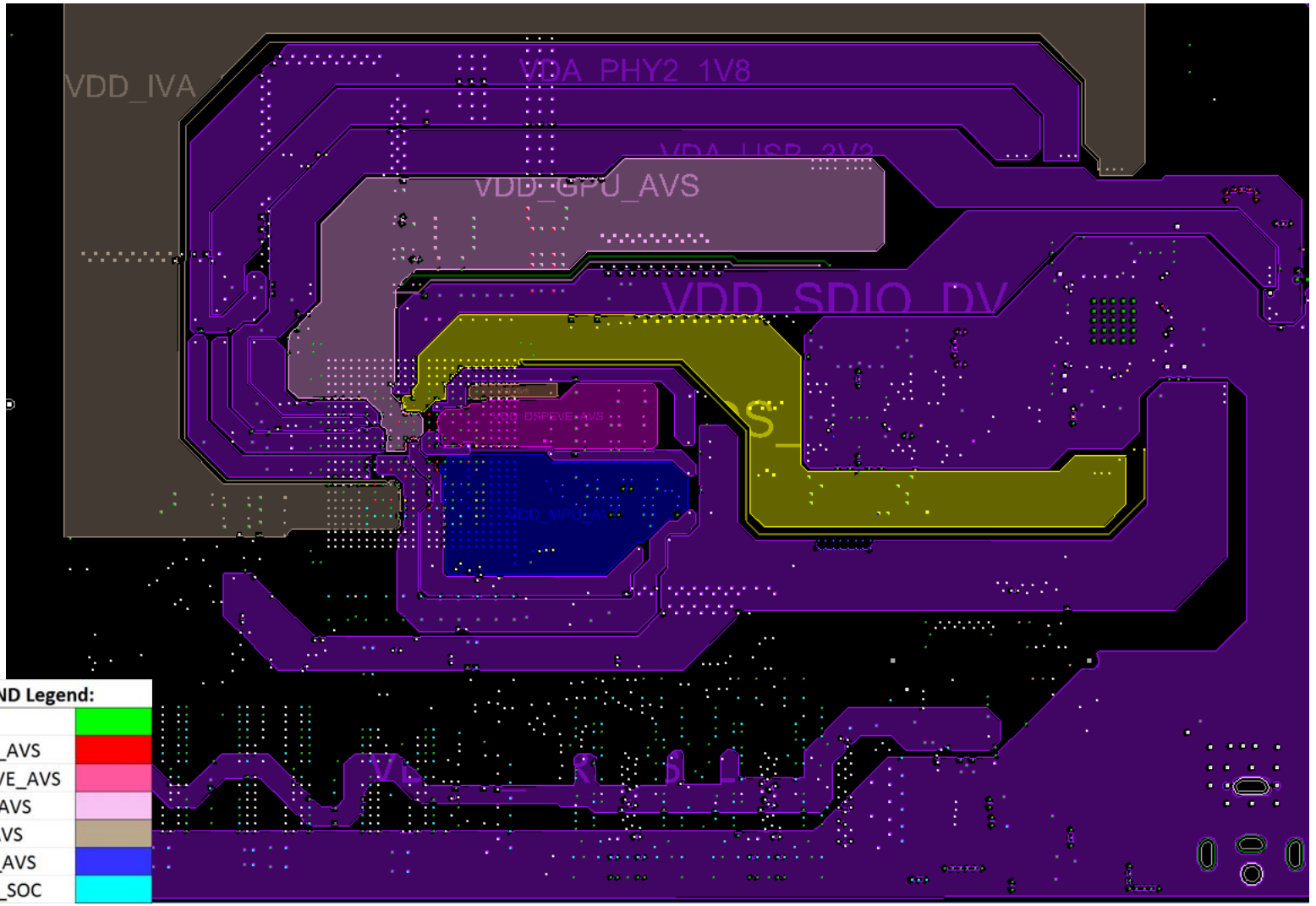
Power & GND Legend:
GND
VDD_CORE_AVS
VDD_DSPEVE_AVS
VDD_GPU_AVS
VDD_IVA_AVS
VDD_MPU_AVS
VDDS_DDR_SOC



10-Layer PDN Overview – Lyr 6 (Signal-3)

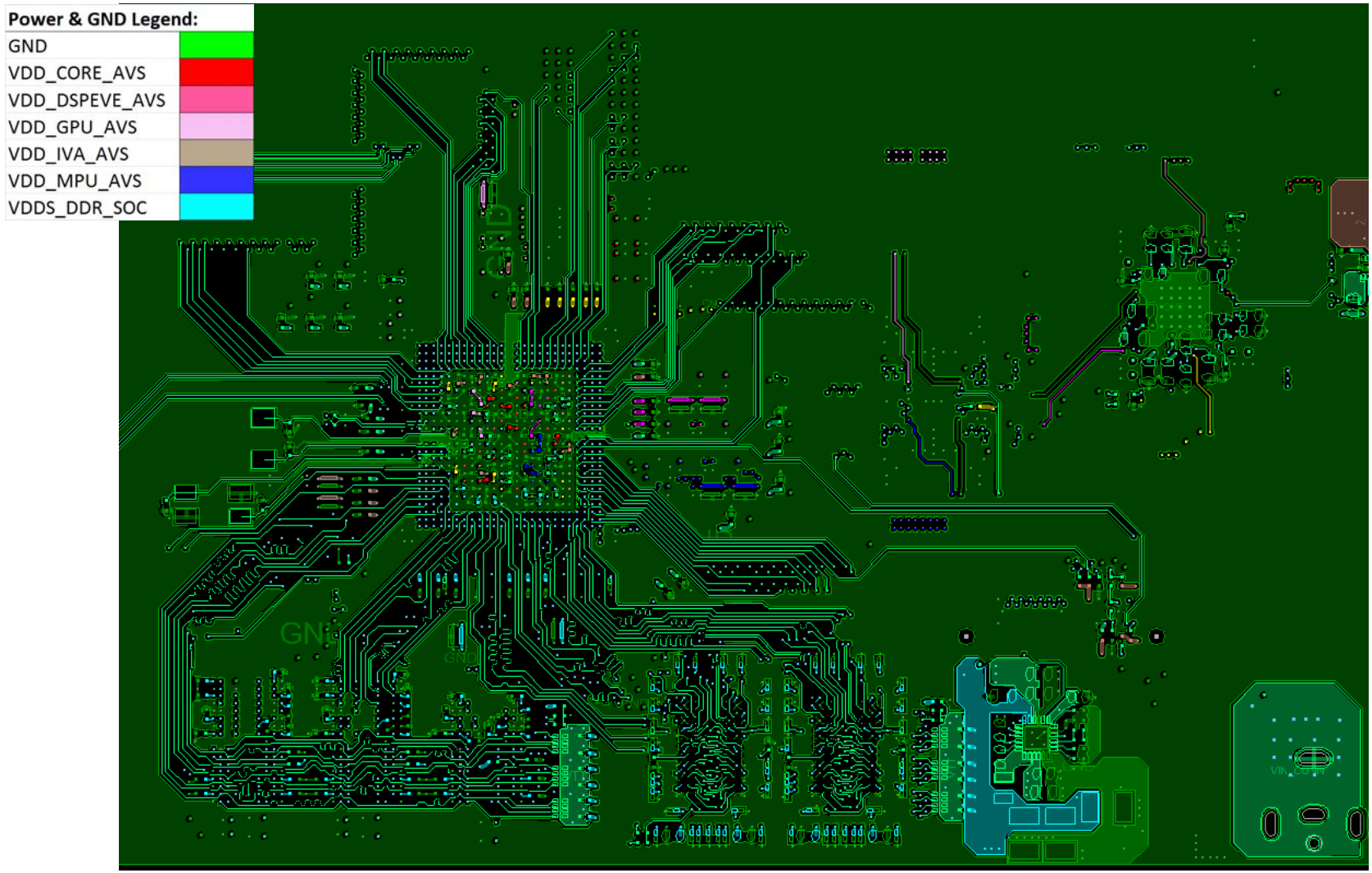


10-Layer PDN Overview – Lyr 8 (Plane-5)



Power & GND Legend:
GND
VDD_CORE_AVS
VDD_DSPEVE_AVS
VDD_GPU_AVS
VDD_IVA_AVS
VDD_MPU_AVS
VDDS_DDR_SOC

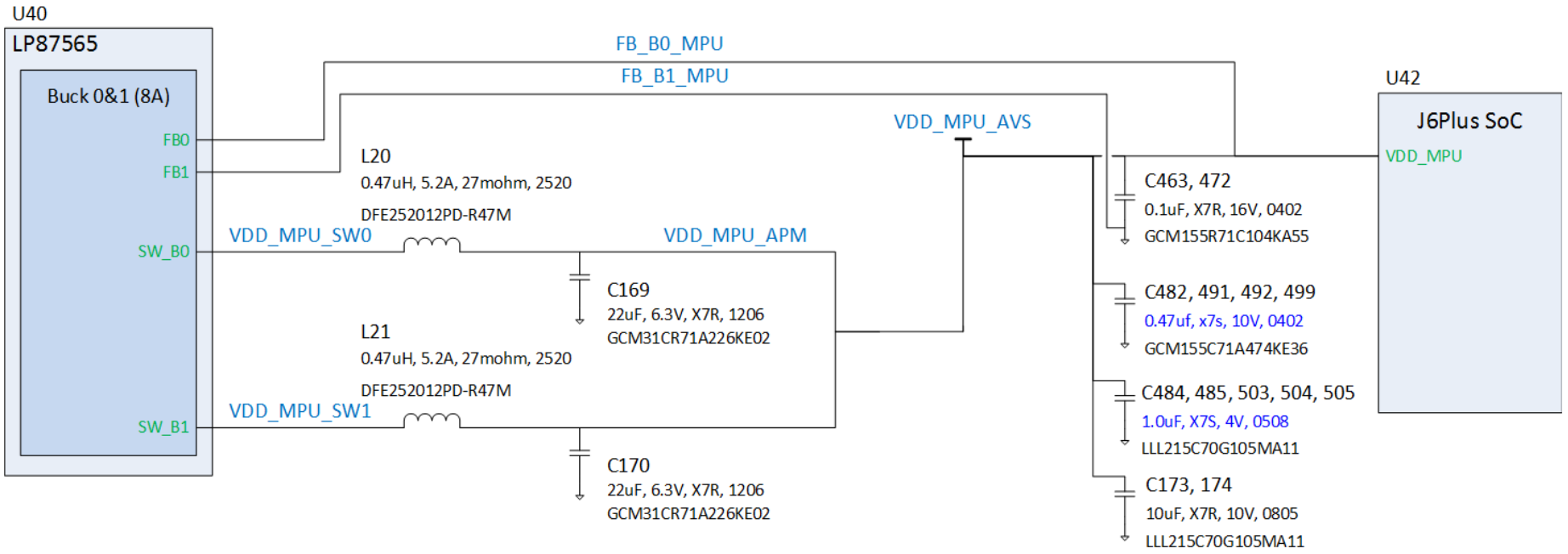
10-Layer PDN Overview – Lyr 10/Bottom (Signal-4)



VDD_MPU_AVS POWER DOMAIN

VDD_MPU_AVS - Simplified Power SCH

J6Plus Ref – VDD_MPU_AVS Power Rail Model

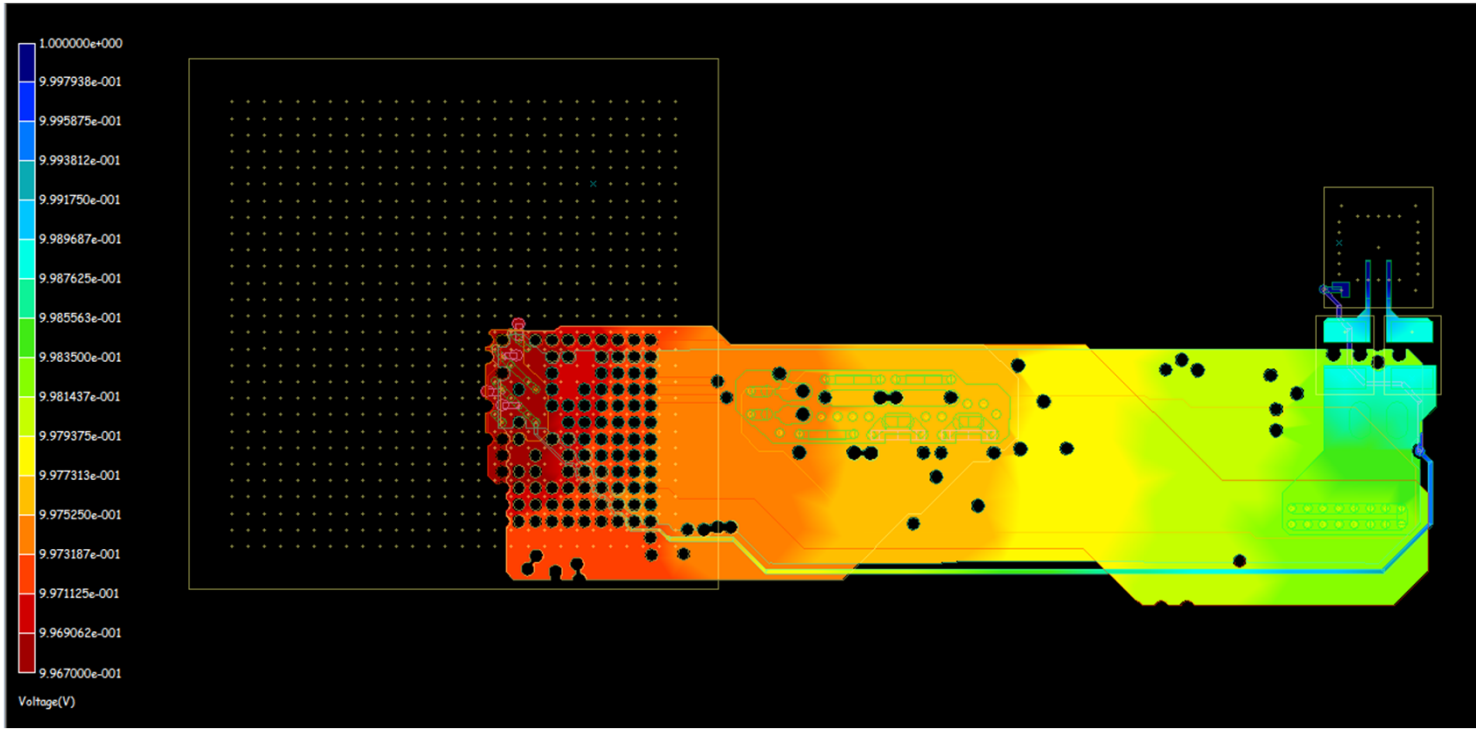


Recommended Dcap Scheme Optimized for PCB Design					Power Rail: VDD_MPU_AVS			
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C173, 174	10	2	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C484, 485, 503, 504, 505	1.0	5	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C482, 491, 492, 499	0.47	4	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
C463, 472	0.1	2	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155R71C104KA55	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B1X7R1C104K050BC
Totals	27.1	13	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDD_MPU_AVS

Derived from: Vdrop Analysis						
Name	Vin [V]	Vout [V]	Vdrop [V]	Current [A]	Reff [Ohms]	Target [mohms]
VDD_MPU_AVS	1.0000					
		0.9967	0.0033	1	0.0033	18.0

Routed on Layers
1
3
5
6
7



Dcap Loop Inductance: VDD_MPU_AVS

- Decoupling Cap's Loop Inductance (LL) Range: 0.309 – 0.745 nH (@ 50 MHz)

Capacitor Footprints (FP)	Footprint Types	Inductance	Code
	2-via, skinny-end exit	Highest	2vSEE
	2-via, wide-end exit		2vWEE
	2-via, wide-side exit		2vWSE
	4-via, wide-side exit		4vWSE
	via in-pad	Lowest	vIP

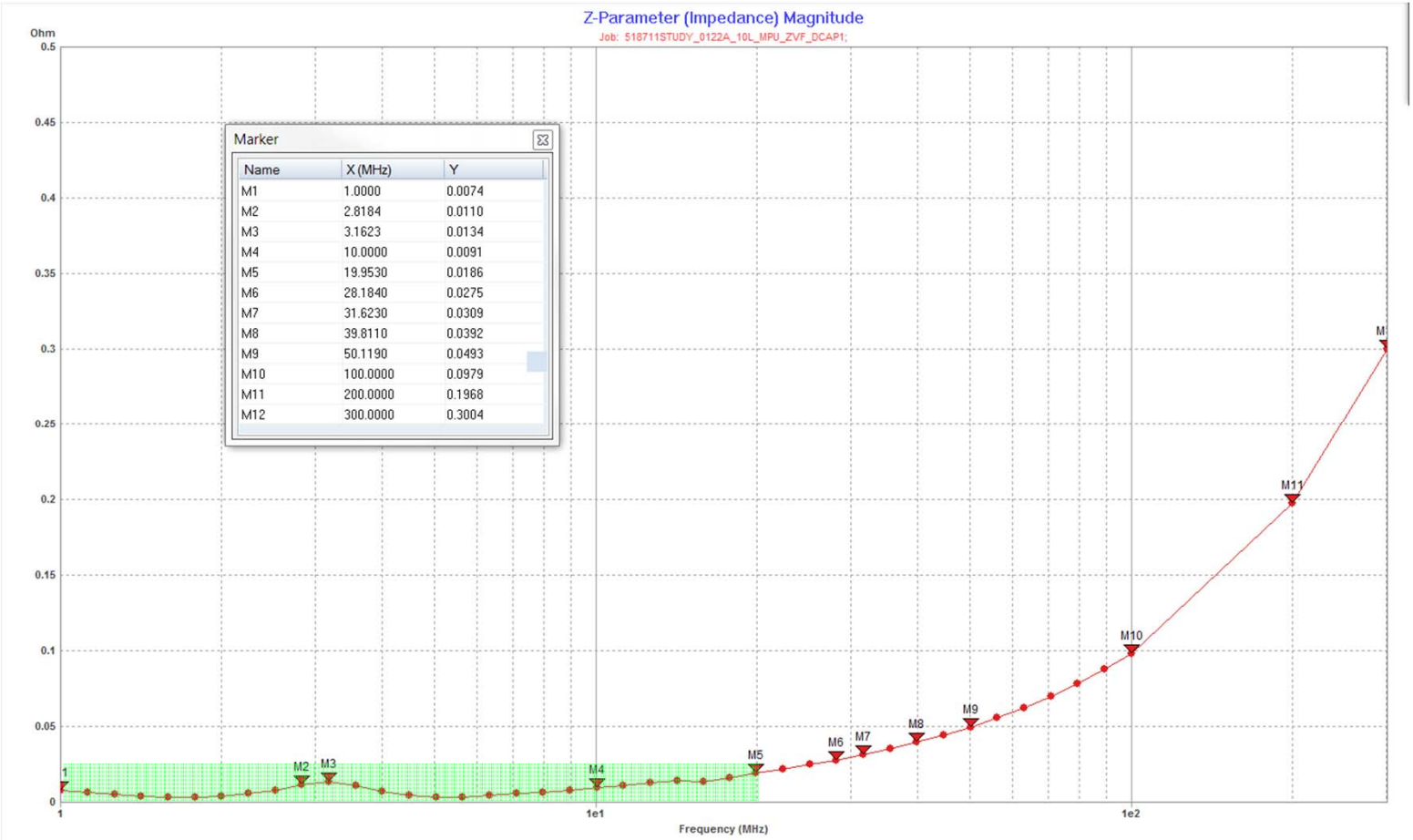
Item #	Cap Ref Des	v0122 Ref PCB Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Pwr Ball-Field (ref ball =K18) [mils]	Value [uF]	Size
1	C463	0.745	2vWSE	Bottom, Under BGA	111	0.1	0402
2	C472	0.725	2vWSE	Bottom, Under BGA	54	0.1	0402
3	C482	0.667	2vWSE	Bottom, Under BGA	79	0.47	0402
4	C491	0.61	2vWEE	Top	458	0.47	0402
5	C492	0.689	2vWSE	Bottom, Under BGA	65	0.47	0402
6	C499	0.562	2vWEE	Top	462	0.47	0402
7	C484	0.326	4vWSE	Top	758	1.0	0508
8	C485	0.314	4vWSE	Top	623	1.0	0508
9	C503	0.528	4vWSE	Bottom	849	1.0	0508
10	C504	0.507	4vWSE	Bottom	715	1.0	0508
11	C505	0.309	4vWSE	Top	582	1.0	0508
12	C173	0.545	4vWSE	Top	712	10	0805
13	C174	0.557	4vWSE	Top	846	10	0805
	Min	0.309					
	Max	0.745					
	Average:	0.545					

Notes:
1) Distances are wrt "middle of Ball Field", Ref pt between: U42-K18 to middle of Dcap's power pad unless specifed

Power Rail Loop Inductance

Item #	Cap Ref Des	v0122 10Lyr Ref PCB Loop Inductance @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Pwr Ball-Field (ref ball =K18) [mils]	Value [uF]	Size
14	C169	0.528	Power Cap	Top	1594.9	22	1206
15	C170	0.873	Power Cap	Top	1664.8	22	1206

Target Impedance: VDD_MPU_AVS

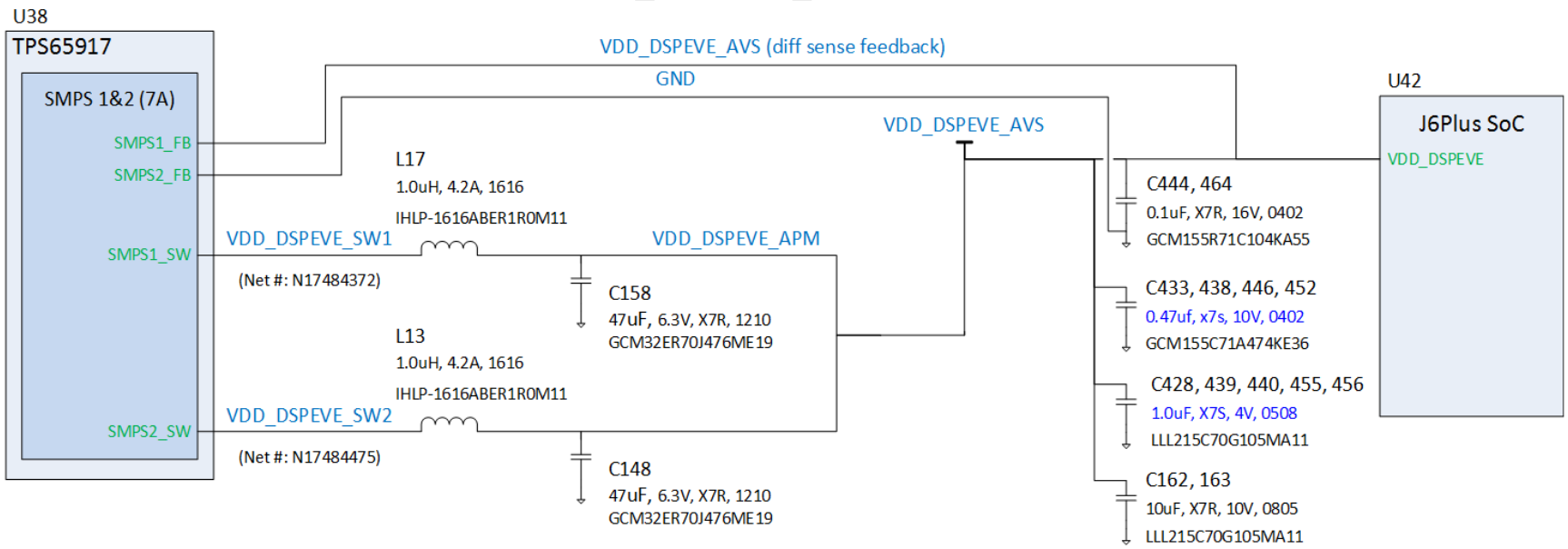


Green box = Power rail's Max Target Impedance of 22mOhm up to "Freq of Interest" 20 MHz

VDD_DSPEVE_AVS POWER DOMAIN

VDD_DSPEVE_AVS – Simplified Power SCH

J6Plus Ref – VDD_DSPEVE_AVS Power Rail Model

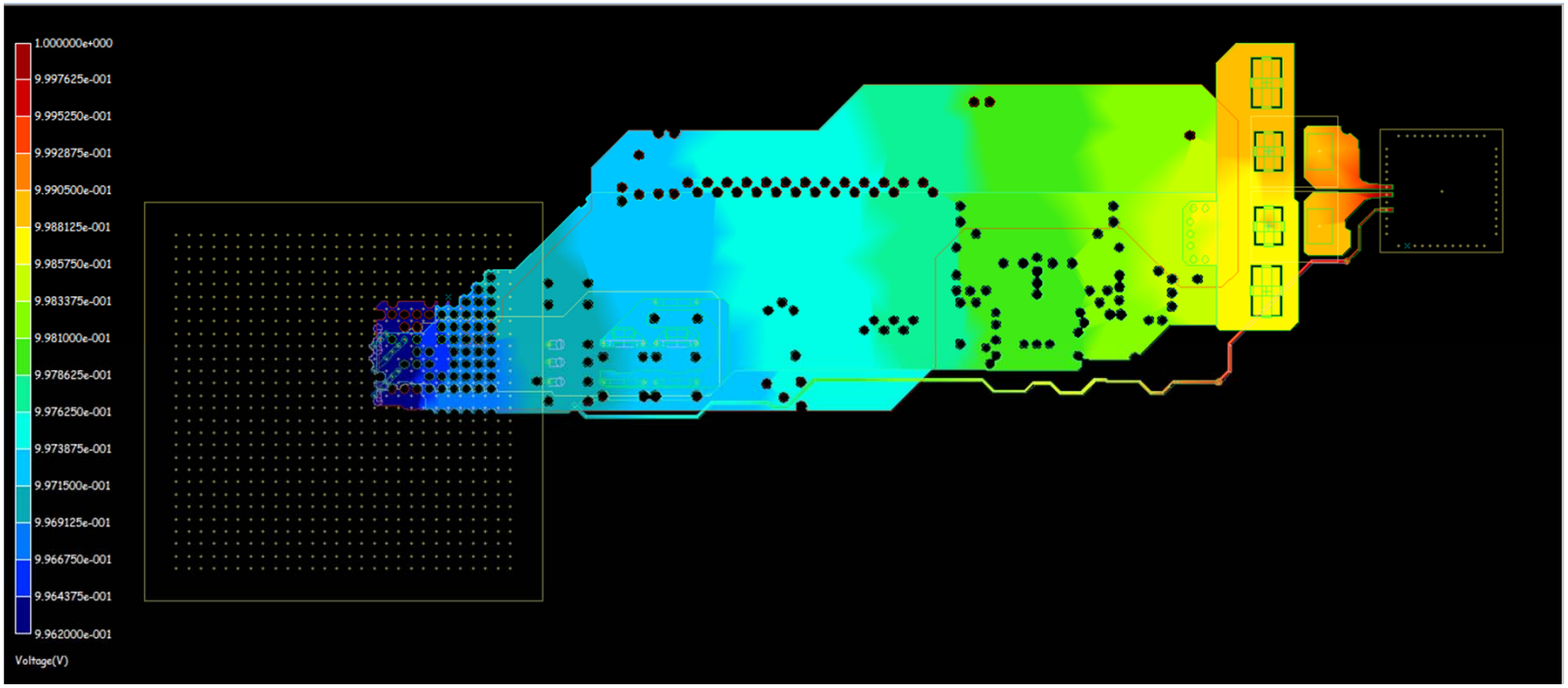


Recommended Dcap Scheme Optimized for PCB Design					Power Rail: VDD_DSPEVE_AVS			
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C162, 163	10	2	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C428, 439, 440, 455, 456	1.0	5	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C433, 438, 446, 452	0.47	4	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
C444, 464	0.1	2	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155R71C104KA55	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B1X7R1C104K050BC
Totals	27.1	13	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDD_DSPEVE_AVS

Derived from: Vdrop Analysis						
Name	**Vin [V]**	**Vout [V]**	**Vdrop [V]**	**Current [A]**	**Reff [Ohms]**	**Target [mohms]**
VDD_DSP_AVS	1.0000					
		0.9962	0.0038	1	0.0038	22.0

Routed on Layers
1
3
5
8



Dcap Loop Inductance: VDD_DSPEVE_AVS

- Decoupling Cap's Loop Inductance (LL) Range: 0.332 – 0.921 nH (@ 50 MHz)

Capacitor Footprints (FP)		Footprint Types	Inductance	Code
		2-via, skinny-end exit	Highest	2vSEE
		2-via, wide-end exit		2vWEE
		2-via, wide-side exit		2vWSE
		4-via, wide-side exit		4vWSE
		via in-pad	Lowest	vIP

Port #	Cap Ref Des	v0122a Ref Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field K10 [mils]	Value [uF]	Size
1	C162	0.416	4vWSE	Top	574	10	0805
2	C163	0.415	4vWSE	Top	708	10	0805
3	C428	0.332	4vWSE	Top	716	1	0508
4	C433	0.663	2vWSE	Bottom, Under BGA	67	0.47	0402
5	C438	0.907	2vWEE	Bottom	413	0.47	0402
6	C439	0.521	4vWSE	Bottom	708	1.0	0508
7	C440	0.506	4vWSE	Bottom	573	1.0	0508
8	C446	0.881	2vWEE	Bottom	415	0.47	0402
9	C452	0.921	2vWEE	Bottom	423	0.47	0402
10	C455	0.446	4vWSE	Top	714	1	0508
11	C456	0.358	4vWSE	Top	580	1	0508
12	C444	0.679	2vWSE	Bottom, Under BGA	53	0.1	0402
13	C464	0.640	2vWSE	Bottom, Under BGA	150	0.1	0402

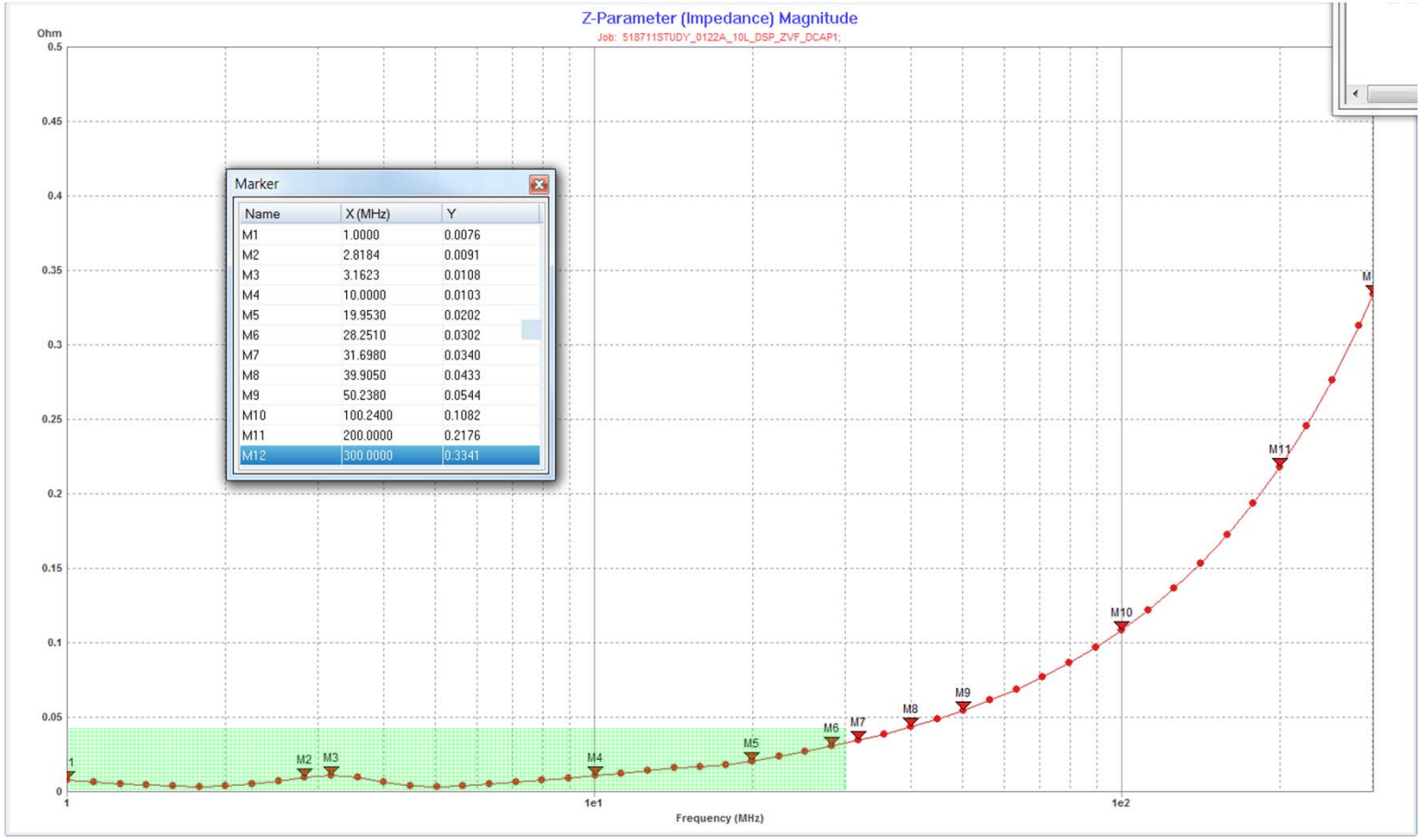
Min	0.332
Max	0.921
Average	0.591

Notes:
1) Distances are wrt "middle of Ball Field", Ref pt between: U42-K10 to middle of Dcap's power pad unless specifed

Power Rail Loop Inductance

Port #	Cap Ref Des	v0122 10Lyr Ref PCB Loop Inductance @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field K10 [mils]	Value [uF]	Size
14	C148	0.816	Power cap	Top	2311	47	1210
15	C158	0.720	Power cap	Top	2216.6	47	1210

Target Impedance: VDD_DSPEVE_AVS



Marker

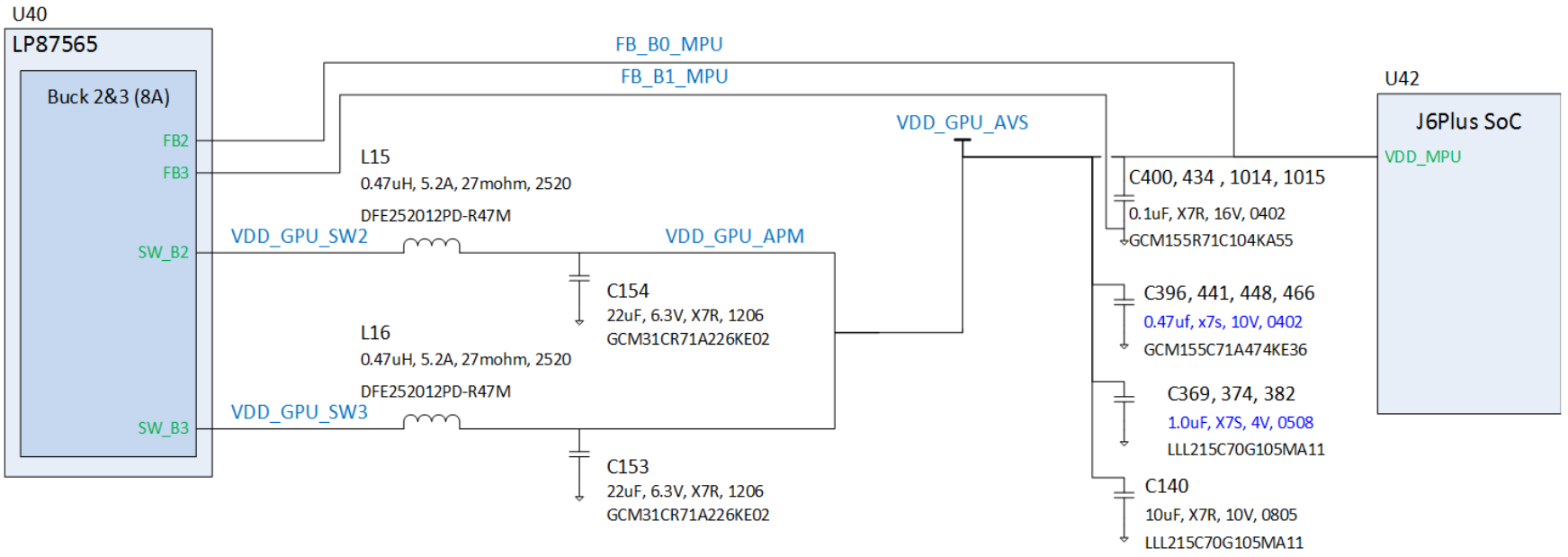
Name	X (MHz)	Y
M1	1.0000	0.0076
M2	2.8184	0.0091
M3	3.1623	0.0108
M4	10.0000	0.0103
M5	19.9530	0.0202
M6	28.2510	0.0302
M7	31.6980	0.0340
M8	39.9050	0.0433
M9	50.2380	0.0544
M10	100.2400	0.1082
M11	200.0000	0.2176
M12	300.0000	0.3341

Green box = Power rail's Max Target Impedance of 40mOhm up to "Freq of Interest" 30 MHz

VDD_GPU_AVS POWER DOMAIN

VDD_GPU_AVS – Simplified Power SCH

J6Plus Ref – VDD_GPU_AVS Power Rail Model



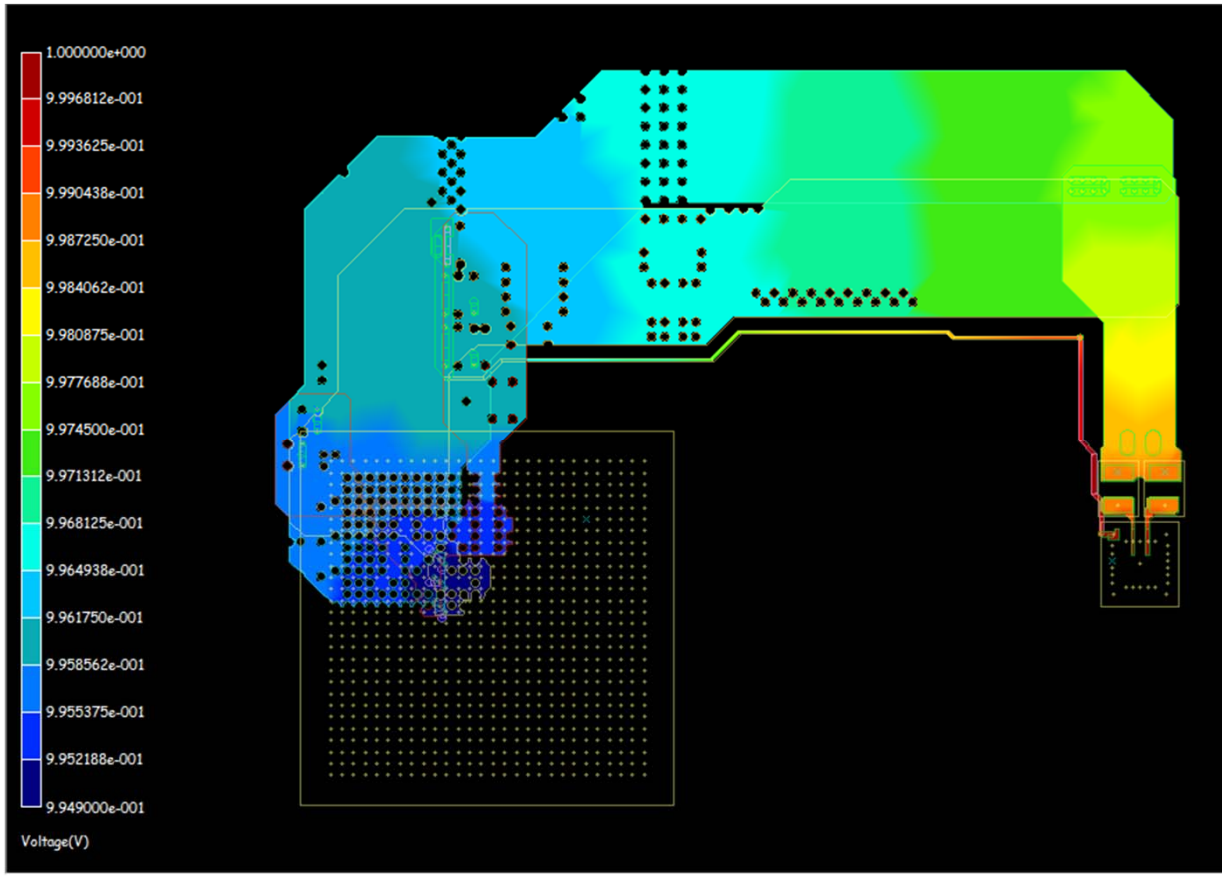
Recommended Dcap Scheme Optimized for PCB Design					Power Rail: VDD_GPU_AVS			
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C140	10	1	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C369, 374, 382	1.0	3	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C396, 441, 448, 466	0.47	4	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
C400, 434, 1014, 1015	0.1	4	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155R71C104KA55	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B1X7R1C104K050BC
Totals	18.9	12	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDD_GPU_AVS

Derived from: Vdrop Analysis

Name	Vin [V]	Vout [V]	Vdrop [V]	Current [A]	Reff [Ohms]	Target [mohms]
VDD_GPU_AVS	1.0000					
		0.9949	0.0051	1	0.0051	13.0

Routed on Layers
1
3
5
8



Dcap Loop Inductance: VDD_GPU_AVS

- Decoupling Cap's Loop Inductance (LL) Range: 0.36 – 0.91 nH (@ 50 MHz)

Capacitor Footprints (FP)		Footprint Types	Inductance	Code
		2-via, skinny-end exit	Highest	2vSEE
		2-via, wide-end exit		2vWEE
		2-via, wide-side exit		2vWSE
		4-via, wide-side exit		4vWSE
		via in-pad	Lowest	vIP

Item #	Cap Ref Des	v0122a 10Lyr opt Ref PCB Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Pwr Ball-Field (ref ball =V10) [mils]	Value [uF]	Size
1	C140	0.476	4vWSE	Top	868	10	0805
2	C369	0.601	4vWSE	Bottom	868	1	0805
3	C374	0.36	4vWSE	Top	734	1	0402
4	C382	0.359	2vWEE	Top	594	1	0402
5	C396	0.704	2vWEE	Top	529	0.47	0402
6	C400	0.707	2vWEE	Top	470	0.1	0508
7	C434	0.664	2vWSE	Bottom, Under BGA	61	0.1	0508
8	C441	0.638	2vWSE	Bottom, Under BGA	15	0.47	0402
9	C448	0.792	2vWSE	Bottom, Under BGA	64	0.47	0402
10	C466	0.905	2vWSE	Bottom, Under BGA	142	0.47	0402
11	C1014	0.534	4vWSE	Top	491	0.1	0402
12	C1015	0.529	4vWSE	Top	526	0.1	0402

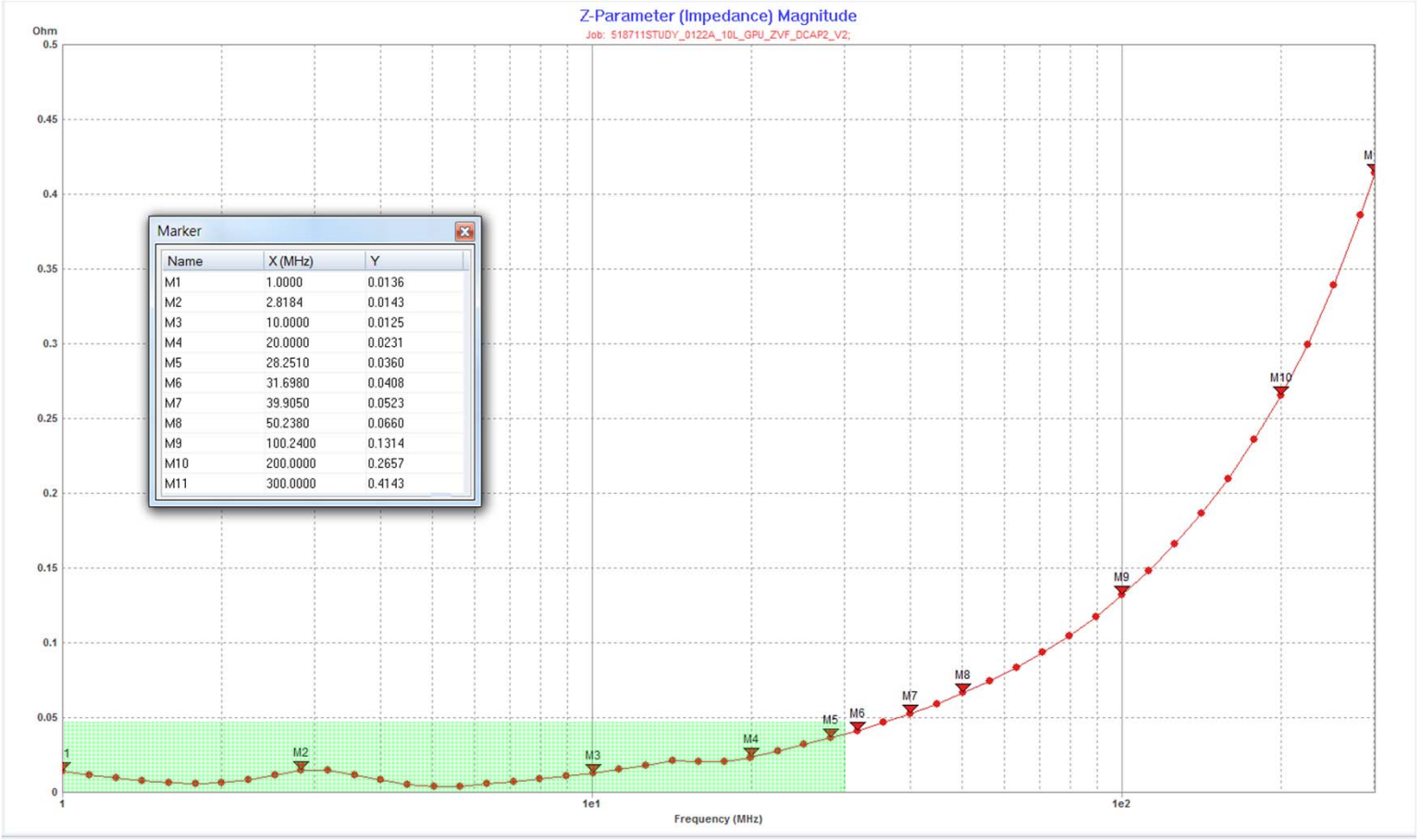
Min	0.36
Max	0.91
Average:	0.61

Notes:
1) Distances are wrt "middle of Ball Field", Ref pt between: U42-V10 to middle of Dcap's power pad unless specifed

Power Rail Loop Inductance

Item #	Cap Ref Des	v0122 Ref 10lyr PCB Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Pwr Ball-Field (ref ball =V10) [mils]	Value [uF]	Size
13	C153	0.84	Power Cap	Top	1875.3	22	1206
14	C154	0.75	Power Cap	Top	1944.2	22	1206

Target Impedance: VDD_GPU_AVS

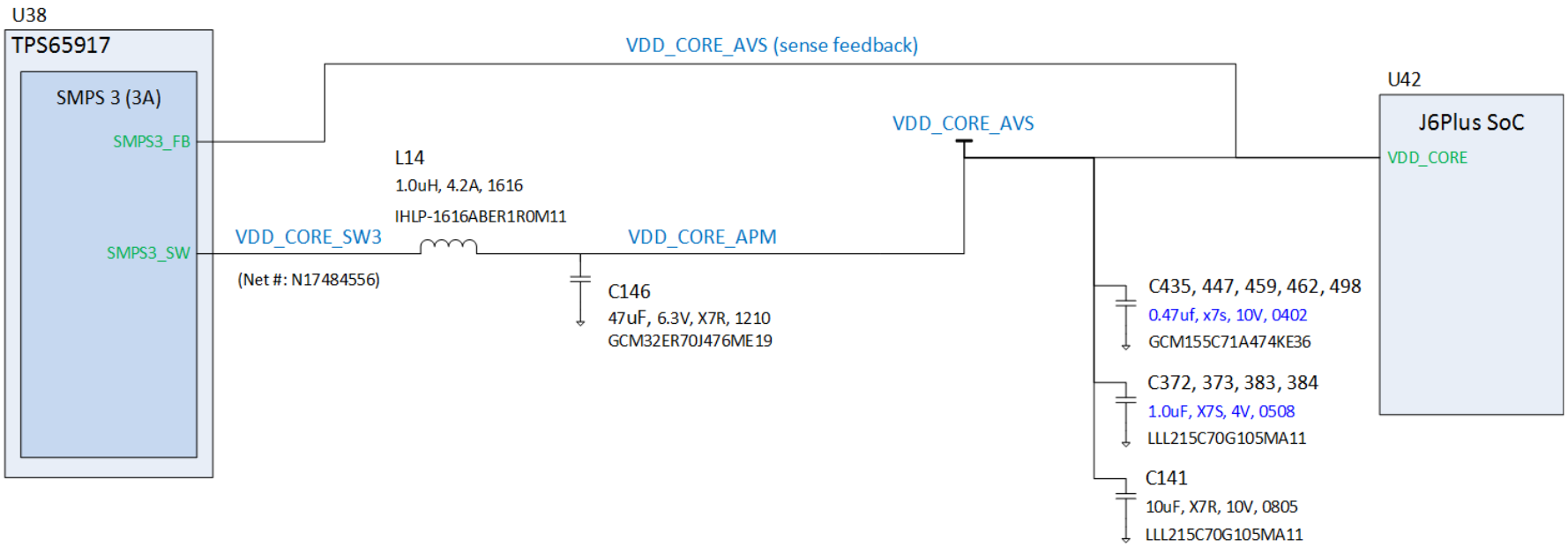


Green box = Power rail's Max Target Impedance of 48mOhm up to "Freq of Interest" 30 MHz

VDD_CORE_AVS POWER DOMAIN

VDD_CORE_AVS – Simplified Power SCH

J6Plus Ref – VDD_CORE_AVS Power Rail Model

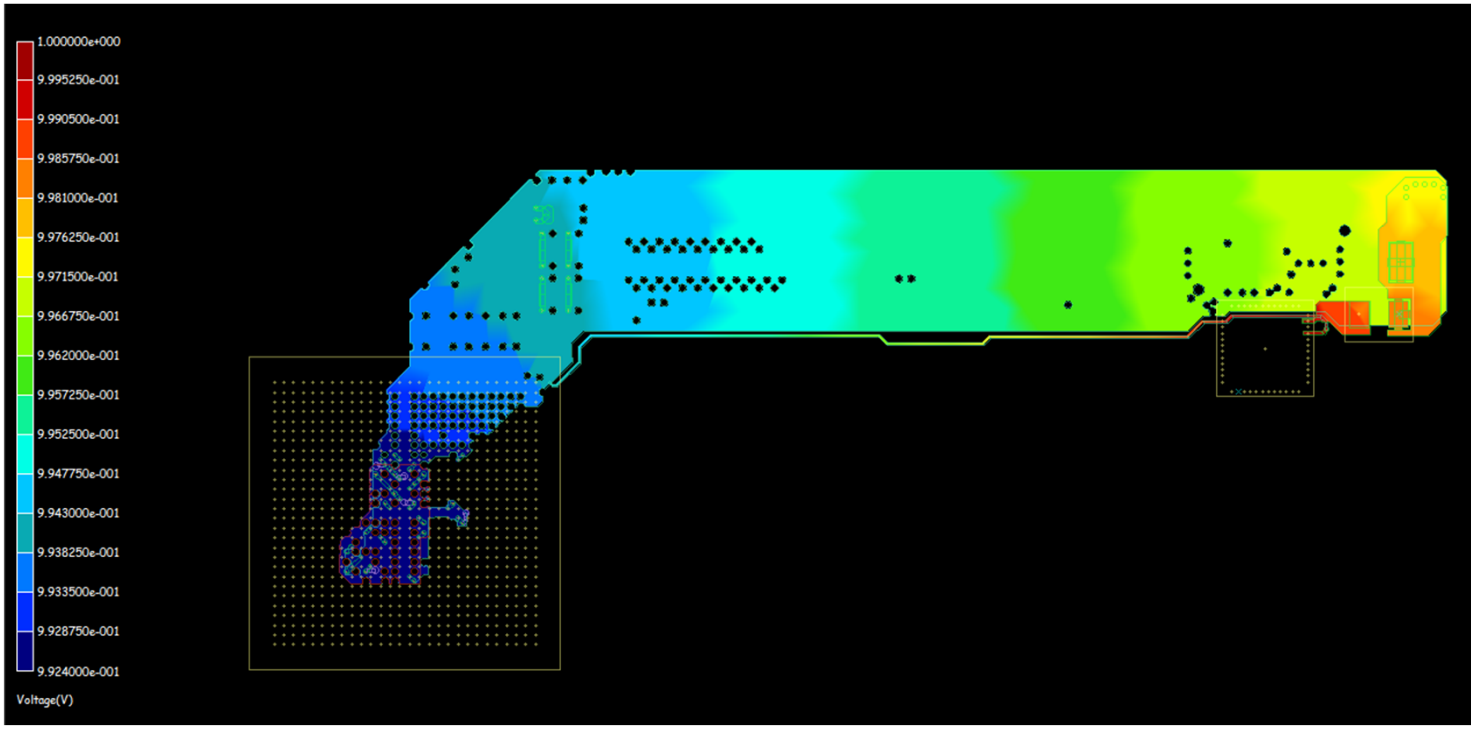


Recommended Dcap Scheme Optimized for PCB Design					Power Rail: VDD_CORE_AVS			
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C141	10	1	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C372, 373, 383, 384	1.0	4	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C435, 447, 459, 462, 498	0.47	5	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
Totals	16.4	10	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDD_CORE_AVS

Derived from: Vdrop Analysis						
Name	**Vin [V]**	**Vout [V]**	**Vdrop [V]**	**Current [A]**	**Reff [Ohms]**	**Target [mohms]**
VDD_CORE_AVS	1.0000					
		0.9924	0.0076	1	0.0076	32.0

Routed on Layers
1
3
5



Dcap Loop Inductance: VDD_CORE_AVS

- Decoupling Cap's Loop Inductance (LL) Range: 0.52 – 1.36 nH (@ 50 MHz)

Capacitor Footprints (FP)		Footprint Types	Inductance	Code
		2-via, skinny-end exit	Highest	2vSEE
		2-via, wide-end exit		2vWEE
		2-via, wide-side exit		2vWSE
		4-via, wide-side exit		4vWSE
		via in-pad	Lowest	vIP

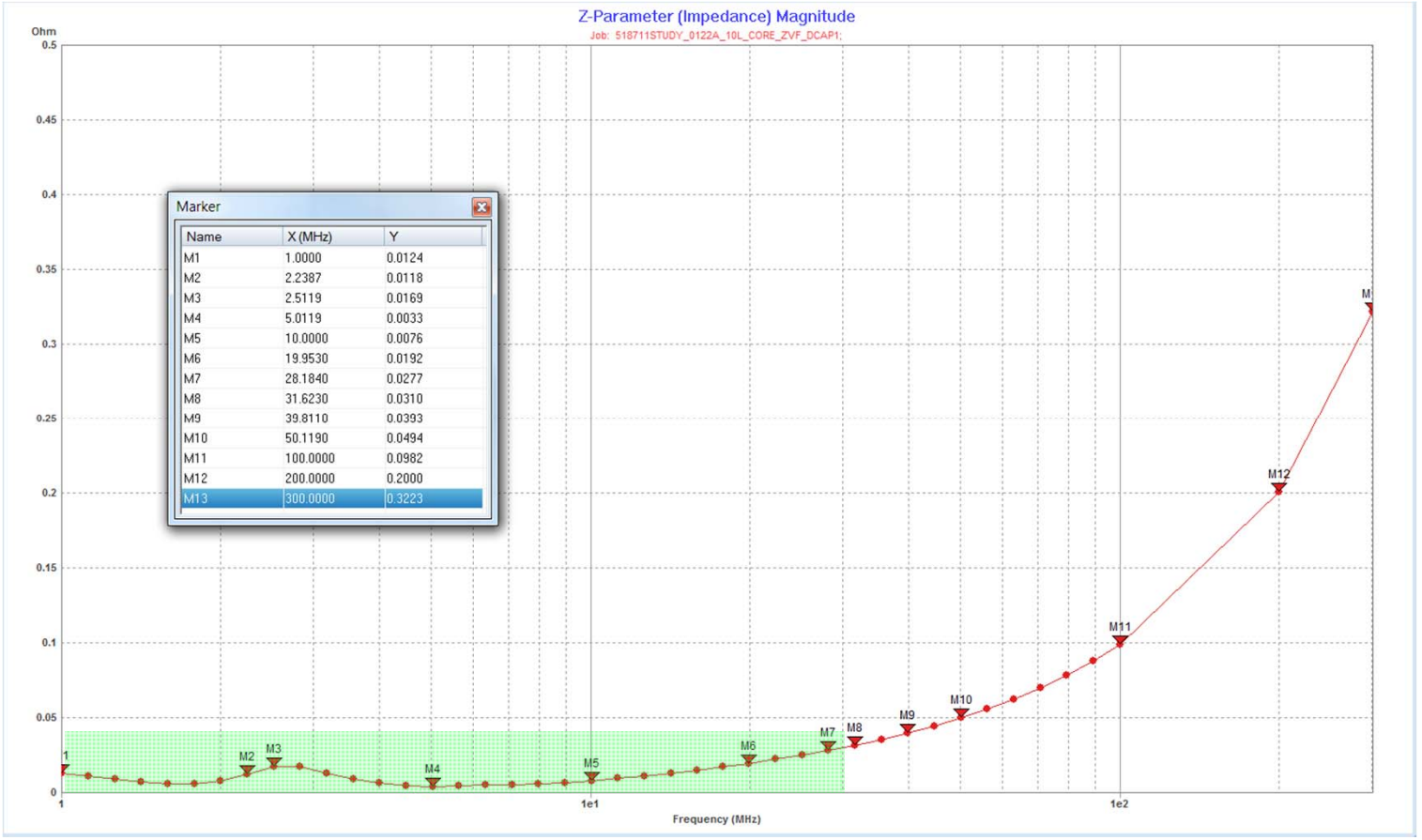
Item #	Cap Ref Des	v0122 10 lyr PCB Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field R13 [mils]	Value [uF]	Size
1	C141	0.780	4vWSE	Top	1041	10	0805
2	C372	0.515	4vWSE	Top	931	1	0508
3	C373	0.520	4vWSE	Top	976	1	0508
4	C383	0.570	4vWSE	Top	808	1	0508
5	C384	0.580	4vWSE	Top	860	1	0508
6	C498	1.090	2vWSE	Bottom, Under BGA	245	0.47	0402
7	C435	1.050	2vWSE	Bottom, Under BGA	129	0.47	0402
8	C447	1.040	2vWSE	Bottom, Under BGA	74	0.47	0402
9	C459	1.060	2vWSE	Bottom, Under BGA	20	0.47	0402
10	C462	1.360	2vWSE	Bottom, Under BGA	220	0.47	0402
	Min	0.52					
	Max	1.36					
	Average:	0.86					

Notes:
1) Distances are wrt "middle of Ball Field", Ref pt between: U42-R13 to middle of Dcap's power pad unless specifed

Power Rail Loop Inductance

Item #	Cap Ref Des	v0122 10 lyr Ref Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field R13 [mils]	Value [uF]	Size
11	C146	1.076	Power Cap	Top	3346.3	47.00	1210

Target Impedance: VDD_CORE_AVS

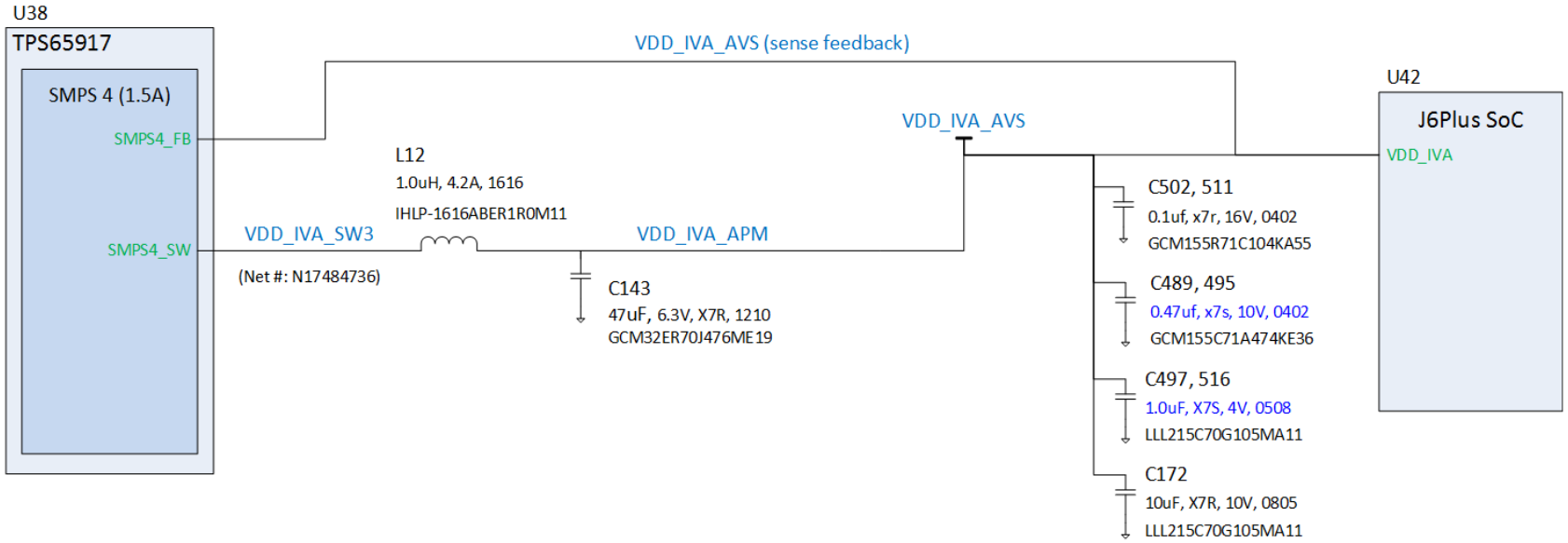


Green box = Power rail's Max Target Impedance of 40mOhm up to "Freq of Interest" 30 MHz

VDD_IVA_AVS POWER DOMAIN

VDD_IVA_AVS – Simplified Power SCH

J6Plus Ref – VDD_IVA_AVS Power Rail Model



Recommended Dcap Scheme Power Rail: VDD_IVA_AVS

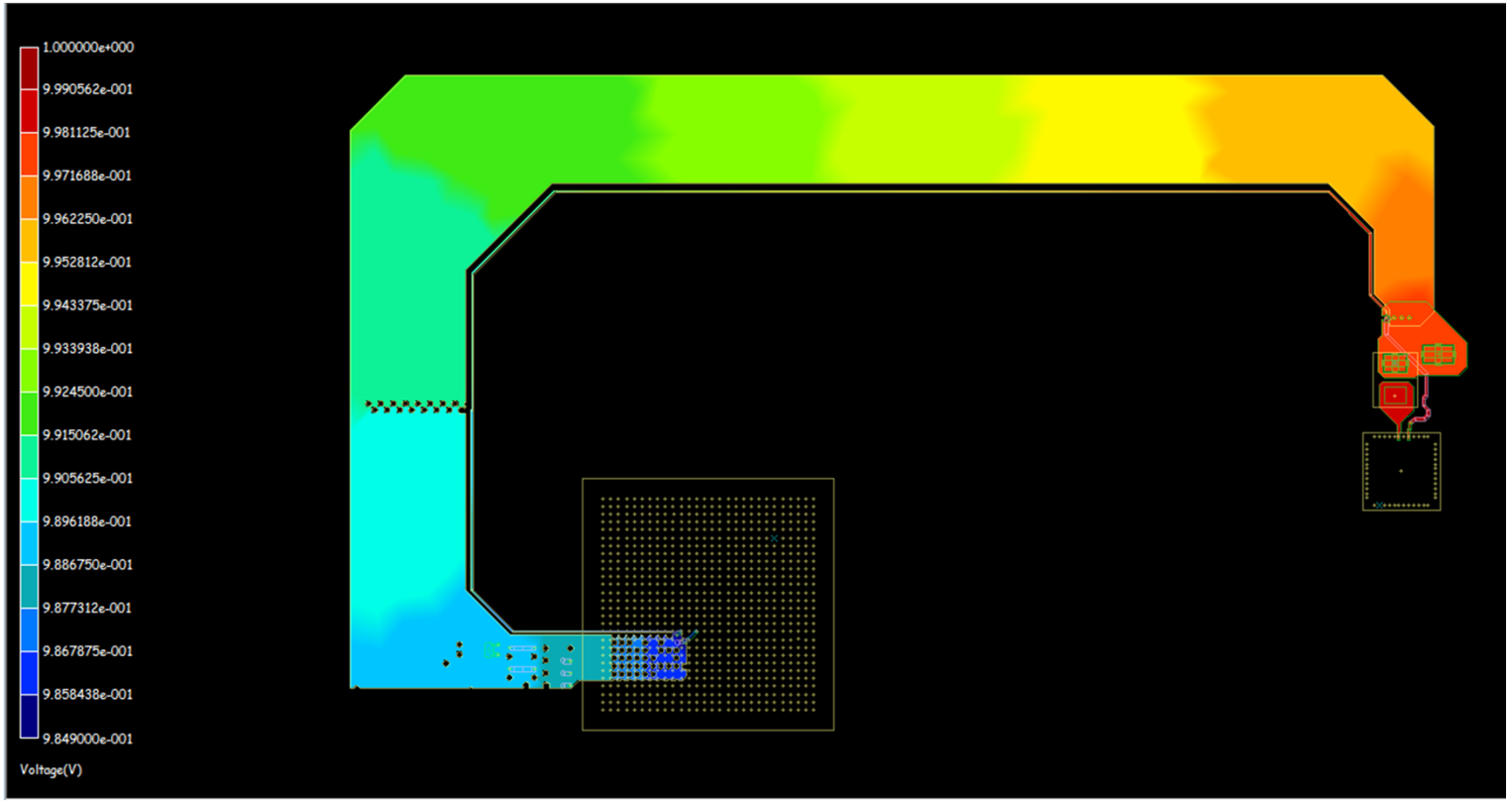
Ref Des	Vaule [uF]	Qty	Description #1	Manufacturer #1	Manf #1 P/N	Description #2	Manufacturer #2	Manf #2 P/N
C172	10	1	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C497, 516	1.0	2	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C489, 495	0.47	2	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
C502, 511	0.1	2	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155R71C104KA55	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B1X7R1C104K050BC
Totals	13.14	7	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDD_IVA_AVS

Derived from: Vdrop Analysis

Name	Vin [V]	Vout [V]	Vdrop [V]	Current [A]	Reff [Ohms]	Target [mohms]
VDD_IVA_AVS	1.0000					
		0.9849	0.0151	1	0.0151	48.0

Routed on Layers
1
8



Dcap Loop Inductance: VDD_IVA_AVS

- Decoupling Cap's Loop Inductance (LL) Range: 1.16 – 2.00 nH (@ 50 MHz)

Capacitor Footprints (FP)	Footprint Types	Inductance	Code
	2-via, skinny-end exit	Highest	2vSEE
	2-via, wide-end exit		2vWEE
	2-via, wide-side exit		2vWSE
	4-via, wide-side exit		4vWSE
	via in-pad	Lowest	vIP

Item #	Cap Ref Des	v0122a 10 lyr Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field(U19) [mils]	Value [uF]	Size
1	C172	2	4vWSE	Top	809	10	0805
2	C497	1.23	4vWSE	Bottom	672	1	0508
3	C516	1.25	4vWSE	Bottom	681	1	0508
4	C489	1.164	2vWEE	Bottom, Under BGA	43	0.47	0402
5	C495	1.409	2vWEE	Bottom	513	0.47	0402
6	C511	1.45	2vWEE	Bottom	524	0.1	0402
7	C502	1.432	2vWEE	Bottom	540	0.1	0402

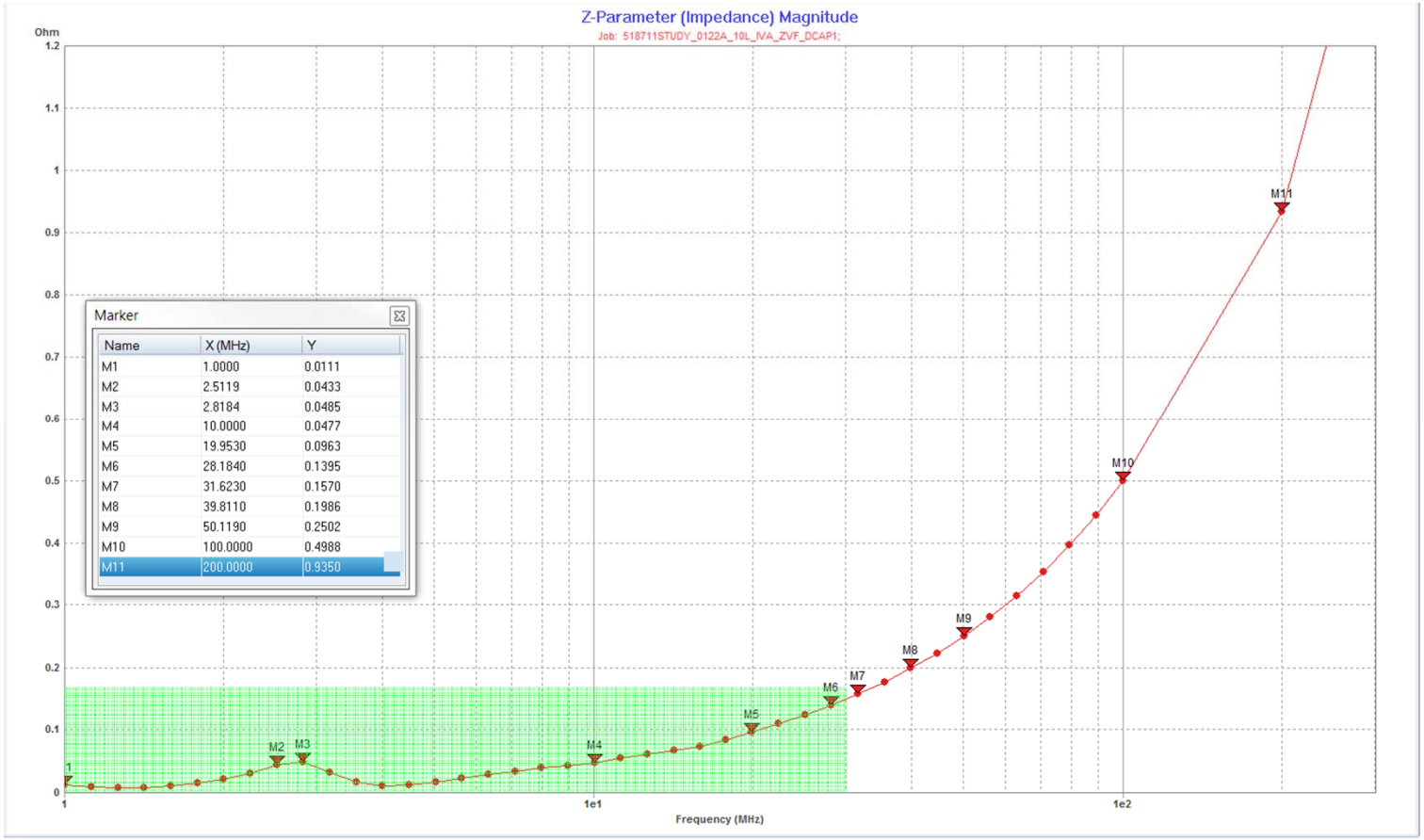
Min	1.16
Max	2.00
Average	1.42

Notes:
1) Distances are wrt "middle of Ball Field", Ref pt between: U42-U19 to middle of Dcap's power pad unless specifed

Power Rail Loop Inductance

Item #	Cap Ref Des	v0122a 10 lyr Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field(U19) [mils]	Value [uF]	Size
8	C143	3.23	Power Cap	Top	3239.3	47.0	1210

Target Impedance: VDD_IVA_AVS

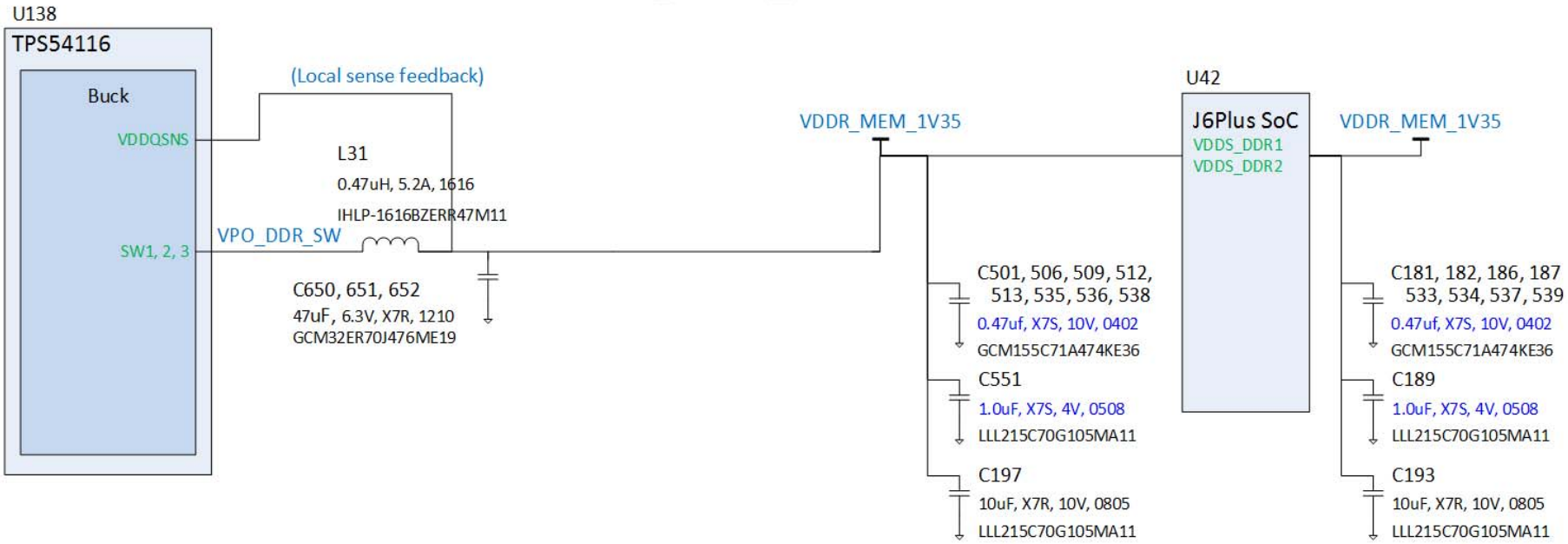


Green box = Power rail's Max Target Impedance of 179mOhm up to "Freq of Interest" 30 MHz

VDDR_MEM_1V35 POWER DOMAIN

VDDR_MEM_1V35 – Simplified Power SCH

J6Plus Ref – VDDR_MEM_1V35 Power Rail Model



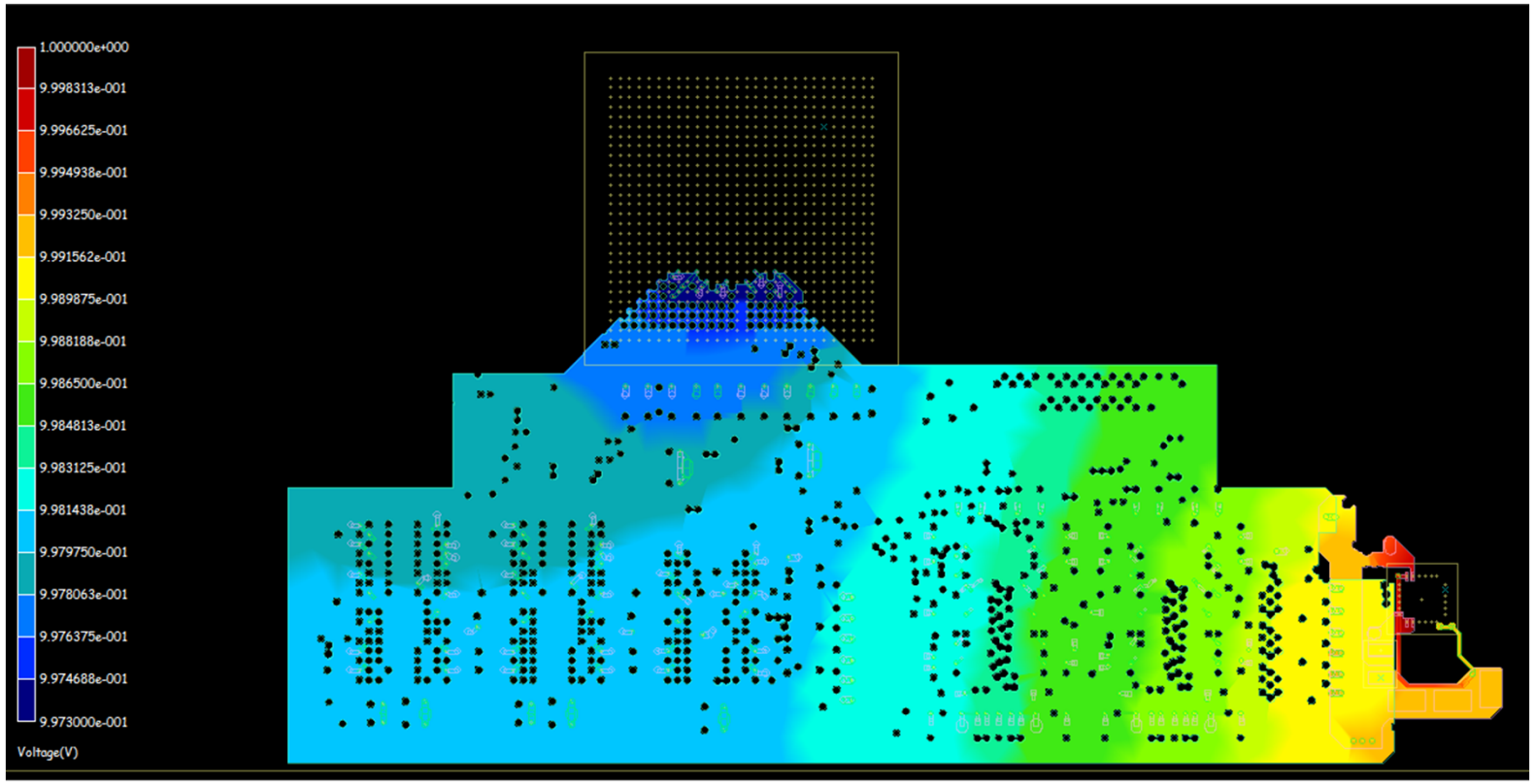
Recommended Dcap Scheme Optimized for PCB Design					Power Rail:	VDDR_MEM_1V35			
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C193, 197	10	2	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA4J1X7R0J106K125AC
C189, 551	1.0	2	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
C181, 182, 186, 187, 533, 534, 537, 539, 501, 506, 509, 512, 513, 535, 536, 538	0.47	16	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	Murata	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap	TDK	CGA2B3X7S1A474K050BB
Totals	29.5	20	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

IR Drop: VDDR_MEM_1V35

Derived from: Vdrop Analysis

Name	Vin [V]	Vout [V]	Vdrop [V]	Current [A]	Reff [Ohms]	Target [mohms]
VDDR_MEM_1V35	1.0000					
		0.9973	0.0027	1	0.0027	18.0

Routed on Layers
3
10



Loop Inductance: VDDR_MEM_1V35

- Decoupling Cap's Loop Inductance (LL) Range: 0.55 – 1.46 nH (@ 50 MHz)

Capacitor Footprints (FP)	Footprint Types	Inductance	Code
	2-via, skinny-end exit	Highest	2vSEE
	2-via, wide-end exit		2vWEE
	2-via, wide-side exit		2vWSE
	4-via, wide-side exit		4vWSE
	via in-pad	Lowest	vIP

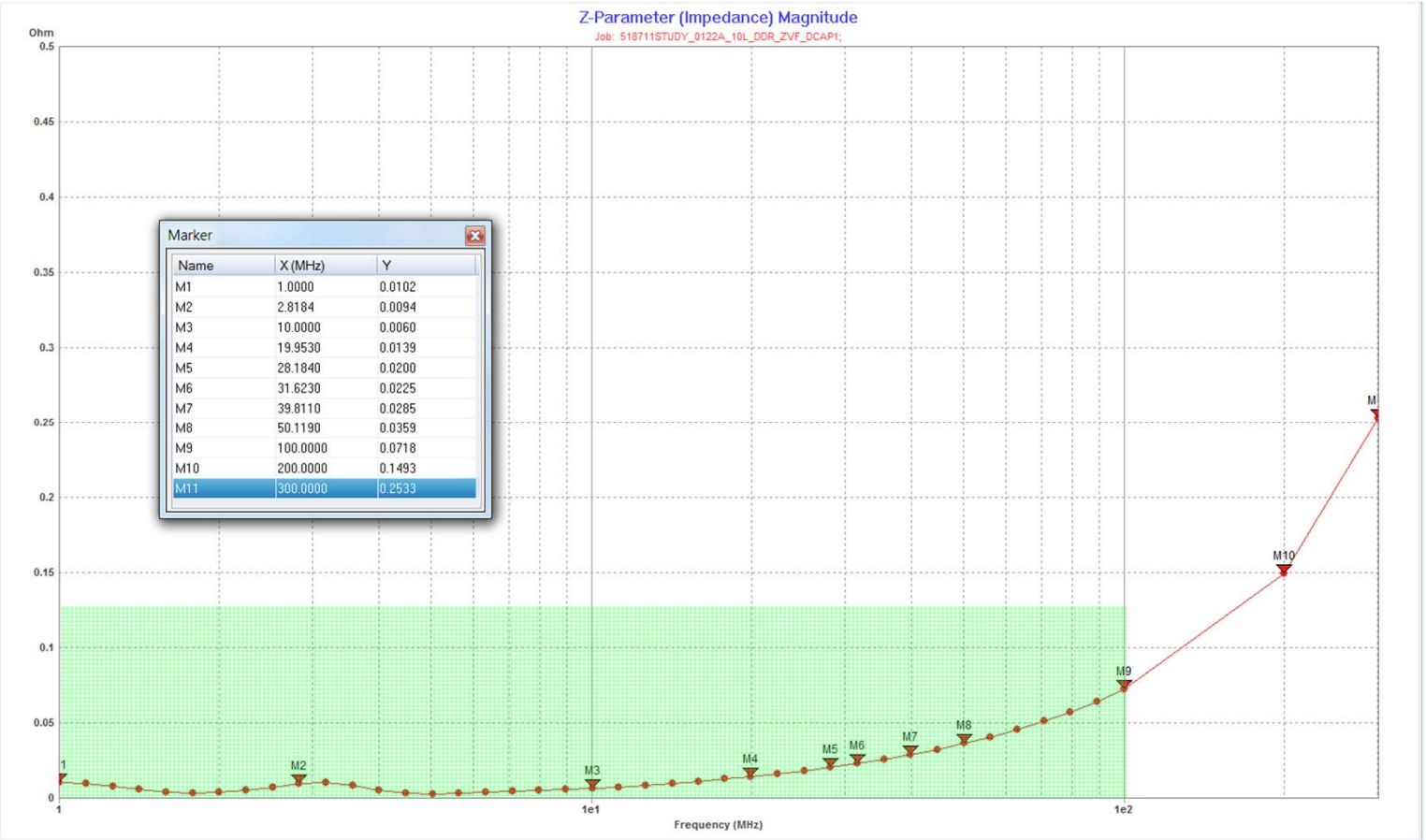
Item #	Cap Ref Des	v0122a Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Distance to Ball-Field [mils]	Value [uF]	Size
1	C181	1.39	2vWEE	Bottom	408	0.47	0402
2	C182	1.37	2vWEE	Bottom	370	0.47	0402
3	C186	0.71	2vWEE	Top	559	0.47	0402
4	C187	1.38	2vWEE	Bottom	417	0.47	0402
5	C189	0.90	4vWSE	Bottom	621	1.0	0508
6	C193	0.65	4vWSE	Top	616	10	0805
7	C197	0.55	4vWSE	Top	646	10	0805
8	C501	1.37	2vWEE	Bottom, Under BGA	107	0.47	0402
9	C506	1.46	2vWEE	Bottom, Under BGA	173	0.47	0402
10	C509	1.25	2vWEE	Bottom, Under BGA	112	0.47	0402
11	C512	1.25	2vWSE	Bottom, Under BGA	45	0.47	0402
12	C513	1.18	2vWSE	Bottom, Under BGA	97	0.47	0402
13	C533	0.69	2vWEE	Top	380	0.47	0402
14	C534	1.39	2vWEE	Bottom	446	0.47	0402
15	C535	1.35	2vWEE	Bottom	492	0.47	0402
16	C536	0.59	2vWEE	Top	368	0.47	0402
17	C537	0.63	2vWEE	Top	505	0.47	0402
18	C538	0.61	2vWEE	Top	457	0.47	0402
19	C539	1.37	2vWEE	Bottom	387	0.47	0402
20	C551	0.83	4vWSE	Bottom	638	1.0	0508

Min	0.55
Max	1.46
Average	1.05

Notes:

1) Distances are wrt "middle of Ball Field", Ref pt between: U5000-N10 to middle of Dcap's power pad unless specifed

Target Impedance: VDDR_MEM_1V35

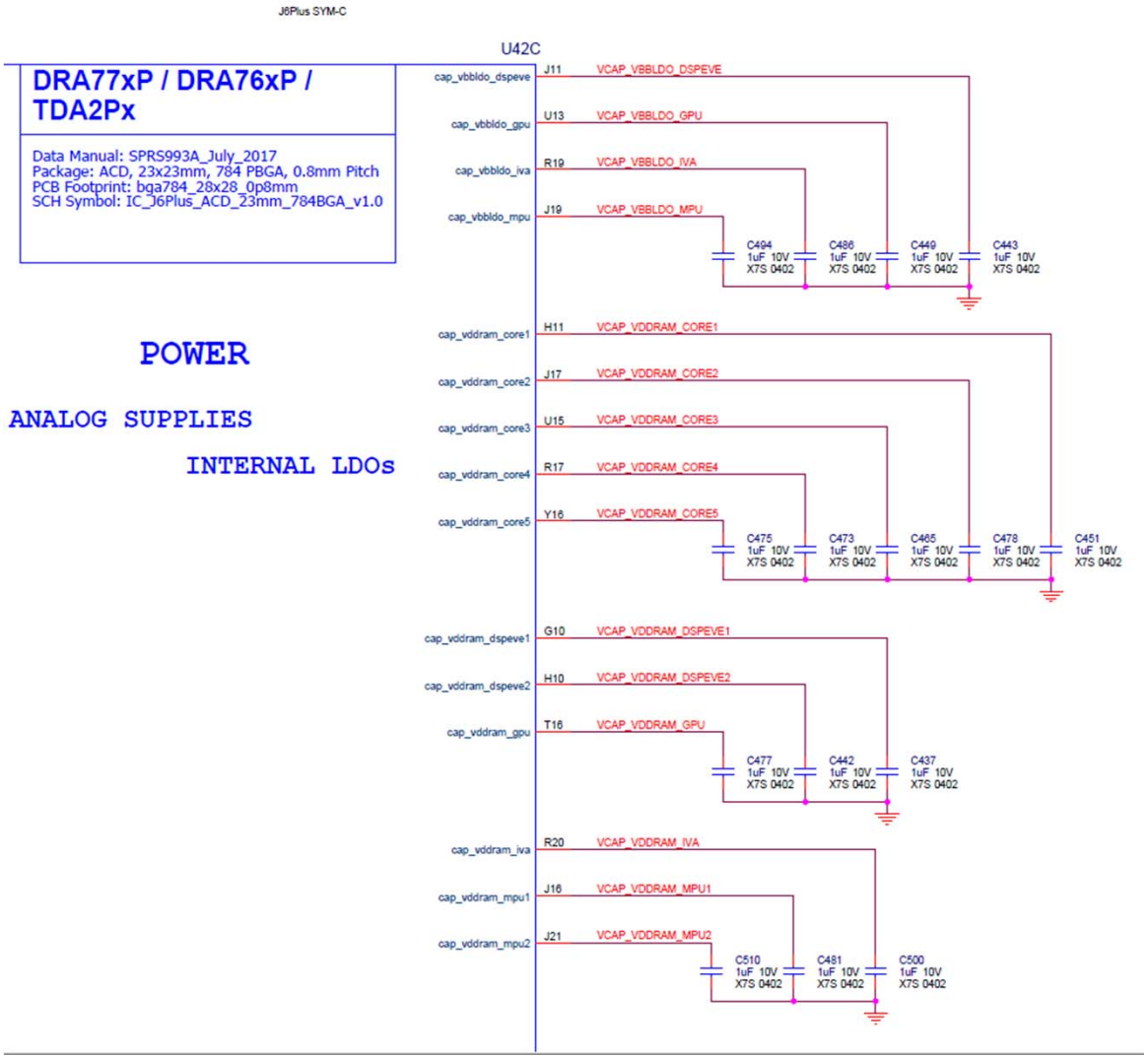


Green box = Power rail's Max Target Impedance of 130mOhm up to "Freq of Interest" 100 MHz

VCAP_XXX
POWER DOMAIN

Recommended Dcap Scheme Optimized for PCB Design				Power Rail:	VCAP_xxx			
Ref Des	**Vaule [uF]**	**Qty**	**Description #1**	**Manufacturer #1**	**Manf #1 P/N**	**Description #2**	**Manufacturer #2**	**Manf #2 P/N**
C494, 486, 449, 443, 475, 473, 465, 478, 451, 477, 442, 437, 510, 481, 500	1.0	15	1.0uF, +/-20%, X7S, 4V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	Murata	LLL215C70G105MA11L	1.0uF, +/-20%, X7R, 6.3V, 0508, -55 to +125C, Low Inductance, Multilayer Ceramic Cap	TDK	C1220X7R0J105M085AC
Totals	15.0	15	Note: Two different dielectric materials are included in this scheme, denoted by blue font					

VCAP_xxx – Simplified SCH



Loop Inductance – VCAP_xxx

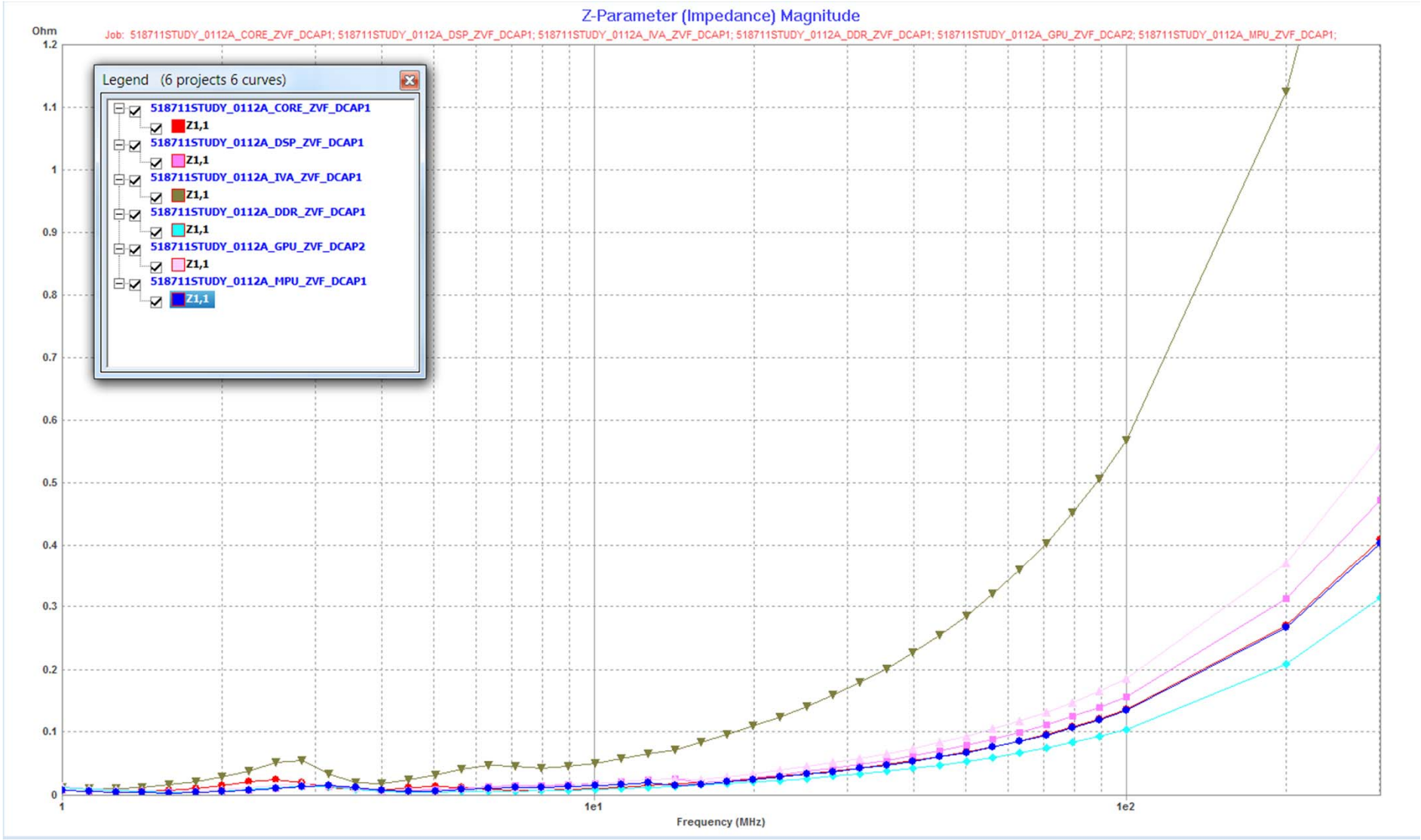
- Decoupling Cap's Loop Inductance (LL) Range: 1.20 – 1.63 nH (@ 50 MHz)

Capacitor Footprints (FP)	Footprint Types	Inductance	Code
	2-via, skinny-end exit	Highest	2vSEE
	2-via, wide-end exit		2vWEE
	2-via, wide-side exit		2vWSE
	4-via, wide-side exit		4vWSE
	via in-pad	Lowest	vIP

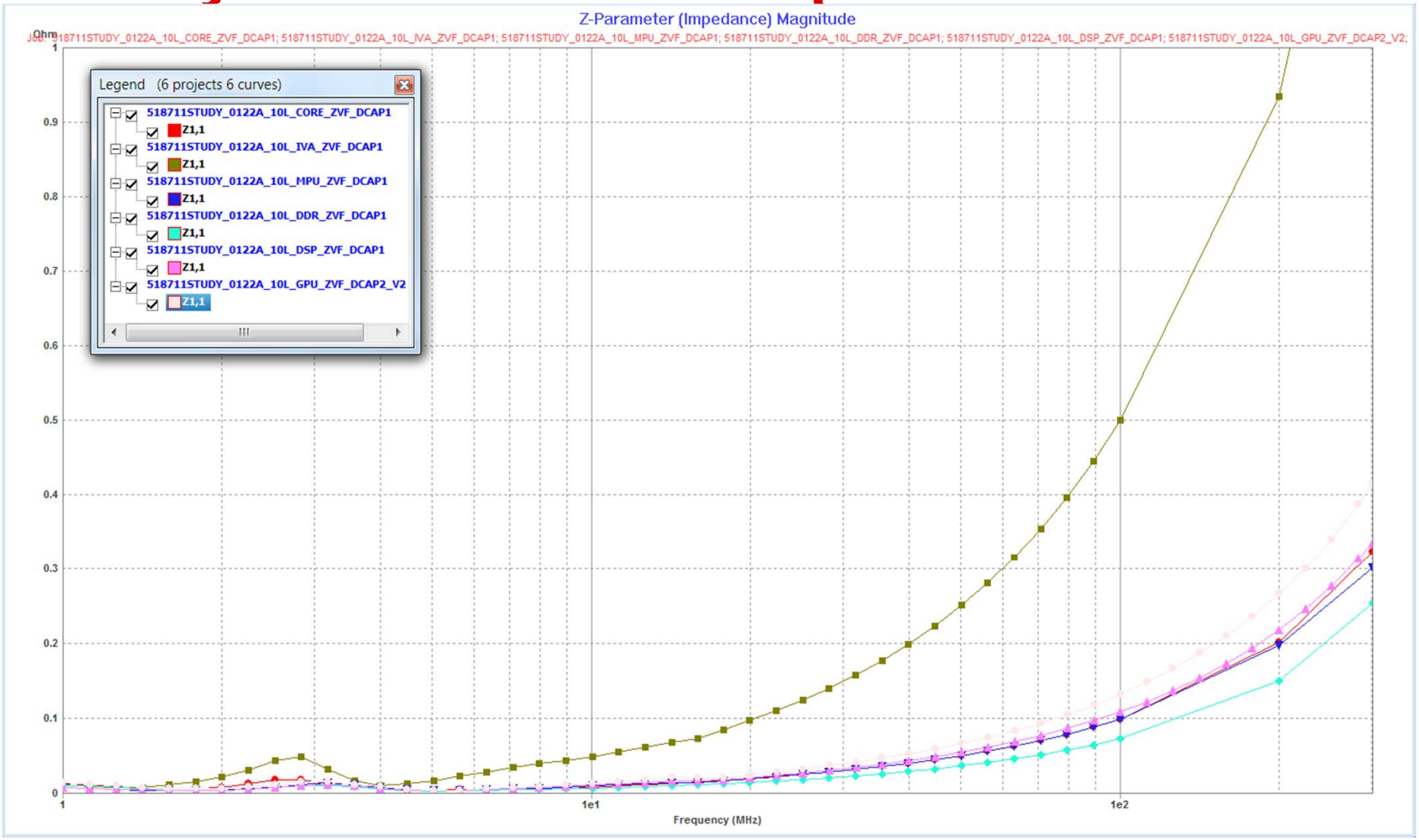
Item #	Cap Ref Des	Loop Inductacne @ 50MHz [nH]	Footprint Types	PCB Side	Value [uF]	Size
1	C437	1.62	2vWEE	Bottom, Under BGA	1	0402
2	C442	1.63	2vWEE	Bottom, Under BGA	1	0402
3	C443	1.544	2vWEE	Bottom, Under BGA	1	0402
4	C449	1.39	2vWEE	Bottom, Under BGA	1	0402
5	C451	1.43	2vWEE	Bottom, Under BGA	1	0402
6	C465	1.2	2vWEE	Bottom, Under BGA	1	0402
7	C473	1.41	2vWEE	Bottom, Under BGA	1	0402
8	C475	1.42	2vWEE	Bottom, Under BGA	1	0402
9	C477	1.519	2vWEE	Bottom, Under BGA	1	0402
10	C478	1.57	2vWEE	Bottom, Under BGA	1	0402
11	C481	1.52	2vWEE	Bottom, Under BGA	1	0402
12	C486	1.44	2vWEE	Bottom, Under BGA	1	0402
13	C494	1.46	2vWEE	Bottom, Under BGA	1	0402
14	C500	1.57	2vWEE	Bottom, Under BGA	1	0402
15	C510	1.53	2vWEE	Bottom, Under BGA	1	0402
	Min	1.20				
	Max	1.63				

Reference

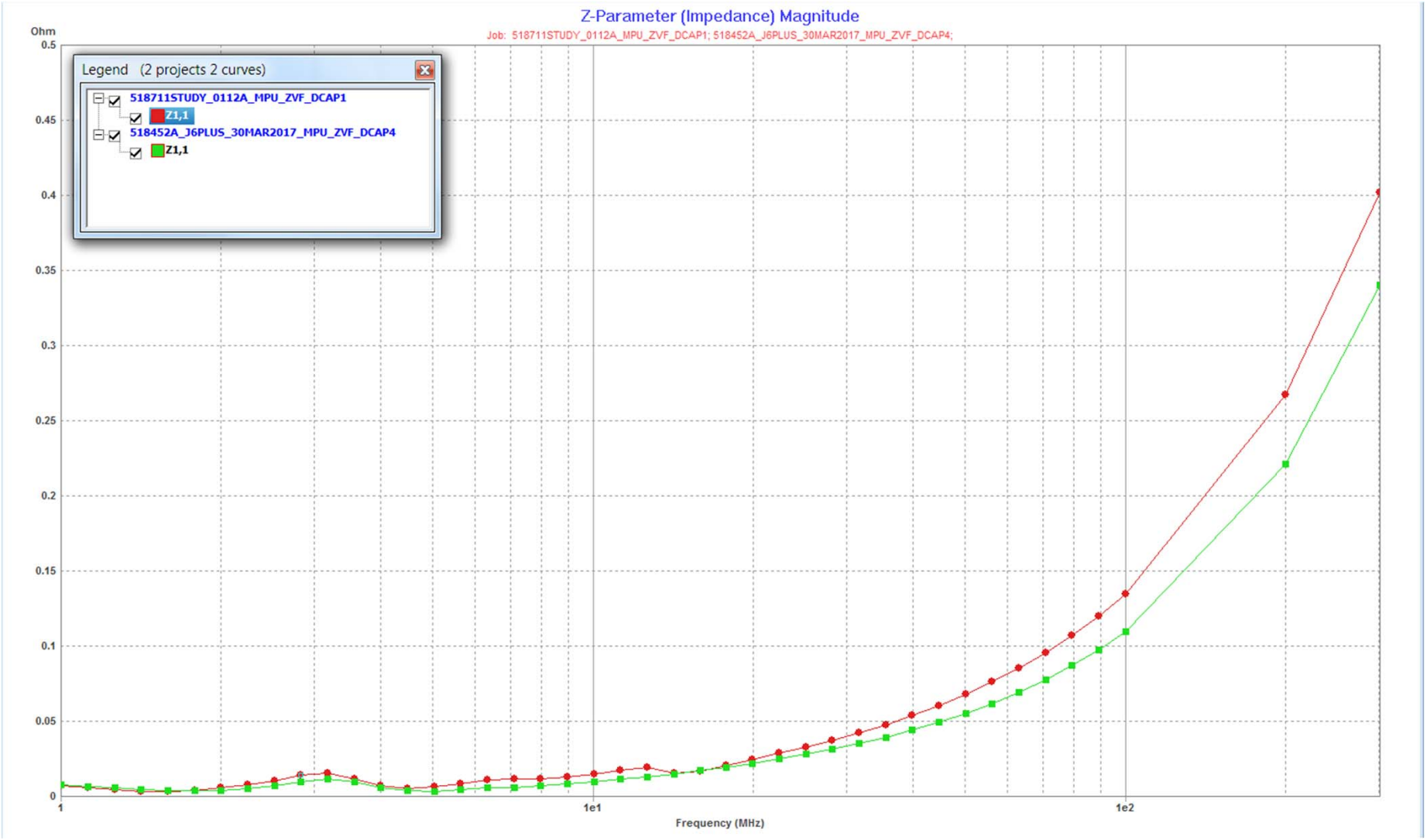
8 Layer Power Rails Composite Plot



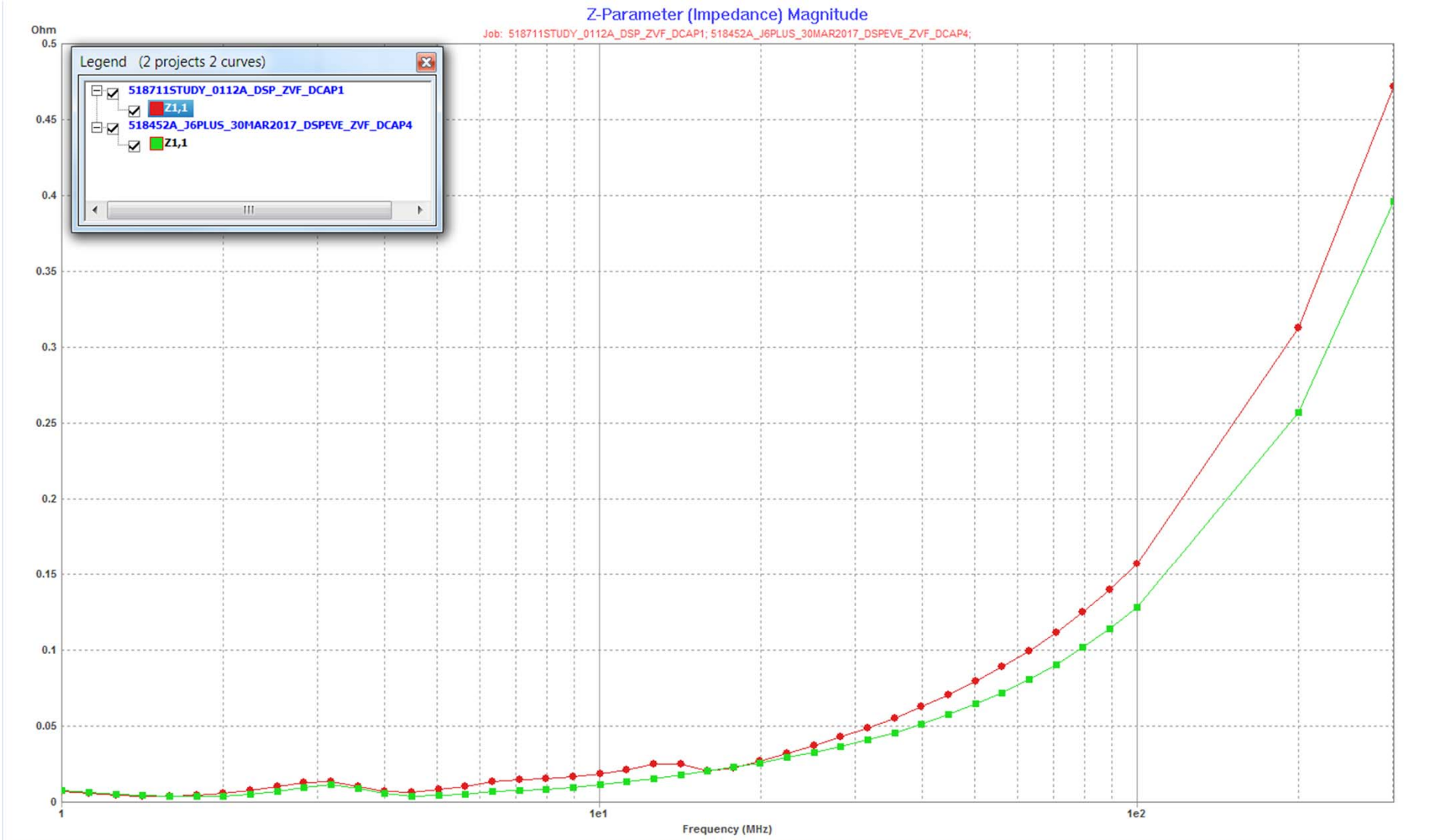
10 Layer Power Rail Composite



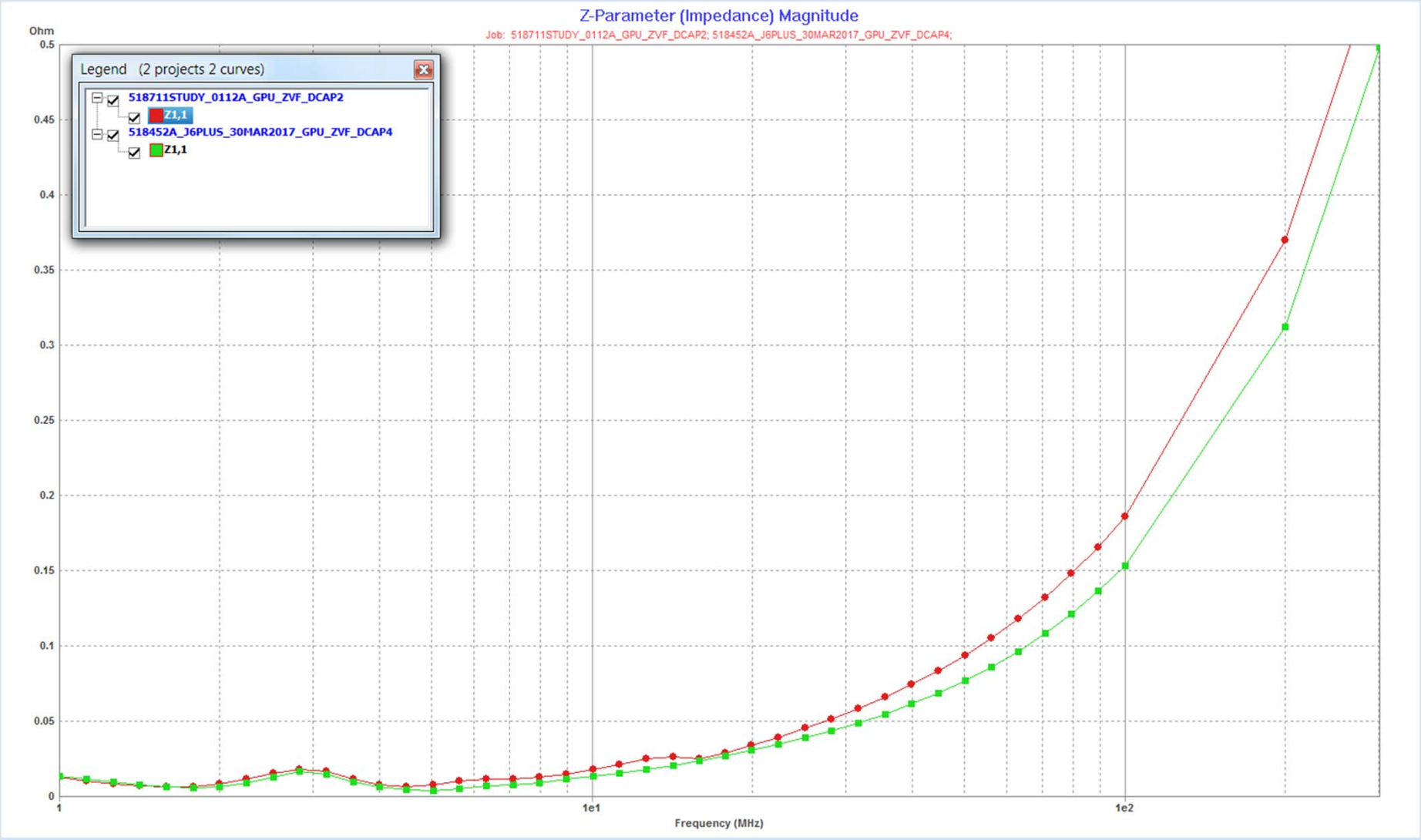
EVM vs 8 Layer – VDD_MPU_AVS



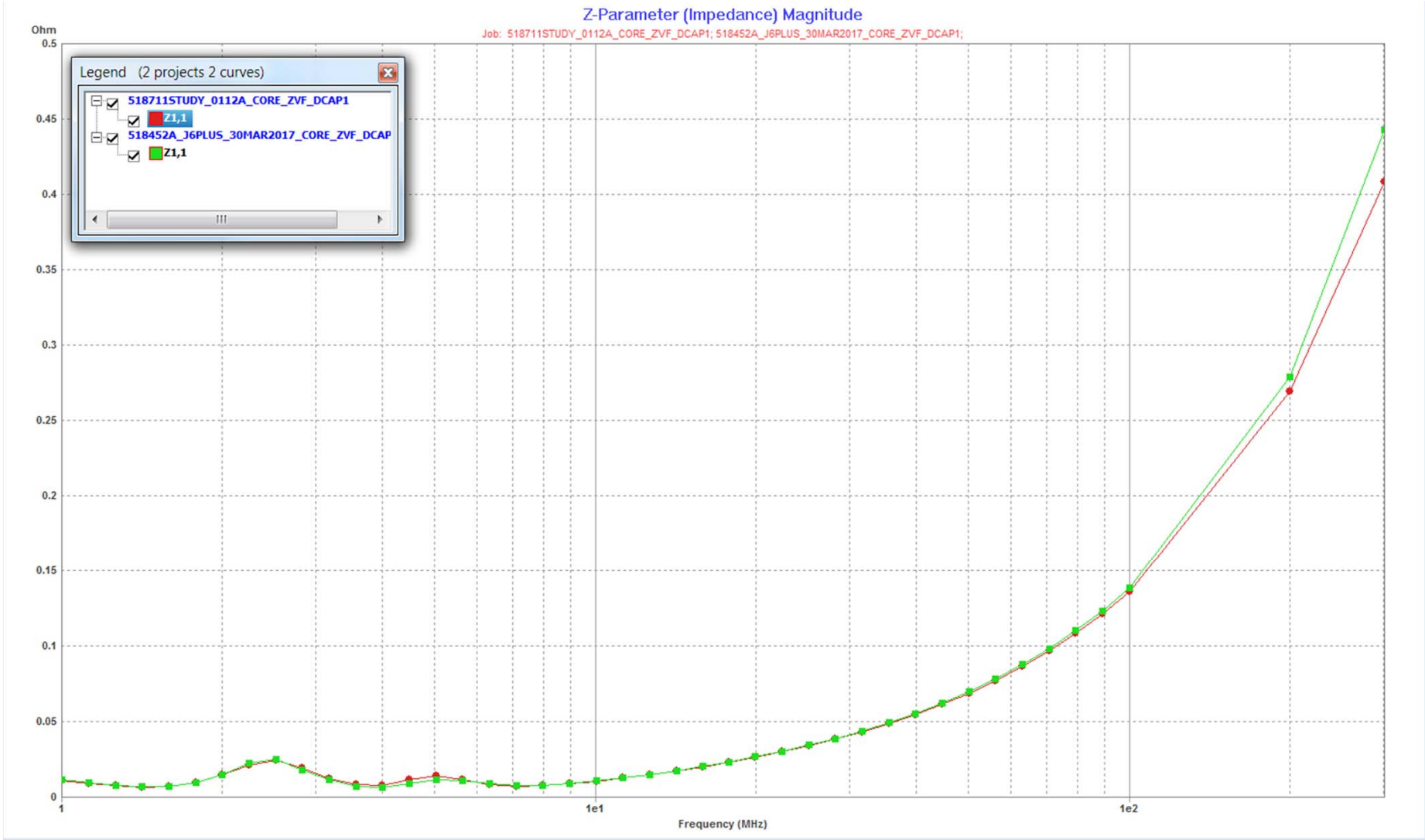
EVM vs 8 Layer – VDD_DSP_AVS



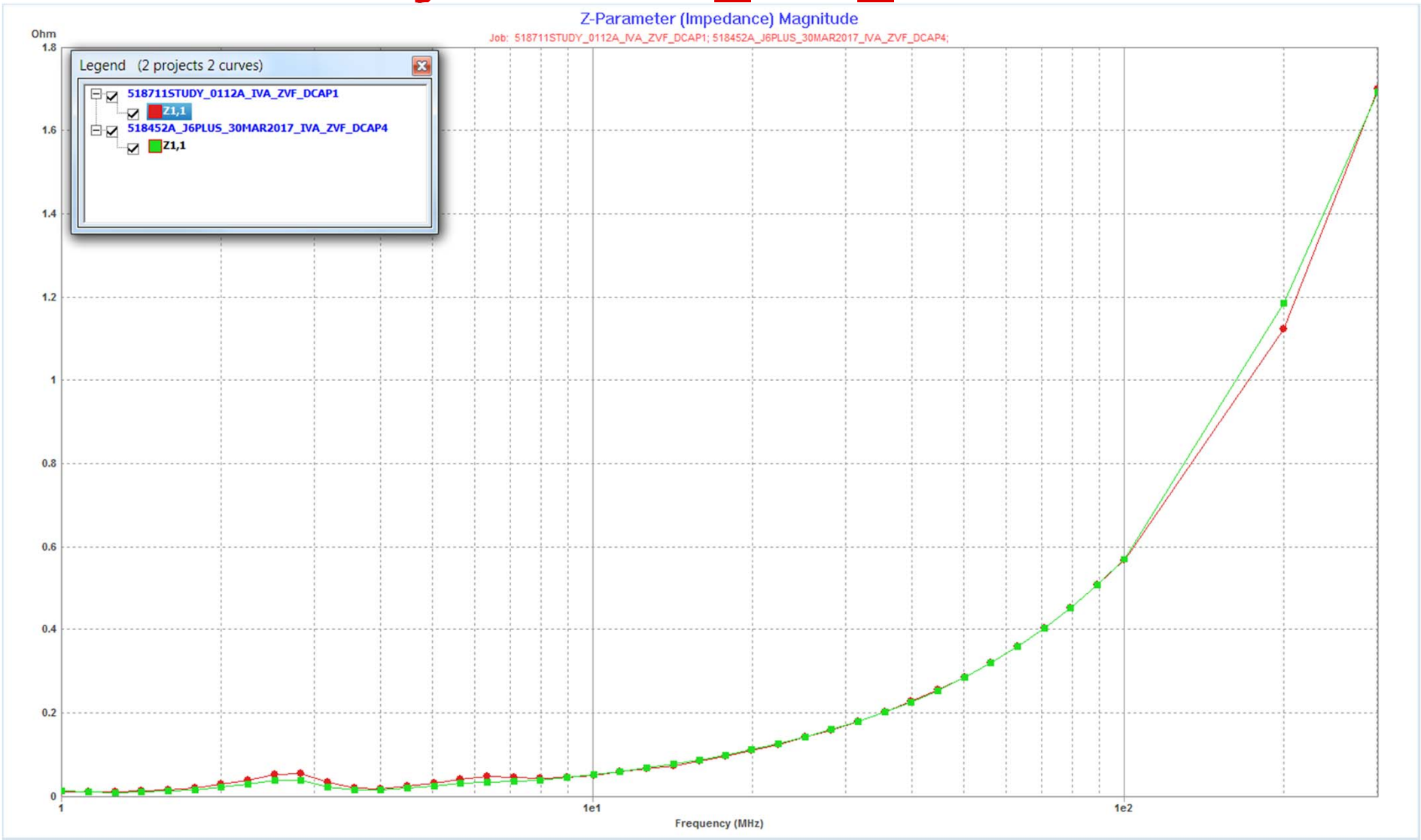
EVM vs 8 Layer – VDD_GPU_AVS



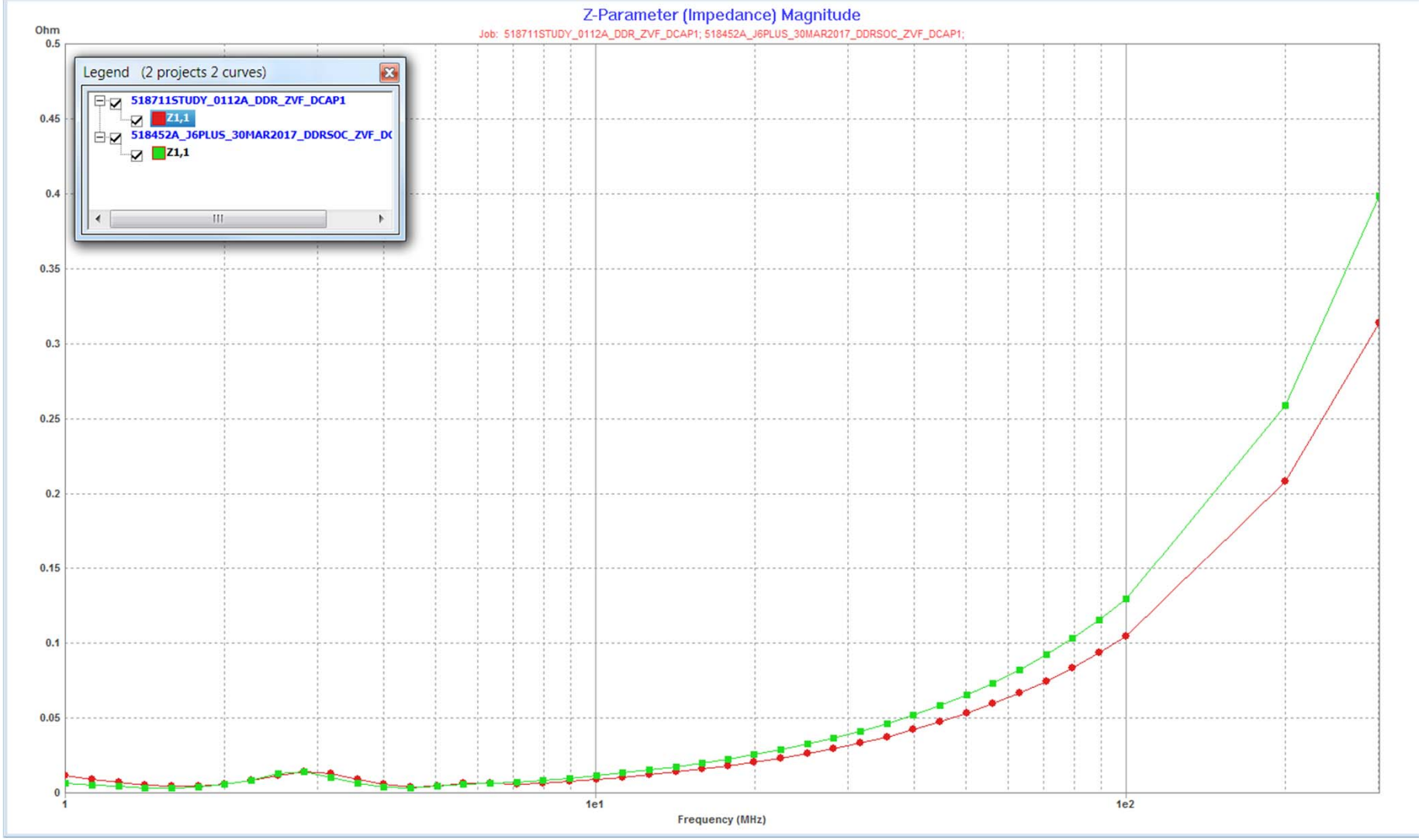
EVM vs 8 Layer – VDD_CORE_AVS



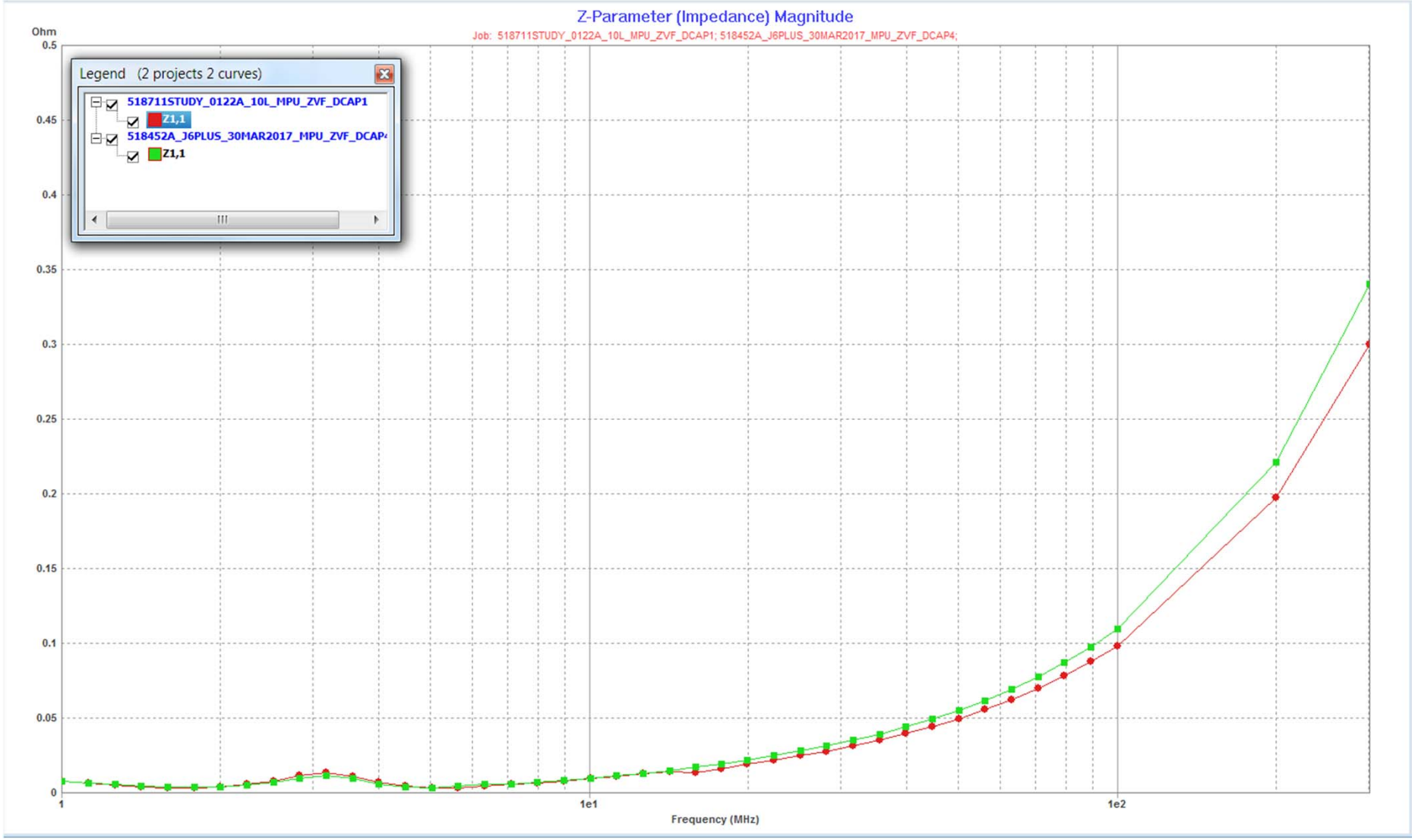
EVM vs 8 Layer – VDD_IVA_AVS



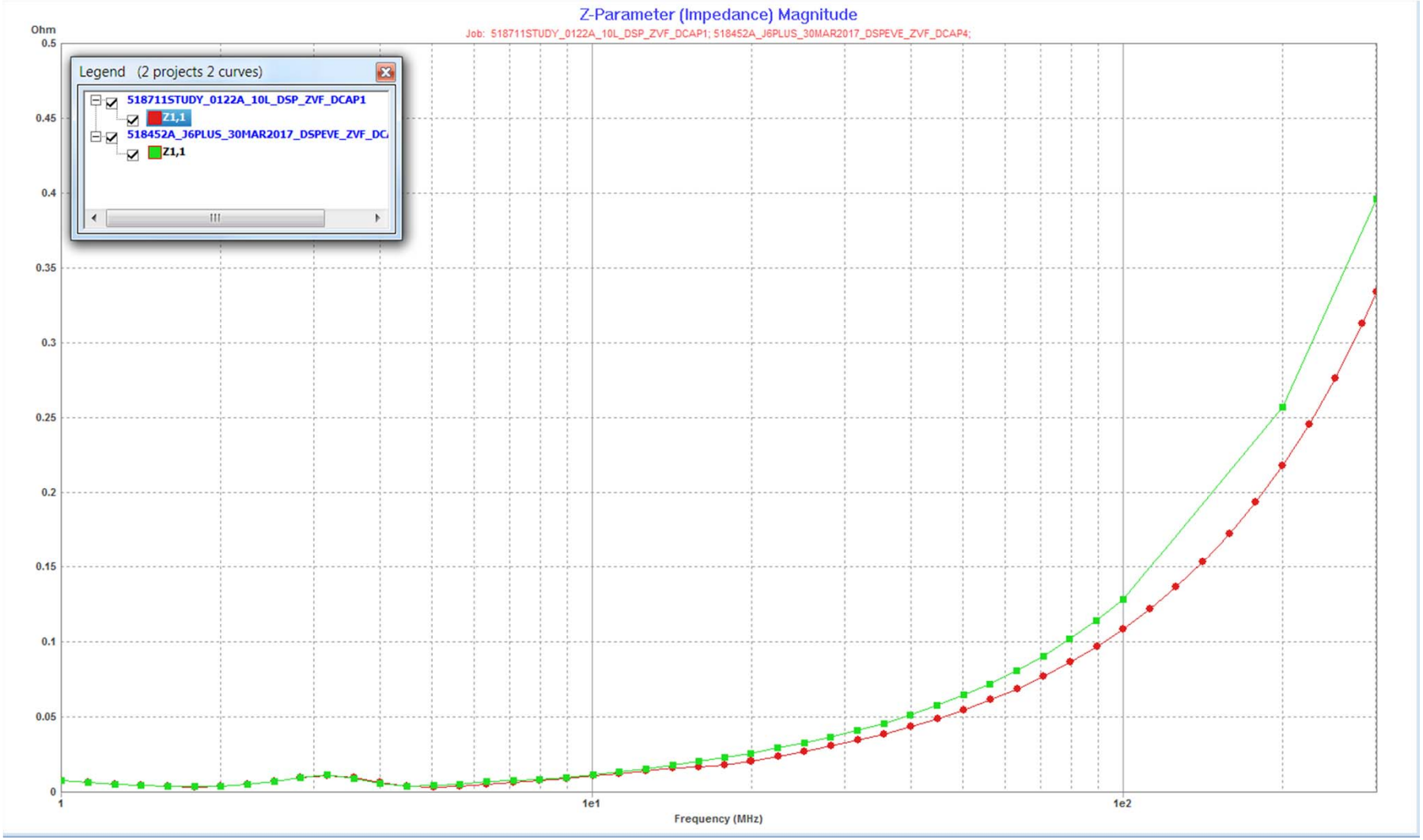
EVM vs 8 Layer – VDDR_MEM_1V35



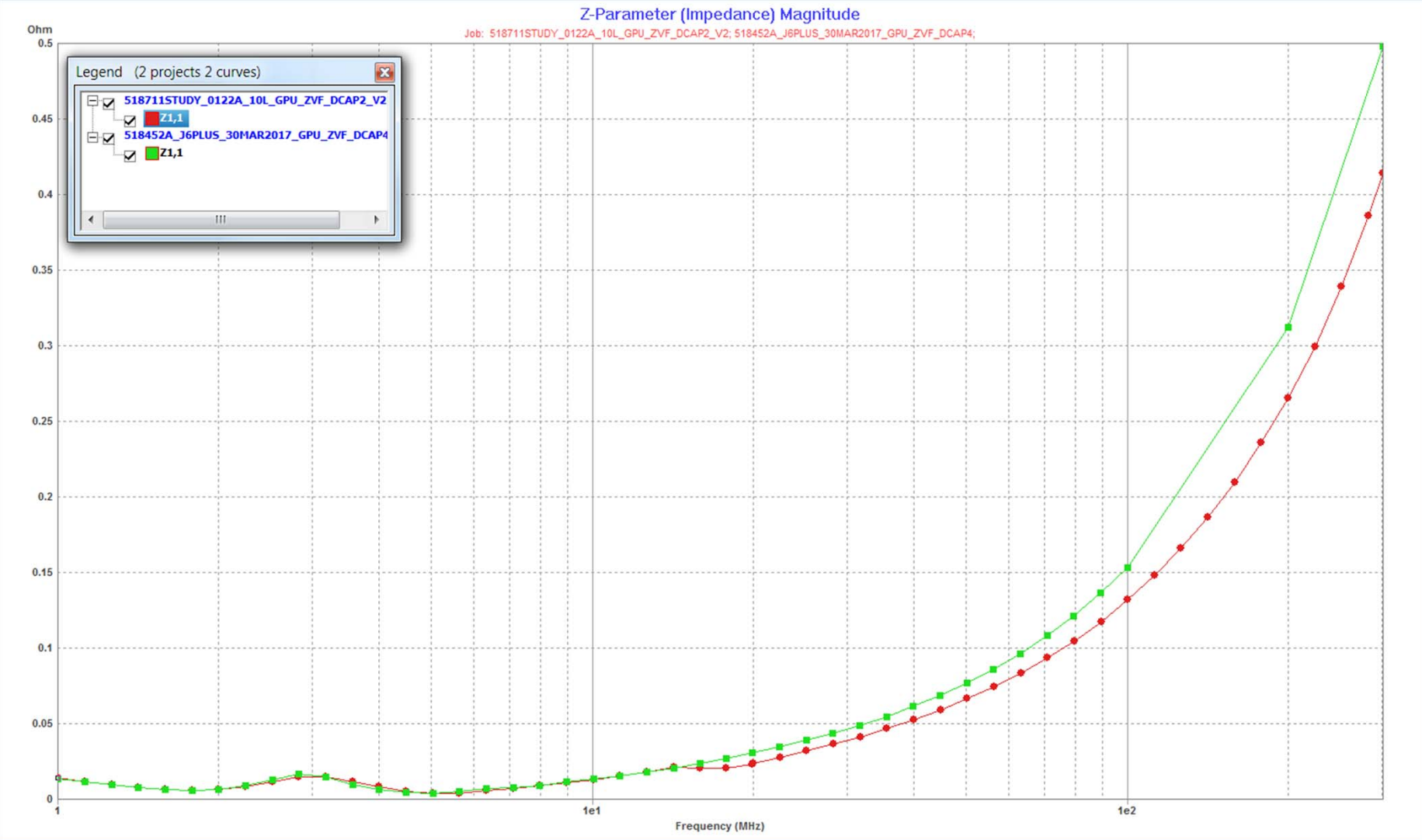
EVM vs 10 Layer – VDD_MPU_AVS



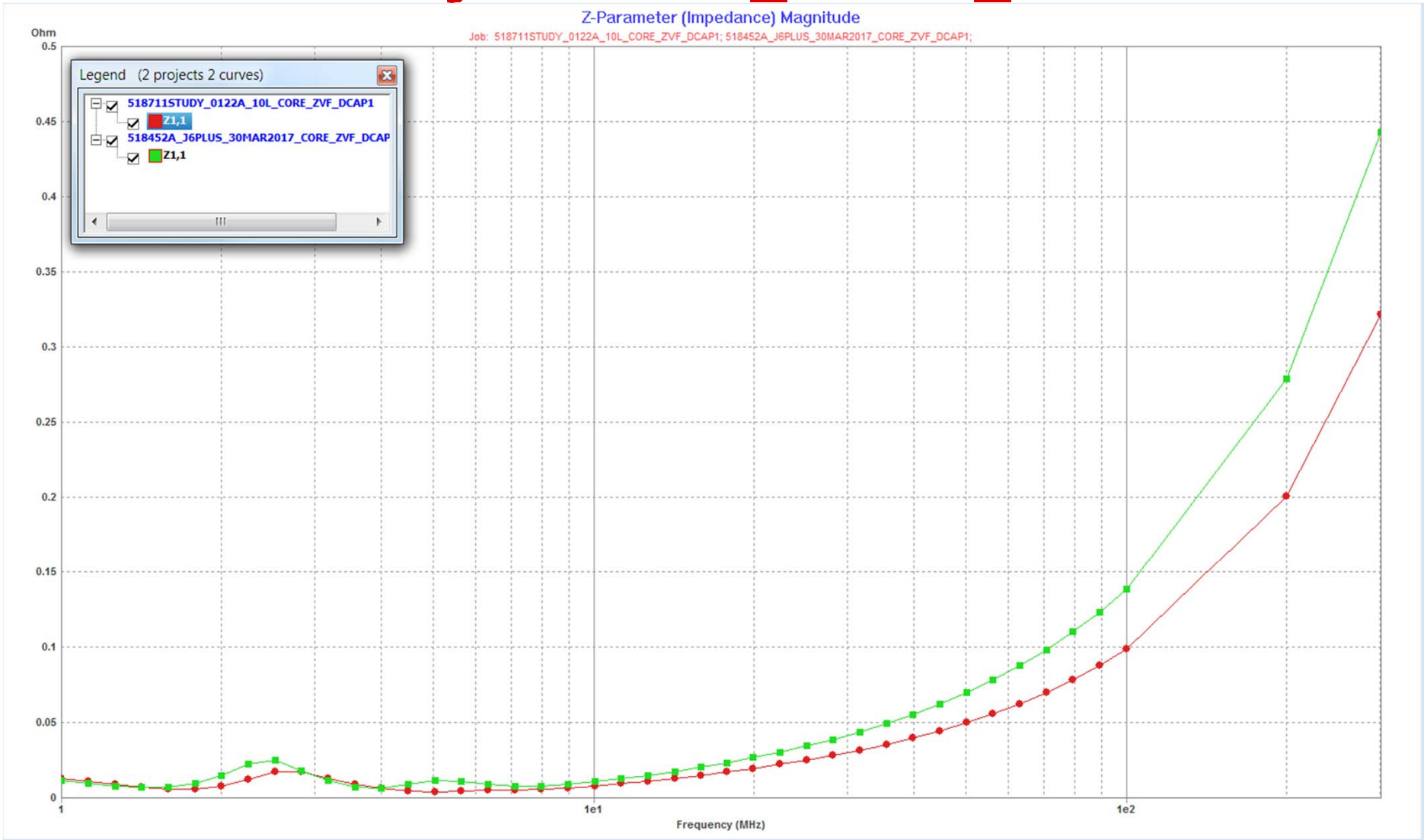
EVM vs 10 Layer – VDD_DSP_AVS



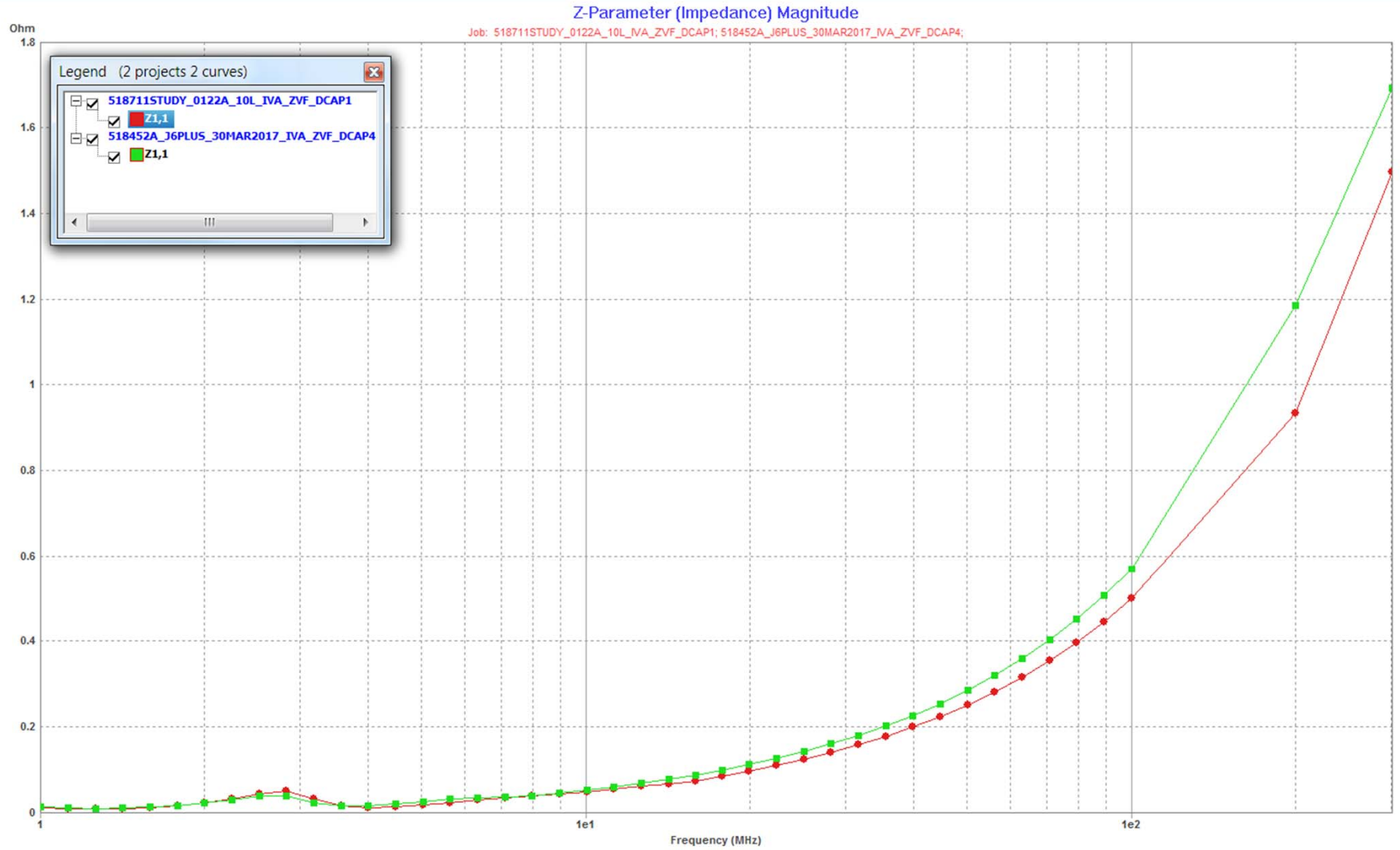
EVM vs 10 Layer – VDD_GPU_AVS



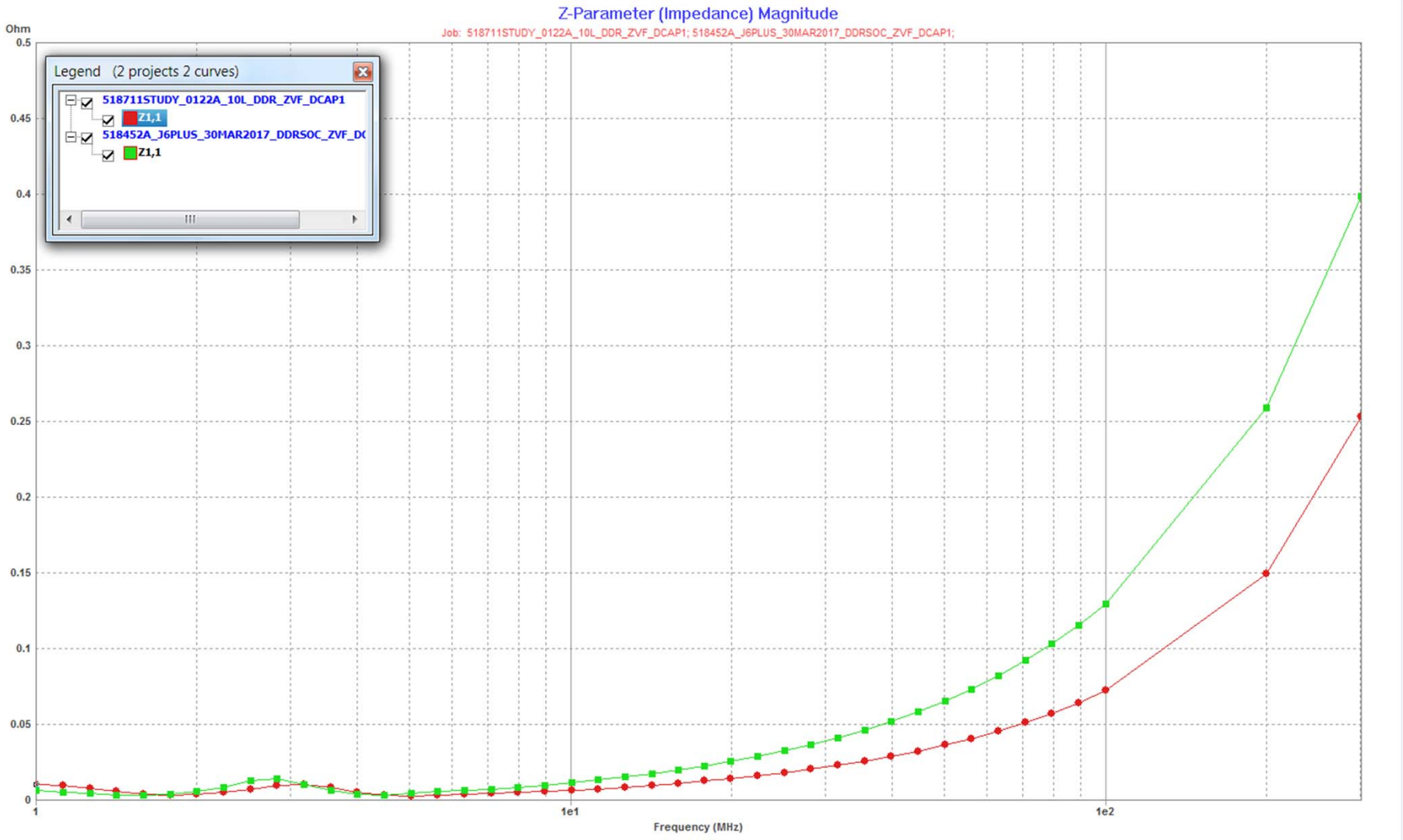
EVM vs 10 Layer – VDD_CORE_AVS



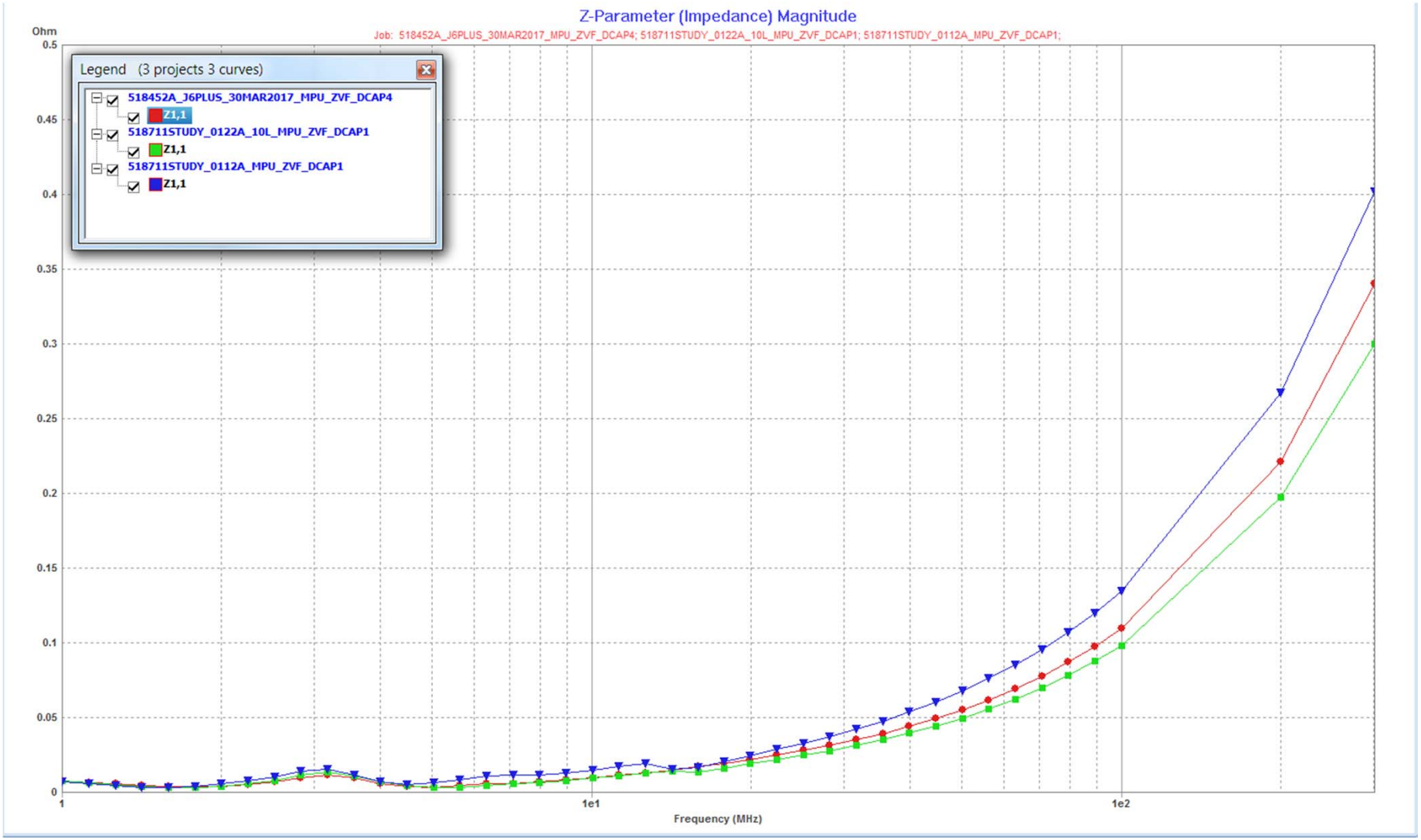
EVM vs 10 Layer – VDD_IVA_AVS



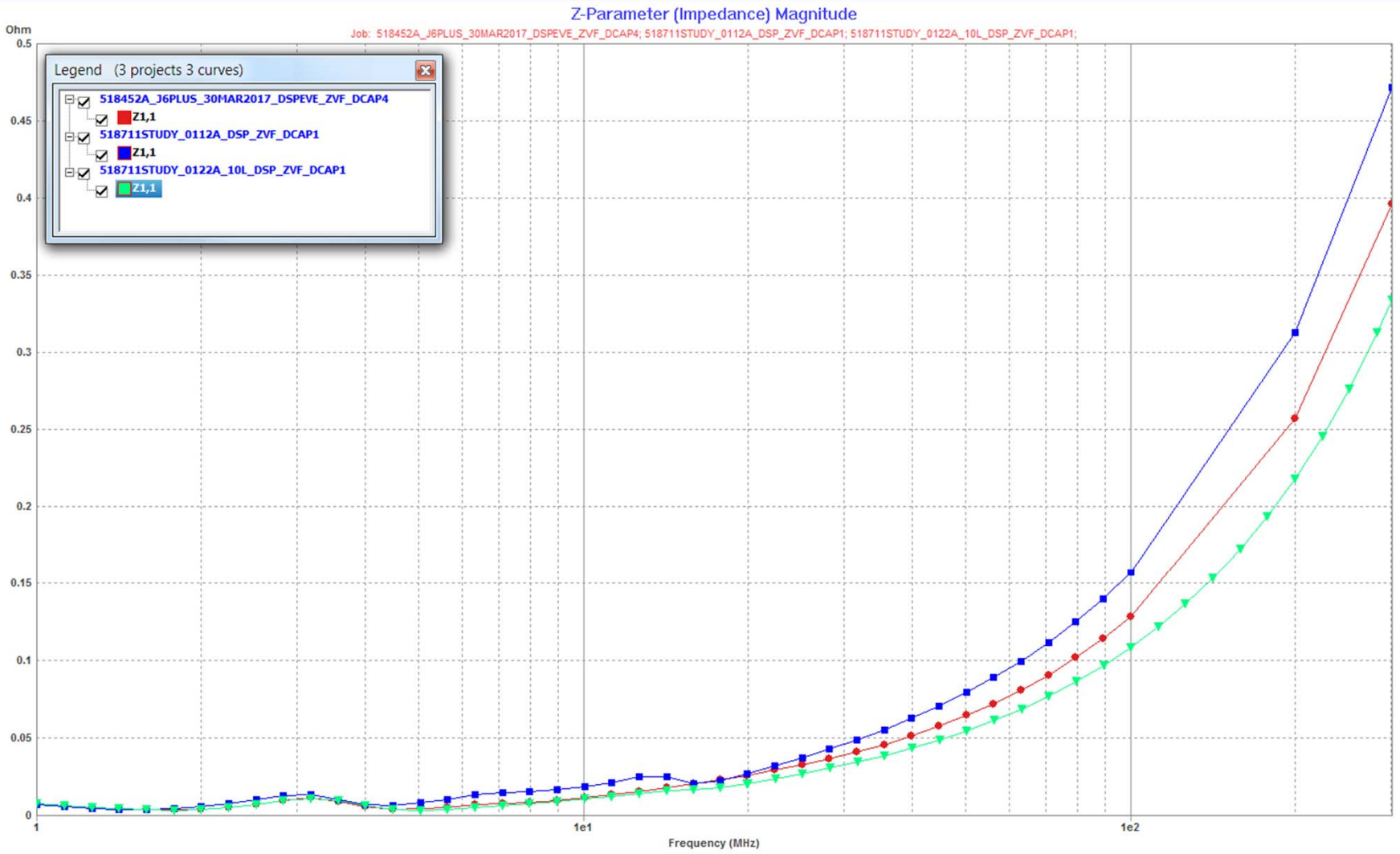
EVM vs 10 Layer – VDDR_MEM_1V35



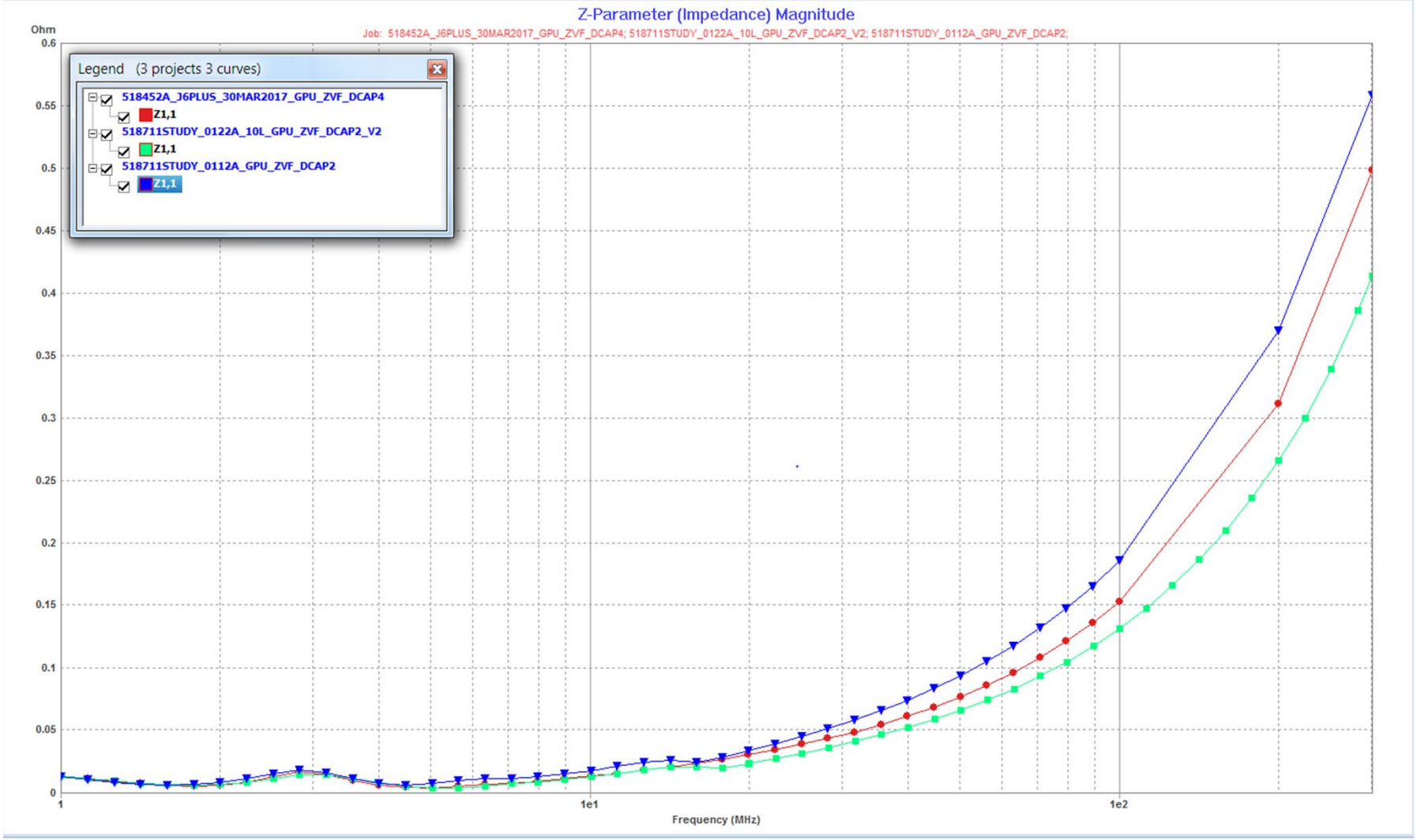
EVM vs 8 Layer vs 10 Layer -VDD_MPU_AVS



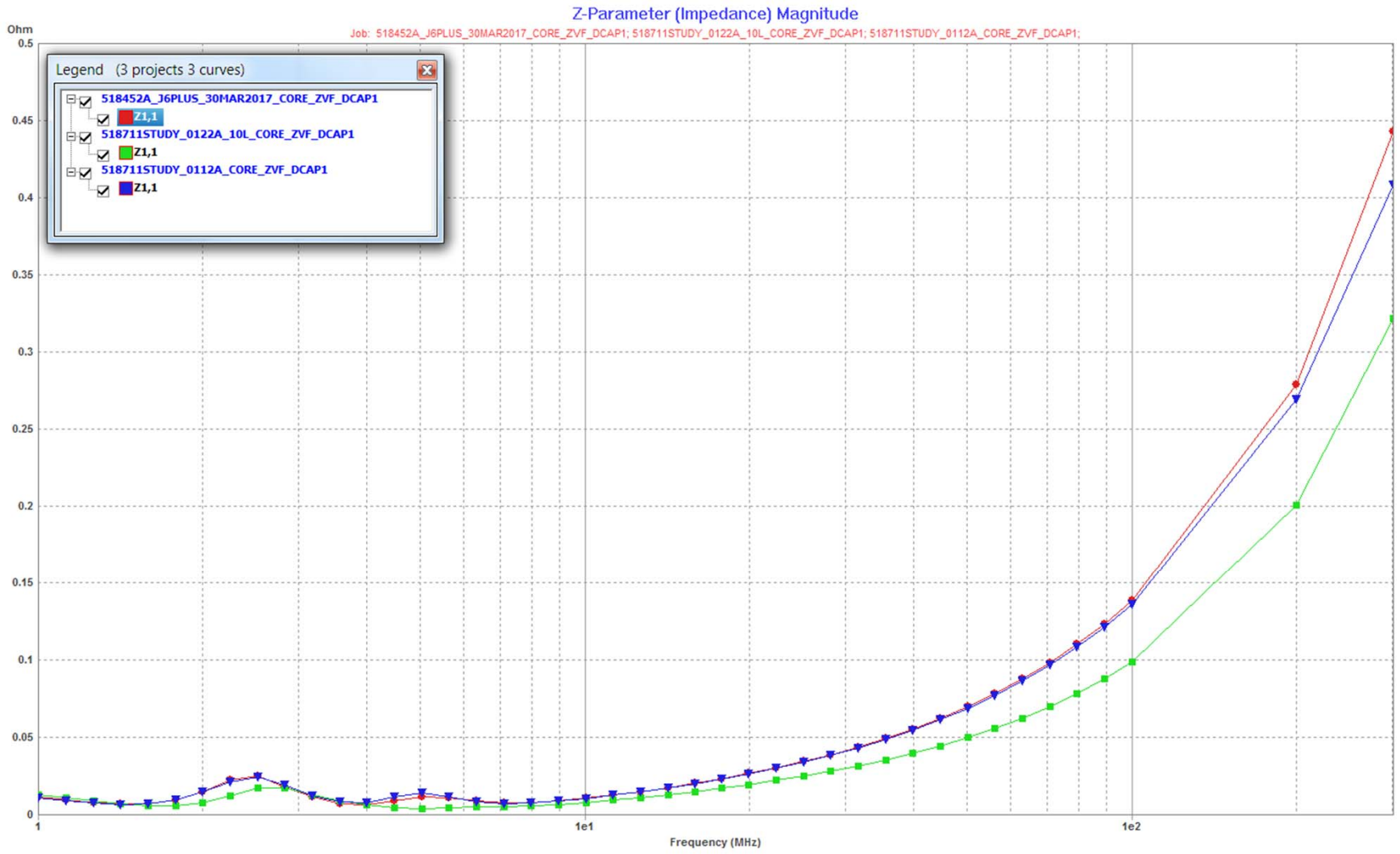
EVM vs 8 Layer vs 10 Layer -VDD_DSP_AVS



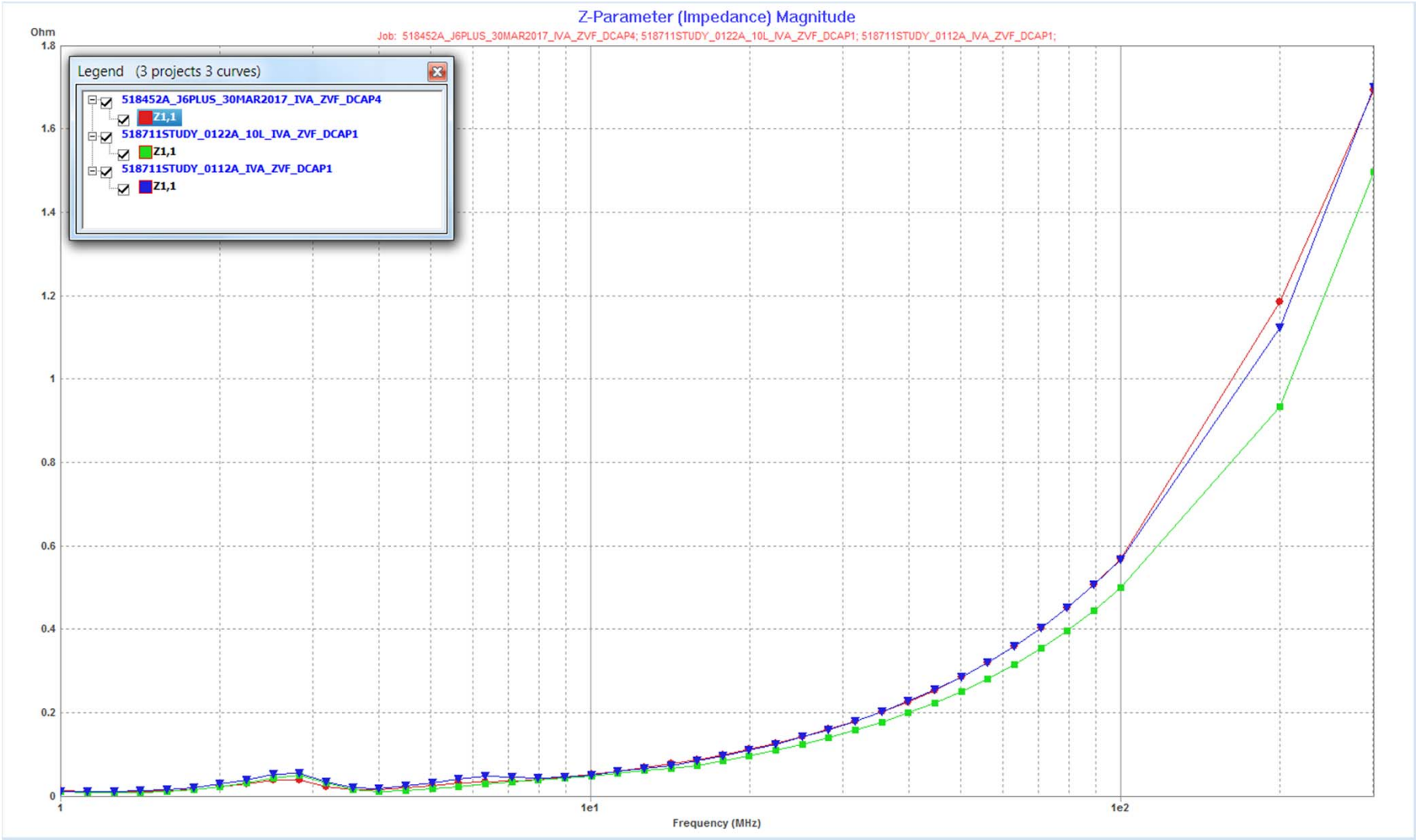
EVM vs 8 Layer vs 10 Layer -VDD_GPU_AVS



EVM vs 8 Layer vs 10 Layer -VDD_CORE_AVS



EVM vs 8 Layer vs 10 Layer -VDD_IVA_AVS



EVM vs 8 Layer vs 10 Layer -VDDR_MEM_AVS