VCL: J7200

J7200 (DRA821) Power Integrity Targets

Date: 11/17/2022 Rev 0.2

		Static Analysis		Dynamic Analysis		
Routing Priority	**SoC (& SDRAM) Voltage Domain**	**Max Reff** [mΩ]	**Max Cap LL [nH]**	**Low Freq Target Z** (ZT1) [mΩ]	**Mid Freq Target Z** (ZT2) [mΩ]	**High Freq Target Z** (ZT3) [mΩ]
1	VDD_CPU	13	1.5	2.0	26	53
2	VDD_CORE	14	1.5	1.4	21	36
3	VDD_MCU	17	2.0	3.0	29	70
4	VDD_DDR_1V1 (@ SoC)	7	2.0	3.0	30	59

Notes:

1). Low Freq range: 0.1 MHz < LF < 1.0 MHz

2.) Mid Freq range: 1.0 MHz < HF < 20 MHz

3.) High Freq range: 20 MHz < HF < 50 MHz

VCL: J7200 (DRA821) EVM SoM Power Integrity Sim Results

Board: 16-Lyr EVM SoM, Proto/Wkup PCB & SCH PN#: PROC105E5

		Static Analysis		Dynamic Analysis		
Routing Priority	**SoC (& SDRAM) Voltage Domain**	**Max Reff**[1] [mΩ]	**Max Cap LL [nH]**	**Low Freq Pk Result Zpk1** [mΩ]	**Mid Freq Pk Result Zpk2** [mΩ]	**High Freq Pk Result Zpk3** [mΩ]
1	VDD_CPU	12.4	1.5	2.0	25.8	52.7
2	VDD_CORE	13.7	1.5	1.4	20.9	35.2
3	VDD_MCU	16.1	2.0	2.5	28.2	69.9
4	VDD_DDR_1V1 (@ SoC)	6.9	2.0	2.9	29.7	58.2

Notes:

1). Low Freq range: 0.1 MHz < LF < 1.0 MHz

2.) Mid Freq range: 1.0 MHz < HF < 20 MHz

3.) High Freq range: 20 MHz < HF < 50 MHz

4.) Estimated Dcap LL, awaiting PI sim results on PROC105E5.