AEN: J722S

J722S (TDA4AEN) Preliminary PCB Power Integrity Targets

Date: 10/22/2024   Rev 0.2   Aligned to J722S EVM Board (PROC170E3_SCH/BRD) PI sim results

Routing Priority	SoC (& SDRAM) Voltage Domain	Static Analysis		Dynamic Analysis		
		Max Reff[4] [mΩ]	Max Cap LL [nH]	Low Freq[1] Target Z (ZT1) [mΩ]	Mid Freq[2] Target Z (ZT2) [mΩ]	High Freq[3] Target Z (ZT3) [mΩ]
1	VDD_CORE	4.3	1.0	2.5	4.3	11.2
2	VDD_DDR_1V1	78.6	2.0	37	74	111

Notes:

1). Low Freq range: Buck Fsw/10 (~0.2 -0.44) MHz < LF < 1.0 MHz

2.) Mid Freq range: 1.0 MHz < HF < 20 MHz

3.) High Freq range: 20 MHz < HF < 50 MHz

4) Max routing resistance from regulator to point of load at remote sense feedback to compensate ~7.5% supply drop.