AHP: J784S4

J784S4 (TDA4AP\AH\VP\VH) PCB Power Integrity Targets Date: 06/17/2024 Rev 0.6

		Static Analysis		Dynamic Analysis		
Routing Priority	SoC (& SDRAM) Voltage Domain	Max Reff[4] [mΩ]	Max Cap LL [nH]	Low Freq[1] Target Z (ZT1) [mΩ]	Mid Freq[2] Target Z (ZT2) [mΩ]	High Freq[3] Target Z (ZT3) [mΩ]
1	VDD_CPU_AVS	1.4	1.0	1.5	2.4	6.3
2	VDD_CORE_0V8	3.7	1.0	2.1	2.8	7.1
3	VDD_DDR_1V1	49.0	2.0	21	35	70
4	VDD_MCU_0V85	47.7	2.0	33	44	88

Notes:

1). Low Freq range: Buck Fsw/10 (~0.2 -0.44) MHz < LF < 1.0 MHz

2.) Mid Freq range: 1.0 MHz < MF < 20 MHz

3.) High Freq range: 20 MHz < HF < 50 MHz

4) Max routing resistance from regulator to point of load at remote sense feedback to compensate ~7.5% supply drop.