Jacinto 7 High-Speed Interface Layout Guidelines

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ABSTRACT

As modern bus interface frequencies scale higher, care must be taken in the printed circuit board (PCB) layout phase of a design to ensure a robust solution.

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1 Introduction

1.1 Overview

This application report can help system designers implement best practices and understand PCB layout options when designing platforms. This document is intended for audiences familiar with PCB manufacturing, layout, and design.

A primary concern when designing a system is accommodating and isolating high-speed signals. As high speed signals are most likely to impact or be impacted by other signals, they must be laid out early in the PCB design process to ensure that prescribed routing rules can be followed.

1.2 Trace Impedance

High speed signals trace impedance needs to designed as to minimize the reflections in traces. The high speed protocol that is being designed for determines what the single and differential trace Impedance the traces need to meet as well as the tolerance for the impedance (50 Ω ±15%). To have designs be robust from PCB manufacturing errors and defects design the traces impedance be as close to the recommended value. The geometry of the traces, the permittivity of the PCB material and the layers surrounding the trace all impact the impedance of the signal trace.

In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production. For PCBs with very tight space limitations (which are usually small) this can work, but for most PCBs, the loosely coupled option is probably best.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier (because each trace is not so fixed in position relative to the other), and trace width variations do not affect impedance as much, therefore, it is easier to maintain an accurate impedance over the length of the signal. For longer routes, the wider traces also show reduced skin effect and often result in better signal integrity with a larger eye diagram opening.

1.3 High-Speed Signal Trace Lengths

As with all high-speed signals, keep total trace length for signal pairs to a minimum. For trace length requirements for each protocol and device, see later sections in this document.

1.4 Differential Signal Length Matching

Match the etch lengths of the relevant differential pair traces. Intra-pair skew is the term used to define the difference between the etch length of the + and - lane of a differential pair. Inter-pair skew is used to describe the difference between the etch lengths of a differential pair from another differential pair of the same group. The etch length of the differential pair groups do not need to match. For example the etch lengths of USB 3.0 TX and RX do not need to match. There are also standards that do not have a Interpair skew requirement because the different lanes do not have to be the same length. When matching the intra-pair skew of the high-speed signals, add serpentine routing to match the lengths as close to the mismatched ends as possible, see Figure 1.

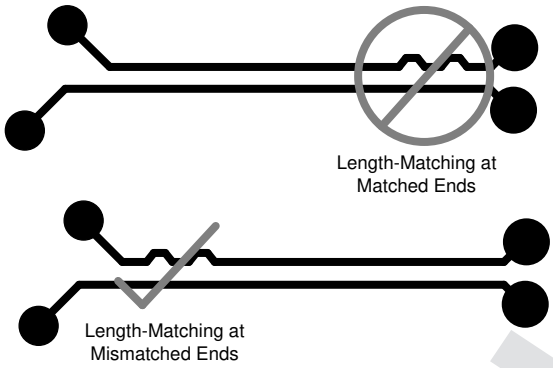


Figure 1. Differential Pair Length Matching

1.5 High-Speed Signal Reference Planes

An electrical circuit must always be a closed loop system. With DC, the return current takes the way back with the lowest resistance for DC signals. At higher frequencies, the return current flows along the lowest impedance path, this lowest impedance path is usually the reference plane adjacent to the signal. For this reason it is always best to have a ground plane or power plane on the layer above or below a signal layer. This solid return path helps to reduce impedance changes and decrease EMI issues.

High-speed signals should be routed over a solid GND reference plane and not across a plane split or a void in the reference plane unless absolutely necessary. TI does not recommend high-speed signal references to power planes.

Routing across a plane split or a void in the reference plane forces return high-frequency current to flow around the split or void. This can result in the following conditions:

- Excess radiated emissions from an unbalanced current flow
- Delays in signal propagation delays due to increased series inductance
- Interference with adjacent signals
- Degraded signal integrity (that is, more jitter and reduced signal amplitude)

For examples of correct and incorrect plane void routing, see Figure 2 and Figure 3.

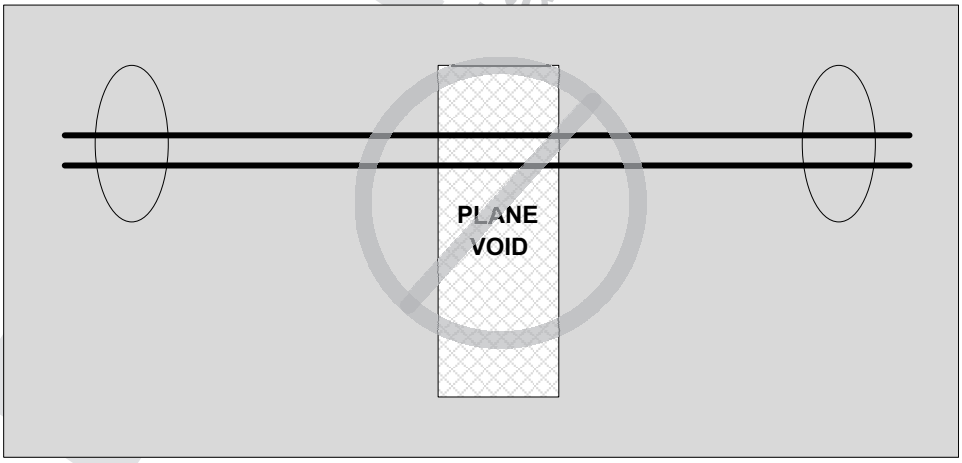


Figure 2. Incorrect Plane Void Routing

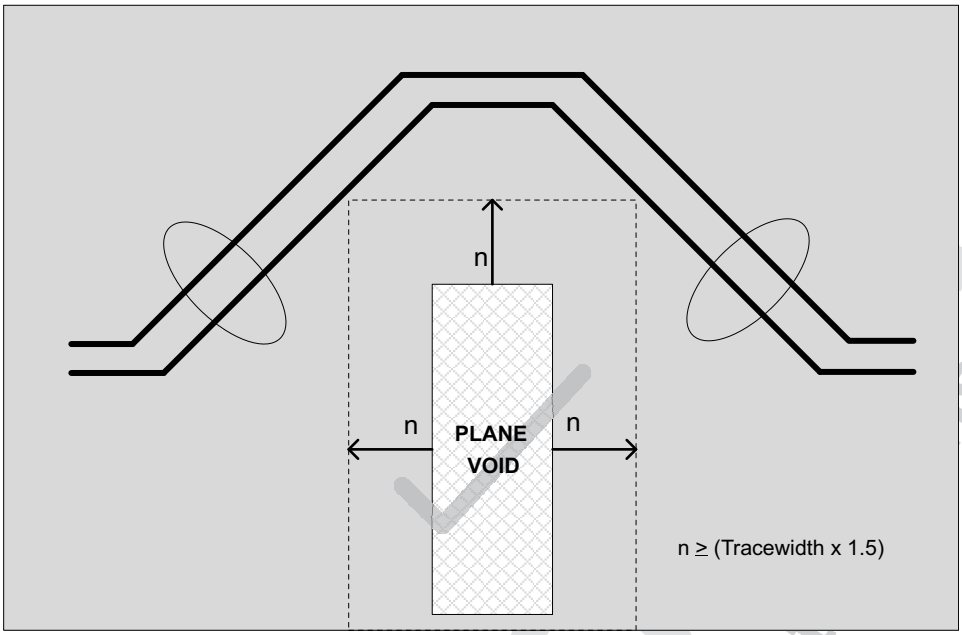


Figure 3. Correct Plane Void Routing

If routing over a plane-split is completely unavoidable, place stitching capacitors across the split to provide a return path for the high-frequency current. These stitching capacitors minimize the current loop area and any impedance discontinuity created by crossing the split. These capacitors should be 1 µF or lower and placed as close as possible to the plane crossing. For examples of incorrect plane-split routing and correct stitch capacitor placement, see Figure 4 and Figure 5.

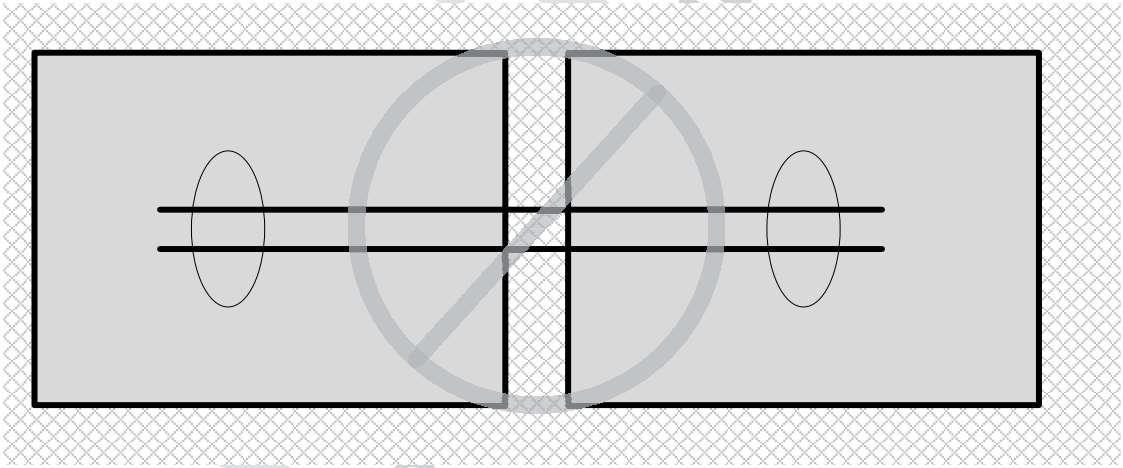


Figure 4. Incorrect Plane-Split Signal Routing

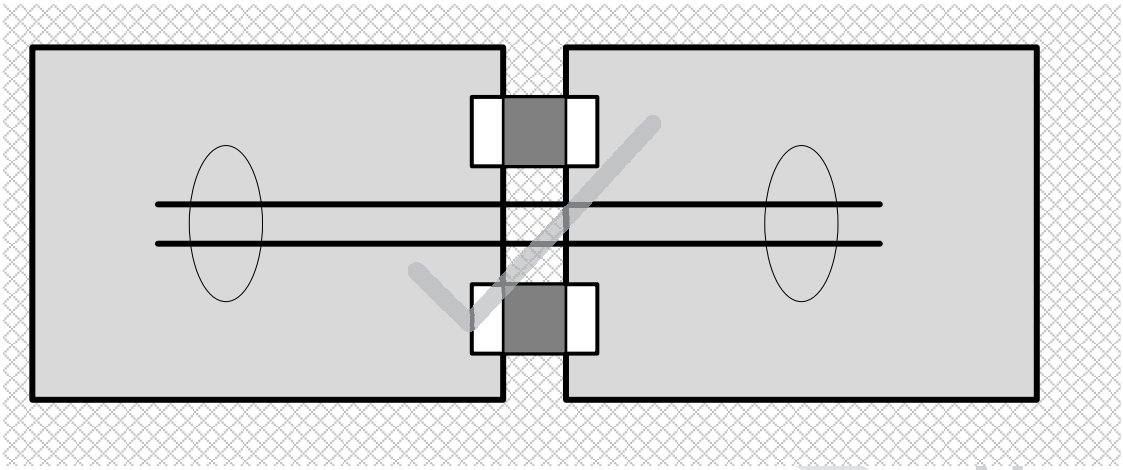


Figure 5. Stitching Capacitor Placement

When planning a PCB stackup, ensure that planes that do not reference each other are not overlapped because this produces unwanted capacitance between the overlapping areas. To see an example of how this capacitance could pass RF emissions from one plane to the other, see Figure 6.

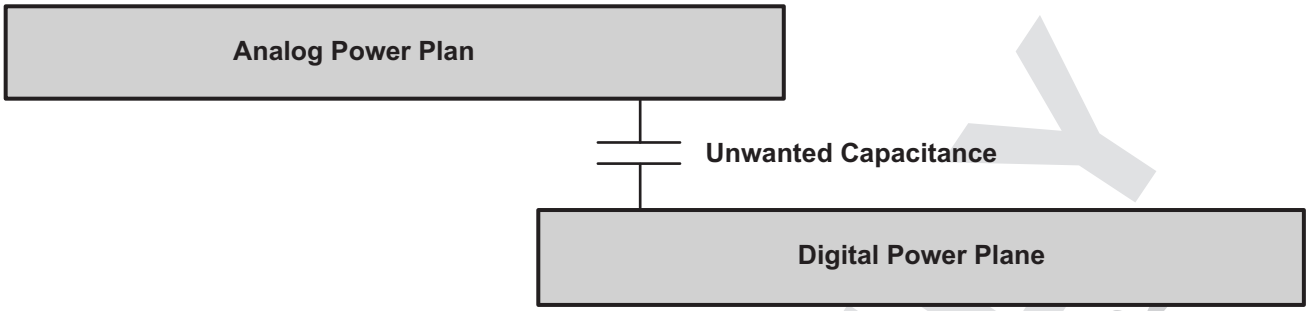


Figure 6. Overlapped Planes

The entirety of any high-speed signal trace should maintain the same GND reference from origination to termination. If unable to maintain the same GND reference, via-stitch both GND planes together to ensure continuous grounding and uniform impedance. Place these stitching vias symmetrically within 200 mils (center-to-center, closer is better) of the signal transition vias. For an example of stitching vias, see Figure 7.

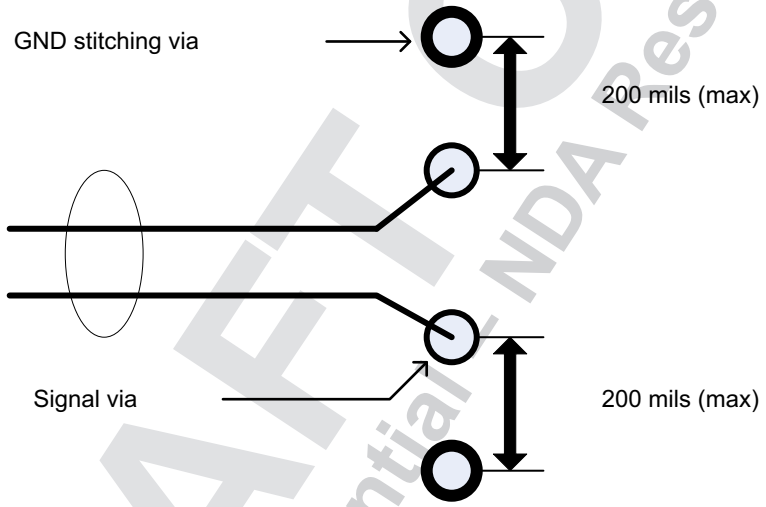


Figure 7. Stitching Vias

TI does not recommend high-speed signal references to power planes unless it is completely unavoidable. If it is unavoidable it is best to use AC coupling capacitors and ground vias to allow the return signal to have a path back from the sink to the source.

1.6 Differential Signal Spacing

To minimize crosstalk in high-speed interface implementations, the spacing between the signal pairs must be a minimum of 5 times the width of the trace. This spacing is referred to as the 5W rule. A PCB design with a calculated trace width of 6 mils requires a minimum of 30 mils spacing between high-speed differential pairs. Also, maintain a minimum keep-out area of 30 mils to any other signal throughout the length of the trace. Where the high-speed differential pairs abut a clock or a periodic signal, increase this keep-out to a minimum of 50 mils to ensure proper isolation. For examples of high-speed differential signal spacing, see Figure 8.

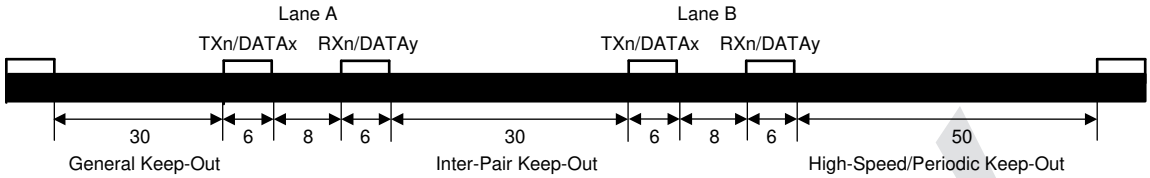


Figure 8. Example of Differential Pair Spacing

1.7 Additional Differential Signal Rules

- Do not place probe or test points on any high-speed differential signal.
- Do not route high-speed traces under or near crystals, oscillators, clock signal generators, switching power regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.
- After BGA breakout, keep high-speed differential signals clear of the SoC because high current transients produced during internal state transitions can be difficult to filter out.
- When possible, route high-speed differential pair signals on the top or bottom layer of the PCB with an adjacent GND layer. TI does not recommend stripline routing of the high-speed differential signals. (or Stripline routing is recommended for all high-speed SerDes signals in the design. This ensures better controlled impedance. Also the signal quality degradation due to EMI is minimized by fabricating traces in between ground planes).
- Ensure that high-speed differential signals are routed ≥ 90 mils from the edge of the reference plane.
- Ensure that high-speed differential signals are routed at least 1.5 W (calculated trace-width × 1.5) away from voids in the reference plane. This rule does not apply where SMD pads on high-speed differential signals are voided.
- Maintain constant trace width after the SoC BGA escape to avoid impedance mismatches in the transmission lines.
- Maximize differential pair-to-pair spacing when possible (loosely coupled).

1.8 Symmetry in the Differential Pairs

Route all high-speed differential pairs together symmetrically and parallel to each other. Deviating from this requirement occurs naturally during package escape and when routing to connector pins. These deviations must be as short as possible and package break-out must occur within 0.25 inches of the package.

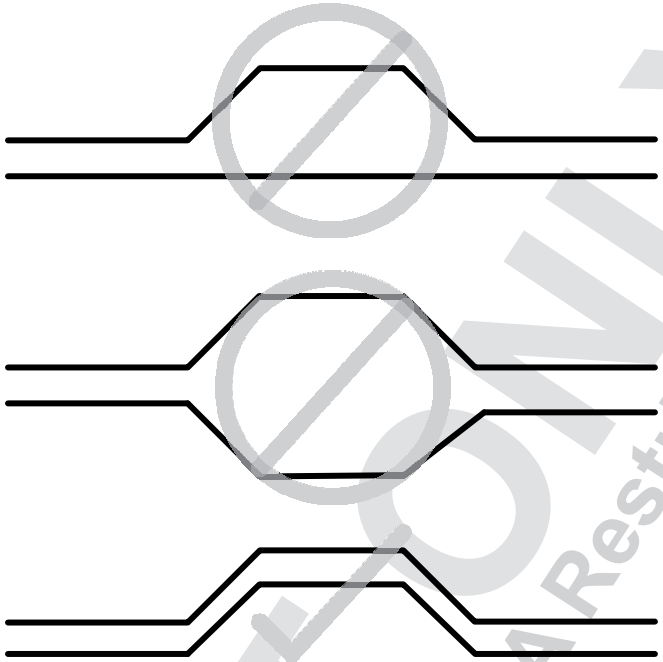


Figure 9. Differential Pair Symmetry

1.9 Connectors and Receptacles

When implementing a through-hole receptacle (like a USB Standard-A), TI recommends making high-speed differential signal connections to the receptacle on the bottom layer of the PCB. Making these connections on the bottom layer of the PCB prevents the through-hole pin from acting as a stub in the transmission path. For surface-mount receptacles such as USB Micro-B and Micro-AB, make high-speed differential signal connections on the top layer. Making these connections on the top layer eliminates the need for vias in the transmission path. For examples of USB through-hole receptacle connections, see Figure 10.

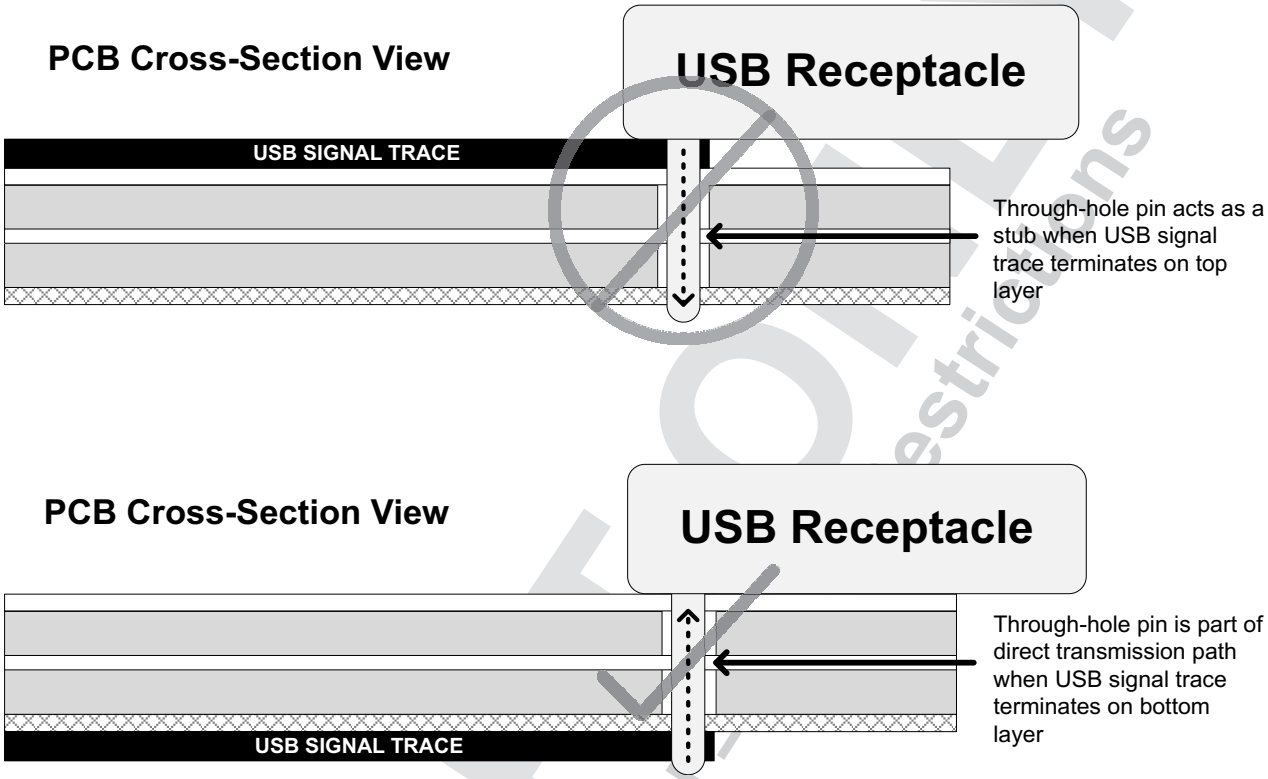


Figure 10. USB Through-Hole Receptacle Connection

1.10 Via Discontinuity Mitigation

A via presents a short section of change in geometry to a trace and can appear as a capacitive and/or an inductive discontinuity. These discontinuities result in reflections and some degradation of a signal as it travels through the via. Reduce the overall via stub length to minimize the negative impacts of vias (and associated via stubs).

Because longer via stubs resonate at lower frequencies and increase insertion loss, keep these stubs as short as possible. In most cases, the stub portion of the via present significantly more signal degradation than the signal portion of the via. TI recommends keeping via stubs to less than 15 mils. Longer stubs must be back-drilled.

For examples of short and long via lengths, see Figure 11 and Figure 12.

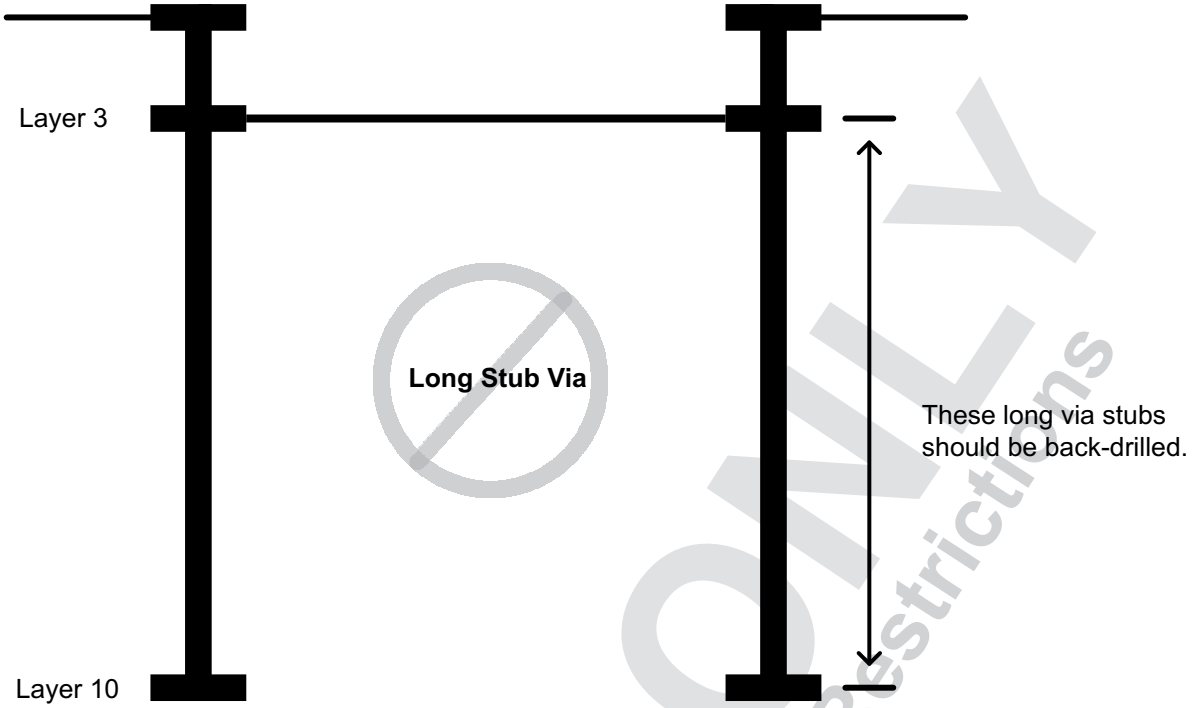


Figure 11. Via Length (Long Stub)

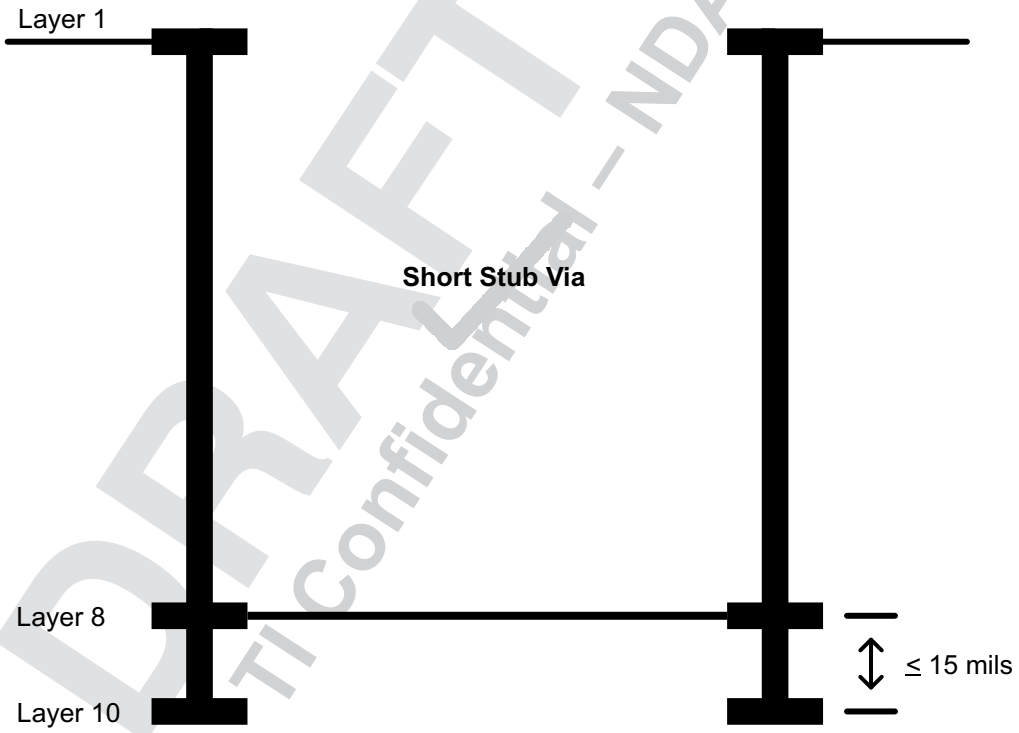


Figure 12. Via Length (Short Stub)

1.11 Back-Drill Via Stubs

Back-drilling is a PCB manufacturing process in which the undesired conductive plating in the stub section of a via is removed. To back-drill, use a drill bit slightly larger in diameter than the drill bit used to create the original via hole. This requires the via's antipad diameter to be increase to fit the drill size (for those layers that are to be removed), to ensure other trace/planes are not affected with via is drilled. When via transitions result in stubs longer than 15 mils, back-drill the resulting stubs to reduce insertion losses and to ensure that they do not resonate.

1.12 Via Anti-Pad Diameter

Via transitions can be significant sources of impedance variation along the trace. The via's anti-pad size across different layers would also need to be adjusted to ensure that the impedance is maintained at a uniform value. Too large an anti-pad would lead to an inductive effect and a corresponding increase in the trace impedance, while too small an anti-pad would similarly result in a capacitive effect and a dip in the overall trace impedance. The copper clearance, indicated by this anti-pad, must be met on all layers where the via exists, including both routing layer and plane layers. The traces connecting to the via barrel contain the only copper allowed in this area; non-functional or unconnected via pads are not permitted. For an example of a via anti-pad diameter, see Figure 13.

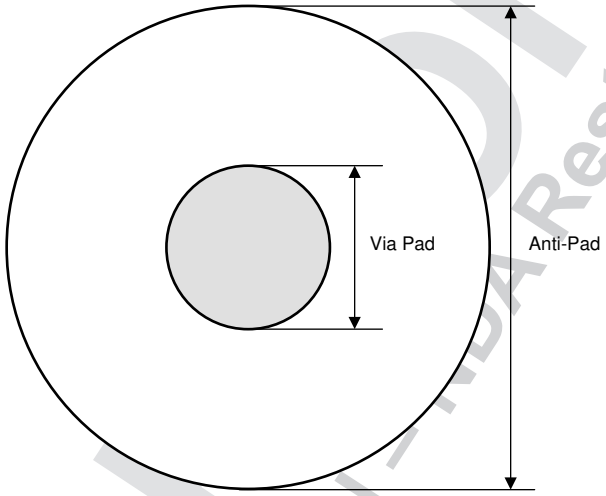


Figure 13. Example of Via Anti-Pad

1.13 Equalize Via Count

If using vias is necessary on a high-speed differential signal trace, ensure that the via count on each member of the differential pair is equal and that the vias are as equally spaced as possible. It is important to make sure that the different lanes that lengths need to match have the same amount of vias on the lines. Also designers should take into account the length of the vias when verifying parameters such as inter pair skew.

1.14 Surface-Mount Device Pad Discontinuity Mitigation

Avoid including surface-mount devices (SMDs) on high-speed signal traces because these devices introduce discontinuities that can negatively affect signal quality. When SMDs are required on the signal traces (for example, the USB SuperSpeed transmit AC coupling capacitors) the maximum permitted component size is 0603. TI strongly recommends using 0402 or smaller. Place these components symmetrically during the layout process to ensure optimum signal quality and to minimize reflection. For examples of correct and incorrect AC coupling capacitor placement, see Figure 14.

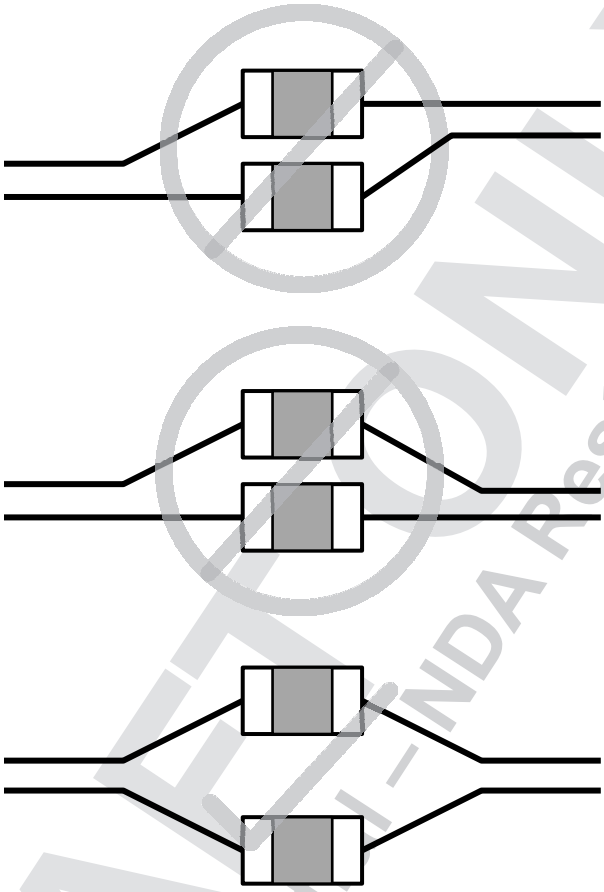


Figure 14. AC-Coupling Placement

To minimize the discontinuities associated with the placement of these components on the differential signal traces, TI recommends voiding the SMD mounting pads of the reference plane by 100%. This void should be at least two PCB layers deep. For an example of a reference plane voiding of surface mount devices, see Figure 15.

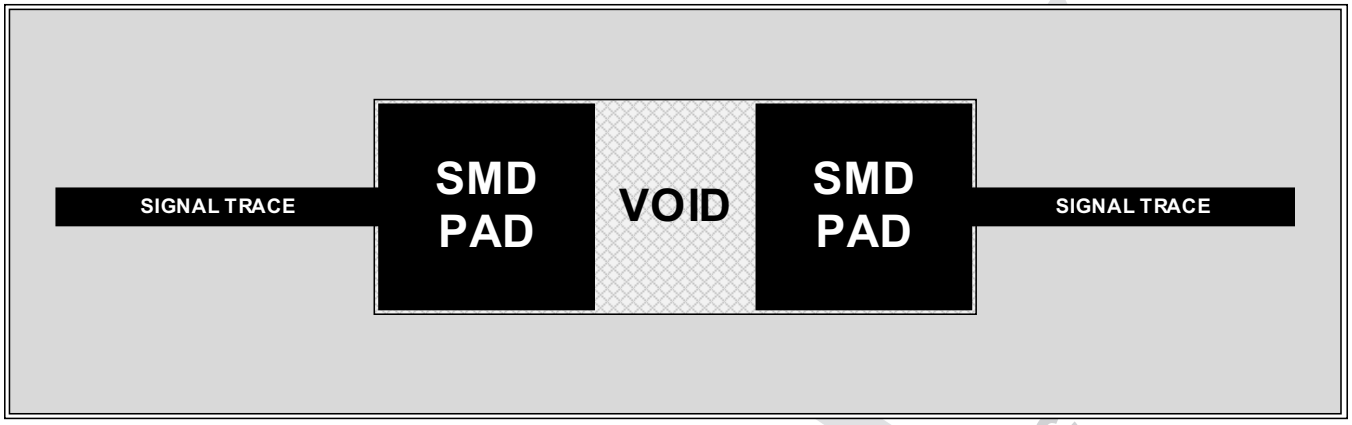


Figure 15. Reference Plane Voiding of Surface-Mount Devices

1.15 Signal Bending

Avoid the introduction of bends into high-speed differential signals. When bending is required, maintain a bend angle greater than 135° to ensure that the bend is as loose as a possible. For an example of high-speed signal bending rules, see Figure 16.

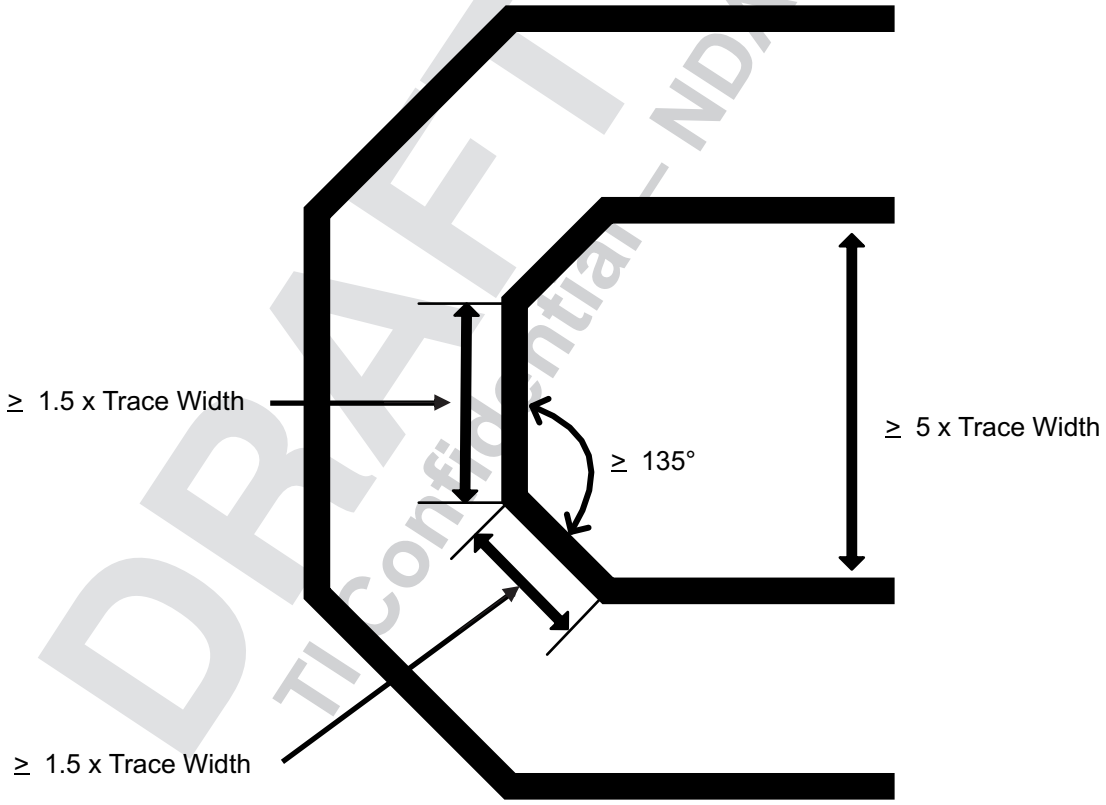


Figure 16. Signal Bending Rules

1.16 ESD/EMI Considerations

When choosing ESD/EMI components, TI recommends selecting devices that permit flow-through routing of the USB differential signal pair because they provide the cleanest routing. For example, the TI TPD4EUSB30 can be combined with the TI TPD2EUSB30 to provide flow-through ESD protection for both USB2 and USB3 differential signals without the need for bends in the signal pairs. For an example of flow-through routing, see Figure 17.

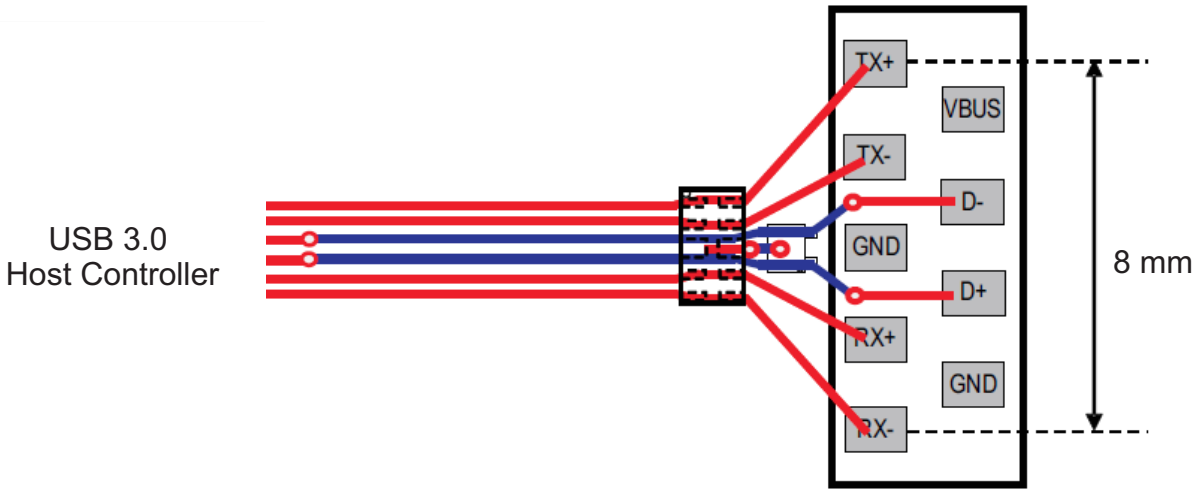


Figure 17. Flow-Through Routing

1.17 ESD/EMI Layout Rules

- Place ESD and EMI protection devices as close as possible to the connector.
- Keep any unprotected traces away from protected traces to minimize EMI coupling.
- Incorporate 60% voids under the ESD/EMI component signal pads to reduce losses.
- Use 0402 0-Ω resistors for common-mode filter (CMF) no-stuff options because larger components will typically introduce more loss that the CMF itself.
- Place any required signal pair AC coupling capacitors on the protected side of the CMF and as close as possible to the CMF.
- If vias are needed to transition to the CMF layer, ensure that the vias are as close as possible to the CMF.
- Keep the overall routing of AC coupling capacitors + CMF + ESD protection as short and as close as possible to the connector.

2 High Speed Board Design and Layout Guidance

There are many differences in the various High speed standards that need to be taken into account when designing the layout of a system. These differences include parameters like data-rates/frequency, AC coupling capacitors, inter-pair skew, intra-pair skew and trace impedance. This chapter includes different sections for each of the different high speed standards. Note these sections are to be used as guidelines are not always exact values.

2.1 USB Board Design and Layout Guidelines

This section discusses guidelines when designing a universal serial bus (USB) system. USB interfaces are commonly used for both on-board and off-board communication, thus designs will vary. This guide is not intended to cover all design possibilities, but to provide general recommendations. The design rules stated within this document are targeted at DEVICE mode electrical compliance. HOST mode and/or systems that do not include the 3m USB cable and far-end 11-inch PCB trace required by DEVICE mode compliance testing may not need the complete list of optimizations shown in this document; however, applying these optimizations to HOST mode systems will lead to optimal DEVICE mode performance.

The use of USB compatible bridges and switches is allowed for interfacing with more than one other processor or USB device.

2.1.1 USB Interface Schematic

The USB interface schematics vary, but general connectivity is straightforward and consistent between implementations. Figure 18 illustrates a USB interface supporting super speed. Note the Device's USB interface might include addition signals such as usb_id, usb_vbus, and usb_drvvbus that are not discussed here. These signals are slow speed interfaces, and nothing special is required for PCB layout of these signals.

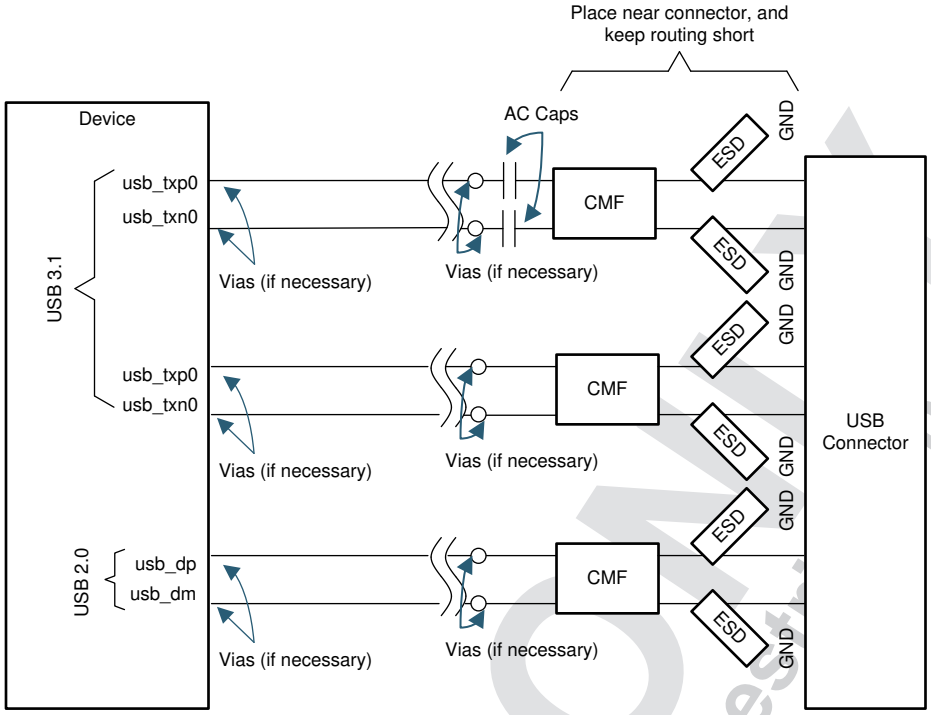


Figure 18. USB Interface High Level Schematic

2.1.1.1 Support Components

AC coupling capacitors are required on the transmit Super Speed data pairs. Table 1 shows the requirements for these capacitors.

Table 1. USB AC Coupling Capacitors Requirements

Parameter	MIN	TYP	MAX	Unit
PCIe AC coupling capacitor value	175	220	265	nF
PCIe AC coupling capacitor package size		0402	0603	EIA (1), (2)

(1) EIA LxW units, for example, a 0402 is a 40×20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

A typical USB interface may also common mode chokes for suppression of high frequency noise. Because USB can interface to off-board peripherals, ESD protection is also included in the example.

Table 2. USB Component Reference

Device	Supplier	Part Number	Comment
ESD	TI	TDP1E05U06	Minimize Capacitance
CMF	Murata	DLW21SZ900HQ2	Support Target Data Rates

Figure 19 shows the placement diagram for USB 3.1 Super Speed signals.

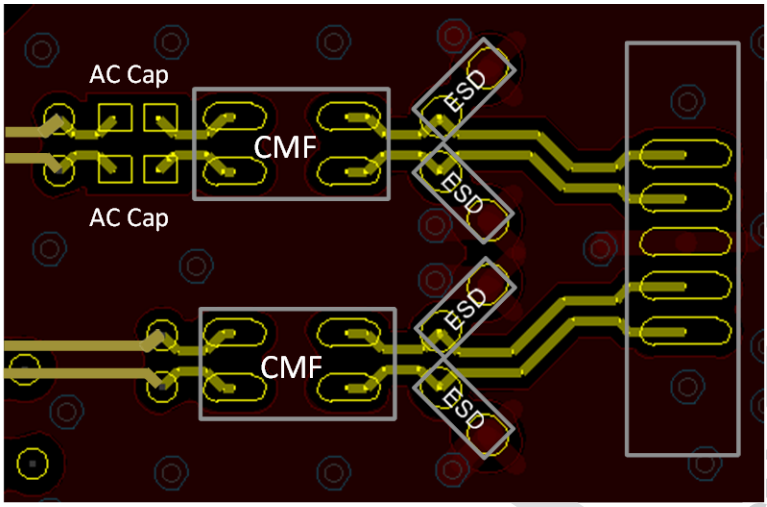


Figure 19. USB 3.1 Super Speed Placement Diagram

2.1.2 Routing Specifications

These parameters are recommendations only, intended to get the design close to success prior to simulation. To ensure the PCB design meets all requirements, it is required the design be simulated and those results compared with the simulation results defined in Section 3.

Table 3. USB3.1 (Super Speed) Routing Specifications

Parameter	MIN	TYP	MAX	Unit
USB3.1 Gen1 Operating Speed (Super Speed signals)			2.5 (1)	GHz
USB3.1 Signal Trace Length			5000 (2)	Mils
USB3.1 Differential Pair Skew			1	ps
USB3.1 Differential Impedance	85.5	90	94.5	Ω
Number of stubs allowed on USB3.1 traces			0	stubs
Number of vias on each USB3.1 trace			2	Vias
Via Stub Length (3)		20		Mils
USB3.1 Differential Pair to any other Trace Spacing (4)	2×DS	3×DS		

(1) For supported data rates, see the device-specific data manual.

(2) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis confirms the desired operation.

(3) Via stub control may be required when operating at higher data rates.

(4) DS = differential spacing of the traces. Exceptions may be necessary in the SoC package BGA area.

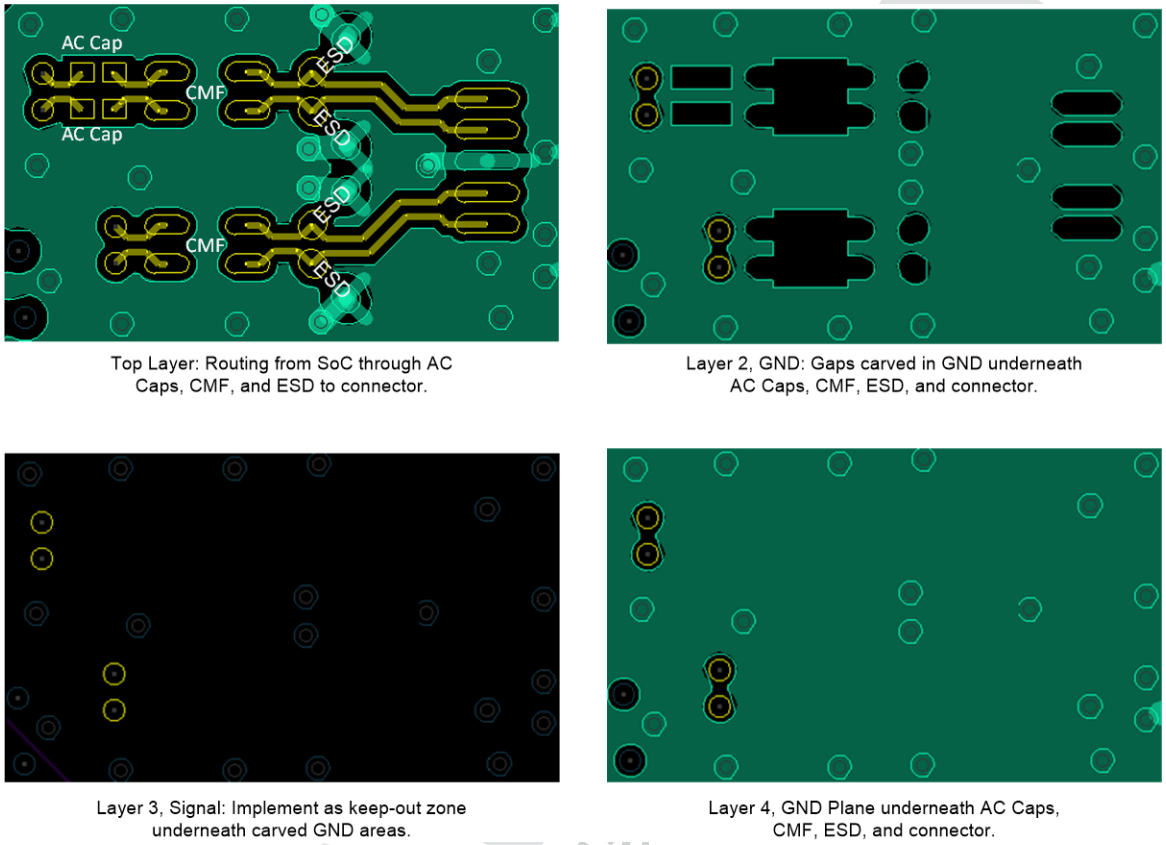
Table 4. USB2.0 Routing Specifications

Parameter	MIN	TYP	MAX	Unit
USB2.0 Operating Speed			240	MHz
USB2.0 Signal Trace Length			7000 (1)	Mils
USB2.0 Differential Pair Skew			5	ps
USB2.0 Differential Impedance	81	90	99	Ω
Number of stubs allowed on USB2.0 traces			0	stubs
Number of vias on each USB2.0 trace			4	Vias
USB2.0 Differential Pair to any other Trace Spacing (2)	2×DS	3×DS		

(1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis confirms the desired operation.

(2) DS = differential spacing of the traces. Exceptions may be necessary in the SoC package BGA area.

Component pads create impedance discontinuities due to the increased widths of the pads. In an effort to minimize impedance discontinuities, voids are created in the reference plane beneath the component pads. Figure 20 presents an example layout, demonstrating the “carve GND” concept. Before and affect effects of the reference plane voids can be seen in TDR plots and simulation results.



Top Layer: Routing from SoC through AC Caps, CMF, and ESD to connector.

Layer 2, GND: Gaps carved in GND underneath AC Caps, CMF, ESD, and connector.

Layer 3, Signal: Implement as keep-out zone underneath carved GND areas.

Layer 4, GND Plane underneath AC Caps, CMF, ESD, and connector.

Figure 20. USB 3.1 Example “carve GND” Layout

2.2 DisplayPort Board Design and Layout Guidelines

The DisplayPort (DP) interfaces on the device are compliant with the DP 1.3 specification. The DP signals are high speed differential pairs, and care must be taken in the PCB layout of these signals to ensure good signal integrity.

2.2.1 DP Interface Schematic

The DP interface schematics vary, depending on the target peripheral implemented. General connectivity is straightforward and consistent between implementations. Figure 21 shows a typical DP interface schematic.

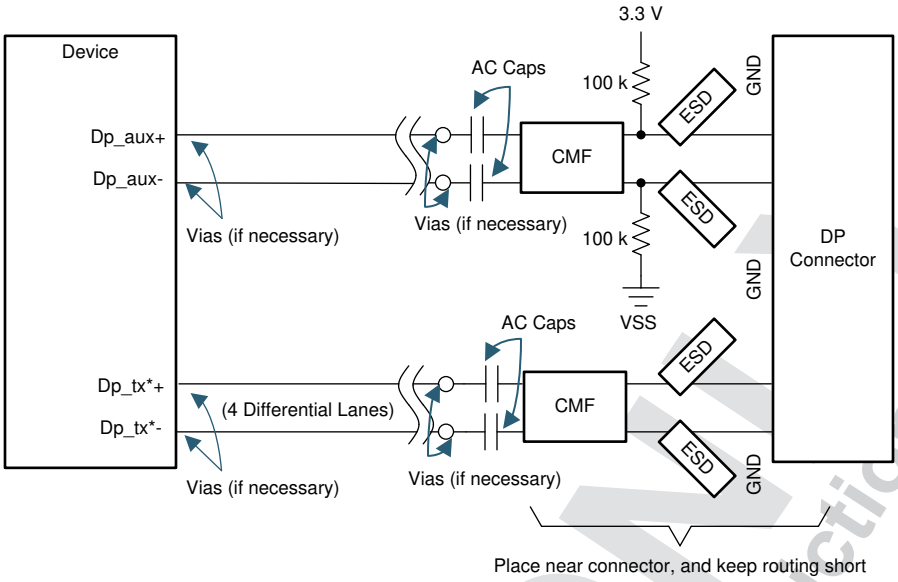


Figure 21. DisplayPort Interface High Level Schematic

2.2.1.1 Support Components

AC coupling capacitors are required on all the DP data pairs. Table 5 shows the requirements for these capacitors.

Table 5. DP AC Coupling Capacitors Requirements

Parameter	MIN	TYP	MAX	Unit
PCIe AC coupling capacitor value	175	220	265	nF
PCIe AC coupling capacitor package size		0402	0603	EIA (1), (2)

(1) EIA LxW units, for example, a 0402 is a 40×20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

A typical DP interface may also common mode chokes for suppression of high frequency noise. Because DP can interface to external monitors, ESD protection is also included in the example.

Table 6. DP Component Reference

Device	Supplier	Part Number	Comment
ESD	TI	TDP1E05U06	Minimize Capacitance
CMF	Murata	DLW21SZ900HQ2	Support Target Data Rates

Figure 22 presents placement diagram for DisplayPort interface.

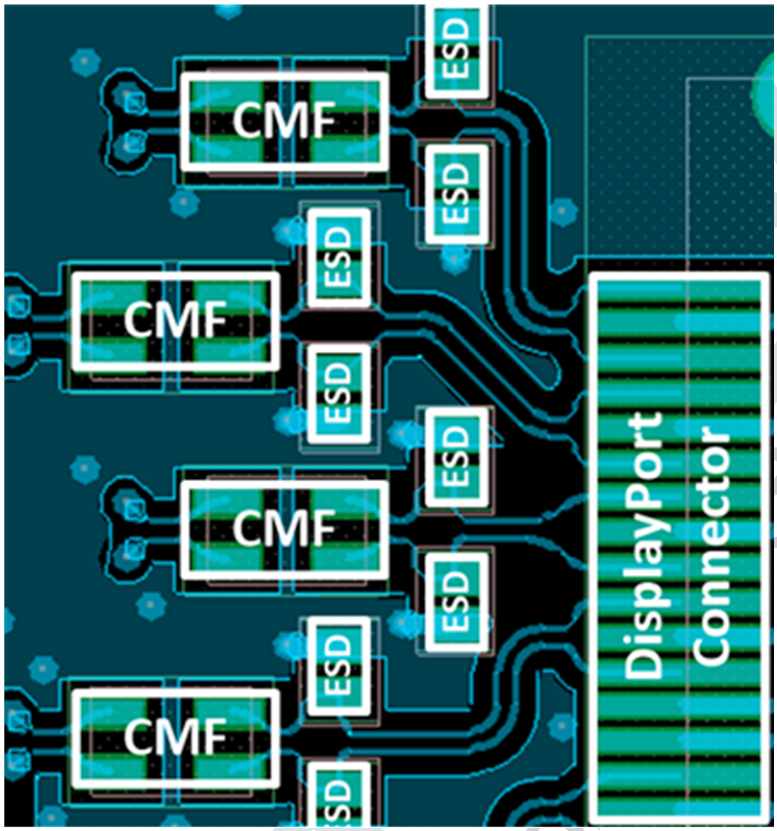


Figure 22. DisplayPort Placement

2.2.2 Routing Specifications

These parameters are recommendations only, intended to get the design close to success prior to simulation. To ensure the PCB design meets all requirements, it is required the design be simulated and those results compared with the simulation results defined in Section 3.

Table 7. DP Routing Specifications

Parameter	MIN	TYP	MAX	Unit
DP Operating Speed			4.05 (1)	GHz
DP Signal Trace Length			4000 (2)	Mils
DP Differential Pair Skew			1	ps
DP Lane Skew (example DP_TX0 to DP_TX1)			1250	ps
DP Differential Impedance	90	100	110	Ω
Number of stubs allowed on DP traces			0	stubs
Number of vias on each DP trace			2	Vias
Via Stub Length (3)		20		Mils
PCIe Differential Pair to any other Trace Spacing	2×DS (4)			

(1) For supported data rates, see the device-specific data manual.

(2) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis confirms the desired operation.

(3) Via stub control may be required when operating at higher data rates.

(4) DS = differential spacing of the traces, Exceptions may be necessary in the SoC package BGA area.

Component pads create impedance discontinuities due to the increased widths of the pads. In an effort to minimize impedance discontinuities, voids are created in the reference plane beneath the component pads. Figure 23 presents an example layout, demonstrating the “carve GND” concept. Before and affect effects of the reference plane voids can be seen in TDR plots and simulation results.

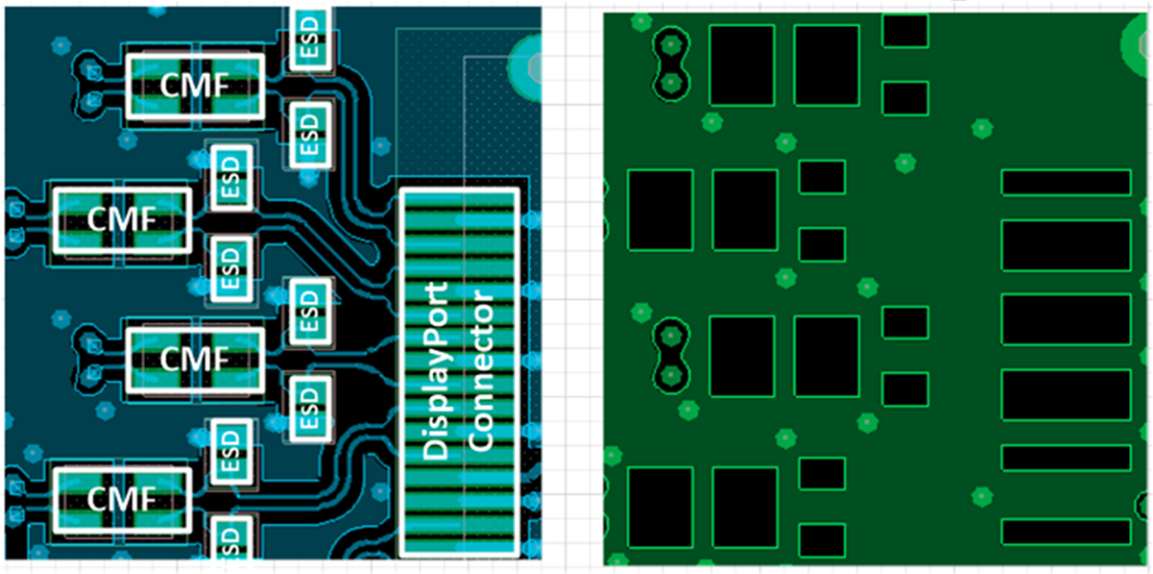


Figure 23. Example “carve GND” Layout

2.3 PCIe Board Design and Layout Guidelines

The PCIe interface on the device is compliant with the PCIe revision 3.0 specification. Please refer to the PCIe specifications for all connections that are described in it. Those recommendations are more descriptive and exhaustive than what is possible here. The PCIe Motherboard Checklist 1.0 document is also available from PCI-SIG (www.pcisig.com).

The following sections contain suggestions for any PCIe connection that is NOT described in the official PCIe specification, such as an on-board Device-to-Device or Device-to-other PCIe compliant processor connection.

The use of PCIe compatible bridges and switches is allowed for interfacing with more than one other processor or PCIe device.

2.3.1 PCIe Interface Schematic

The PCIe interface schematics vary, depending on the number of lanes implemented and where the reference clock is generated internally or externally. General connectivity is straightforward and consistent between implementations. Figure 24 illustrates a single lane, common RefClk Rx clock architecture with device generating the RefClk (output mode).

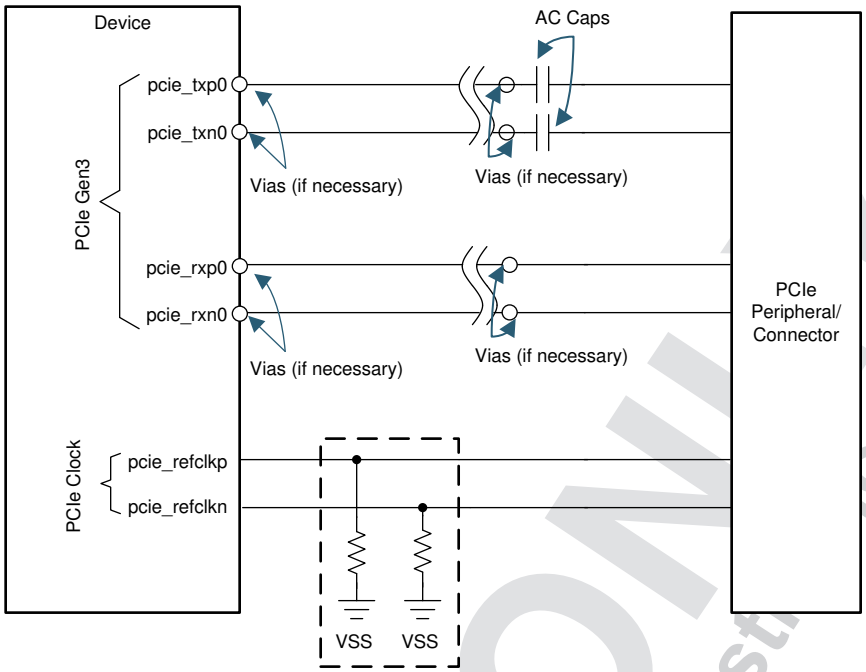


Figure 24. PCIe Interface High Level Schematic

NOTE: AC coupling capacitors are not shown on the receive data pairs as they are typically located on the transmit end of the PCIe differential pair.

2.3.1.1 Polarity Inversion

The PCIe specification requires polarity inversion support. This means for layout purposes, polarity is unimportant because each signal can change its polarity on die inside the chip. This means polarity within a lane is unimportant for layout.

2.3.1.2 Lane Swap

The PCI interface supports lane swapping, meaning Lane 0 of one device can be connected to Lane 1 of second device. (Note this requires both TX and RX signal to remain assigned to same lane). This means for layout purposes, lane assignment is unimportant because each lane can change its assignment on die inside the chip. This means lane assignment is unimportant for layout.

2.3.1.3 REFCLK Connections

Common Refclk Rx Architecture is required to be used for the device PCIe interface. Specifically, two modes of Common Refclk Rx Architecture are supported:

- External REFCLK Mode: An common external 100 MHz clock source is distributed to both the Device and the link partner
- Output REFCLK Mode: A 100 MHz HCSL clock source is output by the device and used by the link partner

In External REFCLK Mode, a high-quality, low-jitter, differential HCSL 100 MHz clock source compliant to the PCIe REFCLK AC Specifications should be provided on the Device's refclkp / refclkn inputs. Alternatively, an LVDS clock source can be used with the following additional requirements:

- External AC coupling capacitors described in Table 8 should be populated at the refclkp / refclkn inputs.

- All termination requirements (parallel 100 Ω termination) from the clock source manufacturer should be followed.

In Output REFCLK Mode, the 100 MHz clock from the Device can be output on the Device's refclkp / refclkn pins and used as the HCSL REFCLK by the link partner. External near- side termination to ground described in Table 8 is required on both of the refclk outputs in this mode.

Table 8. REFCLKP/N Requirements in External LVDS REFCLK Mode

Parameter	MIN	TYP	MAX	Unit
refclkp / refclkn AC coupling capacitor value		100		nF
refclkp / refclkn AC coupling capacitor package size		0402	0603	EIA (1), (2)

(1) EIA LxW units, for example, a 0402 is a 40×20 mils surface mount capacitor.
(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

Table 9. REFCLKP/N Requirements in Output REFCLK Mode

Parameter	MIN	TYP	MAX	Unit
refclkp / refclkn near-side termination to ground value	47.5	50	52.5	Ω

2.3.1.4 Coupling Capacitors

AC coupling capacitors are required on the transmit data pair. Table 10 shows the requirements for these capacitors.

Table 10. PCIe AC Coupling Capacitors Requirements

Parameter	MIN	TYP	MAX	Unit
refclkp / refclkn AC coupling capacitor value		100		nF
refclkp / refclkn AC coupling capacitor package size		0402	0603	EIA (1), (2)

(1) EIA LxW units, for example, a 0402 is a 40×20 mils surface mount capacitor.
(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

2.3.2 Routing Specifications

These parameters are recommendations only, intended to get the design close to success prior to simulation. To ensure the PCB design meets all requirements, it is required the design be simulated and those results compared with the simulation results defined in Section 3.

Table 11. PCI-E Routing Specifications

Parameter	MIN	TYP	MAX	Unit
PCIe Operating Speed			4 (1)	GHz
PCIe Signal Trace Length			5000 (2)	Mils
PCIe Differential Pair Skew			1	ps
PCIe Lane Skew (example PCIe_TX0 to PCIe_TX1)	No matching needed (de-skew built into receiver)			
PCIe Differential Impedance	72.5	85	97.5	Ω
PCIe Single-ended Impedance	38	45	52	Ω
PCIe RefClk Differential Impedance	85	100	115	Ω
Number of stubs allowed on PCIe traces			0	stubs
Number of vias on each PCIe trace			2	Vias
Via Stub Length (3)		20		Mils

Table 11. PCI-E Routing Specifications (continued)

Parameter	MIN	TYP	MAX	Unit
PCIe Differential Pair to any other Trace Spacing	2×DS (4)			

(1) For supported data rates, see the device-specific data manual.

(2) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis confirms the desired operation.

(3) Via stub control may be required when operating at higher data rates.

(4) DS = differential spacing of the traces, Exceptions may be necessary in the SoC package BGA area.

2.4 MIPI D-PHY (CSI2, DSI) Board Design and Layout Guidelines

The CSI2 and DSI interfaces on the device are compliant with the MIPI CSI/DSI 1.3 specification. For all connections that are described in it (specifically the Interconnect and Lane Configuration and Annex B Interconnect Design Guidelines chapters, see the MIPI specifications.

DSI is data transmit interface, typically used to interface with a display panel. CSI2 is a data received interface, typically used to interface with a remote camera. From implementation perspective, the interfaces are very similar and thus are lumped together in this section.

2.4.1 CSI2/DSI Interface Schematic

The CSI2 interface schematics vary, depending on the number of lanes implemented. Depending upon device, each CSI2 interface can include up to four data lanes. General connectivity is straightforward and consistent between implementations. Figure 25 illustrates a CSI2 system using a single lane.

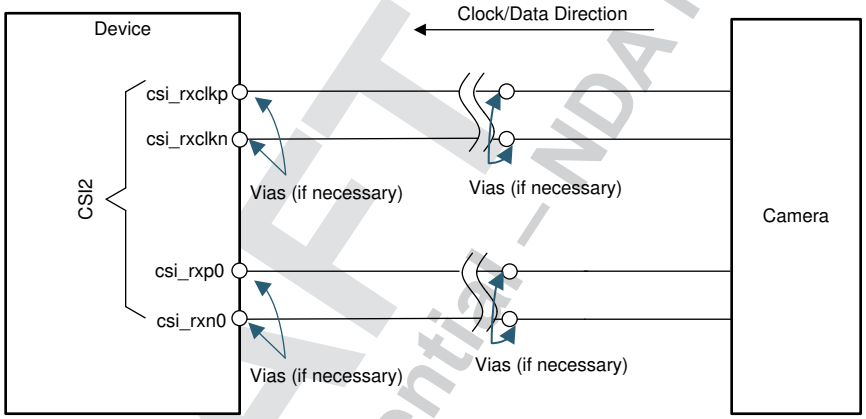


Figure 25. Missing Title - CSI2 Interface High Level Schematic

The DSI interface schematics vary, depending on the number of lanes implemented. Depending upon device, each DSI interface can include up to four data lanes. General connectivity is straightforward and consistent between implementations. Figure 26 illustrates a DSI system using a single lane.

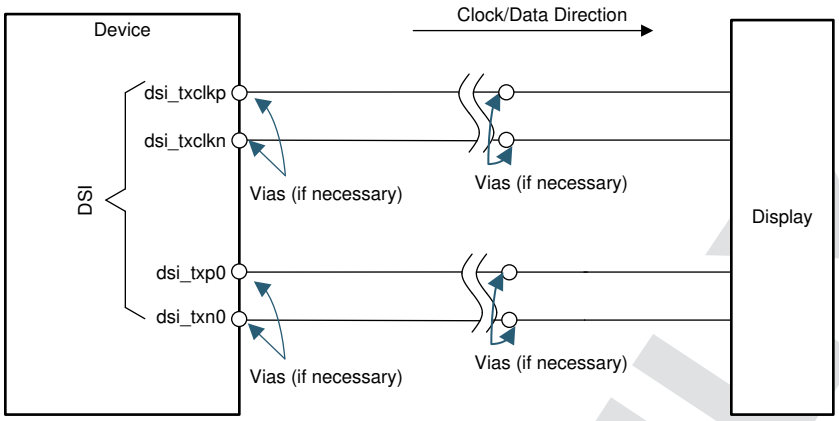


Figure 26. DSI Interface High Level Schematic

2.4.2 Routing Specifications

These parameters are recommendations only, intended to get the design close to success prior to simulation. To ensure the PCB design meets all requirements, it is required the design be simulated and those results compared with the simulation results defined in Section 3.

Table 12. PCI-E Routing Specifications

Parameter	MIN	TYP	MAX	Unit
CSI2/DSI Operating Speed			1.25 (1)	GHz
CSI2/DSI Signal Trace Length			10 (2)	Inches
CSI2/DSI Differential Pair Skew	Have to satisfy mode-conversion S parameters (3)			
CSI2/DSI Lane Skew				
(example DSI_TX0 to DSI_TX1)			40 (4)	ps
CSI2/DSI Differential Impedance (5)	85	100	115	Ω
CSI2/DSI Single-ended Impedance		50		Ω
Number of stubs allowed on CSI2/DSI traces			0	stubs
Number of vias on each CSI2/DSI trace			2	Vias
CSI2/DSI Differential Pair to any other Trace Spacing	2×DS (6)			

(1) For supported data rates, see the device-specific data manual.

(2) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis confirms the desired operation.

(3) Defined in MIPI D-PHY spec, includes sdc12, scd21, scd12, sdc21, scd11, sdc11, scd22, and sdc22. General estimate is UI/50 (where UI = 400 ps for 1.25 GHz).

(4) Defined by MIPI spec as 0.1 x UI (where UI = 400 ps for 1.25 GHz).

(5) Because the MIPI signals are used for low-power, single-ended signaling in addition to their high-speed differential implementation, the pairs must be loosely coupled.

(6) DS = differential spacing of the traces, Exceptions may be necessary in the SoC package BGA area.

2.4.3 Frequency-Domain Specification Guidelines

After the PCB design is implemented, the S-parameters of the PCB differential lines will be extracted with a 3D Maxwell Equation Solver such as the high-frequency structure simulator (HFSS) or equivalent, and compared to the frequency-domain specification as defined in *Section 7* of the *MIPI Alliance Specification for D-PHY Version v1-01-00_r0-03*. If the PCB satisfies the frequency-domain specification, the design is finished. Otherwise, the design needs to be improved.

2.5 UFS Board Design and Layout Guidelines

This section discusses guidelines when designing a universal flash storage (UFS) system. The UFS interfaces on the device are compliant with the UFS 2.1 specification. UFS interfaces are commonly used for either embedded or removable memory storage access.

2.5.1 UFS Interface Schematic

The UFS interface schematics vary, depending on the number of lanes implemented, as depending if the memory is embedded or removable. Depending upon device, each UFS interface can include up to two data lanes (each direction). General connectivity is straightforward and consistent between implementations. Figure 27 illustrates a UFS system using a single lane. The TX and RX signals are implemented as differential pairs. The REF_CLK and RSTN signals are single ended signals. These single ended are slow speed interfaces, and nothing special is required for PCB layout of these signals.

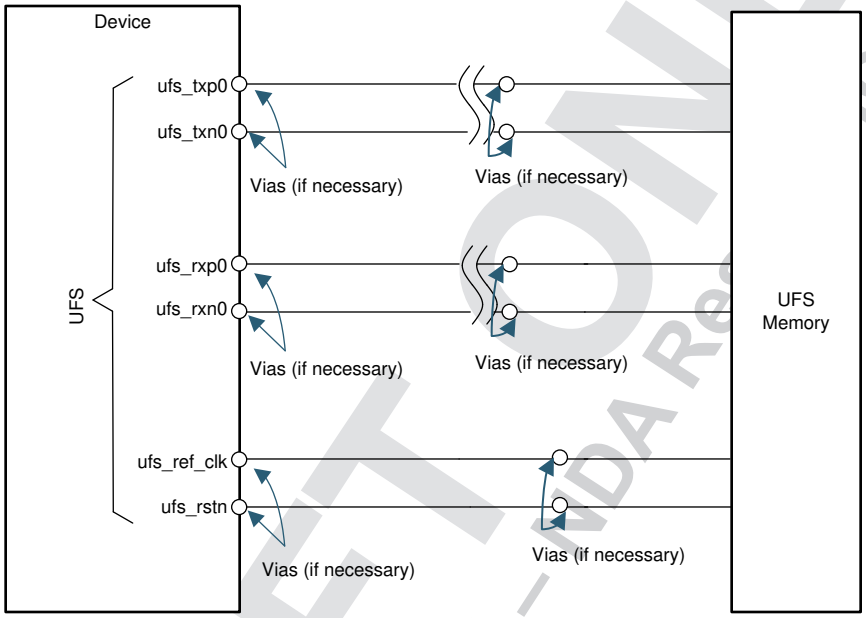


Figure 27. UFS Interface High Level Schematic

2.5.2 Routing Specifications

These parameters are recommendations only, intended to get the design close to success prior to simulation. To ensure the PCB design meets all requirements, it is required the design be simulated and those results compared with the simulation results defined in Section 3.

Table 13. UFS Routing Specifications

Parameter	MIN	TYP	MAX	Unit
UFS Operating Speed			2.9 (1)	GHz
UFS Signal Trace Length			4000 (2)	Mils
UFS Differential Pair Skew			2	ps
UFS Lane Skew (3) (example UFS_TX0 to UFS_TX1)			300	ps
UFS Differential Impedance	85	100	115	Ω
Number of stubs allowed on UFS traces			0	stubs
Number of vias on each UFS trace			2	Vias
Via Stub Length (4)		20		Mils
UFS Differential Pair to any other Trace Spacing	2×DS (5)			

(1) For supported data rates, see the device-specific data manual.
(2) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis confirms the desired operation.
(3) The single ended traces have no skew requirement relative to differential pairs or each other.
(4) Via stub control may be required when operating at higher data rates.
(5) DS = differential spacing of the traces, Exceptions may be necessary in the SoC package BGA area.

2.6 Q/SGMII Board Design and Layout Guidelines

This section discusses guidelines when designing a system that includes serial Gigabit Ethernet. Serial Gigabit Media Independent Interface (SGMII) interfaces on the device are commonly used for communication with Ethernet PHY devices. Quad-Ethernet (QSGMII) is the combination of four Ethernet PHYs onto a single serial stream.

2.6.1 Q/SGMII Interface Schematic

The Q/SGMII interface connectivity is straightforward and consistent between implementations. Figure 28 illustrates a Q/SGMII system. Ethernet PHY designs include other signals like MDIO that are not included in this guideline. These single ended are slow speed interfaces, and nothing special is required for PCB layout of these signals.

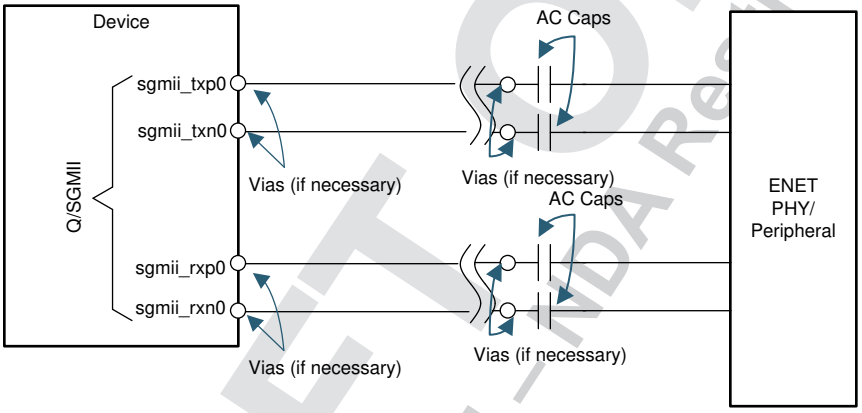


Figure 28. SGMII Interface High Level Schematic

2.6.1.1 Coupling Capacitors

AC coupling capacitors are required on the transmit and receive data pair. Table 14 shows the requirements for these capacitors.

Table 14. Q/SGMII AC Coupling Capacitors Requirements

Parameter	MIN	TYP	MAX	Unit
PCIe AC coupling capacitor value		100		nF
PCIe AC coupling capacitor package size		0402		EIA (1), (2)

(1) EIA LxW units, for example, a 0402 is a 40×20 mils surface mount capacitor.
(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

2.6.2 Routing Specifications

These parameters are recommendations only, intended to get the design close to success prior to simulation. To ensure the PCB design meets all requirements, it is required the design be simulated and those results compared with the simulation results defined in Section 3.

Table 15. G/SGMII Routing Specifications

Parameter	MIN	TYP	MAX	Unit
Q/SGMII Operating Speed			2.5 (1)	GHz
Q/SGMII Signal Trace Length			5000 (2)	Mils
Q/SGMII Differential Pair Skew			2	ps
Q/SGMII Differential Impedance	85	100	115	Ω
Number of stubs allowed on Q/SGMII traces			0	stubs
Number of vias on each Q/SGMII trace			2	Vias
Via Stub Length (3)		20		Mils
Q/SGMII Differential Pair to any other Trace Spacing	2×DS (4)			

(1) For supported data rates, see the the device-specific data manual.

(2) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis confirms the desired operation.

(3) Via stub control may be required when operating at higher data.

(4) DS = differential spacing of the UFS traces. Exceptions may be necessary in the SoC package BGA area.

3 Board Design Simulations

This section is intended to provide an overview of the basic system-level board extraction, simulation, and analysis methodologies for high-speed serial interfaces. This is an essential step to ensure the PCB design meets all the requirements to operate the targeted speeds.

3.1 Board Model Extraction

The board level extraction guidelines listed below are intended to work in any EDA extraction tool and are not tool-specific. It is important to follow the steps outlined in Section 3.2 through Section 3.4 immediately after completing touchstone model extractions. The design should be checked with these steps prior to running IBIS simulations.

- For high speed serial interface extractions, there is no need to extract power and signal nets together in a 3D-EM solver. Simulations are only intended for Signal Integrity.
- Use wide-band models. It is recommended to extract from DC to at least till 6x the Nyquist frequency (for USB3.1 Gen 1, extract the model at least till 15 GHz).
- Check the board stack-up for accurate layer thickness and material properties.
  - It is recommended to use Djordjevic-Sarkar models for the dielectric material definition.
- Use accurate etch profiles and surface roughness for the signal traces across all layers in the stack-up.
- If the board layout is cut prior to extraction (to reduce simulation time), please define a cut boundary that is at least 0.25 inch away from the signal and power nets.
- Check the via padstack definitions
  - Ensure that the non-functional internal layer pads on signal vias are modeled the same way they would be fabricated.
  - These non-functional internal layer pads on signal vias are not recommended by TI
- Use Spice/S-parameter models (typically available from the vendor) for modeling all passives in the system

3.2 Board-Model Validation

The extracted board models need to be checked for the following properties:

- Passivity: This ensures that the board model is a passive network and does not generate energy.
- Causality: This ensures that the board model obeys the causal relationship (output follows input).

These checks can be performed in any standard EDA simulator or extraction engine.

3.3 S-Parameter Inspection

Once the extracted S-parameters have been verified as causal and passive, the S-parameter plots should be inspected. It is recommended to check for the following:

- Insertion Loss: The single-ended insertion loss is recommended to stay within 0 to 10 dB up to 3 times the Nyquist frequency of operation. For example, if the target frequency is 8 Gbps (4 GHz Nyquist), the single-ended insertion loss should stay under 10 dB up to 12 GHz.
- Return Loss: The single-ended return loss is recommended to be less than 15 dB up to 3 times the Nyquist frequency.
- Near and Far end crosstalk (FEXT/NEXT): The FEXT and NEXT are recommended to be under 25 dB for frequencies up to 3 times the Nyquist frequency

3.4 Time Domain Reflectometry (TDR) Analysis

As a lot of the design fixes are targeted towards maintaining uniform trace impedance, an important analysis method used in assessing the quality of the design is the Time Domain Reflectometry (TDR) Analysis. This plots the impedance of a trace as a function of its length. An example of this is shown in Figure 29.

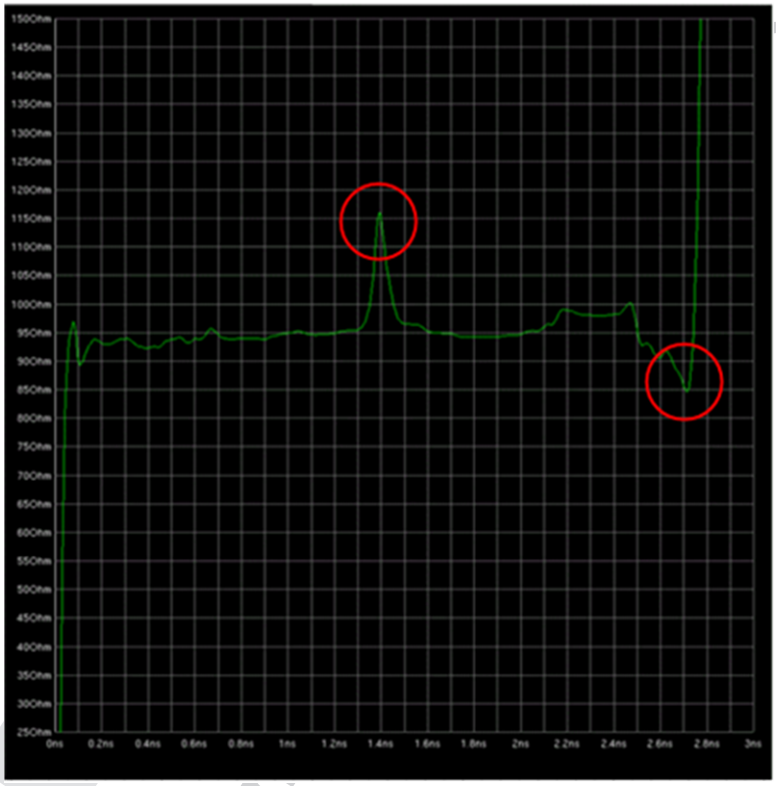


Figure 29. TDR Plot Example With Impedance Mismatch

As shown in Figure 29 (TDR plot example), the TDR plot highlights impedance discontinuities in the trace from one end to the other. This method depends on a reflected waveform from the far-end of the trace. The delay in the plot corresponding to a particular point in the trace actually corresponds to 2 times the distance of that point from the source, owing to the round trip time. This needs to be factored in for assessing the source of impedance discontinuities.

The TDR plot can be generated by reading in the S-parameter models generated by the extraction tool and assessing them in “Time-Domain” mode. A standard EDA simulator such as HyperLynx can perform this function. It is recommended to optimize the design to within a ± 5% deviation from the nominal trace impedance.

3.5 Simulation Integrity Analysis

The general methodology for evaluating signal integrity for high-speed SERDES interfaces is illustrated in Figure 30. This involves running a channel simulation for the serial link. The methodology uses IBIS-AMI (Algorithmic Modeling Interface) models for the Tx/Rx blocks. The basic setup and settings documented here can be used to validate all SerDes links and also across a variety of EDA Signal Integrity simulators. This channel simulation should be performed as a signoff check for all high-speed Serial Link interfaces.

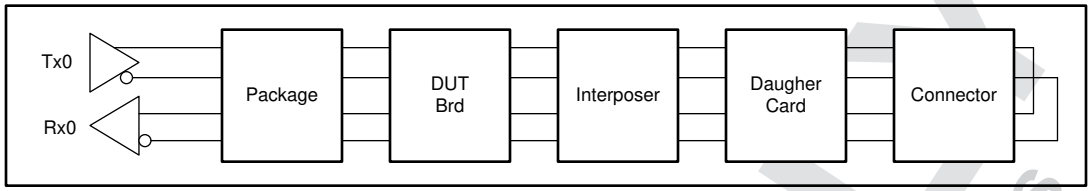


Figure 30. Signal Integrity Analysis Setup - Channel Simulation

3.5.1 Simulator Settings and Model Usage

The following things need to be kept in mind while performing channel simulation:

- Odd mode crosstalk is used to define aggressor and victim switching in opposite directions. This is required if multiple lanes are simulated.
- An important note to keep in mind is that the jitter and noise of Tx/Rx blocks should not be double counted. As the IBIS-AMI models already have the various jitter sources incorporated, the option to include additional jitter in these blocks must be turned off in the EDA simulation engine of choice.

3.5.2 Simulation Parameters

The serial link simulations involve a parametric sweep:

- Corners: The IBIS-AMI models for Tx/Rx are characterized as Fast/Typ/Slow corners. The different Deterministic and Random Jitter budgets are built in to the models using these corners.
- Transmitter Presets: These are specific to each standard and control the coefficients in the transmitter DFE (Decision Feedback Equalizer). These presets also model the level of de-emphasis in the transmit amplifier which are required to equalize the overall system-level response across different frequencies and counteract the impact of ISI (Inter-symbol interference). It is recommended using a parametric sweep and simulate for all different transmitter presets for a given Serial Link protocol. This is due to the fact that the best eye observed can be highly dependent on the system impulse response and therefore different presets could yield the best results on different systems.
- Data Patterns: It is recommended to use PRBS23 or PRBS31 patterns to validate the system, in order to excite larger levels of ISI.

3.5.3 Simulation Methodology

For interfaces where the eye mask is specified in terms of a BER target it is recommended to run the initial channel simulations for around 100K bits and observe the extrapolated bathtub curves for the corresponding target BER, as reported by the simulator. Another simulation for around 500K and 1M bits can be rerun and the bathtub curves can be overlaid to observe the impact of running for larger bit sequences. An example of voltage bathtub curves overlaid is shown in Figure 31. Similar overlay can be made for the jitter bathtub curves.

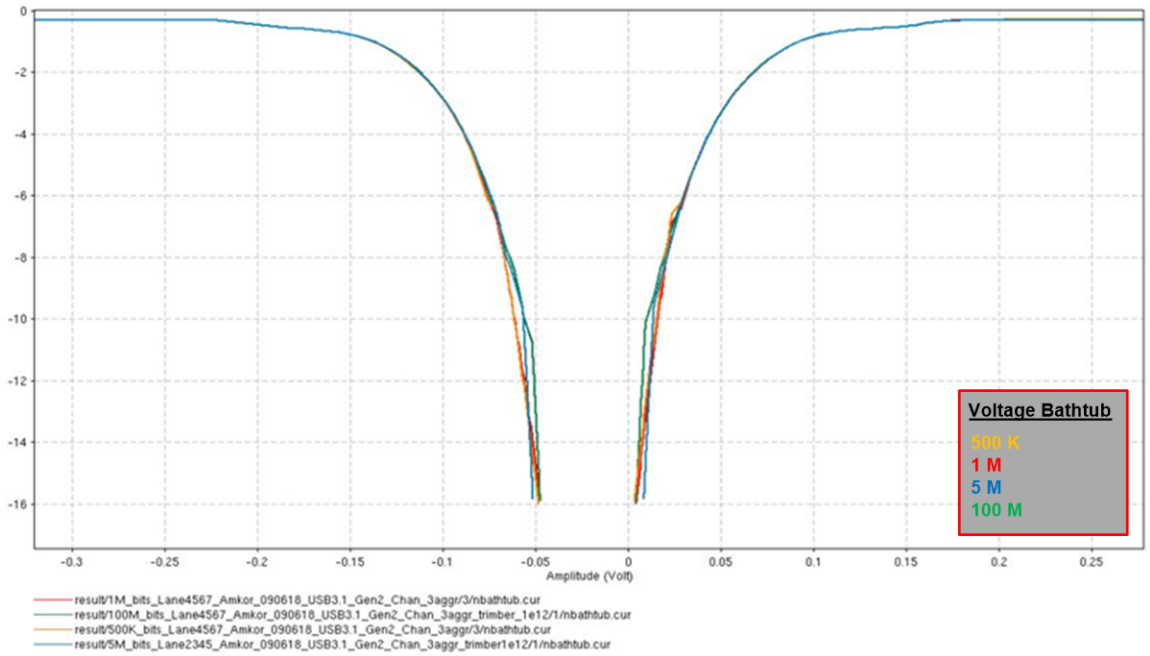


Figure 31. Bathtub Curve Overlay

Typically, all the ISI should be accounted for within the first 100K bits of the simulation and beyond this point, all bathtub curves should converge if the Random Jitter (Rj) in the models is sufficiently small. It is recommended to confirm this convergence up front by running at least one set of system-level channel simulations each for 100K, 500K and 1M bit sequences. If the voltage and jitter bathtub curves from each of these simulations are almost identical, the remainder of the simulations can be run at 100K bits to optimize run times.

For interfaces where the eye mask is not specified for any particular BER target, a 100K bit simulation should suffice.

3.6 Reviewing Simulation Results

The results generated by the channel simulations outlined in the preceding sections are compared against an eye mask spec. This eye mask is summarized in Table 16. This is used as a pass/fail check for the system. Note some protocol are supported on different buffer type. See device data manual pin attributes to determine the buffer type for each IO.

Table 16. Eye Mask Specifications for Different Standards

Protocol	Buffer Type	Eye Height (mV)	Eye Width (pS)	Notes
PCIe Gen3/4	SierraPhy	70	5	Post-equalization eye mask. BER Target 1E-12
USB3.1	SierraPhy	70	5	
DP/eDP	TorrentPhy	N/A	N/A	TP3_EQ eye mask (Section 4.6.1 of eDP_v1.4b_E1 specification) BER Target 1E-09
XFI	SierraPhy	70	5	Post-equalization eye mask. BER Target 1E-12
QSGMII	SierraPhy	70	5	
	TorrentPhy	50	25	
SGMII	SierraPhy	70	5	
	TorrentPhy	50	25	
CSI (Rx)/DSI (Tx)	D-Phy	300 mV/700 mV	N/A	300 mV at the equalizer input; 700 mV at the equalizer output
UFS	M-Phy	± 50 mV	0.7*UI	Remote/Local post-EQ

Table 16. Eye Mask Specifications for Different Standards (continued)

Protocol	Buffer Type	Eye Height (mV)	Eye Width (pS)	Notes
		± 45 mV	0.6*UI	Complete Loopback post-EQ

4 References

- Texas Instruments: *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs*
- Texas Instruments: *High-Speed Interface Layout Guidelines*

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