Jacinto7 J721E Power Solutions

DRA829, TDAVM

v2.4 **10/18/2022**

Agenda

- PDN Strategy
- J721E Power Solution Summary
  - New Universal PDN-3 Schemes
  - Legacy PDNs
- Reference Section

J7 SoC Power Solutions | Design

- Define end product's market, operational temp range & functional safety targets
- Determine SoC peak power demands for full entitlement operation
  - Power design uses PDN SoC power estimates to account for instantaneous peak processing & loads
  - Thermal design uses Thermal SoC power estimates to account for sustained average processing & loads
- Develop a modular PDN scheme per following priorities:
  - Support SoC full entitlement with base power resources
    - Define common orderable PNs whenever possible to enable reuse & minimize PNs
  - Support desired functional safety requirements to enable SoC PDN systems capable of end product ASIL targets.
  - Support SoC low power modes with either base resources or discrete resources (easily removed if not needed)
  - Support all optional end product features with low cost, discrete power resources (easily removed if not needed)
- Assign PMIC GPIO interfaces with required functionality per following priorities:
  - Base PDN operational controls & SoC power sequencing
  - Functional safety targets
  - Low power modes
  - Optional end product features

J7 SoC Power Solutions | Validate

- TI performs SoC VMIN margin validation using EVM recmd'd PDN schemes
- VMIN validation verifies production programmed AVS voltage settings to ensure
  - Robust & optimal processing performance while minimizing power & thermal concerns
  - Volume Production Testing is correlated to realistic EVM/end product board performance
- Customers leveraging recmd'd PDNs, reduce new product dev & 1st pass success
- SoC PDN design risk & development time increases:
  - If a different SoC power component or power resource mapping is used (other than validated PDN schemes),
  - Then regulation accuracy, transient load step & supply noise impacts processor performance
    - Processors can unexpectedly halt, become corrupted or show video &/or display artifacts, especially during high demand use cases.
  - Then functional safety systematic capability impacts end product ASIL performance targets
  - Then reduced VMIN margins protecting for manuf variations, temp ranges & product lifetime impacts product robustness.
  - PDN deviations complicate & extend VMIN margin validation testing recommended to be performed by customers on their end products while running high processing demand use cases to validate product system design robustness.

J7 SoC Power Solutions | Select

1. What is product's desired market? (Automotive, Industrial, opr temp ranges…)
2. What is product's desired Functional Safety (FuSa) requirement?

   If "FuSa" is needed, then:

   a) What is the desired "ASIL level"? (i.e. ASIL-D, ASIL-B, ...)

   b) Is MCU Safety Island processing desired?
      - Independent safety processor monitors overall system operation
      - Isolated MCU & Main PDN is needed to isolate MCU supplies from Main supplies
        - Increases power resources, rail count & PCB area
        - PDN with Freedom From Interference (FFI) is supported
        - MCU Only low power mode is supported

   c) Is Extended MCU Safety processing desired?
      - Increases safety processing resources by using both MCU & Main processors
      - Combined MCU & Main PDN is allowed to group common MCU & Main supplies
        - Reduces total power resources, rail count & PCB area
        - PDN with FFI not supported
        - MCU Only low power mode not supported

3. What is product's desired PDN feature set?

   a) Are any PDN low power modes (MCU Only, DDR Retention, GPIO Retention) desired?

   b) Are any optional features (UHS-1 SD card, USB2.0 I/F, HS Efuse prgm on-board) desired?

J7 SoC Power Solutions | Optimize

Feature Removals	Power Resource & Power Rail Removals	New Supply Mappings
HS SoC EFUSE Programming	Discrete LDO VPP_EFUSE_1V8	SoC: VPPs => No connects
Compliant, USB 2.0 data eye	Discrete LDO VDA_USB_3V3	SoC: VDDA_3P3_USB => filtered VDD_IO_3V3
Compliant, High-Speed SD Card	Discrete LDO VDD_SD_DV	SoC: VDDSHV5 => VDD_IO_3V3 or VDD_IO_1V8
DDR Retention low power mode	Discrete LDO VDD1_DDR_1V8	LPDDR4: VDD1 => VDD_IO_1V8
MCU GPIO Retention low power mode	Discrete LDO VDD_MCU_GPIORET_0V8 Discrete LDSW VDD_MCU_GPIORET_3V3 Discrete SVS	SoC: VDD_MCU_WAKE1 => VDD_MCU_0V85 SoC: VDDSHV0_MCU => VDD_MCUIO_3V3 or VDD_MCUIO_1V8 PMIC: GPIO_10 pulled-up to VCCA_3V3
Main GPIO Retention low power mode	Discrete LDO VDD_GPIORET_0V8 Discrete LDSW VDD_GPIORET_3V3 Discrete SVS	SoC: VDD_WAKE0 => VDD_CORE_0V8 SoC: VDDSHV2 => VDD_IO_3V3 or VDD_IO_1V8 PMIC: GPIO_10 pulled-up to VCCA_3V3

J7 SoC Power Solutions | Identify

PDN ID = <J7 SoC Generic PN> PDN-XY

- All PDNs are initially optimized for a specific “J7 SoC”
  - Generic PN: Orderable PN variants
    - J721E: DRA829, TDA4VM
- PDN – “XY” uses 2 alpha-numeric characters as follows:
  - “X” = Numeric value to signify “base power devices”
    - 0 = 2x TPS6594-Q1 (aka Dual Leo PMICs)
    - 1 = TPS6594-Q1 + LP8764-Q1 (aka Leo + Hera PMICs)
    - 2 = TPS6594-Q1 (aka Single Leo PMIC)
    - 3 = TPS6594-Q1 + HCPS (aka Single Leo + High Current Pwr Stage using discrete high-current bucks)
  - “Y” = Alphabetic character to signify “key resource mapping differences” (i.e. power resources, GPIO signaling)
    - A = 1st PDN designed for base power devices & typically demonstrating maximum PDN features
    - B – F = Variants of 1st PDN to show:
      - Resource mapping changes to improve margins
      - Reduce resources to minimize cost & area after removing PDN features
  - Examples: J721E PDN-0C, J7200 PDN-1A, J7200 PDN-2A, J721S2 PDN-0A, J721S2 PDN-3A, J784S4 PDN-3G

J721E (DRA829, TDA4VM)
UNIVERSAL PDN-3 SCHEMES

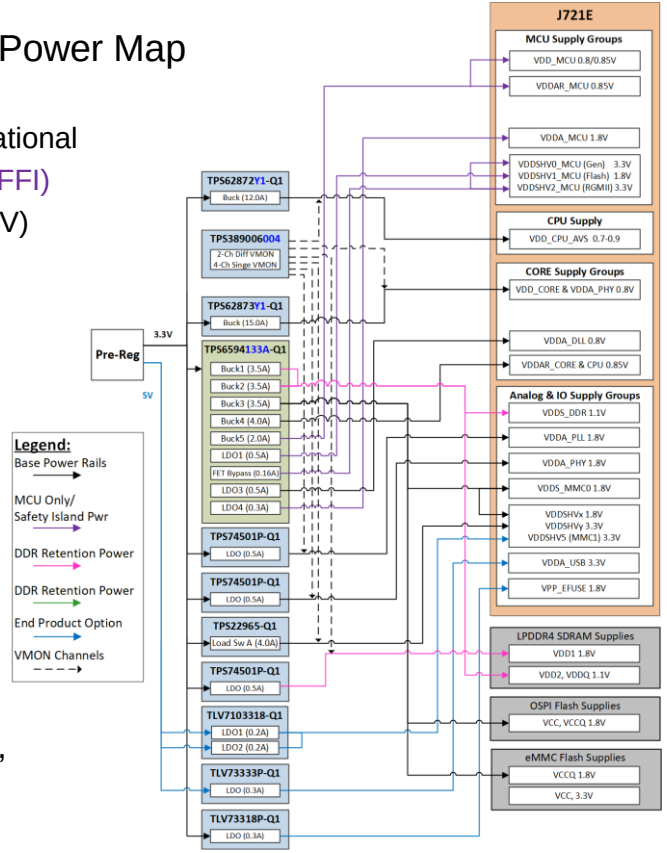
J721E New Universal PDN-3x | SoC Full Entitlement

Processor GPN (OPN)	Safety	PDN Key Features	PDN-ID Base Pwr ICs	PMIC OPNs	Pwr IC Relative Cost	Pwr IC Area [mm^2]	PDN References
J721S2 (TDA4VE) (TDA4AL) (TDA4VL)	ASIL-D Capable	Isolated MCU & Main Power • MCU Island Safety Proc • Power Rail FFI • Low Power Modes • AEC-100, Grade-1 (Tj =+125C)	Legacy PDN-0C 2019 J721E EVM PDN-0C 2x TPS6594-Q1	TPS65941213RWERQ1 (Primary PMIC) TPS65941111RWERQ1 (Secondary PMIC)	1.0	146	J721E CDDS Links (similar to J721E Starter Kit Bd, PDN-0C, PROC112Ex_SCH)
New Universal PDN-3x	ASIL-D Capable	Isolated MCU & Main Power • MCU Island Safety Proc • Power Rail FFI • Low Power Modes • AEC-100, Grade-1 (Tj =+125C)	J721E PDN-3A TPS6594-Q1 + 2x TPS6287-Q1	TPS6594133ARWERQ1 (same PN for all PDN-3x) TPS62873Y1QWRXSRQ1 TPS62872Y1QWRXSRQ1	0.93	144	(similar to J784S4 EVM Bd, PDN-3A, PROC141Ex_SCH)
	ASIL-D Capable	Isolated MCU & Main Power • MCU Island Safety Proc • Power Rail FFI • AEC-100, Grade-1 (Tj =+125C)	J721E PDN-3F TPS6594-Q1 + 2x TPS6287-Q1	TPS6594133ARWERQ1 (same PN for all PDN-3x) TPS62873Y1QWRXSRQ1 TPS62872Y1QWRXSRQ1	0.89	115	(similar to J784S4 EVM Bd, PDN-3A, PROC141Ex_SCH, w/out Low Pwr Modes)
	ASIL-D Capable	Combined MCU & Main Power • Extended MCU Safety Processor • Low Power Modes • AEC-100, Grade-1 (Tj =+125C)	J721E PDN-3G TPS6594-Q1 + 2x TPS6287-Q1	TPS6594133ARWERQ1 (same PN for all PDN-3x) TPS62873Y1QWRXSRQ1 TPS62872Y1QWRXSRQ1	0.86	124	(similar to J784S4 Starter Kit Bd, PDN-3H, PROC154Ex_SCH, Work-in-Progress)
	ASIL-D Capable	Combined MCU & Main Power • Extended MCU Safety Processor • AEC-100, Grade-1 (Tj =+125C)	J721E PDN-3M TPS6594-Q1 + 2x TPS6287-Q1	TPS6594133ARWERQ1 (same PN for all PDN-3x) TPS62873Y1QWRXSRQ1 TPS62872Y1QWRXSRQ1	0.82	95	(similar to J784S4 Starter Kit Bd, PDN-3H, PROC154Ex_SCH, Work-in-Progress)

J721E PDN-3A |TPS6594-Q1 + TPS6287-Q1 (Base Pwr IC PNs)

- Features Supported
  - AEC-100, Grade-1 temp range: -40 < Tj < +125C
  - SoC Performance: Full entitlement up to 2.0GHz clk with SERDES interfaces operational
  - Functional Safety[7]: ASIL-D capable system with Main & MCU isolated power rails (FFI)
  - SDRAM: 2x EMIFs each with LPDDR4 (64Gb, Quad Die, 32b, 4266MTs, VIO = 1.1V)
  - Flash: Octal SPI or Hyper Flash for boot & eMMC for mass storage
  - Signaling Levels: MCU & Main with Dual VIO (3.3/1.8V)
  - Low Power Modes:
    - 3.3V MCU Only,
    - DDR Retention,
  - End Product Options:
    - Compliant, high-speed SD Card
    - Compliant, USB 2.0 data eye
    - Efuse programming
- Same PMIC (TPS6594133A-Q1) PN used for all “J7xxx PDN-3x schemes”

- Power Map

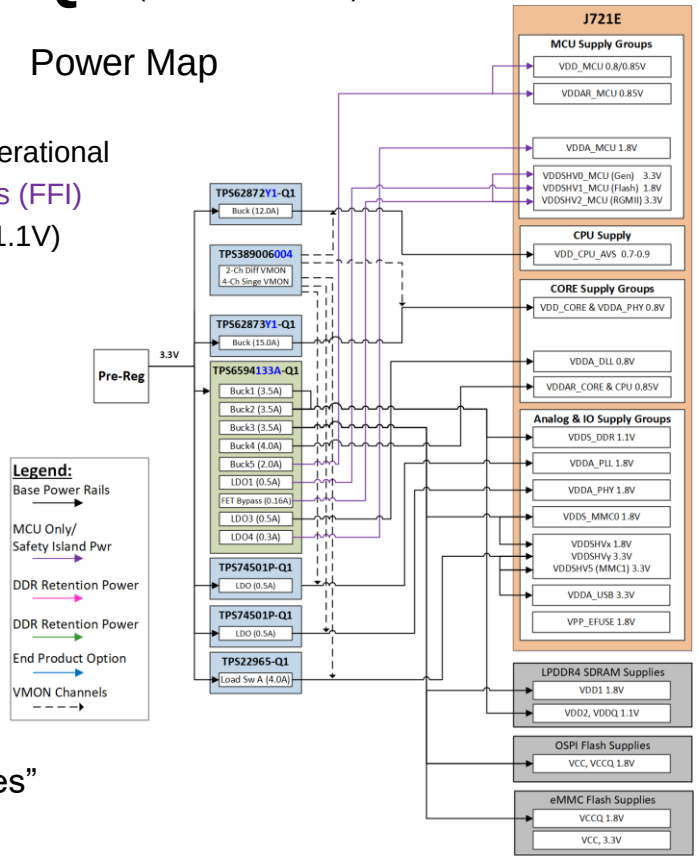


Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented by either an external MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

J721E PDN-3F |TPS6594-Q1 + TPS6287-Q1 (Base Pwr IC PNs)

- Features Supported
  - AEC-100, Grade-1 temp range: -40 < Tj < +125C
  - SoC Performance: Full entitlement up to 2.0GHz clk with SERDES interfaces operational
  - Functional Safety[7]: ASIL-D capable system with Main & MCU isolated power rails (FFI)
  - SDRAM: 2x EMIFs each with LPDDR4 (64Gb, Quad Die, 32b, 4266MTs, VIO = 1.1V)
  - Flash: Octal SPI or Hyper Flash for boot & eMMC for mass storage
  - Signaling Levels: MCU & Main with Dual VIO (3.3/1.8V)
  - Low Power Modes:
    - 3.3V MCU Only,

- Power Map



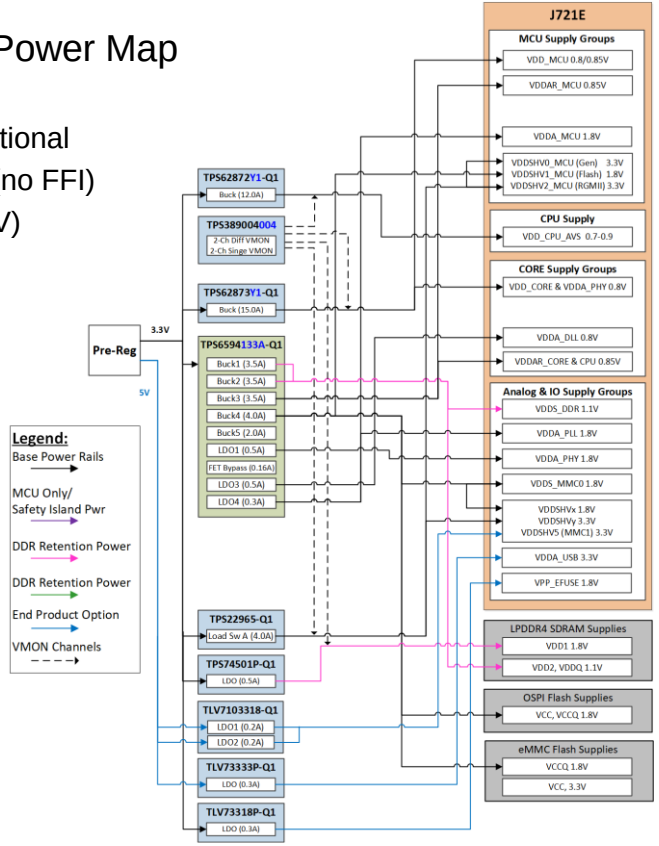
- Same PMIC (TPS6594133A-Q1) PN used for all “J7xxx PDN-3x schemes”

Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented by either an external MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

J721E PDN-3G |TPS6594-Q1 + TPS6287-Q1 (Base Pwr IC PNs)

- Features Supported
  - AEC-100, Grade-1 temp range: -40 < Tj < +125C
  - SoC Performance: Full entitlement up to 2.0GHz clk with SERDES interfaces operational
  - Functional Safety[7]: ASIL-D capable system with Main & MCU Grouped power rails (no FFI)
  - SDRAM: 2x EMIFs each with LPDDR4 (64Gb, Quad Die, 32b, 4266MTs, VIO = 1.1V)
  - Flash: Octal SPI or Hyper Flash for boot & eMMC for mass storage
  - Signaling Levels: MCU & Main with Dual VIO (3.3/1.8V)
  - Low Power Modes:
    - DDR Retention,
  - End Product Options:
    - Compliant, high-speed SD Card
    - Compliant, USB 2.0 data eye
    - Efuse programming
- Same PMIC (TPS6594133A-Q1) PN used for all “J7xxx PDN-3x schemes”

- Power Map

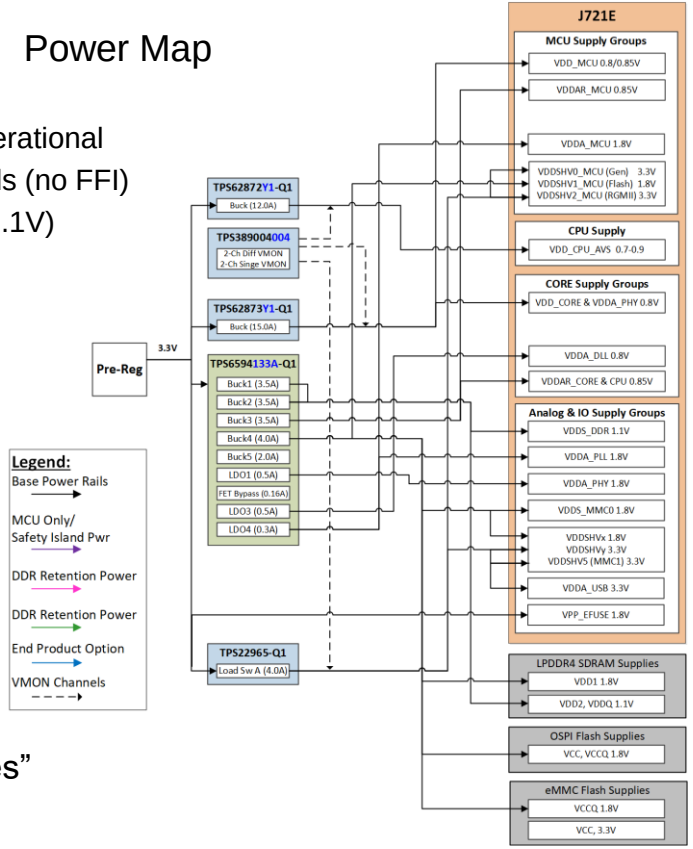


Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented by either an external MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

J721E PDN-3M |TPS6594-Q1 + TPS6287-Q1 (Base Pwr IC PNs)

- Features Supported
  - AEC-100, Grade-1 temp range: -40 < Tj < +125C
  - SoC Performance: Full entitlement up to 2.0GHz clk with SERDES interfaces operational
  - Functional Safety[7]: ASIL-D capable system with Main & MCU Grouped power rails (no FFI)
  - SDRAM: 2x EMIFs each with LPDDR4 (64Gb, Quad Die, 32b, 4266MTs, VIO = 1.1V)
  - Flash: Octal SPI or Hyper Flash for boot & eMMC for mass storage
  - Signaling Levels: MCU & Main with Dual VIO (3.3/1.8V)
  - Low Power Modes:

- Power Map



- Same PMIC (TPS6594133A-Q1) PN used for all “J7xxx PDN-3x schemes”

Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented by either an external MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

J7xxx EVM PDN-3A | GPIO Functions & Priority Map (EVM max features)

PMIC-A Fixed IO & GPIO Resource Assignments & Operational Priorities					PMIC-A PN: TPS6594133ARWERQ1		
PMIC	GPIO # & Fixed I/O	Assigned NVM Function	I/O (OD)	SoC EVM PDN Net Connections	1st Priority PDN Opr & SoC Pwr Seq GPIO	2nd Priority Functional Safety GPIO	3rd Priority Low Power Mode GPIO
Leo PG2.0 PMIC-A	GPIO1	SCL_I2C2	I	H_MCU_I2C0_SCL		Yes	
	GPIO2	SDA_I2C2	I/O	H_MCU_I2C0_SDA		Yes	
	GPIO3	nERR_SoC	I	SoC_SAFETY_ERRn		Yes	
	GPIO4	LP_WKUP1[1] or >> WKUP2	I	SOC_PWR_WKn			Yes
	GPIO5	REGEN	O (OD)	EN_GPIO_RET			Yes
	GPIO6	REGEN	O (OD)	EN_DDR_RET_1V1			Yes
	GPIO7	nERR_MCU	I	MCU_SAFETY_ERRn		Yes	
	GPIO8	DISABLE_WDOG[2] >> GPI	I	WDOG_DISABLE >> MAIN_PWRGRP_IRQn		Yes	
	GPIO9	REGEN	O	EN_VIO_3V3	Yes		Yes
	GPIO10	GPI	I	MCU_PWRGRP_IRQn		Yes	Yes
	GPIO11	nRSTOUT_SoC	O (OD)	H_SOC_PORz_1V8	Yes	Yes	Yes
	nPWRON_ENABLE		I	SOC_PWR_EN	Yes		
	nRTSOUT		O (OD)	H_MCU_PORz_1V8	Yes	Yes	Yes
	nINT		O (OD)	H_MCU_INTn_1V8		Yes	
	SCL_I2C1		I	H_WKUP_I2C0_SCL	Yes		
	SDA_I2C1		I/O	H_WKUP_I2C0_SDA	Yes		
	EN_DRV		O	LEOA_EN_DRV		Yes	

J7xxx PDN-3A HCPS Summary | Discrete Buck PNs

J7 TI Project Name	J7 Generic PNs	J7 Orderable PNs	J7 Marketing Names	CPU Peak Ld [A]	CPU HCPS Tulip: # Phs, Imax (PN), [RTM]	CORE Peak Ld [A]	CORE HCPS Tulip: # Phs, Imax (PN)
J7ES	J721E	TDA4VM DRA829	TDA4V Mid DRA829	9.8	1x, 12A (TPS62872Y1QWRXSRQ1) [tbdQ 202?]	13.4	1x, 15A (TPS62873Y1QWRXSRQ1) [3Q/4Q 2022]
J7VCL	J7200	DRA821	DRA821	4.4	1x, 6A (TPS62870Y1QWRXSRQ1) [tbdQ 202?]	3.8	1x, 6A (TPS62870Y1QWRXSRQ1) [tbdQ 202?]
J7AEP	J721S2	TDA4AL TDA4VL TDA4VE	TDA4A Low TDA4V Low TDA4V Mid Eco	11.4	1x, 15A (TPS62873Y1QWRXSRQ1) [3Q/4Q 2022]	14.1	2x, 9A (TPS62871Y1QWRXSRQ1) [tbdQ 202?]
J7AHP	J784S4	TDA4AP TDA4VP TDA4AH TDA4VH	TDA4A Mid Plus TDA4V Mid Plus TDA4A High TDA4V High	39.8	3x, 15A (TPS62873Y1QWRXSRQ1) [3Q/4Q 2022]	24.8	2x, 15A (TPS62873Y1QWRXSRQ1) [3Q/4Q 2022]

Notes:

1. HCPS = High Current Power Stage
2. J7VCL (DRA821) has lower CPU & Core pk loads (4.4 & 3.8) resulting in higher current margins (27 & 37%) using 6A Tulip PN. However, a J7VCL PDN-3A isolated MCU & Main power scheme enables use of a common PMIC PN (TPS6594133A-Q1) over all J7 SoC products.

J721E (DRA829, TDA4VM)
LEGACY PDN SCHEMES

J721E Legacy PDNs | SoC Full Entitlement

Processor GPN (OPN)	Safety	PDN Key Features	PDN-ID Base Pwr ICs	PMIC OPNs	Pwr IC Relative Cost	Pwr IC Area [mm^2]	PDN References

J721E (DRA829) (TDA4VM)	ASIL-D Capable	Isolated MCU & Main Power
		• MCU Island Safety Processor
		  • Power Rail FFI
		• PDN Max Feature Set
		  • 2x Low Power Modes
		  • 3x End Product Options
			J721E EVM PDN-0C
			
			2x TPS6594-Q1
				TPS6594**1213**RWERQ1
				(Primary PMIC, common PN)
				
				TPS6594**1111**RWERQ1
				(Secondary PMIC)
					1.0	146	J721E CDDS Links
							
							(similar to J721E Starter Kit Bd, PDN-0C, PROC112Ex_SCH)

		(Same as above except as noted) • PDN Base Features + Dual VIO	J721E EVM PDN-0F		0.96	138	

	ASIL-D Capable	Combined MCU & Main Power
		• Extended MCU Safety Processor
		  • No power rail FFI
		• PDN Max Feature Set
		  • 1x Low Power Mode
		  • 3x End Product Options
			J721E PDN-1A
			
			TPS6594-Q1
			+ LP8764-Q1
				TPS6594**1213**RWERQ1
				(Primary PMIC, common PN)
				
				LP8764**11B4**RQKRQ1
				(Secondary PMIC)
					0.83	111.8	J721E CDDS Links

		(Same as above except as noted) • PDN Base Features + Dual VIO	J721E PDN-1F		0.81	105.5	

Legacy PDNs

Notes:
1. **PMIC Datasheets:** Latest TPS6594-Q1 & LP8764-Q1 DS are available on TI.com.
2. **PMIC Samples**: Please allow for 4-6wk lead time after placing ES orders, contact the PMIC marketing team for ordering requirements.
3. **PMIC Custom NVM spins** (different default settings than EVM) will be available with business case approval, please contact the PMIC marketing team for business case approval.
4. **PMIC PN** high-lighted characters uniquely identify PMICs programmed to support a specific J7 SoC PDN design.

J721E Power Solutions | PDN Feature Set Breakdown

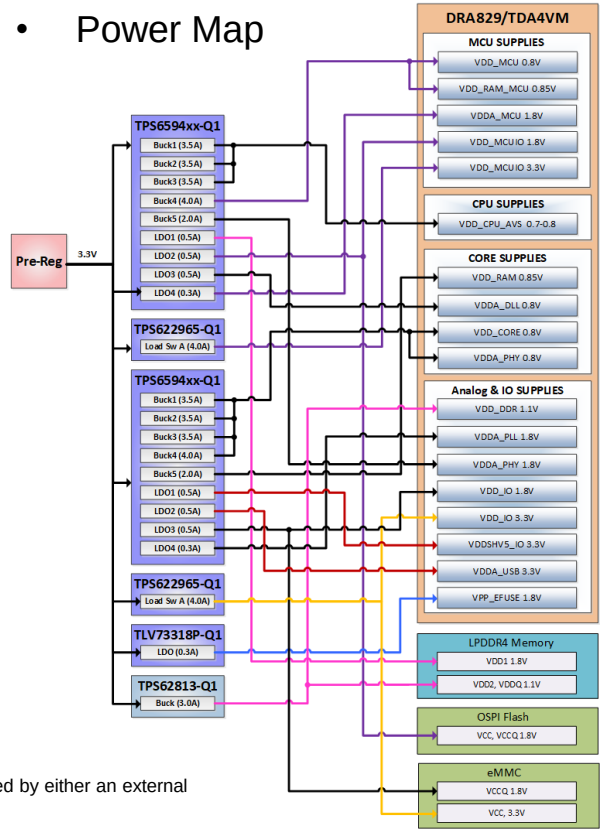
Features	J721E EVM PDN-0C (MCU Safety Island, Isolated MCU & Main)	J721E PDN-1A (Extended MCU, Combined MCU & Main)
Power Devices: AEC-100, Grade-1 (-40<Tj<+125C)	✓	✓
Functional Safety: ASIL-D capable	✓	✓
SoC perf: Full entitlement, 2.0GHz max	✓	✓
SDRAM: LPDDR4 (32Gb, 4x Die, 32b, 4266MTs)	✓	✓
Boot Flash: Octal SPI or Hyper-Flash	✓	✓
Mass Storage Flash: eMMC or UFS	✓	✓
Signaling Levels: Dual voltage 3.3V & 1.8V	O = 3.3V Main VIO	O
Low Power Modes: 1.8V MCU Only	✓	✗
3.3V MCU Only	O = 3.3V MCU VIO	✗
DDR Retention	O = DDR 1.8V	O
GPIO Retention	NA	NA
Compliant, High-speed SD Card	✓	O = 3.3/1.8V VIO
Compliant, USB 2.0 data eye	✓	O = SoC 3.3V Anlg
HS SoC, On-Board, Efuse programming	O = SoC 1.8V Vpp	O
IC Cost & Area Comparison:	**1.0 & 1.0**	**0.83 & 0.77**

✓ = PDN Base feature
O = Optional discrete power resource feature
# = * Impacted SD Card: 12Mbps capable on all PDNs
= ** Impacted USB 2.0: best effort data eye using digital 3.3V
✗ = Not supported

J721E EVM PDN-0C | 3-Ph Dual TPS6594-Q1 (Base Pwr IC PNs)

- Features Supported
  - Power ICs, AEC-100, Grade-1 temp range: -40 < Tj < +125C
  - SoC full performance at max 2.0GHz clock with SERDES interfaces operational
  - Functional Safety[7]: ASIL-D capable system with Main & MCU isolated power rails (FFI)
  - SDRAM: 1x EMIF with LPDDR4 (32Gb, 4x Die, 32b, 4266MTs, VIO = 1.1V)
  - Flash, Octal SPI or Hyper-Flash boot, eMMC & UFS mass storage
  - Dual Voltage Signaling: MCU & Main with Dual VIO (3.3/1.8V)
  - Low Power Modes:
    - 3.3V MCU Only,
    - DDR Retention
  - End Product Options:
    - Compliant, high-speed SD Card
    - Compliant, USB 2.0 data eye
    - Efuse programming

- Power Map



Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented by either an external MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

J721E PDN-0C | Scheme & Loading Summary (EVM max features)

Use Case: J7ES_EVM_Internal_July15_2020.xlsx

Pwr Est Date: 7/15/2020 **PDN-0C Base + EVM features**

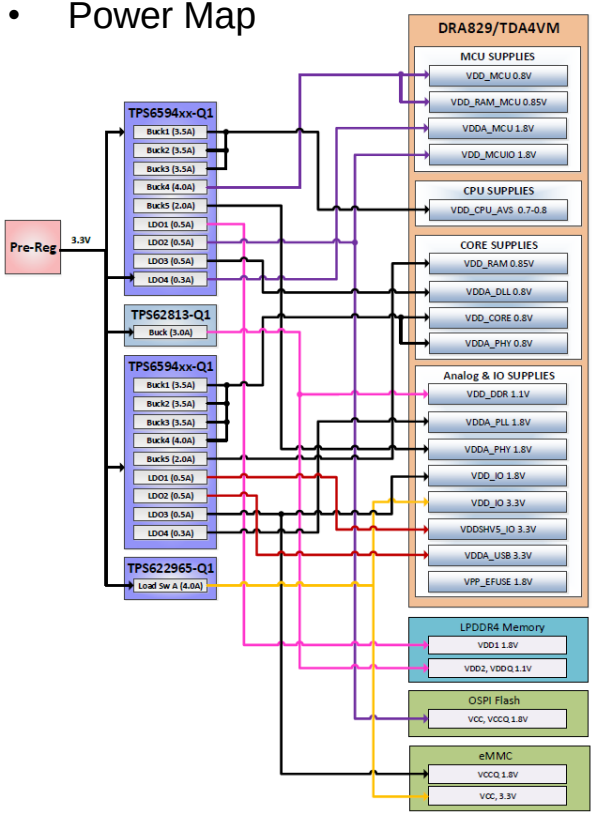
Total Power ICs	Discrete Power ICs	Output Current Capacity	Power Resources	PDN Power Rails	Total SoC Loads [mA]	LPDDR4 [mA]	OSPI & *Hyper Flash* [mA]	eMMC [mA]	UFS [mA]	SD Card [mA]	Total Rail Load [mA]	Current Margins [%]	IC Area [mm^2]
TPS65941x-Q1	PMIC-A	10500	Buck 1	VDD_CPU_AVS	9800						9800	6.7%	64.0
			Buck 2										
			Buck 3										
		3500	Buck 4	VDD_MCU_0V85	1351						1351	61.4%	
		2000	Buck 5	VDD_PHY_1V8	211				340		551	72.5%	
		500	LDO 1	VDD1_LPDDR4_1V8		56					56	88.8%	
		500	LDO 2	VDD_MCUIO_1V8	7		*280*				287	42.6%	
		500	LDO 3	VDA_DLL_0V8	21						21	95.8%	
		300	LDO 4	VDA_MCU_1V8	59						59	80.3%	
TPS65941x-Q1	PMIC-B	14000	Buck 1	VDD_CORE_0V8	13349						13349	4.7%	64.0
			Buck 2										
			Buck 3										
			Buck 4										
		2000	Buck 5	VDD_RAM_0V85	950						950	52.5%	
		500	LDO 1	VDD_SD_DV	7						7	98.6%	
		500	LDO 2	VDA_USB_3V3	6						6	98.8%	
		500	LDO 3	VDD_IO_1V8	130			140			270	46.0%	
		300	LDO 4	VDA_PLL_1V8	193						193	35.7%	
TPS22965W-Q1	LdSw-A	4000	Ld Sw A	VDD_IO_3V3	78			120	125	400	723	81.9%	4.0
TPS22965W-Q1	LdSw-B	4000	Ld Sw B	VDD_MCUIO_3V3	26						26	99.4%	4.0
TPS62813-Q1	BUCK-A	3000	Buck A	VDD_DDR_1V1	563	1530					2093	30.2%	6.0
TLV73318P-Q1	LDO-A	300	LDO	VPP_EFUSE_1V8	124						124	58.7%	4.0
6	**4**	**0**	**22**	**17**								**Totals:**	**146.0**

Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented by either an external MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

J721E PDN-0F | 3-Ph Dual TPS6594-Q1 (Base Pwr IC PNs)

- Features Supported
  - Power ICs, AEC-100, Grade-1 temp range: -40 < Tj < +125C
  - SoC full performance at max 2.0GHz clock with SERDES interfaces operational
  - Functional Safety[7]: ASIL-D capable system with Main & MCU isolated power rails (FFI)
  - SDRAM: 1x EMIF with LPDDR4 (32Gb, 4x Die, 32b, 4266MTs, VIO = 1.1V)
  - Flash, Octal SPI or Hyper-Flash boot, eMMC & UFS mass storage
  - Dual Voltage Signaling: MCU & Main with Dual VIO (3.3/1.8V)
  - Low Power Modes:
    - 1.8V MCU Only,
    - DDR Retention
  - End Product Options:
    - Compliant, high-speed SD Card
    - Compliant, USB 2.0 data eye

- Power Map



Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

J721E PDN-0F | Scheme & Loading Summary (PDN base features + dual VIO)

Use Case: J7ES_EVM_Internal_July15_2020.xlsx

Pwr Est Date: 7/15/2020 **PDN-0C Base + Min features + Main Dual VIO**

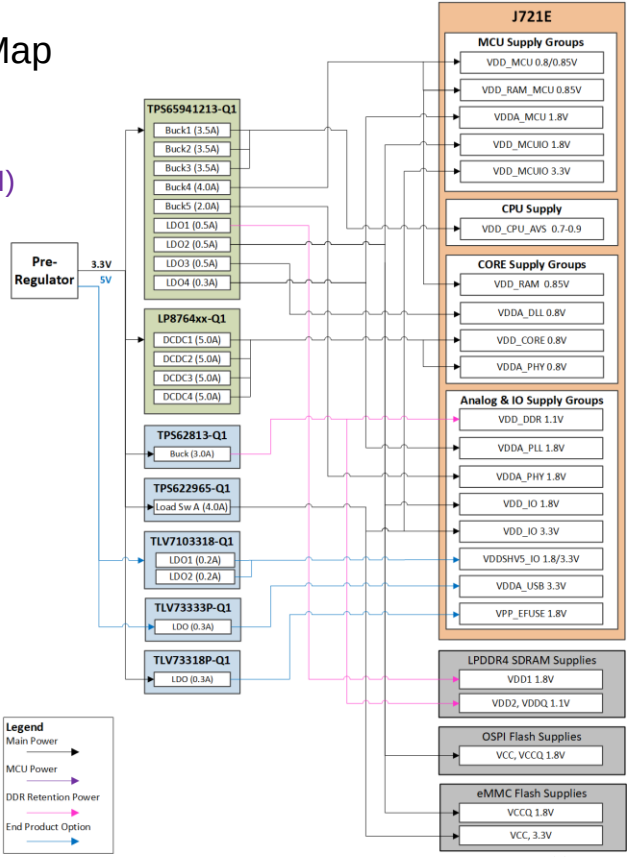
Total Power ICs	Discrete Power ICs	Output Current Capacity	Power Resources	PDN Power Rails	Total SoC Loads [mA]	LPDDR4 [mA]	OSPI & *Hyper Flash* [mA]	eMMC [mA]	UFS [mA]	SD Card [mA]	Total Rail Load [mA]	Current Margins [%]	IC Area [mm^2]
TPS65941x-Q1	PMIC-A	10500	Buck 1	VDD_CPU_AVS	9800						9800	6.7%	64.0
			Buck 2										
			Buck 3										
		3500	Buck 4	VDD_MCU_0V85	1351						1351	61.4%	
		2000	Buck 5	VDD_PHY_1V8	211				340		551	72.5%	
		500	LDO 1	VDD1_LPDDR4_1V8		56					56	88.8%	
		500	LDO 2	VDD_MCUIO_1V8	33		*280*				313	37.4%	
		500	LDO 3	VDA_DLL_0V8	21						21	95.8%	
		300	LDO 4	VDA_MCU_1V8	59						59	80.3%	
TPS65941x-Q1	PMIC-B	14000	Buck 1	VDD_CORE_0V8	13349						13349	4.7%	64.0
			Buck 2										
			Buck 3										
			Buck 4										
		2000	Buck 5	VDD_RAM_0V85	950						950	52.5%	
		500	LDO 1	VDD_SD_DV	7						7	98.6%	
		500	LDO 2	VDA_USB_3V3	6						6	98.8%	
		500	LDO 3	VDD_IO_1V8	130			140			270	46.0%	
		300	LDO 4	VDA_PLL_1V8	193						193	35.7%	
TPS22965W-Q1	LdSw-A	4000	Ld Sw A	VDD_IO_3V3	78			120	125	400	723	81.9%	4.0
TPS62813-Q1	BUCK-A	3000	Buck A	VDD_DDR_1V1	563	1530					2093	30.2%	6.0
4	**2**	**0**	**20**	**15**								**Totals:**	**138.0**

Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented by either an external MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

J721E PDN-1A | TPS6594-Q1 + LP8764-Q1 (Base Pwr IC PNs)

- Features Supported
  - Power ICs, AEC-100, Grade-1 temp range: -40 < Tj < +125C
  - SoC full performance at max 2.0GHz clock with SERDES interfaces operational
  - Functional Safety[7]: ASIL-D capable system with Main & MCU isolated power rails (FFI)
  - SDRAM: 1x EMIF with LPDDR4 (32Gb, 4x Die, 32b, 4266MTs, VIO = 1.1V)
  - Flash, Octal SPI boot, eMMC & UFS mass storage
  - Dual Voltage Signaling: MCU & Main with Dual VIO (3.3/1.8V)
  - Low Power Modes:
    - DDR Retention
  - End Product Options:
    - Compliant, high-speed SD Card
    - Compliant, USB 2.0 data eye
    - Efuse programming

- Power Map



Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented by either an external MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

J721E PDN-1A | Scheme & Loading Summary (PDN max features)

Use Case: J7ES_EVM_Internal_July15_2020.xlsx

Pwr Est Date: 7/15/2020 **PDN-1A-Max Maximum Features**

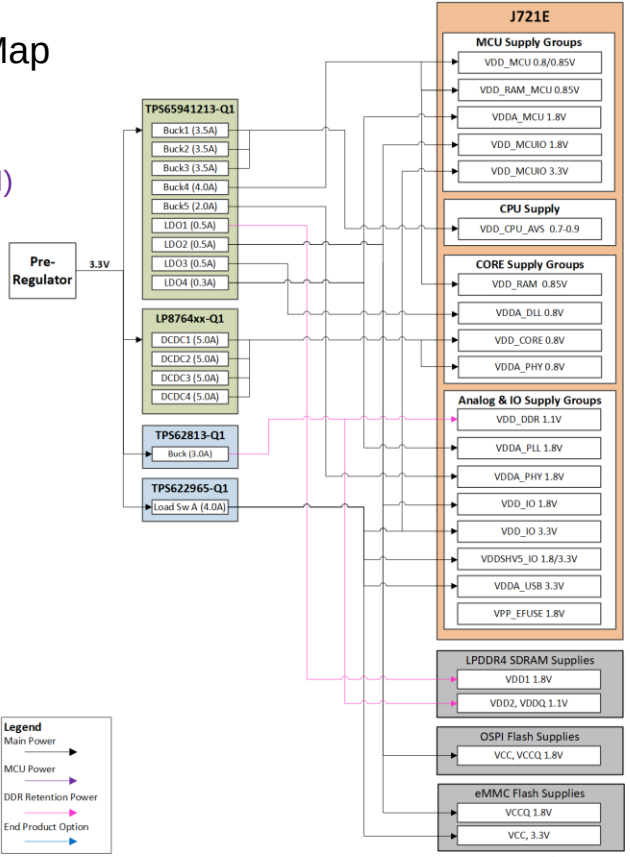
PNs	Power Components	Output Current Capacity	Power Resources	PDN Power Rails	Total SoC Loads [mA]	LPDDR4 [mA]	OSPI [mA]	eMMC [mA]	UFS [mA]	SD Card [mA]	Total Rail Load [mA]	Current Margins [%]	IC Area [mm^2]
TPS65941x-Q1	PMIC-A	10500	Buck 1	VDD_CPU_AVS	9800						9800	6.7%	64.0
			Buck 2										
			Buck 3										
		3500	Buck 4	VDD_MCU_0V85	2301						2301	34.3%	
		2000	Buck 5	VDD_PHY_1V8	211				385		596	70.2%	
		500	LDO 1	VPP_EFUSE_1V8	124						124	75.2%	
		500	LDO 2	VDD_IO_1V8	141		156	140			437	12.5%	
		500	LDO 3	VDA_DLL_0V8	20						20	96.0%	
		300	LDO 4	VDA_LN_1V8	252						252	16.0%	
LP8764x-Q1	PMIC-B	20000	Buck 1	VDD_CORE_0V8	13349						13349	33.3%	27.5
			Buck 2										
			Buck 3										
			Buck 4										
TPS22965W-Q1	LdSw-A	4000	Ld Sw A	VDD_IO_3V3	262			120	130	400	912	77.2%	4.0
TPS62813-Q1	BUCK-A	3000	Buck A	VDD_DDR_1V1	563	1530					2093	30.2%	6.0
TLV73318-Q1	LDO-A	300	LDO	VDD1_LPDDR4_1V8		56					56	81.3%	4.0
TLV7103318-Q1	LDO-B	200	LDO	VDD_SD_DV	36.666667						37	81.7%	2.3
TLV73333-Q1	LDO-C	300	LDO	VDA_USB_3V3	0						0	100.0%	4.0
4	**2**		**15**	**10**								**Total:**	**111.8**

Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented by either an external MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

J721E PDN-1F | TPS6594-Q1 + LP8764-Q1 (Base Pwr IC PNs)

- Features Supported (Base PDN ICs only)
  - Power ICs, AEC-100, Grade-1 temp range: -40 < Tj < +125C
  - SoC full performance at max 2.0GHz clock with SERDES interfaces operational
  - Functional Safety[7]: ASIL-D capable system with Main & MCU isolated power rails (FFI)
  - SDRAM: 1x EMIF with LPDDR4 (32Gb, 4x Die, 32b, 4266MTs, VIO = 1.1V)
  - Flash, Octal SPI boot, eMMC & UFS mass storage
  - Dual Voltage Signaling: MCU & Main with Dual VIO (3.3/1.8V)
  - Low Power Modes:
    - DDR Retention

- Power Map



Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented by either an external MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

J721E PDN-1F | Scheme & Loading Summary (PDN base features + dual VIO)

Use Case: J7ES_EVM_Internal_July15_2020.xlsx

Pwr Est Date: 7/15/2020 **PDN-1A Base + MCU/Main Dual VIO**

PNs	Power Components	Output Current Capacity	Power Resources	PDN Power Rails	Total SoC Loads [mA]	LPDDR4 [mA]	OSPI [mA]	eMMC [mA]	UFS [mA]	SD Card [mA]	Total Rail Load [mA]	Current Margins [%]	IC Area [mm^2]
TPS65941x-Q1	PMIC-A	10500	Buck 1	VDD_CPU_AVS	9800						9800	6.7%	64.0
			Buck 2										
			Buck 3										
		3500	Buck 4	VDD_MCU_0V85	2301						2301	34.3%	
		2000	Buck 5	VDD_PHY_1V8	211	56			385		652	67.4%	
		500	LDO 1	VPP_EFUSE_1V8	124						124	75.2%	
		500	LDO 2	VDD_IO_1V8	141		156	140			437	12.5%	
		500	LDO 3	VDA_DLL_0V8	20						20	96.0%	
		300	LDO 4	VDA_LN_1V8	252						252	16.0%	
LP8764x-Q1	PMIC-B	20000	Buck 1	VDD_CORE_0V8	13349						13349	33.3%	27.5
			Buck 2										
			Buck 3										
			Buck 4										
TPS22965W-Q1	LdSw-A	4000	Ld Sw A	VDD_IO_3V3	298			120	130	400	948	76.3%	4.0
TPS62813-Q1	BUCK-A	3000	Buck A	VDD_DDR_1V1	563	1530					2093	30.2%	6.0
4	**2**		**15**	**10**								**Total:**	**101.5**

Note: 7.) Customer functional safety concept directly impacts PDN design based upon desired ASIL level and safety monitoring processor implemented by either an external MCU device or SoC's MCU Island or Extended MCU schemes. An end product's safety capability will be determined by customer's system FMEDA.

REFERENCE SECTION

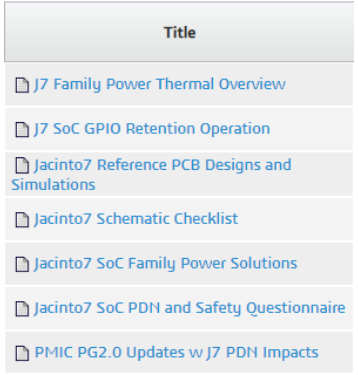
Rev History

Date	Rev	Author	Description
1/14/2022	1.7	Bill McCracken	Removed NDA Restrictions from slides since SoC has been released to production & TI websites.
2/28/2022	1.71	Bill McCracken	Updated to align using Generic PN as reference instead of Orderable PNs
5/16/2022	1.8	Bill McCracken	Aligned to consolidated J7 SoC Family Power Solution slide updates Updated PDN CDDS & TI website links in Reference Section
6/28/2022	1.83	Bill McCracken	Added CDDS link to Ref Section for this Jacinto7 SoC Family Power Solutions overview of all recmd'd PDNs Updated PDN Design, Selection & Identification slides Added "Dscrt Buck PN Summary" table (Ref Section) showing buck PNs for different J7 SoCs using PDN-3A
6/29/2022	1.84	Bill McCracken	Added TI Website link to SK-TDAVM Evaluation Board for PDN-0C SCH reference.
9/13/2022	2.0	Bill McCracken	Updated introduction slides & added Validate slide Added "New Universal PDN-3x" power summary vs Original PDN-0C Added 4 new PDN-3x schemes to show show universal use & flexibility of PDN-3x schemes
9/14/2022	2.1	Bill McCracken	Updated "Universal PDN-3x" power summary slide by removing "Low Pwr Modes" from PDN-3M features Updated PDN-3M Power Map slide from Main & MCU Isolated.. to Main & MCU Grouped power rails(no FFI)
10/18/2022	2.4	Bill McCracken	Corrected Load Switch PN typo on PDM power map diags

Jacinto 7 Family Collateral CDDS Links

CDDS - Folder - Jacinto7 Product Series:
US - https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.31126.27228

CDDS - Folder - Jacinto7 Product Series/J7 Family/AppNote:
US - https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.42490.21252



CDDS - Folder path & file **- Jacinto7 Product Series/J784S4/EA/AppNote/**Jacinto7 SoC Family Power Solutions
US - https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.36054.4530&latestRevision=true

J721E (DRA829/TDA4VM) CDDS & Website Links

CDDS - Folder path & file **- Jacinto7 Product Series/J721E/AppNote/**Jacinto7 J721E Pwr Sols:
US - https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.43295.55377&latestRevision=true

CDDS - Folder path & file **- Jacinto7 Product Series/DRA829 TDA4VM/AppNote/** DRA829_TDA4VM_3Ph_Dual_Leo_PDN-0C:
US - https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.65023.28220&latestRevision=true

TI Website – DRA829/TDA4VM App Notes & Board Design Files
Optimized TPS65941213-Q1 and TPS65941111-Q1 PMIC User Guide for J721E, PDN-0C (Rev. A)

SK-TDA4VM Evaluation board | TI.com

CDDS - Folder path & file **- Jacinto7 Product Series/DRA829 TDA4VM/AppNote/** DRA829_TDA4VM_Leo_Hera_PDN-1A:
US - https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.10891.7971&latestRevision=true

TI Website – DRA829/TDA4VM App Notes
TPS65941213-Q1 and LP876411B4-Q1 PMIC User Guide for J721E, PDN-1A (ti.com)

Power Resource BOM Examples

TPS65941x-Q1

Fsw = 2.2MHz Vin = 3.3V

Modules	Component Type	Value	QTY	Orderable Part Numbers	Description
LV-PMIC	IC	TPS6594x-Q1	2	TPS6594x-Q1	PMIC, 5 Bucks, 4 LDOs, 11 GPIO, NVM Prgm Seqr, I2C Cntl, Safety Appls, 8x8mm, 0.5mm pitch, 56-pin VQFN, -40 to +125C (Temp Grade 1), AEC-Q100
PMIC External Components	Csys	0.47uF	2	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Cldo	2.2uF	2	GCM188R70J225KE22D	2.2uF, +/-10%, X7R, 6.3V, 0603, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Cvio	0.1uF	4	GCM155R71C104KA55D	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Zener Diode	10V	2	MM3Z10VST1G	Zener Diode, 10V, 2%, 0.3W, 0.5uA, 15ohms, SOD-323-2, -65 to +150C
Safety FET	NMOS FET	116A	2	NVMFS4C05NT1G	NMOS Enhancement FET, 116A, 3.6W, 3.4mohm, Vgs 20V, Vds 30V, SO-8 FL, -55 to +175C, AEC-Q101
32k Osc	Xtal Osc	32kHz	1	ECS-327-9-34QCS-TR	Crystal 32.768kHz 9pF 10ppm -40C +125C AEC-Q200
	CL	9pF	2	GCM1555C1H9R0CA16	9pF, +/- %, C0G/NP0, 50V,
Buck External Components	Ci	10uF	10	GCM21BR70J106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Co	47uF	30	GCM32ER70J476ME19K	47uF, +/-20%, X7R, 6.3V, 1210, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Lo	470nH	10	TFM252012ALMAR47MTAA	0.47uH, +/-20%, 24mohm, Is=5.8A, It=4.9A, 20V, 2520, -40 to +125C, AEC-200, Magntc Mtl Pwr Ind
LDO External Components	Ci	2.2uF	8	GCM188R70J225KE22D	2.2uF, +/-10%, X7R, 6.3V, 0603, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Co	2.2uF	12	GCM188R70J225KE22D	2.2uF, +/-10%, X7R, 6.3V, 0603, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Support Components Only			85		
Total Component Area (IC + Components)			87		

TPS22965-Q1

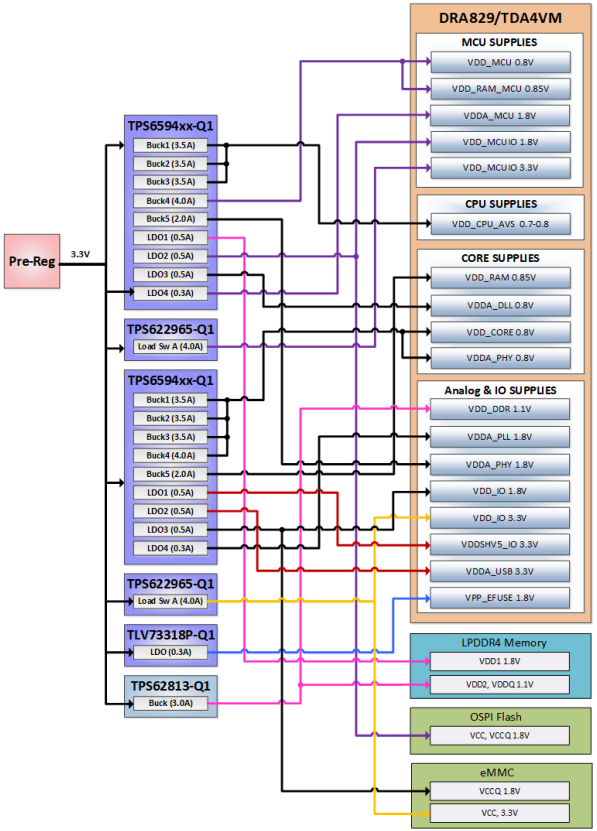
Modules	Component Type	Value	QTY	Orderable Part Numbers	Description
Load Switch	IC	TPS22965	2	TPS22965-Q1DSG	IC, 5.5V, 4A, 16mohm Ron Load Switch with Quick Discharge, 2x2mm, 0.5mm pitch, 8-pin SON, -40 to +105C (Temp Grade 2), AEC-100
Input	Cin	1µF	2	GCM188R71C105KA64	1.0uF, +/-10%, X7R, 16V, 0603, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Support	Ct	220pF	2	GCM155R71H221KA37	220pF, +/-10%, X7R, 50V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Output	Co	0.1uF	2	GCM155R71C104KA55D	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Support Components Only			6		
Total Component Area (IC + Components)			8		

TLV733xxP-Q1

Modules	Component Type	Value	QTY	Orderable Part Numbers	Description
LDO	IC	TLV733xxP-Q1	1	TLV73318PQDBVRQ1	IC, 300mA, 1.4< Vin <5.5V, Fixed 1.0< Vo <3.3V, Ultra-Small, Low Iq LDO, 2.9x1.6mm, 5-pin SOT-23 (DBV), -40 to +125C (Temp Grade 1), AEC-Q100
Input	Cin	1µF	1	GCM188R71C105KA64	1.0uF, +/-10%, X7R, 16V, 0603, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Output	Co	1µF	1	GCM188R71C105KA64	1.0uF, +/-10%, X7R, 16V, 0603, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Support Components Only			2		
Total Component Area (IC + Components)			3		

TPS62813-Q1

Modules	Component Type	Value	QTY	Orderable Part Numbers	Description
Buck Converter	IC	TPS62813-Q1	1	TPS6281320QWRWYRQ1	IC, 3A Buck Converter, 2.25MHz, Vin(2.75 - 6V), Vo Adj (0.6 - 5.5V), 3x2mm, 0.5mm pitch, 9-pin VQFN-HR (RWY) wettable flanks, -40 to +125C (Temp Grade 1), AEC-Q100
Input	Cin	22uF	1	GCM31CR71A226KE02L	22uF, +/-10%, X7R, 10V, 1206, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Support	Css &Cff	0.1uF	2	GCM155R71C104KA55D	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Output	Cout	47uF	1	GCM32ER70J476KE19K	47uF, +/-10%, X7R, 6.3V, 1210, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	L1	0.56uH	1	XEL3515-561ME	0.56uH, +/-20%, 24mohm, Is=4.5, It=6A, 80V, 3532, -40 to +125C, AEC-200, Shielded Pwr Ind
Support Components Only			4		
Total Component Area (IC + Components)			5		



Power Resource BOM Examples

TPS65941x-Q1 Fsw = 2.2MHz Vin = 3.3V

Modules	Component Type	Value	QTY	Orderable Part Numbers	Description
LV-PMIC	IC	TPS6594x-Q1	1	TPS6594x-Q1	PMIC, 5 Bucks, 4 LDOs, 11 GPIO, NVM Prgm Seqr, I2C Cntl, Safety Appls, 8x8mm, 0.5mm pitch, 56-pin VQFN, -40 to +125C (Temp Grade 1), AEC-Q100
PMIC External Components	Csys	0.47uF	1	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Cldo	2.2uF	1	GCM188R70J225KE22D	2.2uF, +/-10%, X7R, 6.3V, 0603, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Cvio	0.1uF	2	GCM155R71C104KA55D	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Zener Diode	10V	1	MM3Z10VST1G	Zener Diode, 10V, 2%, 0.3W, 0.5uA, 15ohms, SOD-323-2, -65 to +150C
Safety FET	NMOS FET	116A	1	NVMFS4C05NT1G	NMOS Enhancement FET, 116A, 3.6W, 3.4mohm, Vgs 20V, Vds 30V, SO-8 FL, -55 to +175C, AEC-Q101
32k Osc	Xtal Osc	32kHz	1	ECS-327-9-34QCS-TR	Crystal 32.768kHz 9pF 10ppm -40C +125C AEC-Q200
	CL	9pF	2	GCM1555C1H9R0CA16	9pF, +/- %, C0G/NP0, 50V,
Buck External Components	Ci	10uF	5	GCM21BR70J106KE22K	10uF, +/-10%, X7R, 6.3V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Co	47uF	15	GCM32ER70J476ME19K	47uF, +/-20%, X7R, 6.3V, 1210, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Lo	470nH	5	TFM252012ALMAR47MTAA	0.47uH, +/-20%, 24mohm, Is=5.8A, It=4.9A, 20V, 2520, -40 to +125C, AEC-200, Magntc Mtl Pwr Ind
LDO External Components	Ci	2.2uF	4	GCM188R70J225KE22D	2.2uF, +/-10%, X7R, 6.3V, 0603, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Co	2.2uF	6	GCM188R70J225KE22D	2.2uF, +/-10%, X7R, 6.3V, 0603, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Support Components Only			44		
Total Component Area (IC + Components)			45		

Note: Alternative Fsw = 4.4MHz is selectable based upon max load & efficiencies then L = 220nH (TFM252012ALMAR22MTAA) would be used, see TPS941x-Q1 data sheet for details.

LP8764x-Q1 Fsw = 2.2MHz Vin = 3.3V 4 Bucks supplying 5A each

Modules	Component Type	Value	QTY	Orderable Part Numbers	Description
LV-PMIC	IC	LP8764x-Q1	1	PLP8764xxxQ1	PMIC, 4 Bucks, 5A each or 20A 4-Phase, 10 GPIO, NVM Prgm Seqr, I2C Cntl, Safety Appls, 5.5x5mm, 0.5mm pitch, 32-pin VQFN, -40 to +125C (Temp Grade 1), AEC-Q100
PMIC External Components	Csys	0.47uF	1	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Cldo	2.2uF	1	GCM188R70J225KE22D	2.2uF, +/-10%, X7R, 6.3V, 0603, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Cvio	0.47uF	1	GCM155C71A474KE36D	0.47uF, +/-10%, X7S, 10V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Buck External Components	Ci	10uF	4	GCM21BR71A106KE22K	10uF, +/-10%, X7R, 10V, 0805, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Co	47uF	8	GCM32ER70J476KE19K	47uF, +/-10%, X7R, 6.3V, 1210, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	Lo	470nH	4	TFM252012ALMAR47MTAA	0.47uH, +/-20%, 24mohm, Is=5.8A, It=4.9A, 20V, 2520, -40 to +125C, AEC-200, Magntc Mtl Pwr Ind
Support Components Only			19		
Total Component Area (IC + Components)			20		

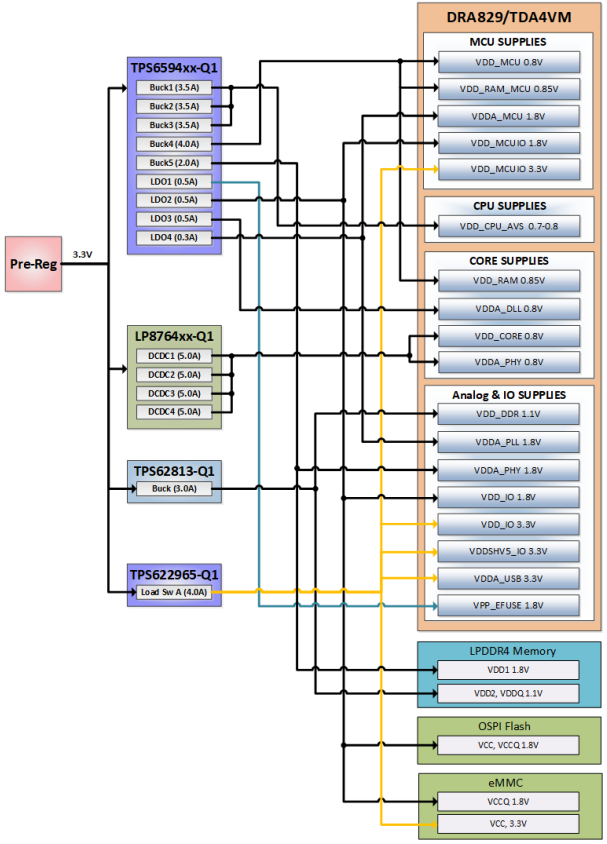
Note: Alternative Fsw = 4.4MHz is selectable based upon max load & efficiencies then L = 220nH (TFM252012ALMAR22MTAA) would be used, see LP8764x-Q1 data sheet for details.

TPS22965-Q1

Modules	Component Type	Value	QTY	Orderable Part Numbers	Description
Load Switch	IC	TPS22965	1	TPS22965-Q1DSG	IC, 5.5V, 4A, 16mohm Ron Load Switch with Quick Discharge, 2x2mm, 0.5mm pitch, 8-pin SON, -40 to +105C (Temp Grade 2), AEC-100
Input	Cin	1µF	1	GCM188R71C105KA64	1.0uF, +/-10%, X7R, 16V, 0603, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Support	Ct	220pF	1	GCM155R71H221KA37	220pF, +/-10%, X7R, 50V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Output	Co	0.1uF	1	GCM155R71C104KA55D	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Support Components Only			3		
Total Component Area (IC + Components)			4		

TPS62813-Q1

Modules	Component Type	Value	QTY	Orderable Part Numbers	Description
Buck Converter	IC	TPS62813-Q1	1	TPS6281320QWRWYRQ1	IC, 3A Buck Converter, 2.25MHz, Vin(2.75 - 6V), Vo Adj (0.6 - 5.5V), 3x2mm, 0.5mm pitch, 9-pin VQFN-HR (RWY) wettable flanks, -40 to +125C (Temp Grade 1), AEC-Q100
Input	Cin	22uF	1	GCM31CR71A226KE02L	22uF, +/-10%, X7R, 10V, 1206, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Support	Css &Cff	0.1uF	2	GCM155R71C104KA55D	0.1uF, +/-10%, X7R, 16V, 0402, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
Output	Cout	47uF	1	GCM32ER70J476KE19K	47uF, +/-10%, X7R, 6.3V, 1210, -55 to +125C, AEC-Q200, Multilayer Ceramic Cap
	L1	0.56uH	1	XEL3515-561ME	0.56uH, +/-20%, 24mohm, Is=4.5, It=6A, 80V, 3532, -40 to +125C, AEC-200, Shielded Pwr Ind
Support Components Only			4		
Total Component Area (IC + Components)			5		



PDN Design | Customer PDN questionnaire form

Jacinto7 SoC PDN Design Questionnaire (v0.9)**:**

11.) Please define key system feature requirements that can impact PDN system:

a.) Max clocking freq for all processors?
b.) Desired end product system Functional Safety level (i.e. ASIL-B, -C or -D)?
(See "FS Safety Questions" sheet for complete system assessment.)

c.) Any system low power modes needed (typical additional PDN requirements shown below)?

1 - MCU Only
a. Enables SoC low power mode with only MCU voltage domains & processor cores energized while all Main domains are disabled (Main power = OFF)
b. Enables internal MCU to act as system safety monitoring processor with independent voltage rails (Free From Interference, FFI) from all Main domains (rest of SoC).
(Impact: adds 2-4 independent power rails & 1 sustained control signal)

2 - GPIO Retention
a. Enables SoC very-low-power mode with only 1-2 low voltage (0.8V) wakeup logic domains & 1-2 dedicated GPIO domains energized while all other MCU & Main domains are de-energized, power = OFF
b. Enables typ 56 IO wakeup sources (e.g. 12-14CAN + 8-10UART + GPIOs) beyond the PMIC capability
c. Avoids reliability concerns & more expensive IO failsafe interfacing solutions
(Impacts: adds 2 independent power rails & 1 sustained control signal)

3 - DDR Retention (aka, Suspend-to-RAM = S2R)
a. Enables SoC ultra-low-power mode with only 3 DDR voltage (1.1V) domains energized while all other MCU & Main domains are de-energized, power = OFF
b. Enables quickest return to operational status
(Impacts:adds 1 independent power rail & 1 sustained control signal)

d.) Will High Security (HS) type SoCs be used & will customer need to program Efuses on-board in the field?
(Impacts: adds 1 independent power rail & 1 non-sustained control signal)

e.) What are targeted SDRAM memory type (LPDDR4 , LPDDR4X) and max data rate (4266, 3733, 3200, 2400) needed?

1 - Please list targeted PN & maximum load currents per SDRAM voltage domain.

f.) Is compliant, high-speed data SD Card operation needed or 3.3V fixed, low data rate acceptable?

g.) Is compliant USB 2.0 interface functionality needed for either end product or development?

1 - Is a compliant USB 2.0 data eye performance needed or low-cost, less robust USB 2.0 acceptable?

h.) Are all targeted Flash memory types & PNs known (i.e Octal SPI, eMMC, Hyper Flash, UFS, etc.)?

1 - Please list targeted PNs & maximum load currents per voltage domain.

i.) Are both 1.8V & 3.3V logic signal interfaces to SoC needed?

1 - If so, please list targeted 1.8V & 3.3V signal types (i.e. OSPI, RGMII, etc.).

j.) What is min power component ambient temp grade/range needed (i.e. Grade 2,-40 to +105C; Grade 1, -40 to +125C)?

- **Feature impacts by Q#s**
  - SoC clock & processing activity (Q8-11a)
    - Inc PDN peak power primarily on CPU & CORE domains
    - Needs multi-phase bucks can lead to more power comps
  - Functional safety requirements (Q11b)
    - ASIL-B needs voltage monitoring all rails, watchdog timer, MCU reset & error monitoring, independent I2C & error indicator
    - ASIL-D needs ASIL-B plus current monitoring, SoC reset & error monitoring
    - External functions beyond (Leo PMIC) plus 4 control signals
  - Low power modes need independent power rails & control signals (Q11c):
    - MCU Only = 2-4 power rails & 1 sustained control
    - GPIO Ret = 2 power rails & 1 sustained control
    - DDR Ret = 1 power rail & 1 sustained control
  - HS SoC with in-field, on-board key updates need:
    - Efuse Prgm = 1 power rail & 1 non-sustained control

PDN Design | System safety impacts

Functional Safety Questionnaire (v0.2):

1. What is your system functional safety concept?
   Please explain the high level data movement in the system.
   What data is deemed to be safety critical?
   Where are safety related decisions are being made (i.e. "ABC" "IC device in "XYZ" processor, etc.).
2. What are your system safety goals?
3. What are the safe states of your system? Do you consider the J7 device powered off as a safe state?
4. What safety requirements will be relevant to the J7 device?
5. Will you be using the J7 SoC's MCU as a safety monitor for the Main domain or the system?
   If so, do you need independence to enable Freedom From Interference (FFI) requirements between different domains?
6. Do you have any independence/Freedom From Interference (FFI) requirements between the two J7 devices in the system?

- Summary ASIL-B system requirements:
  1. A safety monitoring processor independent from SoC
  2. OV monitoring & protection on SoC system's input voltage
  3. OV & UV monitoring on all "safety critical" SoC power rails
  4. Watchdog (WD) monitoring of safety processor
  5. Independent WD comm channel with interrupt to safety proc
  6. Safety processor error monitoring & reset capabilities
  7. Error indicator signal for external safety critical systems
- Additional system requirements for ASIL-C & D:
  (Same as ASIL-B plus items below)
  8. Over current monitoring on all "safety critical" SoC power rails
  9. SoC Main processor error monitoring & reset capabilities

- **Potential Functional Safety Impacts**
  1. SoC's MCU is not system safety processor:
     - Combined MCU & Main voltage domains
       - No **MCU Only** low power mode
       - Simplest & lowest PDN cost
     - Independent MCU & Main voltage domains
       - Enables **MCU Only** low power mode
       - Adds 2-4 power rails & increases PDN cost
  2. SoC's MCU is system safety processor:
     - **Extended Safety Processor** across MCU & Main
       - Combined MCU & Main voltage domains
       - No Power Rail FFI isolation
     - **MCU Island**
       - Independent MCU & Main voltage domains
       - Power Rail FFI isolation

"Safety Critical" power rails supply SoC voltage domains that could cause severe system failures. This classification depends on customer's use case and SoC resources related to system safety concept.

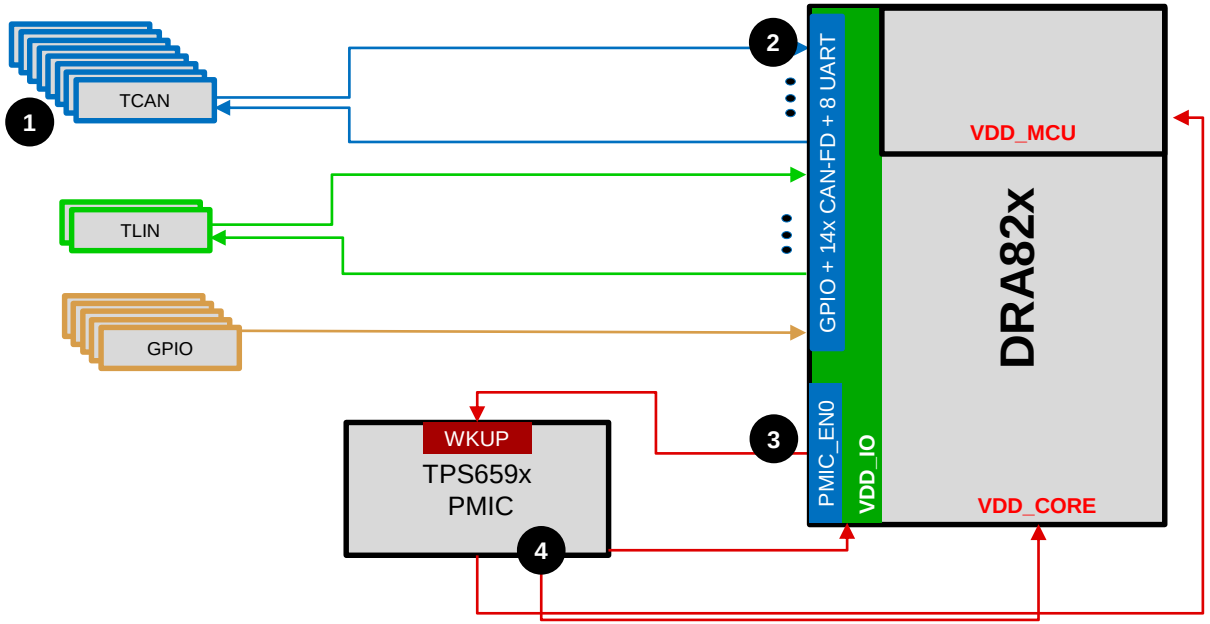
PDN Design | SoC low power modes

Modes	Reasons	Impacts
MCU Only	1. Enables SoC low power mode with only MCU voltage domains & processor cores energized while all Main domains are disabled (Main power = OFF) 2. Enables internal MCU to perform basic processing while remaining SoC resources are disabled to reduce power dissipation	a. Increases sustained PMIC control signals by 1 b. Increases power resources & isolated power rails by 2-4 depending upon IO signaling levels (1.8V only or 1.8 & 3.3V IO) c. Lowest SoC power dissipation state possible
GPIO Retention	1. Enables SoC very-low-power mode with only 1-2 low voltage (0.8V) wakeup logic domains & 1-2 dedicated GPIO domains energized while all other MCU & Main domains are de-energized, power = OFF 2. Enables typ 56 IO wakeup sources (e.g. 12-14CAN + 8-10UART + GPIOs) beyond the PMIC capability 3. Avoids reliability concerns & more expensive IO failsafe interfacing solutions	a. Increases sustained PMIC control signals by 1 b. Increases power resources & isolated power rails by 2 c. Lowest SoC power dissipation state possible
DDR Retention (Suspend-2-RAM, S2R)	1. Enables SoC ultra-low-power mode with only 3 DDR voltage (1.1V) domains energized while all other MCU & Main domains are de-energized, power = OFF 2. Enables quickest return to operational status	a. Increases sustained PMIC control signals by 1 b. Increases power resources & isolated power rails by 1 c. Lowest SoC power dissipation state possible

Jacinto 7 SoC Internal GPIO Retention & Wake-up

- Main Domain: OFF, MCU Domain: OFF, I/O Domain: ON (<200 uA)
- Any CAN/LIN transceiver can be used (no wakeup-pin required)

I/O: ON	MCU: OFF	MAIN: OFF

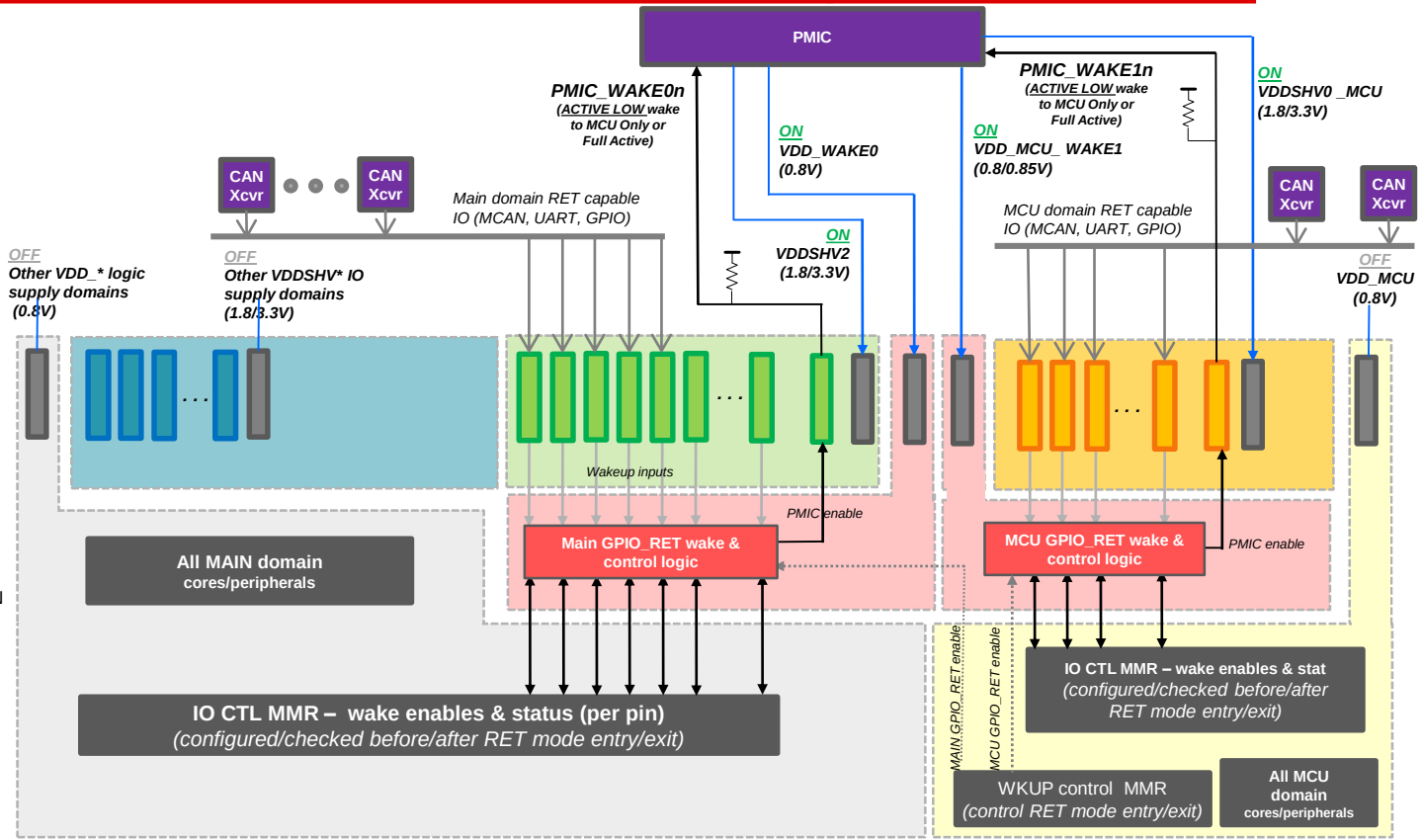


1. Wakeup Event
2. Senses edge on daisy chained I/O
3. Latch logic in I/O domain drives PMIC_EN0
4. PMIC ramps and powers up SoC + get trigger source from internal aggregator

Jacinto7 SoC Main & MCU GPIO Retention Operational Modes

- Main GPIO Retention mode
  - VDD_WAKE0 = ON
  - VDDSHV2 = ON
  - All other MAIN supplies = OFF
  - *Any VDDSHV2 IO signal edge → PMIC_WAKE0 set active (low) → PMIC to exit GPIO_RET → either*
    *1) Full Active operation when PMIC_WAKE0 = GPIOx = WKUP1**
    *2) MCU Only operation when PMIC_WAKE0 = GPIOx = WKUP2**
- MCU GPIO Retention mode
  - VDD_MCU_WAKE1 = ON
  - VDDSVH0_MCU = ON
  - All other MCU supplies = OFF
  - *Any VDDSHV0_MCU IO signal edge → PMIC_WAKE1 set active (low) → PMIC to exit GPIO_RET → either*
    *1) Full Active operation when PMIC_WAKE1 = GPIOx = WKUP1**
    *2) MCU Only operation when PMIC_WAKE1 = GPIOx = WKUP2**
- Combined Main & MCU GPIO Ret mode
  - VDD_WAKE0 & VDD_MCU_WAKE1 = ON
  - VDDSHV2 & VDDSVH0_MCU = ON
  - All other Main & MCU supplies = OFF
  - *Any VDDSHV0_MCU IO signal edge → PMIC_WAKE0/1 set active (low) → PMIC to exit GPIO_RET → either*
    *1) Full Active operation when PMIC_WAKE0/1 = GPIOx = WKUP1**
    *2) MCU Only operation when PMIC_WAKE0/1 = GPIOx = WKUP2**

*Note: * PMIC's PN/NVM settings determines whether GPIOx = WKUP1 or WKUP2 function.*



NOTE: System must be in safety state during wakeup, no safety function is executing. If VDD_WAKE* power rail glitch corrupts wakeup logic, must rely on PMIC watchdog to recover SoC, no local POR/Monitor.

GPIO Retention Wakeup Capable IOs

Device	MCU GPIO Retention wakeup capable pins	MAIN GPIO Retention wakeup capable pins
J7ES	Not supported	Not supported
J7VCL	Up to 33	Up to 49
J7AEP	Up to 31	Up to 49
J7AHP	Up to 31	Up to 49

TPS6594-Q1 and LP8764-Q1 Functional Safety Capability

Systematic

- Developed according SafeTI™ Development Process with TÜV SÜD certification for ISO26262 ASIL-D target

CERTIFICATE

No. Q4B 088989 0009 Rev. 00

Holder of Certificate: Texas Instruments Inc.
12500 TI Boulevard
Dallas TX 75243-4136
USA

Factory(ies): Texas Instruments Inc.
12500 TI Boulevard, Dallas TX 75243-4136, USA

Certification Mark:

Scope of Certificate: SafeTI™ Functional Safety Hardware

Applied Standard(s): IEC 61508-1:2010
IEC 61508-2:2010
ISO 26262-2:2018
ISO 26262-5:2018
ISO 26262-7:2018
ISO 26262-8:2018
ISO 26262-9:2018

The Certification Body of TÜV SÜD Product Service GmbH certifies that the company mentioned above has established and is maintaining a management system which meets the requirements of the listed standards. The results are documented in a report. See also notes overleaf.

Report No.: TD94012C
Valid until: 2022-06-13

Date, 2019-06-14 (Christian Ormeier)

Page 1 of 1
TÜV SÜD Product Service GmbH • Certification Body • Ridlerstraße 65 • 80339 Munich • Germany

ZERTIFIKAT ◆ CERTIFICATE ◆ 認證證書 ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

Hardware Metrics

- **> 99% Single-Point Metric** and **>90% Latent-Fault Metrics**
- Accurate and fast Output Voltage Monitoring
- Accurate and fast Input Voltage Monitoring
- Fast Over-Voltage Protection
- Q&A Watchdog
- Error Signal Monitors
- CRC on Communication Interfaces and SPMI bus
- CRC on Configuration Registers
- CRC on internal memory
- Built-In Self-Tests on Voltage Monitors, State Machine, SPMI Bus, Watchdog and Error Signal Monitors

Supporting tools and documents

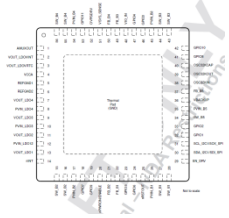
- FMEDA
- Safety Manual
- Functional Safety Analysis Report:
  - DFMEA
  - pin-FMEA
  - FTA & DFA
- Technical Reference Manual(s) for Powering **Jacinto™ 7** with TPS6594x / LP8764x PMICs
- **SDK for Jacinto™ 7**

TPS6594x-Q1(Leo) | Integrated Power Management IC for processors

Development

Features:

- 5 Buck converters with Vin: 2.7V – 5.5V. Vout: 0.3 V – 3.4V, 5mV/10 mV steps:
  - **4x 3.5A per phase (BUCK4 single-phase with 4A).** Multiphase capable.
  - **BUCK5** low-power Buck with 2A capability.
  - All with AVS and soft-start to limit in-rush current.
- 3 LDO/LSW: 500mA load current per LDO, all with bypass capability. Vin: 1.2V - 5.5V. Vout: 0.4V - 3.3V, 25mV steps
- 1 LowNoise LDO: 300mA load current. Vin: 2.2V – 5.5V, Vout: 1.2V – 3.3V, 25mV steps
- **>2MHz F_{SW} with external clock sync capability; internal fallback 2.2MHz or 4.4MHz F_{SW} with output buffer, with Integrated spread spectrum modulation**
- **NVM configurable sequencing with self-check and safe power up/down**
- **Suspend-to-RAM mode with <0.4mA Iq and low-power mode with <15uA Iq**
- Integrated sequence control and interface+GPIOs, **Q&A WDT,** and **2x Error Signal Monitors,** each with a configurable error handling (for SoC vs. MCU errors)
- **Input voltage monitor with OVP and UVLO; output voltage monitor with under or window Power-Good indicator; output current limit and OCP**
- **External voltage monitor input for unused LDOs**
- **32kHz Crystal Oscillator and RTC with fast start**
- Thermal monitoring, warning & shut down
- Supports I2C (3.4MHz) or SPI compatible interfaces
- **125˚C Ambient and 150˚C Junction, AEC-Q100 Grade 1**



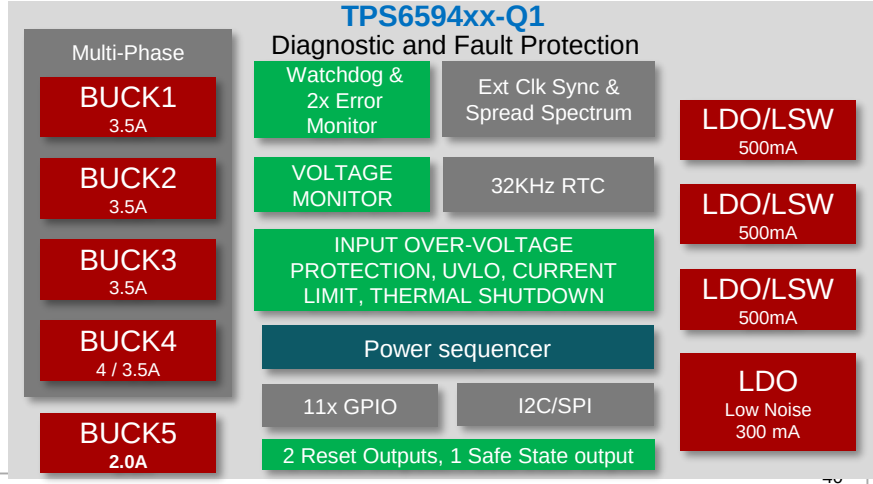
56-pin 8x8mm² WF-QFN package with 0.5mm pitch

Applications:

- Processor power supply for infotainment systems, surround view, ADAS, sensor fusion systems, industrial and automation, personal electronics

Benefits:

- **Supply flexibility, excellent load-step performance, fully integrated w/minimal external components and glue logic. Seamless attach to all variants of J7 processors**
- **Agnostic for any kind of Pre-Regulator**
- **Configurable detection & handling of safety-critical errors**
- **Minimal EMI**
- **Lower board costs / simple design, low ψ JB → good thermal performance**
- **Enables low-power system sleep with fast wake-up response**
- **Safe-TI process . Target ASIL-D / SIL-3 for functional safety systems**



LP8764x-Q1(Hera) | Independent or companion PMIC

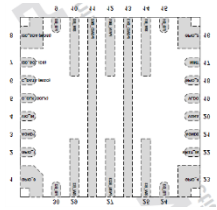
Development

Features:

- 4 Buck converters: Multiphase capable (20A, 15A+5A, 10A+10A, 10A+5A+5A, 5A+5A+5A+5A)
- 5A per phase, 20A (4-phase, VIN > 2.5V)
- V_{IN} 2.7 V – 5.5 V
- V_{OUT} 0.3 V – 3.3V, 5mV/10 mV steps.
- Dynamic Voltage Scaling with programmable slew-rate 5-30mV/us.
- Differential Output voltage sensing in multiphase mode
- Selectable **2.2MHz or 4.4MHz F_{SW}** with spread spectrum and PWM Dithering for EMI Reduction
- Low IQ/PFM + PWM auto mode change, forced PWM mode, forced MP mode.
- Automatic phase adding and shedding according to load current
- 10 GPIOs with programmable functions, including power button & VMON function for external rails, watchdog / error signal, reset and safe-state outputs
- **NVM configurable sequencing with self-check and safe power up/down**
- **Q&A WDT** and **Error Signal Monitor**
- **2 external Voltage Monitor inputs**
- Supports I2C (3.4MHz) or SPI compatible interfaces
- **125˚C Ambient and 150˚C Junction, AEC-Q100 Grade 1.**

Applications:

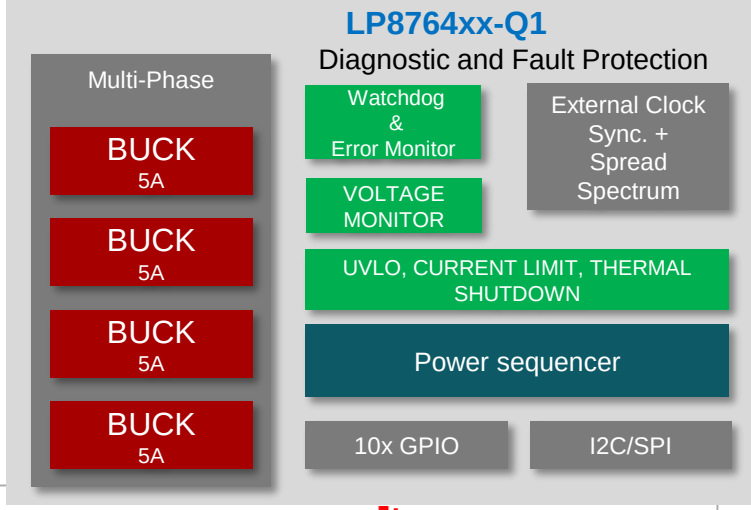
- Processor power supply for infotainment systems, surround view, ADAS, sensor fusion systems, industrial & automation



30-pin 5x5mm² VQFN package with 0.5mm pitch

Benefits:

- **Supply flexibility, excellent load-step performance, fully integrated w/minimal external components and glue logic. Seamless attach to all variants of J7 processors together with TPS6594-Q1**
- **Configurable detection and handling of safety-critical errors**
- **Minimal EMI**
- **Lower board costs / simple design, low ψ JB → good thermal performance**
- **Enables low-power system sleep with fast wake-up response**
- **Safe-TI process. Target ASIL-D / SIL-3 for functional safety systems**



TPS6287x-Q1 – 6A, 9A, 12A, 15A Automotive Buck Converter

Samples Now
RTM 2Q22

FEATURES

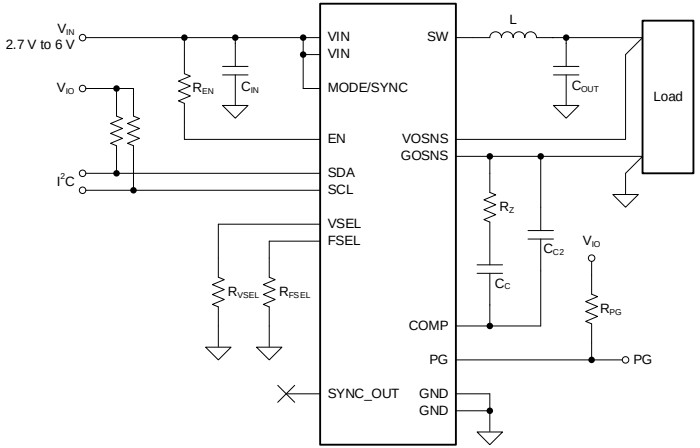
- AEC-Q100-qualified (temperature grade 1, T_A = –40 °C to 125 °C)
- Functional safety capable
- Input voltage: 2.7V to 6V
- Output voltage: 0.4V to 3.35V ±1% (programmable)
- Output current: 6A, 9A, 12A,15A (device-specific)
- Differential remote sensing
- I^2C-compatible interface: up to 1 MHz
- Switching frequency: 1.5 MHz, 2.25 MHz, 2.5 MHz, 3 MHz
- Spread-spectrum clocking capable
- Short-circuit protection, thermal shutdown
- Stackable
- 16-Pin, 2.55-mm × 3.55-mm WQFN package with wettable flanks

APPLICATIONS

- Infotainment and cluster, ADAS
- FPGA, SoC, processor core supply
- DDR memory supply
- Optical networks

BENEFITS

- Tight output voltage regulation
- Fast transient response
- Can be stacked to increase output current capability and/or reduce device power dissipation
- High power density
- Output current capability from 6 A to 15A in pin-to-pin compatible packages



TPS62811/812/813/810-Q1 (Orbea) | Discrete power

1A/2A/3A/4A high efficiency Buck converter for Automotive

Features

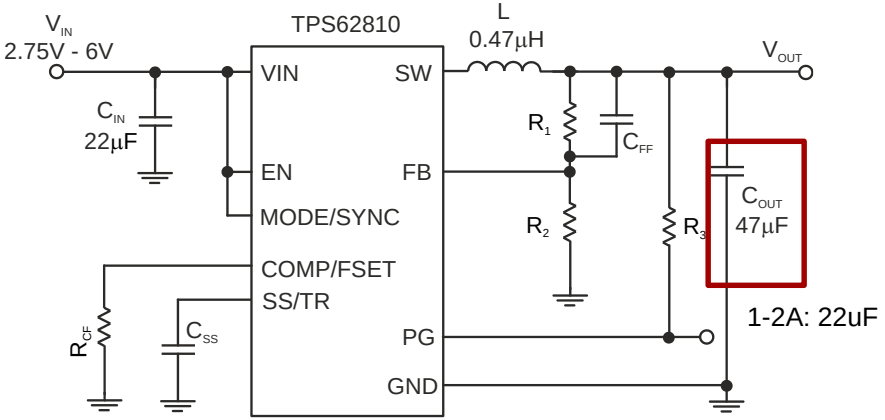
- 2.75V to 6V input voltage range
- Adjustable output voltage from 0.6V to Vin
- **-40ºC to 150ºC operating junction temperature range**
- **HotRod™ QFN 3.0x2.0mm with wettable flanks**
- 1% output voltage accuracy
- 15uA Quiescent current
- **Fixed frequency operation**, per default at 2.25MHz
- Adjustable switching frequency and compensation
- **Forced PWM and external synchronization (1.8 – 4MHz)**
- SS/TR provides **adjustable soft-start and tracking** capability
- Output discharge for defined ramp-down of Vout
- **Spread Spectrum Clocking** for decreased noise (optional)

Applications

- Infotainment: Head Unit, Telematics Control Unit, Cluster
- Body Electronics: Body Control Module, Gateway
- ADAS: Camera System ECU, Sensor Fusion

Benefits

- **Small solution size with minimal external components**
- Fixed frequency, external sync and Spread Spectrum Clocking **facilitates design for low EMI**
- Short min on-time of 50ns allows **direct conversion of 5V to 1V at f>2MHz**
- **Allows wide range of output capacitance** to meet requirements for input of FPGAs or MCUs



Automotive Reference Designs: PMP21669, PMP22063, PMP30670

Texas Instruments

Greenland (TPS389006)

Samples: June 2021
RTM: 2Q2022

6 Channel window Reset IC, High Accuracy, I2C Interface, AEC-Q100,ASIL-D

Key Features

Operating Voltage 2V to 5.5V
ASIL D compliant
Iq target is <350µA
6 channel Supervisor including 2 Remote sense
Interrupt and Sleep function
Sequence logging and rail tagging with SYNC pin (multiple parts)

6 Channel Window Supervisor
High threshold accuracy: 0.5% over temp range
Threshold tolerance (trip point from nominal rail): 5mV steps
Hysteresis: 10mV to 60mV

I2C features
- Program threshold level (0.2V to 5.5V)
- Logging capability
  - -Threshold excursion event flag
  - -Type of excursion (OV/UV)
  - -Channel number and Monitored sequence up and down log
- Address selection

Voltage Detector
- Analog window voltage comparators (OV&UV <100ns)
- Oscillation detect with ultra fast comparator (<100ns)
- Voltage drift detect with ADC
- Programmable Low Pass Filter

Applications

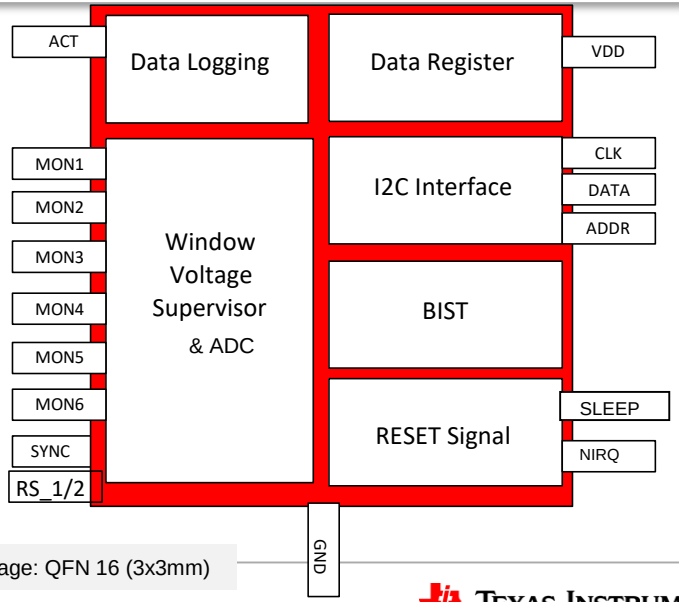
Automotive and industrial ECU and GPU safety voltage rail monitoring

Benefits

Flexible and programmable voltage rail monitoring capabilities minimize system design effort to meet ASIL requirements.

High threshold accuracy and dynamic threshold scaling capability provides a precise monitoring to the critical dynamic voltage scaling processor core rails

Save board space with 6-window channels in small 3x3mm package



RTE Package: QFN 16 (3x3mm)

Texas Instruments