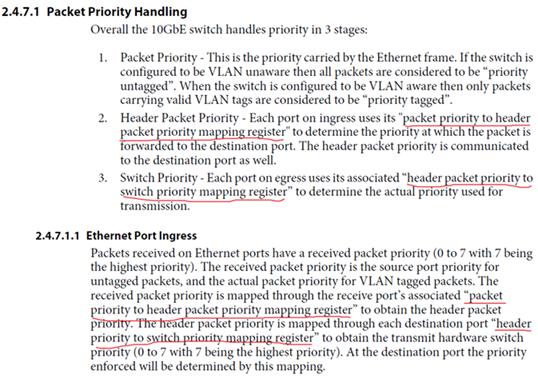
**There are some questions about KeyStone II 10 Gigabit Ethernet(3-port) itself QoS capabilities, list as blow:**

1. **Packet strict priority scheduling**

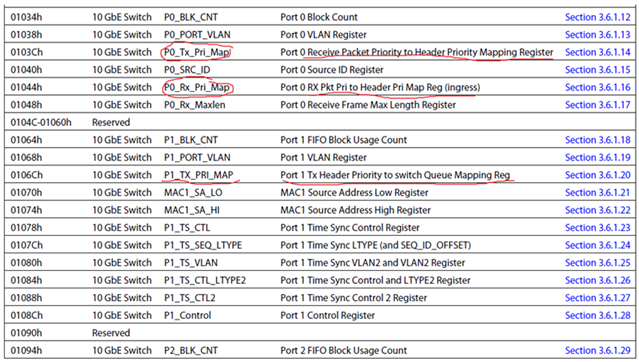
From "KeyStone II Architecture 10 Gigabit Ethernet Subsystem User Guide.pdf", there are description about packet priority handling for this 10G switch:



Basically, **there are two level registers for priority mapping per each port:**

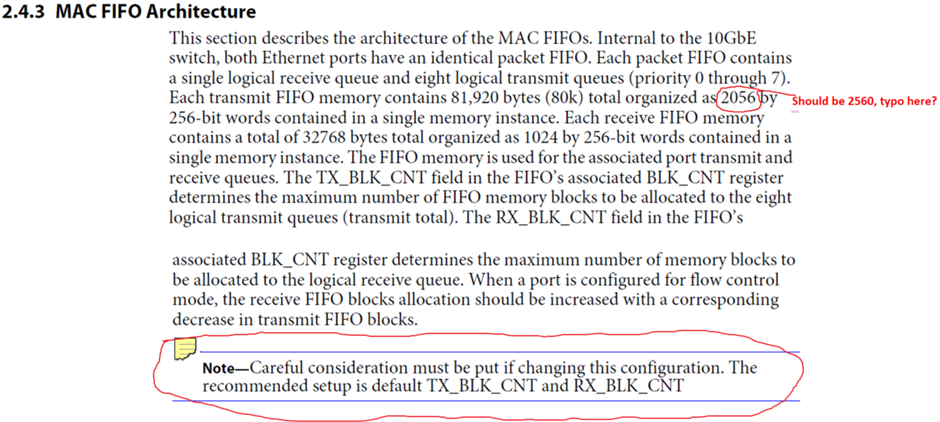
1. packet priority to header packet priority mapping register
2. header priority to switch priority mapping register

But from register list, such two registers only available for P0(host port), for other two ethernet ports(P1&P2), there is only one register (TX\_PRI\_MAP):



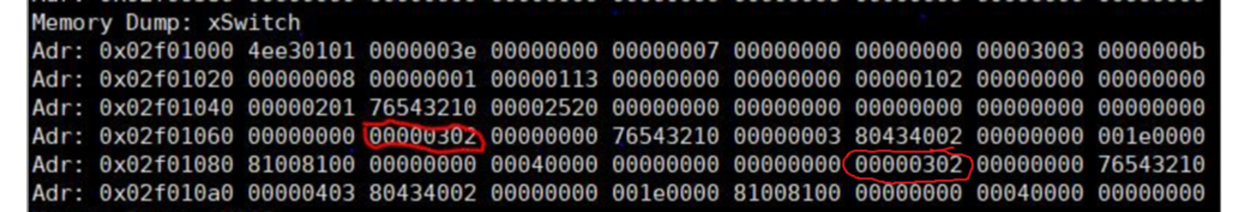
Some questions are:

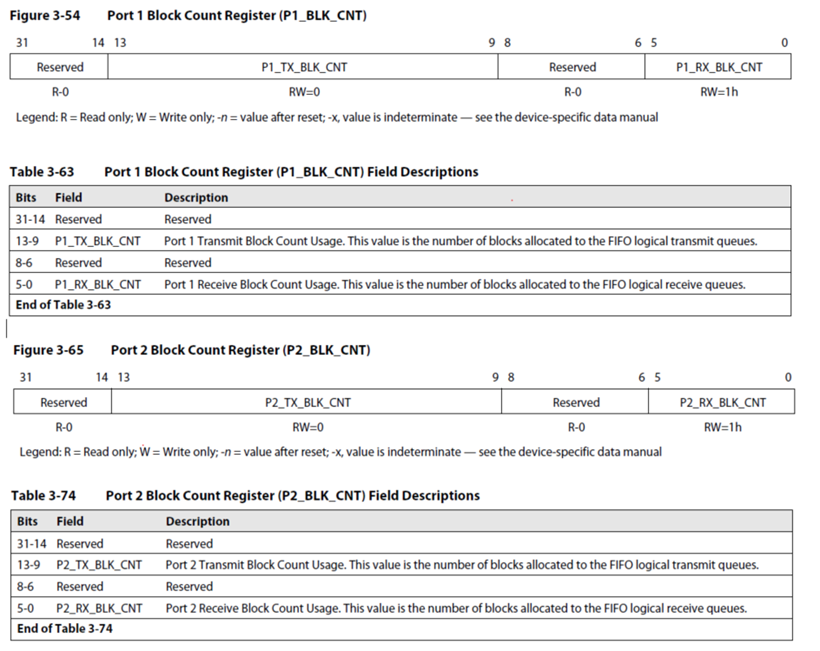
1. Why missing another (RX\_PRI\_MAP) for P1&P2?
2. Do these two Ethernet ports(P1&P2) support packet priority handling?
3. What’s packet priority handling algorism? Does it mean strict priority scheduling？
4. **Queue size per priority**



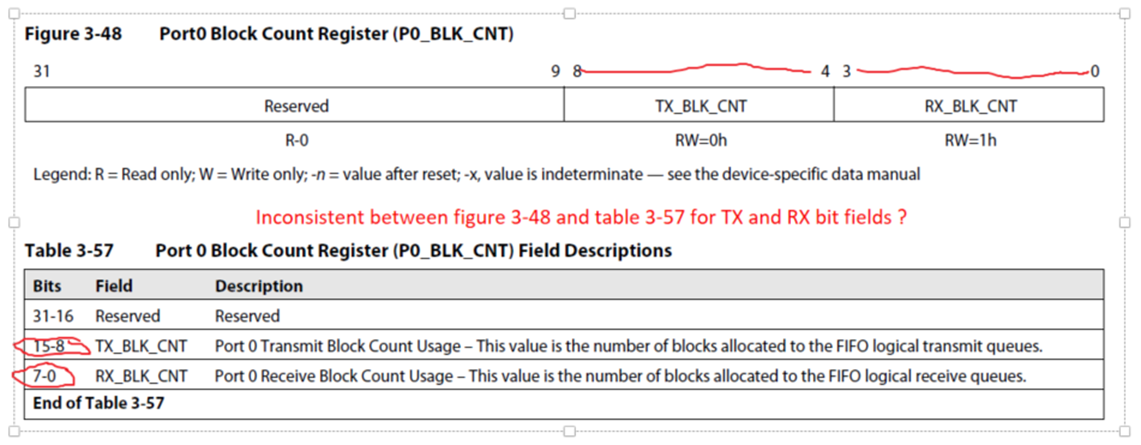
Based on above statement, my understanding **this switch doesn’t support queue size per priority**, but can change TX\_BLK\_CNT field to limit the maximum queue size for all eight priority in total.

**From register dump:**





Both two ports(1&2) value are 0x00000302, the strange thing is the **bits field definition is very weird, RX\_BLK\_CNT has 6bits while TX\_BLK\_CNT has 5bits**, my understanding is both should have 8bits so that can provide range 0-255 for count setting which should similar as port 0 definition:



But port0 still has inconsistent definition, check above tagged red color part.

Some questions are:

1. Since TX\_BLK\_CNT bit fields are BIT9-BIT13, and from register memory dump, the value is 0x00000302, then it looks both P1&P2 TX\_BLK\_CNT are set to “1”:
   1. What’s the memory block size?
   2. The number of memory blocks is “1”, what’s the amount of memory represent for?
   3. Are BIT9-BIT13 correct for TX\_BLK\_CNT bit fields