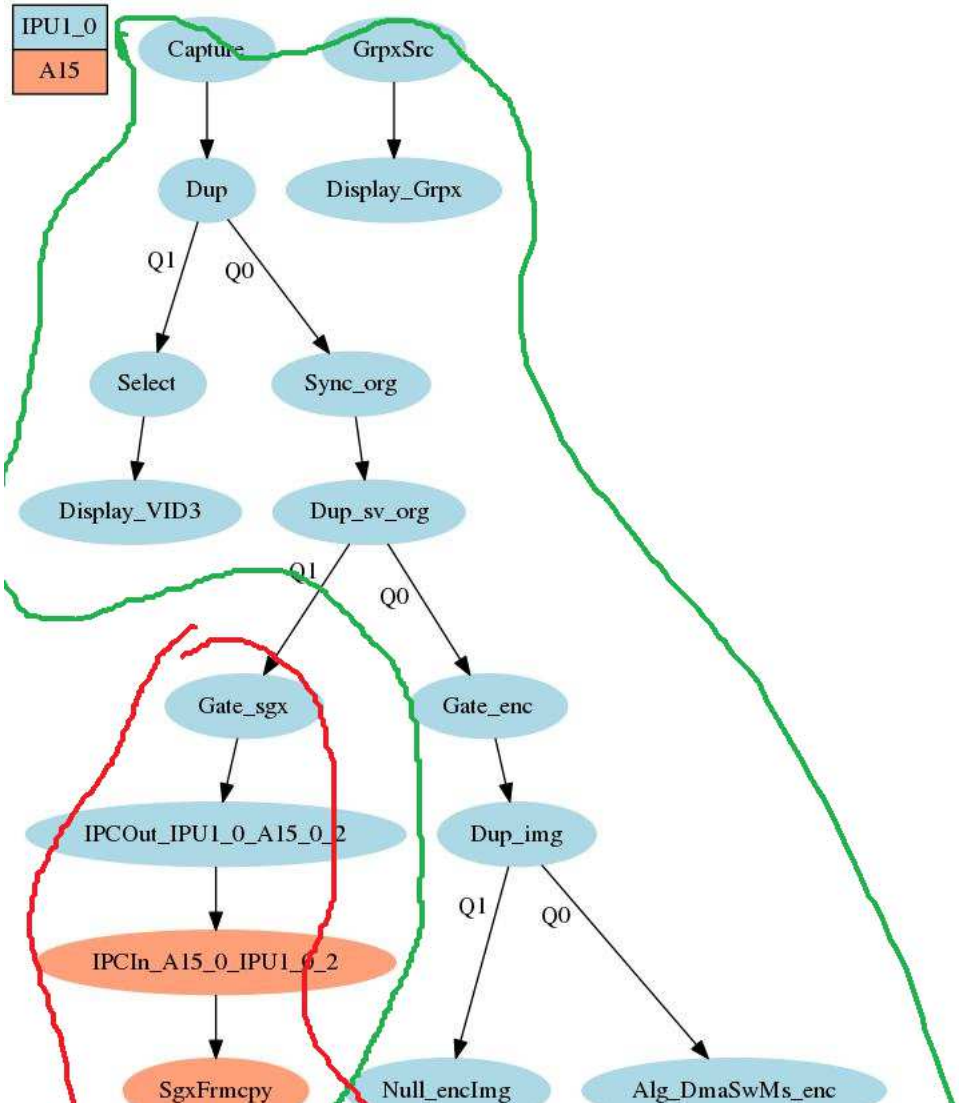
LCD flick issue

test chain picture

- Green links：Original 4 way 720p video capture Dispplay_VID3，TI log overlay display links Display_Grpx，DMA combine 4 ways 1280x720 image, encode to H.264 video and drop it.
- Red links：gpu renderer SRV video，then display it at Dispplay_VID2 layer；
- Yellow links：From the combined 4 ways 2560*1440 crop the display video，then display it at Dispplay_VID1 layer；


IPU1_0
A15
Capture
GrpxSrc
Dup
Display_Grpx
Q1
Q0
Select
Sync_org
Display_VID3
Dup_sv_org
Q1
Q0
Gate_sgx
Gate_enc
IPCOut_IPU1_0_A15_0_2
Dup_img
Q1
Q0
IPCIn_A15_0_IPU1_0_2
SgxFrmcpy
Null_encImg
Alg_DmaSwMs_enc

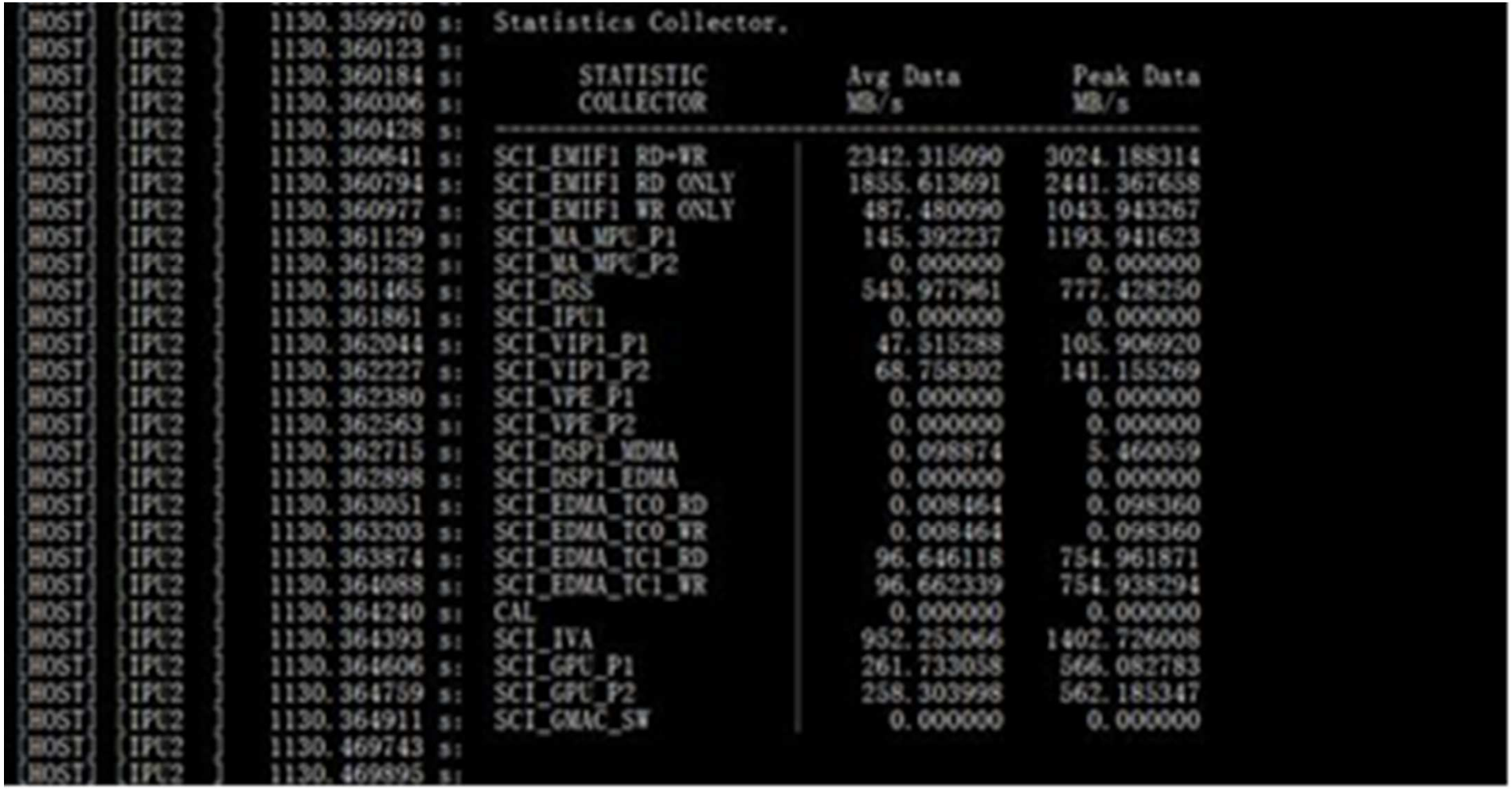
Test method.

- Case 1: First run Green links (Display is OK)
  after 5 seconds run Yellows link.
  (Display OK)
  After 10 seconds run red links
  (Display flick)
  Attached video1 is test result record video.

Test method

- Case 2:First run Green links (Display is OK)
  after 5 seconds run Red link.
  (Display OK)
  After 10 seconds run Yellow links
  (Display flick)
  Attached video1 is test result record video.

Two case DDR bandwidth

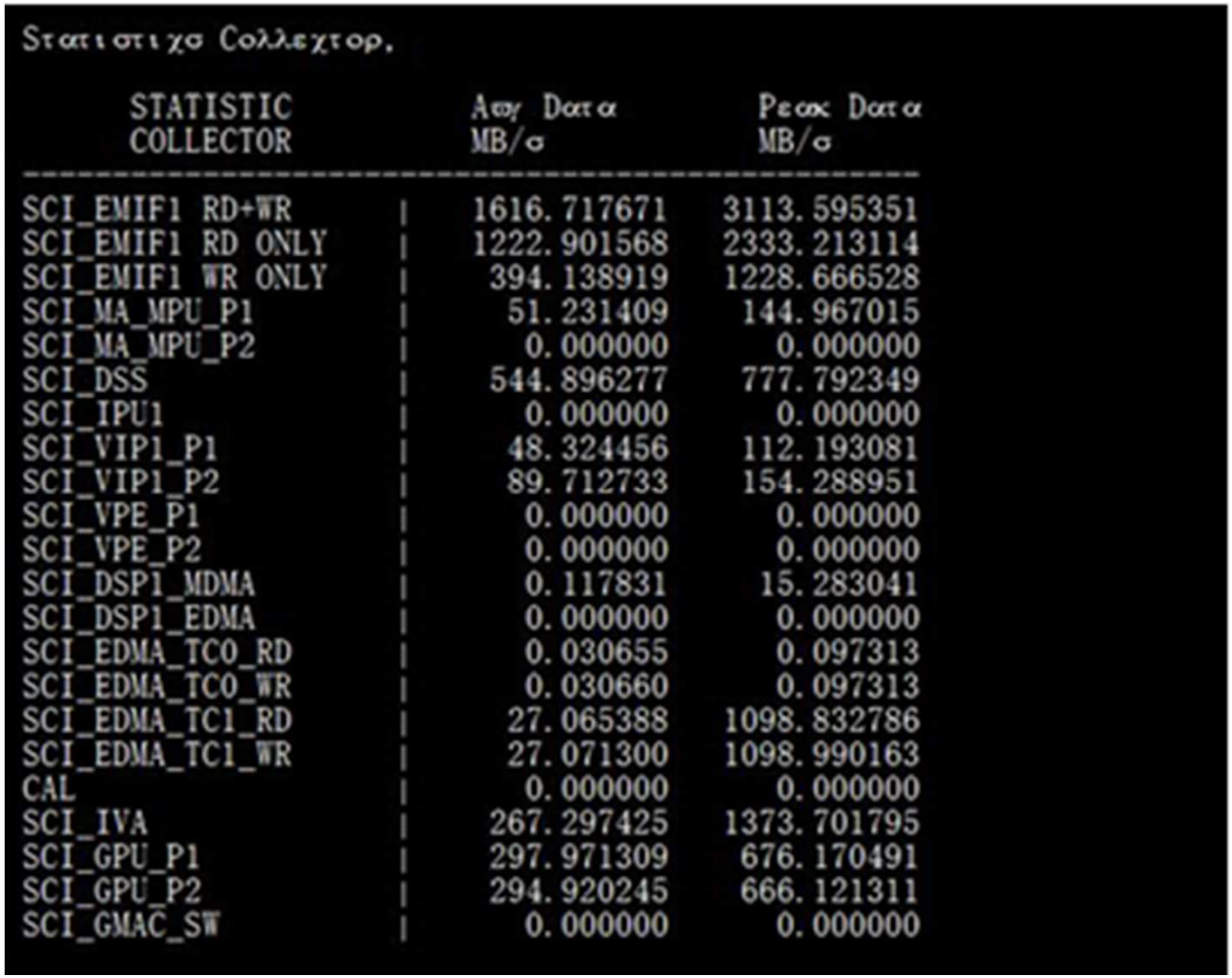


```
[HOST] [IPU2] 1130.359970 s: Statistics Collector.
[HOST] [IPU2] 1130.360123 s:
[HOST] [IPU2] 1130.360184 s:      STATISTIC          Avg Data        Peak Data
[HOST] [IPU2] 1130.360306 s:      COLLECTOR          MB/s            MB/s
[HOST] [IPU2] 1130.360428 s:  ------------------------------------------------
[HOST] [IPU2] 1130.360641 s:  SCI_EMIF1 RD+WR      2342.315090     3024.188314
[HOST] [IPU2] 1130.360794 s:  SCI_EMIF1 RD ONLY    1855.613691     2441.367658
[HOST] [IPU2] 1130.360977 s:  SCI_EMIF1 WR ONLY     487.480090     1043.943267
[HOST] [IPU2] 1130.361129 s:  SCI_MA_MPU_P1         145.392237     1193.941623
[HOST] [IPU2] 1130.361282 s:  SCI_MA_MPU_P2           0.000000        0.000000
[HOST] [IPU2] 1130.361465 s:  SCI_DSS               543.977961      777.428250
[HOST] [IPU2] 1130.361861 s:  SCI_IPU1                0.000000        0.000000
[HOST] [IPU2] 1130.362044 s:  SCI_VIP1_P1            47.515288      105.906920
[HOST] [IPU2] 1130.362227 s:  SCI_VIP1_P2            68.758302      141.155269
[HOST] [IPU2] 1130.362380 s:  SCI_VPE_P1              0.000000        0.000000
[HOST] [IPU2] 1130.362563 s:  SCI_VPE_P2              0.000000        0.000000
[HOST] [IPU2] 1130.362715 s:  SCI_DSP1_MDMA           0.098874        5.460059
[HOST] [IPU2] 1130.362898 s:  SCI_DSP1_EDMA           0.000000        0.000000
[HOST] [IPU2] 1130.363051 s:  SCI_EDMA_TC0_RD         0.008464        0.098360
[HOST] [IPU2] 1130.363203 s:  SCI_EDMA_TC0_WR         0.008464        0.098360
[HOST] [IPU2] 1130.363874 s:  SCI_EDMA_TC1_RD        96.646118      754.961871
[HOST] [IPU2] 1130.364088 s:  SCI_EDMA_TC1_WR        96.662339      754.938294
[HOST] [IPU2] 1130.364240 s:  CAL                     0.000000        0.000000
[HOST] [IPU2] 1130.364393 s:  SCI_IVA               952.253066     1402.726008
[HOST] [IPU2] 1130.364606 s:  SCI_GPU_P1            261.733058      566.082783
[HOST] [IPU2] 1130.364759 s:  SCI_GPU_P2            258.303998      562.185347
[HOST] [IPU2] 1130.364911 s:  SCI_GMAC_SW             0.000000        0.000000
[HOST] [IPU2] 1130.469743 s:
[HOST] [IPU2] 1130.469895 s:
```

Debug method

- At Alg_FrameCopy_enc module，add usleep at every frame crop process，those enalbe Red/Yellow/Green all 3 function. LCD display is OK. Like record video3 . You can find at the video，left side video frame rate is low about 6~7 FPS. Other frame is normally about 25 FPS.

Add delay DDR bandwidth reduced



Στατιστιχσ Χολλεχτορ.

STATISTIC COLLECTOR	Αϖγ Δατα MB/σ	Ρεακ Δατα MB/σ
SCI_EMIF1 RD+WR	1616.717671	3113.595351
SCI_EMIF1 RD ONLY	1222.901568	2333.213114
SCI_EMIF1 WR ONLY	394.138919	1228.666528
SCI_MA_MPU_P1	51.231409	144.967015
SCI_MA_MPU_P2	0.000000	0.000000
SCI_DSS	544.896277	777.792349
SCI_IPU1	0.000000	0.000000
SCI_VIP1_P1	48.324456	112.193081
SCI_VIP1_P2	89.712733	154.288951
SCI_VPE_P1	0.000000	0.000000
SCI_VPE_P2	0.000000	0.000000
SCI_DSP1_MDMA	0.117831	15.283041
SCI_DSP1_EDMA	0.000000	0.000000
SCI_EDMA_TC0_RD	0.030655	0.097313
SCI_EDMA_TC0_WR	0.030660	0.097313
SCI_EDMA_TC1_RD	27.065388	1098.832786
SCI_EDMA_TC1_WR	27.071300	1098.990163
CAL	0.000000	0.000000
SCI_IVA	267.297425	1373.701795
SCI_GPU_P1	297.971309	676.170491
SCI_GPU_P2	294.920245	666.121311
SCI_GMAC_SW	0.000000	0.000000

Debug method

- Change Alg_DmaSwMs_enc module，down resize video to 1280x720 resolution，Then run encoder. IVA used DDR bandwidth will reduce to small. At this user case yellow links' display is not full size.（This is right result, you can forget those abnormally display），The LCD display remain have flick issue, but flick frequency reduced，You can find it video4.

Reduce encode video size DDR BW

Statistics Collector,

STATISTIC COLLECTOR	Avg Data MB/s	Peak Data MB/s
SCI_EMIF1 RD+WR	1492.745777	2251.638129
SCI_EMIF1 RD ONLY	1081.333776	1823.863995
SCI_EMIF1 WR ONLY	411.702558	611.726468
SCI_MA_MPU_P1	61.974396	314.155218
SCI_MA_MPU_P2	0.000000	0.000000
SCI_DSS	545.074465	776.677529
SCI_IPU1	0.000000	0.000000
SCI_VIP1_P1	44.753875	86.518992
SCI_VIP1_P2	93.234750	154.053097
SCI_VPE_P1	0.000000	0.000000
SCI_VPE_P2	0.000000	0.000000
SCI_DSP1_MDMA	0.119838	17.288012
SCI_DSP1_EDMA	0.000000	0.000000
SCI_EDMA_TC0_RD	0.023875	0.096336
SCI_EDMA_TC0_WR	0.023878	0.096336
SCI_EDMA_TC1_RD	34.539877	292.385786
SCI_EDMA_TC1_WR	34.539877	292.385786
CAL	0.000000	0.000000
SCI_IVA	128.814535	688.968225
SCI_GPU_P1	297.231960	675.168141
SCI_GPU_P2	294.290183	666.905872
SCI_GMAC_SW	0.000000	0.000000

Debug method

- Reduce LCD FPS number, the flick will disappear.

summary

- Enable all customer SRV + CBB chains function， LCD display have flick issue. The FPS higher, the flick frequency will increase.
- Just verify Chains single function， every function display is OK；
- Through debug test we think when DDR occupy change low, the LCD flick will disappear.
- At slice 7 debug method. Through add usleep at A15 side， reduce A15 access memory speed， The LCD did not flick. Because A15 have special BUS directly access DDR, did not through L3 bus. We think high probability is A15 conflict with DSS module occupy DDR3 bandwith；

A15 directly access DDR3

Figure 14-1. Interconnec