HyperLynx®

DDR Simulation Report - LPDDR4_Controller40odt_ODT60_VOH25_Read_Rerun

Data Read

Data Read Worstcases

- To investigate any result further, click on the link in the cell to open the waveforms. Viewing waveforms requires a valid EZwave license.
- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Data Read Worstcases

	Signal/DRAM/Controller			Status	Corner		Setup	Hold	Pulse Width	Overshoot	Undershoot	Overshoot Area	Undershoot Area
#	Signal	Driving DRAM.Pin	Receiving Controller.Pin	Pass/Fail	Case	Reference Voltage Used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]
1	LPDDR4_DQ0	U6.B2	U1.A5	Pass	*Typ*	161.0	50.800	50.300	N/A	300.0	283.3	0.100	0.099
2	LPDDR4_DQ1	U6.C2	U1.A6	Pass	*Typ*	161.0	49.900	49.100	N/A	300.0	284.3	0.100	0.099
3	LPDDR4_DQ10	U6.E11	U1.F1	Pass	*Typ*	161.0	56.900	56.600	N/A	300.0	280.1	0.100	0.098
4	LPDDR4_DQ11	U6.F11	U1.G2	Pass	*Typ*	161.0	57.200	56.400	N/A	300.0	281.0	0.100	0.099
5	LPDDR4_DQ12	U6.F9	U1.F2	Pass	*Typ*	161.0	57.200	56.200	N/A	300.0	281.5	0.100	0.099
6	LPDDR4_DQ13	U6.E9	U1.F3	Pass	*Typ*	161.0	56.5	56.700	N/A	300.0	282.0	0.100	0.099
7	LPDDR4_DQ14	U6.C9	U1.D3	Pass	*Typ*	161.0	56.400	57.0	N/A	300.0	280.4	0.100	0.099
8	LPDDR4_DQ15	U6.B9	U1.F5	Pass	*Typ*	161.0	56.400	56.800	N/A	300.0	281.4	0.100	0.099
9	LPDDR4_DQ16	U6.AA2	U1.L5	Pass	*Typ*	161.0	53.900	53.100	N/A	300.0	282.8	0.100	0.097
10	LPDDR4_DQ17	U6.Y2	U1.M5	Pass	*Typ*	161.0	54.600	55.300	N/A	300.0	287.3	0.100	0.098
11	LPDDR4_DQ18	U6.V2	U1.N5	Pass	*Typ*	161.0	52.700	51.900	N/A	300.0	282.2	0.100	0.097
12	LPDDR4_DQ19	U6.U2	U1.L4	Pass	*Typ*	161.0	53.900	54.700	N/A	300.0	287.7	0.100	0.098
13	LPDDR4_DQ2	U6.E2	U1.B5	Pass	*Typ*	161.0	49.900	49.600	N/A	300.0	281.2	0.100	0.098
14	LPDDR4_DQ20	U6.U4	U1.L2	Pass	*Typ*	161.0	51.200	55.300	N/A	300.0	286.0	0.100	0.098
15	LPDDR4_DQ21	U6.V4	U1.L1	Pass	*Typ*	161.0	53.600	54.200	N/A	300.0	282.5	0.100	0.097
16	LPDDR4_DQ22	U6.Y4	U1.N2	Pass	*Typ*	161.0	51.400	54.5	N/A	300.0	284.0	0.100	0.097
17	LPDDR4_DQ23	U6.AA4	U1.N4	Pass	*Typ*	161.0	54.100	54.0	N/A	300.0	282.8	0.100	0.097
18	LPDDR4_DQ24	U6.AA11	U1.T3	Pass	*Typ*	161.0	49.800	53.200	N/A	300.0	278.4	0.100	0.098
19	LPDDR4_DQ25	U6.Y11	U1.T2	Pass	*Typ*	161.0	49.800	52.700	N/A	300.0	278.2	0.100	0.098
20	LPDDR4_DQ26	U6.V11	U1.P2	Pass	*Typ*	161.0	50.400	50.700	N/A	300.0	279.4	0.100	0.099
21	LPDDR4_DQ27	U6.U11	U1.P3	Pass	*Typ*	161.0	49.900	53.900	N/A	300.0	279.2	0.100	0.099
22	LPDDR4_DQ28	U6.U9	U1.P5	Pass	*Typ*	161.0	52.5	52.900	N/A	300.0	278.5	0.100	0.098
23	LPDDR4_DQ29	U6.V9	U1.R4	Pass	*Typ*	161.0	51.300	51.300	N/A	300.0	278.8	0.100	0.098
24	LPDDR4_DQ3	U6.F2	U1.C2	Pass	*Typ*	161.0	50.200	50.900	N/A	300.0	283.0	0.100	0.099
25	LPDDR4_DQ30	U6.Y9	U1.T4	Pass	*Typ*	161.0	52.400	51.900	N/A	300.0	278.6	0.100	0.098
26	LPDDR4_DQ31	U6.AA9	U1.T5	Pass	*Typ*	161.0	51.900	52.0	N/A	300.0	278.9	0.100	0.098
27	LPDDR4_DQ4	U6.F4	U1.B4	Pass	*Typ*	161.0	51.200	50.0	N/A	300.0	281.2	0.100	0.098
28	LPDDR4_DQ5	U6.E4	U1.C3	Pass	*Typ*	161.0	50.100	50.300	N/A	300.0	281.5	0.100	0.098
29	LPDDR4_DQ6	U6.C4	U1.A2	Pass	*Typ*	161.0	49.900	50.800	N/A	300.0	280.6	0.100	0.099
30	LPDDR4_DQ7	U6.B4	U1.A4	Pass	*Typ*	161.0	51.400	51.0	N/A	300.0	282.2	0.100	0.099
31	LPDDR4_DQ8	U6.B11	U1.D1	Pass	*Typ*	161.0	58.100	57.100	N/A	300.0	280.0	0.100	0.098
32	LPDDR4_DQ9	U6.C11	U1.C4	Pass	*Typ*	161.0	57.0	55.900	N/A	300.0	282.4	0.100	0.099

	Signal/DRAM/Controller			Status	Corner		Setup	Hold	Pulse Width	Overshoot	Undershoot	Overshoot Area	Undershoot Area
#	Signal	Driving DRAM.Pin	Receiving Controller.Pin	Pass/Fail	Case	Reference Voltage Used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]
33	LPDDR4_DQ0	U6.B2	U1.A5	Pass	*Slow*	158.4	44.400	45.100	N/A	300.0	282.3	0.100	0.098
34	LPDDR4_DQ1	U6.C2	U1.A6	Pass	*Slow*	158.4	43.700	43.0	N/A	300.0	287.3	0.100	0.099
35	LPDDR4_DQ10	U6.E11	U1.F1	Pass	*Slow*	158.4	50.200	51.300	N/A	300.0	280.5	0.100	0.098
36	LPDDR4_DQ11	U6.F11	U1.G2	Pass	*Slow*	158.4	50.100	51.300	N/A	300.0	281.2	0.100	0.098
37	LPDDR4_DQ12	U6.F9	U1.F2	Pass	*Slow*	158.4	52.0	51.300	N/A	300.0	282.7	0.100	0.098
38	LPDDR4_DQ13	U6.E9	U1.F3	Pass	*Slow*	158.4	51.400	50.800	N/A	300.0	283.1	0.100	0.098
39	LPDDR4_DQ14	U6.C9	U1.D3	Pass	*Slow*	158.4	50.400	50.700	N/A	300.0	280.9	0.100	0.098
40	LPDDR4_DQ15	U6.B9	U1.F5	Pass	*Slow*	158.4	50.800	51.100	N/A	300.0	281.7	0.100	0.098
41	LPDDR4_DQ16	U6.AA2	U1.L5	Pass	*Slow*	158.4	49.5	49.400	N/A	300.0	283.5	0.100	0.097
42	LPDDR4_DQ17	U6.Y2	U1.M5	Pass	*Slow*	158.4	51.400	51.300	N/A	300.0	288.2	0.100	0.098
43	LPDDR4_DQ18	U6.V2	U1.N5	Pass	*Slow*	158.4	48.400	47.900	N/A	300.0	285.0	0.100	0.097
44	LPDDR4_DQ19	U6.U2	U1.L4	Pass	*Slow*	158.4	49.700	50.400	N/A	300.0	286.5	0.100	0.098
45	LPDDR4_DQ2	U6.E2	U1.B5	Pass	*Slow*	158.4	44.200	43.100	N/A	300.0	280.6	0.100	0.098
46	LPDDR4_DQ20	U6.U4	U1.L2	Pass	*Slow*	158.4	47.800	50.600	N/A	300.0	287.7	0.100	0.098
47	LPDDR4_DQ21	U6.V4	U1.L1	Pass	*Slow*	158.4	50.600	49.600	N/A	300.0	285.0	0.100	0.097
48	LPDDR4_DQ22	U6.Y4	U1.N2	Pass	*Slow*	158.4	47.100	50.700	N/A	300.0	286.2	0.100	0.097
49	LPDDR4_DQ23	U6.AA4	U1.N4	Pass	*Slow*	158.4	50.200	50.400	N/A	300.0	285.8	0.100	0.097
50	LPDDR4_DQ24	U6.AA11	U1.T3	Pass	*Slow*	158.4	47.900	49.600	N/A	300.0	279.9	0.100	0.098
51	LPDDR4_DQ25	U6.Y11	U1.T2	Pass	*Slow*	158.4	47.900	48.600	N/A	300.0	279.6	0.100	0.098
52	LPDDR4_DQ26	U6.V11	U1.P2	Pass	*Slow*	158.4	48.100	47.200	N/A	300.0	282.0	0.100	0.098
53	LPDDR4_DQ27	U6.U11	U1.P3	Pass	*Slow*	158.4	49.0	50.200	N/A	300.0	280.9	0.100	0.098
54	LPDDR4_DQ28	U6.U9	U1.P5	Pass	*Slow*	158.4	49.5	50.0	N/A	300.0	280.3	0.100	0.097
55	LPDDR4_DQ29	U6.V9	U1.R4	Pass	*Slow*	158.4	49.100	48.200	N/A	300.0	281.2	0.100	0.098
56	LPDDR4_DQ3	U6.F2	U1.C2	Pass	*Slow*	158.4	44.600	44.700	N/A	300.0	282.7	0.100	0.098
57	LPDDR4_DQ30	U6.Y9	U1.T4	Pass	*Slow*	158.4	49.800	48.400	N/A	300.0	280.2	0.100	0.098
58	LPDDR4_DQ31	U6.AA9	U1.T5	Pass	*Slow*	158.4	48.900	48.800	N/A	300.0	280.7	0.100	0.098
59	LPDDR4_DQ4	U6.F4	U1.B4	Pass	*Slow*	158.4	44.300	44.700	N/A	300.0	280.5	0.100	0.098
60	LPDDR4_DQ5	U6.E4	U1.C3	Pass	*Slow*	158.4	44.0	43.700	N/A	300.0	280.7	0.100	0.098
61	LPDDR4_DQ6	U6.C4	U1.A2	Pass	*Slow*	158.4	44.100	44.200	N/A	300.0	283.5	0.100	0.098
62	LPDDR4_DQ7	U6.B4	U1.A4	Pass	*Slow*	158.4	44.700	45.5	N/A	300.0	282.7	0.100	0.098
63	LPDDR4_DQ8	U6.B11	U1.D1	Pass	*Slow*	158.4	51.600	51.600	N/A	300.0	280.6	0.100	0.098
64	LPDDR4_DQ9	U6.C11	U1.C4	Pass	*Slow*	158.4	50.200	49.900	N/A	300.0	283.4	0.100	0.098
65	LPDDR4_DQ0	U6.B2	U1.A5	Pass	*Fast*	177.5	53.100	54.200	N/A	300.0	282.8	0.100	0.099
66	LPDDR4_DQ1	U6.C2	U1.A6	Pass	*Fast*	177.5	52.900	52.900	N/A	300.0	283.6	0.100	0.099
67	LPDDR4_DQ10	U6.E11	U1.F1	Pass	*Fast*	177.5	60.5	60.700	N/A	300.0	279.4	0.100	0.099
68	LPDDR4_DQ11	U6.F11	U1.G2	Pass	*Fast*	177.5	59.800	59.700	N/A	300.0	280.2	0.100	0.099
69	LPDDR4_DQ12	U6.F9	U1.F2	Pass	*Fast*	177.5	59.300	60.400	N/A	300.0	279.9	0.100	0.099
70	LPDDR4_DQ13	U6.E9	U1.F3	Pass	*Fast*	177.5	60.300	61.0	N/A	300.0	280.8	0.100	0.099
71	LPDDR4_DQ14	U6.C9	U1.D3	Pass	*Fast*	177.5	60.300	60.300	N/A	300.0	279.4	0.100	0.099
72	LPDDR4_DQ15	U6.B9	U1.F5	Pass	*Fast*	177.5	60.200	59.700	N/A	300.0	280.2	0.100	0.099
73	LPDDR4_DQ16	U6.AA2	U1.L5	Pass	*Fast*	177.5	57.200	57.200	N/A	300.0	279.9	0.100	0.098
74	LPDDR4_DQ17	U6.Y2	U1.M5	Pass	*Fast*	177.5	57.800	58.5	N/A	300.0	282.7	0.100	0.099
75	LPDDR4_DQ18	U6.V2	U1.N5	Pass	*Fast*	177.5	56.400	56.300	N/A	300.0	279.0	0.100	0.097
76	LPDDR4_DQ19	U6.U2	U1.L4	Pass	*Fast*	177.5	57.800	58.200	N/A	300.0	289.5	0.100	0.099
77	LPDDR4_DQ2	U6.E2	U1.B5	Pass	*Fast*	177.5	53.800	53.0	N/A	300.0	281.9	0.100	0.099
78	LPDDR4_DQ20	U6.U4	U1.L2	Pass	*Fast*	177.5	55.700	58.900	N/A	300.0	281.9	0.100	0.099
79	LPDDR4_DQ21	U6.V4	U1.L1	Pass	*Fast*	177.5	58.0	56.900	N/A	300.0	278.8	0.100	0.098

	Signal/DRAM/Controller			Status	Corner		Setup	Hold	Pulse Width	Overshoot	Undershoot	Overshoot Area	Undershoot Area
#	Signal	Driving DRAM.Pin	Receiving Controller.Pin	Pass/Fail	Case	Reference Voltage Used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]
80	LPDDR4_DQ22	U6.Y4	U1.N2	**Pass**	*Fast*	177.5	55.700	58.100	N/A	300.0	281.5	0.100	0.098
81	LPDDR4_DQ23	U6.AA4	U1.N4	**Pass**	*Fast*	177.5	57.200	57.200	N/A	300.0	279.3	0.100	0.098
82	LPDDR4_DQ24	U6.AA11	U1.T3	**Pass**	*Fast*	177.5	53.5	57.200	N/A	300.0	277.0	0.100	0.099
83	LPDDR4_DQ25	U6.Y11	U1.T2	**Pass**	*Fast*	177.5	53.0	57.5	N/A	300.0	276.7	0.100	0.099
84	LPDDR4_DQ26	U6.V11	U1.P2	**Pass**	*Fast*	177.5	54.600	54.600	N/A	300.0	277.4	0.100	0.099
85	LPDDR4_DQ27	U6.U11	U1.P3	**Pass**	*Fast*	177.5	54.0	56.800	N/A	300.0	277.0	0.100	0.099
86	LPDDR4_DQ28	U6.U9	U1.P5	**Pass**	*Fast*	177.5	55.800	56.800	N/A	300.0	276.2	0.100	0.099
87	LPDDR4_DQ29	U6.V9	U1.R4	**Pass**	*Fast*	177.5	55.0	54.800	N/A	300.0	277.0	0.100	0.099
88	LPDDR4_DQ3	U6.F2	U1.C2	**Pass**	*Fast*	177.5	53.600	54.100	N/A	300.0	282.1	0.100	0.099
89	LPDDR4_DQ30	U6.Y9	U1.T4	**Pass**	*Fast*	177.5	55.5	56.300	N/A	300.0	276.7	0.100	0.099
90	LPDDR4_DQ31	U6.AA9	U1.T5	**Pass**	*Fast*	177.5	56.100	55.400	N/A	300.0	277.0	0.100	0.099
91	LPDDR4_DQ4	U6.F4	U1.B4	**Pass**	*Fast*	177.5	54.700	53.5	N/A	300.0	281.6	0.100	0.099
92	LPDDR4_DQ5	U6.E4	U1.C3	**Pass**	*Fast*	177.5	53.200	53.800	N/A	300.0	281.6	0.100	0.099
93	LPDDR4_DQ6	U6.C4	U1.A2	**Pass**	*Fast*	177.5	53.600	53.5	N/A	300.0	280.7	0.100	0.099
94	LPDDR4_DQ7	U6.B4	U1.A4	**Pass**	*Fast*	177.5	53.900	54.700	N/A	300.0	281.3	0.100	0.099
95	LPDDR4_DQ8	U6.B11	U1.D1	**Pass**	*Fast*	177.5	61.300	60.600	N/A	300.0	279.5	0.100	0.099
96	LPDDR4_DQ9	U6.C11	U1.C4	**Pass**	*Fast*	177.5	60.300	60.100	N/A	300.0	281.2	0.100	0.099

Address

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- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Address Worstcases

	Signal/Dram		Status	Corner		Setup	Hold	Pulse Width	tDIVW_1bit	Min Slew Rate	Max Slew Rate	Voltage Margin between Signal and Eye-Mask	Peak Voltage	Overshoot	Undershoot	Overshoot Area	Undershoot Area	
#	Signal	Accessed DRAM	Pass/Fail	Case	Reference voltage used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [V/ns]	Margin [V/ns]	Margin [mV]	Above/Below Reference Voltage Margin [mV]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Monotonic
1	LPDDR4_CA0	U6.H2	Pass	*Typ*	253.6	154.6	155.3	195.0	N/A	1.130	3.746	71.072	125.3	300.0	272.0	0.100	0.096	Pass
2	LPDDR4_CA0	U6.R2	Pass	*Typ*	253.6	154.6	155.3	195.0	N/A	1.130	3.746	71.076	125.3	300.0	272.0	0.100	0.096	Pass
3	LPDDR4_CA1	U6.J2	Pass	*Typ*	253.6	156.5	156.3	196.4	N/A	1.182	3.745	84.005	124.3	300.0	274.9	0.100	0.096	Pass
4	LPDDR4_CA1	U6.P2	Pass	*Typ*	253.6	156.3	156.3	196.3	N/A	1.178	3.745	83.975	124.3	300.0	275.1	0.100	0.096	Pass
5	LPDDR4_CA2	U6.H9	Pass	*Typ*	253.6	155.5	155.3	195.7	N/A	1.071	3.782	66.415	124.0	300.0	270.3	0.100	0.096	Pass
6	LPDDR4_CA2	U6.R9	Pass	*Typ*	253.6	154.5	155.8	195.3	N/A	1.060	3.788	66.333	123.6	300.0	270.7	0.100	0.096	Pass
7	LPDDR4_CA3	U6.H10	Pass	*Typ*	253.6	154.3	154.3	196.3	N/A	1.072	3.724	72.290	124.2	300.0	274.6	0.100	0.096	Pass
8	LPDDR4_CA3	U6.R10	Pass	*Typ*	253.6	154.9	154.4	196.4	N/A	1.078	3.723	72.436	124.3	300.0	274.4	0.100	0.096	Pass
9	LPDDR4_CA4	U6.H11	Pass	*Typ*	253.6	161.5	161.7	200.6	N/A	1.446	3.440	98.616	122.3	300.0	275.2	0.100	0.097	Pass
10	LPDDR4_CA4	U6.R11	Pass	*Typ*	253.6	162.100	161.3	200.8	N/A	1.451	3.443	98.691	122.8	300.0	275.1	0.100	0.097	Pass
11	LPDDR4_CA5	U6.J11	Pass	*Typ*	253.6	166.1	165.3	202.6	N/A	1.724	3.130	89.105	118.1	300.0	277.9	0.100	0.097	Pass
12	LPDDR4_CA5	U6.P11	Pass	*Typ*	253.6	165.4	165.5	202.4	N/A	1.698	3.139	89.008	117.9	300.0	278.0	0.100	0.097	Pass
13	LPDDR4_CSN0_0	U6.H4	Pass	*Typ*	253.6	145.4	206.600	210.0	N/A	2.319	1.782	154.909	160.6	300.0	255.2	0.100	0.090	Pass
14	LPDDR4_CSN0_1	U6.R4	Pass	*Typ*	253.6	151.3	199.8	208.3	N/A	2.343	1.698	157.410	161.5	300.0	263.0	0.100	0.089	Pass
15	LPDDR4_CA0	U6.H2	Pass	*Slow*	256.3	147.4	146.8	187.8	N/A	0.841	3.853	51.101	91.0	300.0	270.9	0.100	0.095	Pass
16	LPDDR4_CA0	U6.R2	Pass	*Slow*	256.3	147.4	146.8	187.8	N/A	0.841	3.853	51.103	91.0	300.0	270.9	0.100	0.095	Pass
17	LPDDR4_CA1	U6.J2	Pass	*Slow*	256.3	148.9	148.8	189.4	N/A	0.898	3.860	61.981	90.0	300.0	272.5	0.100	0.096	Pass
18	LPDDR4_CA1	U6.P2	Pass	*Slow*	256.3	148.3	148.9	189.3	N/A	0.893	3.859	62.083	90.0	300.0	272.6	0.100	0.096	Pass
19	LPDDR4_CA2	U6.H9	Pass	*Slow*	256.3	148.9	147.8	188.5	N/A	0.821	3.879	46.385	89.6	300.0	267.1	0.100	0.095	Pass
20	LPDDR4_CA2	U6.R9	Pass	*Slow*	256.3	147.3	148.4	188.1	N/A	0.803	3.884	46.233	89.3	300.0	267.6	0.100	0.095	Pass
21	LPDDR4_CA3	U6.H10	Pass	*Slow*	256.3	146.7	147.2	188.5	N/A	0.793	3.815	52.876	89.8	300.0	271.4	0.100	0.096	Pass
22	LPDDR4_CA3	U6.R10	Pass	*Slow*	256.3	146.9	147.0	188.6	N/A	0.800	3.814	52.996	89.8	300.0	271.2	0.100	0.096	Pass
23	LPDDR4_CA4	U6.H11	Pass	*Slow*	256.3	152.5	153.3	195.3	N/A	1.033	3.526	67.562	90.6	300.0	272.9	0.100	0.097	Pass
24	LPDDR4_CA4	U6.R11	Pass	*Slow*	256.3	153.4	152.9	195.4	N/A	1.054	3.527	67.575	90.9	300.0	272.7	0.100	0.097	Pass
25	LPDDR4_CA5	U6.J11	Pass	*Slow*	256.3	158.600	157.5	198.4	N/A	1.226	3.276	71.709	90.9	300.0	276.6	0.100	0.097	Pass
26	LPDDR4_CA5	U6.P11	Pass	*Slow*	256.3	157.600	157.6	198.1	N/A	1.198	3.286	71.720	90.9	300.0	276.7	0.100	0.097	Pass
27	LPDDR4_CSN0_0	U6.H4	Pass	*Slow*	256.3	140.5	206.1	206.0	N/A	2.265	2.219	152.915	163.5	300.0	258.6	0.100	0.092	Pass
28	LPDDR4_CSN0_1	U6.R4	Pass	*Slow*	256.3	148.0	199.600	205.5	N/A	2.393	2.146	155.127	164.6	300.0	265.4	0.100	0.091	Pass
29	LPDDR4_CA0	U6.H2	Pass	*Fast*	263.1	158.100	158.4	197.2	N/A	1.268	3.833	100.069	155.6	300.0	273.8	0.100	0.096	Pass
30	LPDDR4_CA0	U6.R2	Pass	*Fast*	263.1	158.100	158.4	197.2	N/A	1.268	3.833	100.072	155.6	300.0	273.8	0.100	0.096	Pass
31	LPDDR4_CA1	U6.J2	Pass	*Fast*	263.1	159.6	159.4	198.1	N/A	1.320	3.813	112.210	151.7	300.0	276.7	0.100	0.097	Pass
32	LPDDR4_CA1	U6.P2	Pass	*Fast*	263.1	159.4	159.6	198.0	N/A	1.316	3.814	112.175	151.7	300.0	276.8	0.100	0.097	Pass
33	LPDDR4_CA2	U6.H9	Pass	*Fast*	263.1	157.3	157.3	198.1	N/A	1.205	3.896	96.039	154.7	300.0	272.8	0.100	0.096	Pass
34	LPDDR4_CA2	U6.R9	Pass	*Fast*	263.1	156.3	158.1	197.8	N/A	1.195	3.900	95.961	153.9	300.0	273.1	0.100	0.096	Pass
35	LPDDR4_CA3	U6.H10	Pass	*Fast*	263.1	157.100	158.4	198.9	N/A	1.217	3.847	99.923	152.0	300.0	276.3	0.100	0.096	Pass
36	LPDDR4_CA3	U6.R10	Pass	*Fast*	263.1	157.5	158.100	199.0	N/A	1.222	3.845	100.081	152.1	300.0	276.3	0.100	0.096	Pass

	Signal/Dram		Status	Corner		Setup	Hold	Pulse Width	tDIVW_1bit	Min Slew Rate	Max Slew Rate	Voltage Margin between Signal and Eye-Mask	Peak Voltage	Overshoot	Undershoot	Overshoot Area	Undershoot Area	
#	Signal	Accessed DRAM	Pass/Fail	Case	Reference voltage used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [V/ns]	Margin [V/ns]	Margin [mV]	Above/Below Reference Voltage Margin [mV]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Monotonic
37	LPDDR4_CA4	U6.H11	**Pass**	*Fast*	263.1	163.4	162.8	199.3	N/A	1.553	3.526	127.469	147.9	300.0	277.6	0.100	0.097	Pass
38	LPDDR4_CA4	U6.R11	**Pass**	*Fast*	263.1	163.9	162.5	199.6	N/A	1.558	3.525	127.574	148.4	300.0	277.4	0.100	0.097	Pass
39	LPDDR4_CA5	U6.J11	**Pass**	*Fast*	263.1	167.100	166.3	200.7	N/A	1.841	3.236	118.622	145.3	300.0	279.7	0.100	0.097	Pass
40	LPDDR4_CA5	U6.P11	**Pass**	*Fast*	263.1	166.8	166.4	200.5	N/A	1.826	3.240	118.036	145.3	300.0	279.8	0.100	0.097	Pass
41	LPDDR4_CSN0_0	U6.H4	**Pass**	*Fast*	263.1	142.1	209.4	208.2	N/A	2.336	1.889	166.858	169.2	300.0	256.8	0.100	0.090	Pass
42	LPDDR4_CSN0_1	U6.R4	**Pass**	*Fast*	263.1	147.3	202.5	205.2	N/A	2.355	1.579	169.258	169.8	300.0	263.0	0.100	0.089	Pass

Differential Nets

Differential Nets Worstcases

- To investigate any result further, click on the link in the cell to open the waveforms. Viewing waveforms requires a valid EZwave license.
- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Differential Nets Worstcases

	Signal/Driver/Receicer				Status	Corner	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Vix	Vinse Peak-to-peak	Vinse High	Vinse Low	
#	Signal	Driver.Pins	Receiver.Pins	Operation	Pass/Fail	Case	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Margin [mV]	Margin [mV]	Margin [mV]	Margin [mV]	Monotonic
1	LPDDR4_CK_T	U1.H1&J1	U6.J8&J9	Write rank(1,1)	Pass	*Typ*	300.0	297.7	0.100	0.100	21.0	163.5	31.1	132.1	Pass
2	LPDDR4_CK_T	U1.H1&J1	U6.P8&P9	Write rank(1,1)	Pass	*Typ*	300.0	297.7	0.100	0.100	20.0	163.8	32.1	131.7	Pass
3	LPDDR4_DQS0_P	U6.D3&E3	U1.B2&B1	Read rank(1,1)	Pass	*Typ*	300.0	288.1	0.100	0.099	N/A	154.4	87.9	74.5	N/A
4	LPDDR4_DQS0_P	U1.B2&B1	U6.D3&E3	Write rank(1,1)	Pass	*Typ*	297.8	295.0	0.100	0.100	No Vref	684.8	No Vref	No Vref	Pass
5	LPDDR4_DQS1_P	U6.D10&E10	U1.E3&E2	Read rank(1,1)	Pass	*Typ*	300.0	296.1	0.100	0.100	N/A	149.9	84.5	70.7	N/A
6	LPDDR4_DQS1_P	U1.E3&E2	U6.D10&E10	Write rank(1,1)	Pass	*Typ*	296.9	294.4	0.100	0.100	No Vref	617.2	No Vref	No Vref	Pass
7	LPDDR4_DQS2_P	U6.W3&V3	U1.M3&M2	Read rank(1,1)	Pass	*Typ*	300.0	299.7	0.100	0.100	N/A	161.5	98.7	61.3	N/A
8	LPDDR4_DQS2_P	U1.M3&M2	U6.W3&V3	Write rank(1,1)	Pass	*Typ*	297.8	295.0	0.100	0.100	No Vref	679.8	No Vref	No Vref	Pass
9	LPDDR4_DQS3_P	U6.W10&V10	U1.R2&R1	Read rank(1,1)	Pass	*Typ*	300.0	299.3	0.100	0.100	N/A	147.1	95.5	59.0	N/A
10	LPDDR4_DQS3_P	U1.R2&R1	U6.W10&V10	Write rank(1,1)	Pass	*Typ*	296.7	293.7	0.100	0.100	No Vref	658.6	No Vref	No Vref	Pass
11	LPDDR4_CK_T	U1.H1&J1	U6.J8&J9	Write rank(1,1)	Pass	*Slow*	300.0	297.5	0.100	0.100	30.6	141.7	17.1	127.4	Pass
12	LPDDR4_CK_T	U1.H1&J1	U6.P8&P9	Write rank(1,1)	Pass	*Slow*	300.0	297.5	0.100	0.100	29.3	141.8	17.2	127.1	Pass
13	LPDDR4_DQS0_P	U6.D3&E3	U1.B2&B1	Read rank(1,1)	Pass	*Slow*	300.0	291.9	0.100	0.100	N/A	156.6	89.2	68.5	N/A
14	LPDDR4_DQS0_P	U1.B2&B1	U6.D3&E3	Write rank(1,1)	Pass	*Slow*	297.5	295.5	0.100	0.100	No Vref	603.9	No Vref	No Vref	Pass
15	LPDDR4_DQS1_P	U6.D10&E10	U1.E3&E2	Read rank(1,1)	Pass	*Slow*	300.0	297.3	0.100	0.100	N/A	146.7	84.1	63.9	N/A
16	LPDDR4_DQS1_P	U1.E3&E2	U6.D10&E10	Write rank(1,1)	Pass	*Slow*	296.7	294.3	0.100	0.100	No Vref	524.2	No Vref	No Vref	Pass
17	LPDDR4_DQS2_P	U6.W3&V3	U1.M3&M2	Read rank(1,1)	Pass	*Slow*	300.0	299.6	0.100	0.100	N/A	139.6	89.2	52.6	N/A
18	LPDDR4_DQS2_P	U1.M3&M2	U6.W3&V3	Write rank(1,1)	Pass	*Slow*	297.4	295.4	0.100	0.100	No Vref	604.1	No Vref	No Vref	Pass
19	LPDDR4_DQS3_P	U6.W10&V10	U1.R2&R1	Read rank(1,1)	Pass	*Slow*	300.0	299.3	0.100	0.100	N/A	127.1	82.1	51.3	N/A
20	LPDDR4_DQS3_P	U1.R2&R1	U6.W10&V10	Write rank(1,1)	Pass	*Slow*	296.6	293.9	0.100	0.100	No Vref	583.3	No Vref	No Vref	Pass
21	LPDDR4_CK_T	U1.H1&J1	U6.J8&J9	Write rank(1,1)	Pass	*Fast*	300.0	298.6	0.100	0.100	17.4	193.3	53.7	140.2	Pass
22	LPDDR4_CK_T	U1.H1&J1	U6.P8&P9	Write rank(1,1)	Pass	*Fast*	300.0	298.5	0.100	0.100	16.5	193.3	54.0	139.7	Pass
23	LPDDR4_DQS0_P	U6.D3&E3	U1.B2&B1	Read rank(1,1)	Pass	*Fast*	300.0	288.9	0.100	0.100	N/A	170.4	86.2	90.5	N/A
24	LPDDR4_DQS0_P	U1.B2&B1	U6.D3&E3	Write rank(1,1)	Pass	*Fast*	298.7	296.2	0.100	0.100	No Vref	731.1	No Vref	No Vref	Pass
25	LPDDR4_DQS1_P	U6.D10&E10	U1.E3&E2	Read rank(1,1)	Pass	*Fast*	300.0	296.3	0.100	0.100	N/A	163.8	78.8	85.5	N/A
26	LPDDR4_DQS1_P	U1.E3&E2	U6.D10&E10	Write rank(1,1)	Pass	*Fast*	298.0	296.2	0.100	0.100	No Vref	696.0	No Vref	No Vref	Pass
27	LPDDR4_DQS2_P	U6.W3&V3	U1.M3&M2	Read rank(1,1)	Pass	*Fast*	300.0	298.8	0.100	0.100	N/A	173.9	100.4	82.3	N/A
28	LPDDR4_DQS2_P	U1.M3&M2	U6.W3&V3	Write rank(1,1)	Pass	*Fast*	298.7	296.3	0.100	0.100	No Vref	731.0	No Vref	No Vref	Pass
29	LPDDR4_DQS3_P	U6.W10&V10	U1.R2&R1	Read rank(1,1)	Pass	*Fast*	300.0	299.9	0.100	0.100	N/A	154.9	92.6	79.0	N/A
30	LPDDR4_DQS3_P	U1.R2&R1	U6.W10&V10	Write rank(1,1)	Pass	*Fast*	297.8	295.3	0.100	0.100	No Vref	719.9	No Vref	No Vref	Pass

CLK-DQS Skew

CLK-DQS Skew Worstcases

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- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

CLK-DQS Skew Worstcases

	Signal/Dram				Status	Corner	DQSS - Earliest DQS	DQSS - Latest DQS	tDSS	tDSH
#	Signal	Accessed DRAM	DRAM CLK Pins	DRAM DQS Pins	Pass/Fail	Case	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]
1	LPDDR4_DQS0_P	U6	J8&J9	D3&E3	Pass	*Typ*	147.1	122.1	179.1	177.5
2	LPDDR4_DQS1_P	U6	J8&J9	D10&E10	Pass	*Typ*	147.2	130.5	179.3	177.0
3	LPDDR4_DQS2_P	U6	J8&J9	W3&V3	Pass	*Typ*	145.2	135.2	172.7	160.3
4	LPDDR4_DQS3_P	U6	J8&J9	W10&V10	Pass	*Typ*	144.1	129.5	165.7	154.6
5	LPDDR4_DQS0_P	U6	J8&J9	D3&E3	Pass	*Slow*	147.1	119.6	178.5	177.5
6	LPDDR4_DQS1_P	U6	J8&J9	D10&E10	Pass	*Slow*	145.2	130.4	178.7	176.6
7	LPDDR4_DQS2_P	U6	J8&J9	W3&V3	Pass	*Slow*	144.2	133.4	172.3	174.7
8	LPDDR4_DQS3_P	U6	J8&J9	W10&V10	Pass	*Slow*	144.1	126.0	164.3	153.9
9	LPDDR4_DQS0_P	U6	J8&J9	D3&E3	Pass	*Fast*	146.7	123.1	178.1	176.1
10	LPDDR4_DQS1_P	U6	J8&J9	D10&E10	Pass	*Fast*	147.0	125.6	180.0	176.9
11	LPDDR4_DQS2_P	U6	J8&J9	W3&V3	Pass	*Fast*	146.1	134.7	172.0	148.8
12	LPDDR4_DQS3_P	U6	J8&J9	W10&V10	Pass	*Fast*	143.9	133.7	168.1	147.7

Eye Density Links

Eye Density Links

Eye Density Links

#	Eye Density Links	Data/Address	Case
1	Load Eye Density Plots	Data	Typ
2	Load Eye Density Plots	Address	Typ
3	Load Eye Density Plots	Data	Slow
4	Load Eye Density Plots	Address	Slow
5	Load Eye Density Plots	Data	Fast
6	Load Eye Density Plots	Address	Fast

Setup Info

Design: odbjob.tgz

VX2.8 build 17344847

Date: May-13-2021 13h-21m

Setup Information

Interface Setup

Parameter	Value
DDR Interface	LPDDR4
Crosstalk	Disabled
Power-Aware	Disabled
IC Corners	Fast, Typ, Slow
Probing location	Controller - at Die, DRAM - at Die
Total Run Time	0 Days, 00 Hours, 04 Minutes 40 Seconds

Rank Setup

Rank	Ref. Des.	IBIS File	Component	Timing Model	Speed Grade
Controller	U1	J721E_DRA829_TDA4VM.ibs	J7ES	C:\MentorGraphics\HLVX.2.8\SDD_HOME\hyperlynx64\Libs\lpddr4_ctl.v	DDR_3200
Rank[1,1]	U6	43_46lq32256ea_11.ibs	43_46lq32256ea	C:\MentorGraphics\HLVX.2.8\SDD_HOME\hyperlynx64\Libs\lpddr4_dram.v	DDR_3200

IBIS Model Selectors

Rank	CLK	Addr	CTL
Controller	lpddr4_ocd_40p_40n_diff	lpddr4_ocd_40p_40n	lpddr4_ocd_40p_40n
Rank[1,1]	CA_RCV_ODT60_VOH25	CA_RCV_ODT60_VOH25	CA_RCV_ODT60_VOH25

ODT Setup Information

ODT - Write to Slot 1

Rank	DQS	DQ	DM
Controller	lpddr4_ocd_40p_40n_diff,	lpddr4_ocd_40p_40n,	lpddr4_ocd_40p_40n,
Rank[1,1]	DQ_SOC80_PD40_VOH25	DQ_SOC80_PD40_VOH25	DQ_SOC80_PD40_VOH25

ODT - Read from Slot 1

Rank	DQS	DQ	DM
Controller	lpddr4_odt_40_diff,	lpddr4_odt_40,	lpddr4_odt_40,
Rank[1,1]	DQ_SOC80_PD40_VOH25	DQ_SOC80_PD40_VOH25	DQ_SOC80_PD40_VOH25