HyperLynx®

DDR Simulation Report - LPDDR4_Controller40p40n_ODT60_VOH25_Rcv48_All_Apr-15-2021_19h-34m

Data Write

Data Write Worstcases

- To investigate any result further, click on the link in the cell to open the waveforms. Viewing waveforms requires a valid EZwave license.
- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Data Write Worstcases

	Signal/Controller/DRAM			Status	Corner		Setup	Hold	Pulse Width	tDIVW_1bit	Min Slew Rate	Max Slew Rate	Voltage Margin between Signal and Eye-Mask	Peak Voltage	Overshoot	Undershoot	Overshoot Area	Undershoot Area	
#	Signal	Driving Controller.Pin	Receiving DRAM.Pin	Pass/Fail	Case	Reference voltage used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [V/ns]	Margin [V/ns]	Margin [mV]	Above/Below Reference Voltage Margin [mV]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Monotonic
1	LPDDR4_DM0_DBI0#	U1.A3	U6.C3	Pass	*Typ*	261.6	83.6	83.9	145.3	N/A	2.884	1.889	132.465	165.4	300.0	259.9	0.100	0.096	Pass
2	LPDDR4_DM1_DBI1#	U1.E4	U6.C10	Pass	*Typ*	261.6	88.9	88.0	147.2	N/A	3.253	1.759	131.259	153.8	300.0	271.3	0.100	0.096	Pass
3	LPDDR4_DM2_DBI2#	U1.N1	U6.Y3	Pass	*Typ*	261.6	88.0	87.4	147.2	N/A	3.003	1.749	129.394	150.3	300.0	262.3	0.100	0.095	Pass
4	LPDDR4_DM3_DBI3#	U1.R5	U6.Y10	Pass	*Typ*	261.6	88.300	87.5	144.6	N/A	2.757	1.466	135.717	154.8	300.0	270.9	0.100	0.095	Pass
5	LPDDR4_DQ0	U1.A5	U6.B2	Pass	*Typ*	261.6	85.4	85.1	145.4	N/A	3.083	1.831	127.543	164.6	300.0	264.1	0.100	0.097	Pass
6	LPDDR4_DQ1	U1.A6	U6.C2	Pass	*Typ*	261.6	84.300	84.4	145.3	N/A	2.970	2.078	127.969	169.7	300.0	261.1	0.100	0.096	Pass
7	LPDDR4_DQ10	U1.F1	U6.E11	Pass	*Typ*	261.6	86.300	85.800	147.8	N/A	2.886	1.864	137.452	161.5	300.0	265.5	0.100	0.096	Pass
8	LPDDR4_DQ11	U1.G2	U6.F11	Pass	*Typ*	261.6	85.9	86.300	147.4	N/A	2.856	1.847	139.930	160.0	300.0	265.2	0.100	0.096	Pass
9	LPDDR4_DQ12	U1.F2	U6.F9	Pass	*Typ*	261.6	87.300	87.4	146.8	N/A	2.969	1.855	138.337	159.4	300.0	268.6	0.100	0.096	Pass
10	LPDDR4_DQ13	U1.F3	U6.E9	Pass	*Typ*	261.6	88.1	88.9	147.2	N/A	3.021	1.967	134.133	149.4	300.0	270.7	0.100	0.095	Pass
11	LPDDR4_DQ14	U1.D3	U6.C9	Pass	*Typ*	261.6	86.300	86.800	148.1	N/A	2.947	1.894	134.641	158.9	300.0	266.9	0.100	0.095	Pass
12	LPDDR4_DQ15	U1.F5	U6.B9	Pass	*Typ*	261.6	86.1	86.700	148.4	N/A	2.894	1.912	133.657	155.4	300.0	265.6	0.100	0.096	Pass
13	LPDDR4_DQ16	U1.L5	U6.AA2	Pass	*Typ*	261.6	89.0	88.200	146.9	N/A	3.160	1.737	125.172	149.0	300.0	256.8	0.100	0.095	Pass
14	LPDDR4_DQ17	U1.M5	U6.Y2	Pass	*Typ*	261.6	89.0	88.4	149.1	N/A	3.372	1.834	125.526	148.0	300.0	266.0	0.100	0.096	Pass
15	LPDDR4_DQ18	U1.N5	U6.V2	Pass	*Typ*	261.6	86.9	86.4	147.3	N/A	2.754	1.710	132.753	150.9	300.0	264.4	0.100	0.095	Pass
16	LPDDR4_DQ19	U1.L4	U6.U2	Pass	*Typ*	261.6	88.4	88.200	150.2	N/A	3.252	1.841	126.355	136.2	300.0	256.0	0.100	0.094	Pass
17	LPDDR4_DQ2	U1.B5	U6.E2	Pass	*Typ*	261.6	85.0	85.1	145.9	N/A	2.959	2.002	132.609	163.9	300.0	260.6	0.100	0.097	Pass
18	LPDDR4_DQ20	U1.L2	U6.U4	Pass	*Typ*	261.6	88.700	89.0	147.9	N/A	3.400	1.844	132.279	150.5	300.0	264.9	0.100	0.096	Pass
19	LPDDR4_DQ21	U1.L1	U6.V4	Pass	*Typ*	261.6	87.300	86.4	146.7	N/A	2.822	1.620	125.501	149.5	300.0	256.1	0.100	0.095	Pass
20	LPDDR4_DQ22	U1.N2	U6.Y4	Pass	*Typ*	261.6	87.300	87.200	147.4	N/A	2.927	1.696	129.152	149.9	300.0	267.0	0.100	0.096	Pass
21	LPDDR4_DQ23	U1.N4	U6.AA4	Pass	*Typ*	261.6	87.300	87.300	148.1	N/A	2.876	1.614	125.515	149.6	300.0	256.7	0.100	0.095	Pass
22	LPDDR4_DQ24	U1.T3	U6.AA11	Pass	*Typ*	261.6	88.5	88.4	146.6	N/A	2.836	1.491	142.830	157.9	300.0	270.5	0.100	0.095	Pass
23	LPDDR4_DQ25	U1.T2	U6.Y11	Pass	*Typ*	261.6	87.6	86.9	143.3	N/A	2.737	1.480	138.940	156.1	300.0	273.3	0.100	0.096	Pass
24	LPDDR4_DQ26	U1.P2	U6.V11	Pass	*Typ*	261.6	88.0	88.0	144.7	N/A	2.921	1.612	139.411	159.0	300.0	269.5	0.100	0.095	Pass
25	LPDDR4_DQ27	U1.P3	U6.U11	Pass	*Typ*	261.6	87.9	88.800	146.5	N/A	3.007	1.575	132.535	152.6	300.0	265.5	0.100	0.094	Pass
26	LPDDR4_DQ28	U1.P5	U6.U9	Pass	*Typ*	261.6	88.300	89.1	145.8	N/A	3.002	1.496	129.848	151.4	300.0	263.6	0.100	0.094	Pass
27	LPDDR4_DQ29	U1.R4	U6.V9	Pass	*Typ*	261.6	87.9	88.1	143.3	N/A	2.847	1.518	138.599	157.3	300.0	269.1	0.100	0.095	Pass
28	LPDDR4_DQ3	U1.C2	U6.F2	Pass	*Typ*	261.6	82.700	83.700	145.4	N/A	3.003	1.822	125.914	167.7	300.0	262.5	0.100	0.097	Pass
29	LPDDR4_DQ30	U1.T4	U6.Y9	Pass	*Typ*	261.6	88.6	87.9	144.5	N/A	2.870	1.550	134.725	153.4	300.0	266.2	0.100	0.094	Pass
30	LPDDR4_DQ31	U1.T5	U6.AA9	Pass	*Typ*	261.6	87.9	87.9	144.3	N/A	2.973	1.601	135.195	153.1	300.0	271.6	0.100	0.095	Pass
31	LPDDR4_DQ4	U1.B4	U6.F4	Pass	*Typ*	261.6	83.800	84.0	145.3	N/A	2.918	1.915	132.381	160.0	300.0	260.2	0.100	0.096	Pass

	Signal/Controller/DRAM			Status	Corner		Setup	Hold	Pulse Width	tDIVW_1bit	Min Slew Rate	Max Slew Rate	Voltage Margin between Signal and Eye-Mask	Peak Voltage	Overshoot	Undershoot	Overshoot Area	Undershoot Area	
#	Signal	Driving Controller.Pin	Receiving DRAM.Pin	Pass/Fail	Case	Reference voltage used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [V/ns]	Margin [V/ns]	Margin [mV]	Above/Below Reference Voltage Margin [mV]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Monotonic
32	LPDDR4_DQ5	U1.C3	U6.E4	Pass	Typ	261.6	83.4	83.9	144.8	N/A	2.919	2.011	131.247	163.4	300.0	261.2	0.100	0.096	Pass
33	LPDDR4_DQ6	U1.A2	U6.C4	Pass	Typ	261.6	82.6	83.1	145.7	N/A	2.946	1.845	129.603	167.4	300.0	261.7	0.100	0.096	Pass
34	LPDDR4_DQ7	U1.A4	U6.B4	Pass	Typ	261.6	84.4	84.4	146.6	N/A	3.111	1.738	128.872	164.6	300.0	261.0	0.100	0.096	Pass
35	LPDDR4_DQ8	U1.D1	U6.B11	Pass	Typ	261.6	87.200	86.4	148.2	N/A	2.918	1.835	139.829	159.6	300.0	266.2	0.100	0.096	Pass
36	LPDDR4_DQ9	U1.C4	U6.C11	Pass	Typ	261.6	86.6	85.6	146.9	N/A	2.801	2.028	139.925	152.2	300.0	270.0	0.100	0.096	Pass
37	LPDDR4_DM0_DBI0#	U1.A3	U6.C3	Pass	Slow	270.9	80.9	80.1	147.0	N/A	2.527	2.116	145.405	174.2	300.0	261.8	0.100	0.096	Pass
38	LPDDR4_DM1_DBI1#	U1.E4	U6.C10	Pass	Slow	270.9	86.0	86.0	148.0	N/A	2.695	1.996	139.973	164.4	300.0	271.4	0.100	0.096	Pass
39	LPDDR4_DM2_DBI2#	U1.N1	U6.Y3	Pass	Slow	270.9	87.9	86.6	147.4	N/A	2.901	2.121	134.143	152.6	300.0	261.7	0.100	0.095	Pass
40	LPDDR4_DM3_DBI3#	U1.R5	U6.Y10	Pass	Slow	270.9	86.5	86.5	146.4	N/A	2.695	1.864	137.354	160.2	300.0	270.1	0.100	0.095	Pass
41	LPDDR4_DQ0	U1.A5	U6.B2	Pass	Slow	270.9	82.0	82.300	145.9	N/A	2.720	2.089	138.722	172.3	300.0	265.1	0.100	0.096	Pass
42	LPDDR4_DQ1	U1.A6	U6.C2	Pass	Slow	270.9	80.8	81.5	145.6	N/A	2.635	2.279	139.638	178.4	300.0	262.6	0.100	0.096	Pass
43	LPDDR4_DQ10	U1.F1	U6.E11	Pass	Slow	270.9	83.0	83.6	148.9	N/A	2.394	2.137	148.623	164.9	300.0	265.5	0.100	0.096	Pass
44	LPDDR4_DQ11	U1.G2	U6.F11	Pass	Slow	270.9	83.4	83.300	148.1	N/A	2.304	2.144	151.749	163.7	300.0	265.5	0.100	0.096	Pass
45	LPDDR4_DQ12	U1.F2	U6.F9	Pass	Slow	270.9	85.1	83.9	147.1	N/A	2.454	2.123	150.555	162.9	300.0	268.9	0.100	0.096	Pass
46	LPDDR4_DQ13	U1.F3	U6.E9	Pass	Slow	270.9	87.1	86.200	148.0	N/A	2.535	2.214	145.712	153.8	300.0	270.8	0.100	0.095	Pass
47	LPDDR4_DQ14	U1.D3	U6.C9	Pass	Slow	270.9	83.800	83.1	148.5	N/A	2.388	2.137	146.538	162.4	300.0	267.1	0.100	0.095	Pass
48	LPDDR4_DQ15	U1.F5	U6.B9	Pass	Slow	270.9	83.700	83.200	149.1	N/A	2.368	2.159	145.169	159.5	300.0	265.4	0.100	0.096	Pass
49	LPDDR4_DQ16	U1.L5	U6.AA2	Pass	Slow	270.9	88.700	88.0	147.2	N/A	3.155	1.997	129.806	153.3	300.0	257.5	0.100	0.094	Pass
50	LPDDR4_DQ17	U1.M5	U6.Y2	Pass	Slow	270.9	88.0	87.300	148.3	N/A	3.181	1.950	131.029	148.8	300.0	264.4	0.100	0.096	Pass
51	LPDDR4_DQ18	U1.N5	U6.V2	Pass	Slow	270.9	86.200	86.6	147.1	N/A	2.757	1.936	136.487	152.9	300.0	263.3	0.100	0.095	Pass
52	LPDDR4_DQ19	U1.L4	U6.U2	Pass	Slow	270.9	88.800	88.800	151.4	N/A	3.029	1.984	133.032	143.3	300.0	257.1	0.100	0.094	Pass
53	LPDDR4_DQ2	U1.B5	U6.E2	Pass	Slow	270.9	79.6	79.9	145.9	N/A	2.607	2.164	142.212	173.4	300.0	262.8	0.100	0.096	Pass
54	LPDDR4_DQ20	U1.L2	U6.U4	Pass	Slow	270.9	87.800	88.300	147.5	N/A	3.076	2.213	138.849	151.7	300.0	264.5	0.100	0.095	Pass
55	LPDDR4_DQ21	U1.L1	U6.V4	Pass	Slow	270.9	87.300	86.5	146.5	N/A	2.845	1.852	128.828	149.1	300.0	255.9	0.100	0.095	Pass
56	LPDDR4_DQ22	U1.N2	U6.Y4	Pass	Slow	270.9	86.800	86.5	147.2	N/A	2.883	2.036	134.113	149.7	300.0	265.5	0.100	0.095	Pass
57	LPDDR4_DQ23	U1.N4	U6.AA4	Pass	Slow	270.9	86.9	87.300	147.7	N/A	2.884	1.877	128.689	149.5	300.0	256.9	0.100	0.094	Pass
58	LPDDR4_DQ24	U1.T3	U6.AA11	Pass	Slow	270.9	88.0	87.1	148.2	N/A	2.721	2.073	145.547	163.2	300.0	270.7	0.100	0.095	Pass
59	LPDDR4_DQ25	U1.T2	U6.Y11	Pass	Slow	270.9	86.5	87.0	144.7	N/A	2.608	1.859	140.807	161.5	300.0	273.3	0.100	0.095	Pass
60	LPDDR4_DQ26	U1.P2	U6.V11	Pass	Slow	270.9	86.6	86.700	146.2	N/A	2.887	1.910	140.847	165.2	300.0	269.6	0.100	0.095	Pass
61	LPDDR4_DQ27	U1.P3	U6.U11	Pass	Slow	270.9	87.0	87.200	148.0	N/A	2.941	1.828	135.807	158.0	300.0	265.2	0.100	0.094	Pass
62	LPDDR4_DQ28	U1.P5	U6.U9	Pass	Slow	270.9	87.5	87.6	147.1	N/A	2.880	1.839	132.946	156.8	300.0	263.1	0.100	0.094	Pass
63	LPDDR4_DQ29	U1.R4	U6.V9	Pass	Slow	270.9	86.0	86.9	144.9	N/A	2.730	2.036	141.055	162.9	300.0	269.3	0.100	0.095	Pass
64	LPDDR4_DQ3	U1.C2	U6.F2	Pass	Slow	270.9	79.7	80.2	147.7	N/A	2.736	2.090	138.531	176.7	300.0	264.0	0.100	0.097	Pass
65	LPDDR4_DQ30	U1.T4	U6.Y9	Pass	Slow	270.9	87.5	87.300	146.1	N/A	2.831	1.883	137.532	158.4	300.0	265.3	0.100	0.094	Pass
66	LPDDR4_DQ31	U1.T5	U6.AA9	Pass	Slow	270.9	87.1	86.700	145.9	N/A	2.874	1.867	139.144	158.0	300.0	271.3	0.100	0.095	Pass
67	LPDDR4_DQ4	U1.B4	U6.F4	Pass	Slow	270.9	81.200	81.5	146.0	N/A	2.591	2.092	141.891	170.5	300.0	261.6	0.100	0.096	Pass
68	LPDDR4_DQ5	U1.C3	U6.E4	Pass	Slow	270.9	81.300	81.300	145.1	N/A	2.695	2.174	141.645	172.7	300.0	262.0	0.100	0.096	Pass
69	LPDDR4_DQ6	U1.A2	U6.C4	Pass	Slow	270.9	79.4	79.4	145.9	N/A	2.628	2.107	140.328	175.6	300.0	262.9	0.100	0.096	Pass
70	LPDDR4_DQ7	U1.A4	U6.B4	Pass	Slow	270.9	80.9	81.700	145.0	N/A	2.657	2.016	142.113	172.5	300.0	262.2	0.100	0.096	Pass
71	LPDDR4_DQ8	U1.D1	U6.B11	Pass	Slow	270.9	83.5	83.800	149.0	N/A	2.367	2.117	150.844	161.5	300.0	266.1	0.100	0.096	Pass
72	LPDDR4_DQ9	U1.C4	U6.C11	Pass	Slow	270.9	82.9	82.800	147.8	N/A	2.270	2.280	151.110	157.1	300.0	269.9	0.100	0.096	Pass
73	LPDDR4_DM0_DBI0#	U1.A3	U6.C3	Pass	Fast	269.1	84.6	84.6	143.7	N/A	2.711	2.209	139.527	173.0	300.0	261.7	0.100	0.097	Pass
74	LPDDR4_DM1_DBI1#	U1.E4	U6.C10	Pass	Fast	269.1	88.6	88.0	145.5	N/A	3.326	1.915	137.562	164.0	300.0	273.2	0.100	0.096	Pass
75	LPDDR4_DM2_DBI2#	U1.N1	U6.Y3	Pass	Fast	269.1	85.300	85.9	147.4	N/A	2.607	1.466	133.671	160.0	300.0	267.2	0.100	0.096	Pass
76	LPDDR4_DM3_DBI3#	U1.R5	U6.Y10	Pass	Fast	269.1	86.5	87.300	144.6	N/A	2.629	1.358	142.561	161.7	300.0	272.5	0.100	0.096	Pass
77	LPDDR4_DQ0	U1.A5	U6.B2	Pass	Fast	269.1	85.300	86.0	143.4	N/A	2.887	2.082	133.714	172.1	300.0	265.3	0.100	0.097	Pass

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#	Signal	Driving Controller.Pin	Receiving DRAM.Pin	Pass/Fail	Case	Reference voltage used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [V/ns]	Margin [V/ns]	Margin [mV]	Above/Below Reference Voltage Margin [mV]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Monotonic
78	LPDDR4_DQ1	U1.A6	U6.C2	**Pass**	*Fast*	269.1	83.5	84.200	143.3	N/A	2.783	2.029	134.900	167.7	300.0	262.7	0.100	0.097	Pass
79	LPDDR4_DQ10	U1.F1	U6.E11	**Pass**	*Fast*	269.1	86.200	85.9	146.8	N/A	2.940	1.933	143.836	170.3	300.0	267.4	0.100	0.096	Pass
80	LPDDR4_DQ11	U1.G2	U6.F11	**Pass**	*Fast*	269.1	86.1	86.300	145.6	N/A	2.959	1.926	145.343	169.9	300.0	267.3	0.100	0.096	Pass
81	LPDDR4_DQ12	U1.F2	U6.F9	**Pass**	*Fast*	269.1	87.300	87.4	145.1	N/A	3.072	1.916	144.178	168.8	300.0	270.2	0.100	0.096	Pass
82	LPDDR4_DQ13	U1.F3	U6.E9	**Pass**	*Fast*	269.1	88.300	88.5	145.5	N/A	3.117	2.061	140.118	158.9	300.0	271.7	0.100	0.096	Pass
83	LPDDR4_DQ14	U1.D3	U6.C9	**Pass**	*Fast*	269.1	86.300	86.800	146.3	N/A	2.998	1.962	141.045	168.3	300.0	268.2	0.100	0.096	Pass
84	LPDDR4_DQ15	U1.F5	U6.B9	**Pass**	*Fast*	269.1	87.1	85.9	146.8	N/A	3.002	2.006	140.098	164.2	300.0	267.3	0.100	0.096	Pass
85	LPDDR4_DQ16	U1.L5	U6.AA2	**Pass**	*Fast*	269.1	86.4	87.1	146.1	N/A	2.841	1.413	130.247	155.3	300.0	261.3	0.100	0.095	Pass
86	LPDDR4_DQ17	U1.M5	U6.Y2	**Pass**	*Fast*	269.1	87.0	86.300	147.2	N/A	3.037	1.501	131.118	157.4	300.0	271.6	0.100	0.096	Pass
87	LPDDR4_DQ18	U1.N5	U6.V2	**Pass**	*Fast*	269.1	84.9	84.300	146.9	N/A	2.523	1.435	136.676	162.5	300.0	270.1	0.100	0.096	Pass
88	LPDDR4_DQ19	U1.L4	U6.U2	**Pass**	*Fast*	269.1	87.6	86.6	146.8	N/A	3.010	1.527	128.788	144.6	300.0	259.0	0.100	0.095	Pass
89	LPDDR4_DQ2	U1.B5	U6.E2	**Pass**	*Fast*	269.1	84.6	85.1	144.0	N/A	2.795	2.037	141.689	171.7	300.0	262.1	0.100	0.097	Pass
90	LPDDR4_DQ20	U1.L2	U6.U4	**Pass**	*Fast*	269.1	88.9	87.9	147.5	N/A	3.038	1.531	138.251	161.3	300.0	269.7	0.100	0.096	Pass
91	LPDDR4_DQ21	U1.L1	U6.V4	**Pass**	*Fast*	269.1	84.200	84.4	145.9	N/A	2.485	1.308	129.346	158.5	300.0	260.9	0.100	0.096	Pass
92	LPDDR4_DQ22	U1.N2	U6.Y4	**Pass**	*Fast*	269.1	85.0	85.300	146.9	N/A	2.543	1.391	133.365	160.4	300.0	272.4	0.100	0.096	Pass
93	LPDDR4_DQ23	U1.N4	U6.AA4	**Pass**	*Fast*	269.1	84.700	85.1	147.7	N/A	2.547	1.302	130.893	158.7	300.0	261.7	0.100	0.095	Pass
94	LPDDR4_DQ24	U1.T3	U6.AA11	**Pass**	*Fast*	269.1	87.1	87.4	146.8	N/A	2.743	1.412	149.548	165.2	300.0	271.5	0.100	0.095	Pass
95	LPDDR4_DQ25	U1.T2	U6.Y11	**Pass**	*Fast*	269.1	86.1	85.6	143.7	N/A	2.641	1.433	145.626	162.9	300.0	273.8	0.100	0.096	Pass
96	LPDDR4_DQ26	U1.P2	U6.V11	**Pass**	*Fast*	269.1	87.800	87.700	145.6	N/A	2.739	1.482	145.601	165.5	300.0	270.9	0.100	0.095	Pass
97	LPDDR4_DQ27	U1.P3	U6.U11	**Pass**	*Fast*	269.1	87.700	87.1	146.4	N/A	2.878	1.429	139.427	158.7	300.0	269.1	0.100	0.095	Pass
98	LPDDR4_DQ28	U1.P5	U6.U9	**Pass**	*Fast*	269.1	87.200	87.700	146.4	N/A	2.688	1.374	135.965	157.0	300.0	267.3	0.100	0.094	Pass
99	LPDDR4_DQ29	U1.R4	U6.V9	**Pass**	*Fast*	269.1	87.200	88.800	143.5	N/A	2.811	1.435	143.822	163.9	300.0	270.5	0.100	0.095	Pass
100	LPDDR4_DQ3	U1.C2	U6.F2	**Pass**	*Fast*	269.1	83.1	84.200	142.9	N/A	2.836	2.042	133.939	174.3	300.0	264.0	0.100	0.097	Pass
101	LPDDR4_DQ30	U1.T4	U6.Y9	**Pass**	*Fast*	269.1	86.9	86.4	144.8	N/A	2.752	1.436	140.553	159.9	300.0	270.0	0.100	0.094	Pass
102	LPDDR4_DQ31	U1.T5	U6.AA9	**Pass**	*Fast*	269.1	88.700	87.9	144.9	N/A	2.703	1.455	140.988	159.6	300.0	272.5	0.100	0.095	Pass
103	LPDDR4_DQ4	U1.B4	U6.F4	**Pass**	*Fast*	269.1	82.9	84.200	143.7	N/A	2.829	2.021	138.077	165.0	300.0	262.4	0.100	0.097	Pass
104	LPDDR4_DQ5	U1.C3	U6.E4	**Pass**	*Fast*	269.1	83.0	84.0	143.0	N/A	2.812	2.011	138.108	167.0	300.0	262.3	0.100	0.096	Pass
105	LPDDR4_DQ6	U1.A2	U6.C4	**Pass**	*Fast*	269.1	83.5	82.9	143.3	N/A	2.777	2.150	137.772	174.6	300.0	263.4	0.100	0.097	Pass
106	LPDDR4_DQ7	U1.A4	U6.B4	**Pass**	*Fast*	269.1	85.9	85.700	145.5	N/A	2.948	2.022	136.429	172.9	300.0	262.8	0.100	0.097	Pass
107	LPDDR4_DQ8	U1.D1	U6.B11	**Pass**	*Fast*	269.1	86.6	87.300	146.2	N/A	3.028	1.891	145.249	170.1	300.0	268.0	0.100	0.096	Pass
108	LPDDR4_DQ9	U1.C4	U6.C11	**Pass**	*Fast*	269.1	85.800	85.9	144.8	N/A	2.953	2.119	143.478	161.7	300.0	271.2	0.100	0.096	Pass

Address

Address Worstcases

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- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column

Address Worstcases

	Signal/Dram		Status	Corner		Setup	Hold	Pulse Width	tDIVW_1bit	Min Slew Rate	Max Slew Rate	Voltage Margin between Signal and Eye-Mask	Peak Voltage	Overshoot	Undershoot	Overshoot Area	Undershoot Area	
#	Signal	Accessed DRAM	Pass/Fail	Case	Reference voltage used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [V/ns]	Margin [V/ns]	Margin [mV]	Above/Below Reference Voltage Margin [mV]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Monotonic
1	LPDDR4_CA0	U6.H2	**Pass**	*Typ*	253.8	154.600	155.3	195.1	N/A	1.124	3.735	70.506	125.2	300.0	272.3	0.100	0.096	Pass
2	LPDDR4_CA0	U6.R2	**Pass**	*Typ*	253.8	154.600	155.3	195.1	N/A	1.124	3.735	70.509	125.2	300.0	272.3	0.100	0.096	Pass
3	LPDDR4_CA1	U6.J2	**Pass**	*Typ*	253.8	156.3	156.0	196.1	N/A	1.178	3.724	83.989	124.3	300.0	274.6	0.100	0.096	Pass
4	LPDDR4_CA1	U6.P2	**Pass**	*Typ*	253.8	156.0	156.100	196.0	N/A	1.174	3.723	83.958	124.2	300.0	274.7	0.100	0.096	Pass
5	LPDDR4_CA2	U6.H9	**Pass**	*Typ*	253.8	155.6	155.100	195.7	N/A	1.069	3.780	66.275	124.9	300.0	270.0	0.100	0.096	Pass
6	LPDDR4_CA2	U6.R9	**Pass**	*Typ*	253.8	154.3	156.1	195.4	N/A	1.058	3.786	66.183	124.4	300.0	270.5	0.100	0.096	Pass
7	LPDDR4_CA3	U6.H10	**Pass**	*Typ*	253.8	154.3	154.100	194.2	N/A	1.065	3.716	72.080	122.6	300.0	274.3	0.100	0.096	Pass
8	LPDDR4_CA3	U6.R10	**Pass**	*Typ*	253.8	154.9	154.0	194.3	N/A	1.070	3.715	72.226	122.7	300.0	274.3	0.100	0.096	Pass
9	LPDDR4_CA4	U6.H11	**Pass**	*Typ*	253.8	161.5	161.600	200.5	N/A	1.448	3.439	98.197	121.4	300.0	275.3	0.100	0.097	Pass
10	LPDDR4_CA4	U6.R11	**Pass**	*Typ*	253.8	162.0	161.3	200.6	N/A	1.453	3.441	98.277	121.8	300.0	275.1	0.100	0.097	Pass
11	LPDDR4_CA5	U6.J11	**Pass**	*Typ*	253.8	166.1	166.0	202.7	N/A	1.756	3.119	87.982	118.2	300.0	277.7	0.100	0.097	Pass
12	LPDDR4_CA5	U6.P11	**Pass**	*Typ*	253.8	165.4	166.100	202.4	N/A	1.729	3.129	87.874	118.0	300.0	277.8	0.100	0.097	Pass
13	LPDDR4_CSN0_0	U6.H4	**Pass**	*Typ*	253.8	145.1	205.8	208.4	N/A	2.324	1.791	154.948	158.6	300.0	254.5	0.100	0.091	Pass
14	LPDDR4_CSN0_1	U6.R4	**Pass**	*Typ*	253.8	151.3	200.1	208.6	N/A	2.354	1.700	158.203	159.4	300.0	262.5	0.100	0.089	Pass
15	LPDDR4_CA0	U6.H2	**Pass**	*Slow*	255.9	148.3	147.3	188.4	N/A	0.843	3.840	51.640	91.5	300.0	271.1	0.100	0.095	Pass
16	LPDDR4_CA0	U6.R2	**Pass**	*Slow*	255.9	148.3	147.3	188.4	N/A	0.842	3.840	51.642	91.5	300.0	271.1	0.100	0.095	Pass
17	LPDDR4_CA1	U6.J2	**Pass**	*Slow*	255.9	148.9	148.8	189.6	N/A	0.902	3.843	61.854	90.7	300.0	272.2	0.100	0.096	Pass
18	LPDDR4_CA1	U6.P2	**Pass**	*Slow*	255.9	148.5	148.9	189.5	N/A	0.897	3.842	61.953	90.7	300.0	272.3	0.100	0.096	Pass
19	LPDDR4_CA2	U6.H9	**Pass**	*Slow*	255.9	149.2	147.9	189.0	N/A	0.825	3.883	46.732	91.2	300.0	266.9	0.100	0.095	Pass
20	LPDDR4_CA2	U6.R9	**Pass**	*Slow*	255.9	147.3	148.8	188.6	N/A	0.808	3.887	46.581	90.7	300.0	267.3	0.100	0.095	Pass
21	LPDDR4_CA3	U6.H10	**Pass**	*Slow*	255.9	146.8	147.2	187.5	N/A	0.794	3.815	52.783	88.9	300.0	271.3	0.100	0.096	Pass
22	LPDDR4_CA3	U6.R10	**Pass**	*Slow*	255.9	147.3	146.8	187.6	N/A	0.800	3.814	52.901	89.0	300.0	271.1	0.100	0.096	Pass
23	LPDDR4_CA4	U6.H11	**Pass**	*Slow*	255.9	152.8	153.4	195.5	N/A	1.036	3.529	67.762	90.8	300.0	273.2	0.100	0.097	Pass
24	LPDDR4_CA4	U6.R11	**Pass**	*Slow*	255.9	154.0	152.8	195.7	N/A	1.058	3.530	67.757	91.1	300.0	273.0	0.100	0.097	Pass
25	LPDDR4_CA5	U6.J11	**Pass**	*Slow*	255.9	159.5	158.3	198.8	N/A	1.270	3.267	71.088	91.2	300.0	276.3	0.100	0.097	Pass
26	LPDDR4_CA5	U6.P11	**Pass**	*Slow*	255.9	158.5	158.4	198.6	N/A	1.242	3.276	71.102	91.2	300.0	276.4	0.100	0.097	Pass
27	LPDDR4_CSN0_0	U6.H4	**Pass**	*Slow*	255.9	140.6	205.0	204.2	N/A	2.260	2.224	152.005	160.8	300.0	257.6	0.100	0.092	Pass
28	LPDDR4_CSN0_1	U6.R4	**Pass**	*Slow*	255.9	147.9	199.9	205.5	N/A	2.393	2.160	154.877	161.3	300.0	264.8	0.100	0.091	Pass
29	LPDDR4_CA0	U6.H2	**Pass**	*Fast*	262.8	158.5	158.6	197.7	N/A	1.267	3.833	99.258	156.5	300.0	274.1	0.100	0.096	Pass
30	LPDDR4_CA0	U6.R2	**Pass**	*Fast*	262.8	158.5	158.6	197.7	N/A	1.267	3.834	99.261	156.5	300.0	274.1	0.100	0.096	Pass
31	LPDDR4_CA1	U6.J2	**Pass**	*Fast*	262.8	159.8	159.100	198.2	N/A	1.317	3.805	113.276	151.8	300.0	276.3	0.100	0.097	Pass
32	LPDDR4_CA1	U6.P2	**Pass**	*Fast*	262.8	159.5	159.4	198.1	N/A	1.314	3.805	113.244	151.7	300.0	276.4	0.100	0.097	Pass
33	LPDDR4_CA2	U6.H9	**Pass**	*Fast*	262.8	157.5	157.5	198.6	N/A	1.207	3.900	96.590	155.5	300.0	272.5	0.100	0.096	Pass
34	LPDDR4_CA2	U6.R9	**Pass**	*Fast*	262.8	156.6	158.0	198.3	N/A	1.197	3.904	96.488	154.6	300.0	272.9	0.100	0.096	Pass
35	LPDDR4_CA3	U6.H10	**Pass**	*Fast*	262.8	157.100	158.100	196.6	N/A	1.217	3.844	100.411	151.3	300.0	276.0	0.100	0.096	Pass
36	LPDDR4_CA3	U6.R10	**Pass**	*Fast*	262.8	157.5	158.0	196.7	N/A	1.222	3.843	100.568	151.4	300.0	276.0	0.100	0.096	Pass

	Signal/Dram		Status	Corner		Setup	Hold	Pulse Width	tDIVW_1bit	Min Slew Rate	Max Slew Rate	Voltage Margin between Signal and Eye-Mask	Peak Voltage	Overshoot	Undershoot	Overshoot Area	Undershoot Area	
#	Signal	Accessed DRAM	Pass/Fail	Case	Reference voltage used [mV]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [V/ns]	Margin [V/ns]	Margin [mV]	Above/Below Reference Voltage Margin [mV]	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Monotonic
37	LPDDR4_CA4	U6.H11	**Pass**	*Fast*	262.8	163.5	162.8	199.9	N/A	1.558	3.528	127.248	148.1	300.0	277.6	0.100	0.097	Pass
38	LPDDR4_CA4	U6.R11	**Pass**	*Fast*	262.8	164.1	162.6	200.1	N/A	1.563	3.528	127.353	148.6	300.0	277.4	0.100	0.097	Pass
39	LPDDR4_CA5	U6.J11	**Pass**	*Fast*	262.8	167.5	166.5	201.3	N/A	1.847	3.227	118.964	146.5	300.0	279.7	0.100	0.097	Pass
40	LPDDR4_CA5	U6.P11	**Pass**	*Fast*	262.8	167.0	166.3	201.1	N/A	1.832	3.231	118.378	146.5	300.0	279.8	0.100	0.097	Pass
41	LPDDR4_CSN0_0	U6.H4	**Pass**	*Fast*	262.8	141.0	209.8	206.4	N/A	2.309	1.925	166.339	167.3	300.0	256.7	0.100	0.090	Pass
42	LPDDR4_CSN0_1	U6.R4	**Pass**	*Fast*	262.8	147.3	203.0	205.3	N/A	2.357	1.571	169.533	168.0	300.0	262.4	0.100	0.088	Pass

Differential Nets

Differential Nets Worstcases

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Differential Nets Worstcases

	Signal/Driver/Receicer				Status	Corner	Overshoot	Undershoot	Overshoot Area	Undershoot Area	Vix	Vinse Peak-to-peak	Vinse High	Vinse Low	
#	Signal	Driver.Pins	Receiver.Pins	Operation	Pass/Fail	Case	Margin [mV]	Margin [mV]	Margin [V*ns]	Margin [V*ns]	Margin [mV]	Margin [mV]	Margin [mV]	Margin [mV]	Monotonic
1	LPDDR4_CK_T	U1.H1&J1	U6.J8&J9	Write rank(1,1)	**Pass**	*Typ*	300.0	297.7	0.100	0.100	20.8	163.5	31.0	132.2	Pass
2	LPDDR4_CK_T	U1.H1&J1	U6.P8&P9	Write rank(1,1)	**Pass**	*Typ*	300.0	297.7	0.100	0.100	19.8	163.8	31.9	131.8	Pass
3	LPDDR4_DQS0_P	U1.B2&B1	U6.D3&E3	Write rank(1,1)	**Pass**	*Typ*	300.0	289.7	0.100	0.100	106.9	438.9	271.3	164.9	Pass
4	LPDDR4_DQS1_P	U1.E3&E2	U6.D10&E10	Write rank(1,1)	**Pass**	*Typ*	300.0	296.6	0.100	0.100	95.4	397.5	252.9	146.5	Pass
5	LPDDR4_DQS2_P	U1.M3&M2	U6.W3&V3	Write rank(1,1)	**Pass**	*Typ*	300.0	296.8	0.100	0.100	120.2	419.4	259.8	160.5	Pass
6	LPDDR4_DQS3_P	U1.R2&R1	U6.W10&V10	Write rank(1,1)	**Pass**	*Typ*	300.0	296.1	0.100	0.100	129.3	401.9	245.3	156.4	Pass
7	LPDDR4_CK_T	U1.H1&J1	U6.J8&J9	Write rank(1,1)	**Pass**	*Slow*	300.0	297.5	0.100	0.100	31.0	141.7	17.5	127.0	Pass
8	LPDDR4_CK_T	U1.H1&J1	U6.P8&P9	Write rank(1,1)	**Pass**	*Slow*	300.0	297.5	0.100	0.100	29.7	141.8	17.6	126.7	Pass
9	LPDDR4_DQS0_P	U1.B2&B1	U6.D3&E3	Write rank(1,1)	**Pass**	*Slow*	300.0	287.5	0.100	0.099	109.5	395.4	222.6	173.2	Pass
10	LPDDR4_DQS1_P	U1.E3&E2	U6.D10&E10	Write rank(1,1)	**Pass**	*Slow*	300.0	296.3	0.100	0.100	97.2	351.2	197.0	154.2	Pass
11	LPDDR4_DQS2_P	U1.M3&M2	U6.W3&V3	Write rank(1,1)	**Pass**	*Slow*	300.0	296.9	0.100	0.100	110.9	373.6	210.2	162.3	Pass
12	LPDDR4_DQS3_P	U1.R2&R1	U6.W10&V10	Write rank(1,1)	**Pass**	*Slow*	300.0	296.0	0.100	0.100	107.7	360.0	199.8	159.6	Pass
13	LPDDR4_CK_T	U1.H1&J1	U6.J8&J9	Write rank(1,1)	**Pass**	*Fast*	300.0	298.6	0.100	0.100	17.8	193.3	54.1	139.8	Pass
14	LPDDR4_CK_T	U1.H1&J1	U6.P8&P9	Write rank(1,1)	**Pass**	*Fast*	300.0	298.5	0.100	0.100	16.8	193.3	54.4	139.3	Pass
15	LPDDR4_DQS0_P	U1.B2&B1	U6.D3&E3	Write rank(1,1)	**Pass**	*Fast*	300.0	294.9	0.100	0.100	111.6	479.9	305.5	166.7	Pass
16	LPDDR4_DQS1_P	U1.E3&E2	U6.D10&E10	Write rank(1,1)	**Pass**	*Fast*	300.0	297.5	0.100	0.100	98.7	451.4	300.9	153.7	Pass
17	LPDDR4_DQS2_P	U1.M3&M2	U6.W3&V3	Write rank(1,1)	**Pass**	*Fast*	300.0	297.8	0.100	0.100	132.6	459.4	294.3	167.4	Pass
18	LPDDR4_DQS3_P	U1.R2&R1	U6.W10&V10	Write rank(1,1)	**Pass**	*Fast*	300.0	297.1	0.100	0.100	136.2	446.0	283.9	162.4	Pass

CLK-DQS Skew

CLK-DQS Skew Worstcases

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CLK-DQS Skew Worstcases

	Signal/Dram				Status	Corner	DQSS - Earliest DQS	DQSS - Latest DQS	tDSS	tDSH
#	Signal	Accessed DRAM	DRAM CLK Pins	DRAM DQS Pins	Pass/Fail	Case	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]
1	LPDDR4_DQS0_P	U6	J8&J9	D3&E3	Pass	*Typ*	147.3	138.4	179.3	176.8
2	LPDDR4_DQS1_P	U6	J8&J9	D10&E10	Pass	*Typ*	147.2	142.6	178.9	176.6
3	LPDDR4_DQS2_P	U6	J8&J9	W3&V3	Pass	*Typ*	148.3	143.7	178.4	178.4
4	LPDDR4_DQS3_P	U6	J8&J9	W10&V10	Pass	*Typ*	148.0	148.3	178.2	175.3
5	LPDDR4_DQS0_P	U6	J8&J9	D3&E3	Pass	*Slow*	147.9	137.6	175.9	178.2
6	LPDDR4_DQS1_P	U6	J8&J9	D10&E10	Pass	*Slow*	148.3	142.8	178.5	177.6
7	LPDDR4_DQS2_P	U6	J8&J9	W3&V3	Pass	*Slow*	147.8	144.0	179.3	178.7
8	LPDDR4_DQS3_P	U6	J8&J9	W10&V10	Pass	*Slow*	148.3	147.3	178.8	176.6
9	LPDDR4_DQS0_P	U6	J8&J9	D3&E3	Pass	*Fast*	147.8	139.1	179.2	175.4
10	LPDDR4_DQS1_P	U6	J8&J9	D10&E10	Pass	*Fast*	145.7	141.7	179.6	174.7
11	LPDDR4_DQS2_P	U6	J8&J9	W3&V3	Pass	*Fast*	146.6	146.0	178.2	174.4
12	LPDDR4_DQS3_P	U6	J8&J9	W10&V10	Pass	*Fast*	147.0	148.3	176.9	172.8

Eye Density Links

Eye Density Links

Eye Density Links

#	Eye Density Links	Data/Address	Case
1	Load Eye Density Plots	Data	Typ
2	Load Eye Density Plots	Address	Typ
3	Load Eye Density Plots	Data	Slow
4	Load Eye Density Plots	Address	Slow
5	Load Eye Density Plots	Data	Fast
6	Load Eye Density Plots	Address	Fast

Setup Info

Design: odbjob.tgz

VX2.8 build 17344847

Date: Apr-15-2021 19h-34m

Setup Information

Interface Setup

Parameter	Value
DDR Interface	LPDDR4
Crosstalk	Disabled
Power-Aware	Disabled
IC Corners	Fast, Typ, Slow
Probing location	Controller - at Die, DRAM - at Die
Total Run Time	0 Days, 00 Hours, 05 Minutes 13 Seconds

Rank Setup

Rank	Ref. Des.	IBIS File	Component	Timing Model	Speed Grade
Controller	U1	J721E_DRA829_TDA4VM.ibs	J7ES	C:\MentorGraphics\HLVX.2.8\SDD_HOME\hyperlynx64\Libs\lpddr4_ctl.v	DDR_3200
Rank[1,1]	U6	43_46lq32256ea_11.ibs	43_46lq32256ea	C:\MentorGraphics\HLVX.2.8\SDD_HOME\hyperlynx64\Libs\lpddr4_dram.v	DDR_3200

IBIS Model Selectors

Rank	CLK	Addr	CTL
Controller	lpddr4_ocd_40p_40n_diff	lpddr4_ocd_40p_40n	lpddr4_ocd_40p_40n
Rank[1,1]	CA_RCV_ODT60_VOH25	CA_RCV_ODT60_VOH25	CA_RCV_ODT60_VOH25

ODT Setup Information

ODT - Write to Slot 1

Rank	DQS	DQ	DM
Controller	lpddr4_ocd_40p_40n_diff,	lpddr4_ocd_40p_40n,	lpddr4_ocd_40p_40n,
Rank[1,1]	DQ_RCV_ODT48_VOH25	DQ_RCV_ODT48_VOH25	DQ_RCV_ODT48_VOH25

ODT - Read from Slot 1

Rank	DQS	DQ	DM
Controller	lpddr4_ocd_40p_40n_diff,	lpddr4_ocd_40p_40n,	lpddr4_ocd_40p_40n,
Rank[1,1]	DQ_RCV_ODTOFF	DQ_RCV_ODTOFF	DQ_RCV_ODTOFF