

MCU ADC basic parameters-*without calibration*

- Analog front -end

3.2 ADC reference

/*Vref extreme values are he, the detailed info at voltage reference section

- Vref extreme values are normal mode, not in calibration state:

$$E_{VREF_1V8} := (VREF_{1V8_max} - VREF_{1V8_nom}) = 13 \text{ mV}$$

$$VREF_{1V8_min} = 1.787 \text{ V} \quad VREF_{1V8_max} = 1.813 \text{ V}$$

$$\text{VREF error: } \frac{VREF_{1V8_max} - VREF_{1V8_nom}}{LSB} = 29 \quad /*LSB$$

3.3 Input stage-sampling /*Rs, Cs-sampling parasitics

$$\text{Sampling parasitics: } R_{sw} \equiv 1.2 \text{ k}\Omega \quad C_h \equiv 8 \text{ pF}$$

$$\text{Sampling time: } T_{sample} \equiv 75 \text{ ns}$$

$$\text{Conversion time: } T_{conv} \equiv 250 \text{ ns}$$

6.8.2.3 ADC Input Model

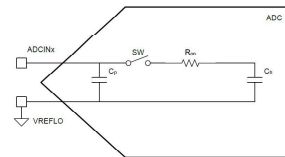


Figure 6-1. ADC Input Model

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Product Folder Link(s): AM263P4, AM263P2, AM263P4 Q1, AM263P2 Q1
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Sampling loss (due to finite samplin time)

$$\text{Sampling parasitic time constant: } T_{sp} := R_{sw} \cdot C_h$$

$$\text{Settling factor during sampling: } 1 - \left(e^{-\frac{T_{sample}}{T_{sp}}} \right) = 9.996 \cdot 10^{-1}$$

$$\text{Sampling loss(fractional)} \quad loss_s := \left(e^{-\frac{T_{sample}}{T_{sp}}} \right) = 0.0405\% \quad /*of sampled value- prportional with the amplitude$$

$$loss_s \frac{3.3 \text{ V}}{LSB} = 3.038 \quad /* 3*LSB @full scale, negligible?$$

Note: all of sampled sub-circuit attached by 10 -15nF so sampledcharge loss calculation is not necessary

3.4 Input stage AMP-Gain and offset

$$\text{Gain Error: } E_G := 5 \cdot LSB$$

$$\text{Offset Error: } E_O := 4 \cdot LSB$$

$$\text{Input leak current: } I_{leak} := 1.2 \text{ }\mu\text{A}$$

- ADC conversion parameters:

3.5 Digitizing error params /*TUE-Total Unadjusted Error, INL, DNL

$$\text{Differential Non-linearity} \quad DNL := 1 \cdot LSB = 0.44 \text{ mV}$$

$$\text{Integral Non-linearity} \quad INL := 2 \cdot LSB = 0.879 \text{ mV}$$

$$\text{TUE/*TUE-Total Unadjusted Error} \quad \text{Not defined separately}$$

3.6 ADC resolution-By amplitude /*count

$$ADC_{bit} \equiv 12$$

$$ADC_{resolution} := 2^{ADC_{bit}} - 1 = 4.095 \cdot 10^3$$

$$LSB \equiv \frac{VREF_{1V8_nom}}{2^{ADC_{bit}} - 1} = 0.44 \text{ mV} \quad /*most ADC parameters are expressed in LSB$$

MCU ADC basic parameters-expressed by calibration reference

- Analog front -end

3.7 ADC reference

/*Vref extreme values are he, the detailed info at voltage reference section

- Vref extreme values are normal mode, not in calibration state:

$$VREF_{cal_min} = 1.638 \text{ V} \quad VREF_{cal_max} \quad VREF_{cal_nom} = 1.65 \text{ V} \quad E_{VREF_cal} := (VREF_{cal_max} - VREF_{cal_nom}) = 12 \text{ mV}$$

$$VREF \text{ cal error: } \frac{E_{VREF_cal}}{LSB_cal} = 29 \quad /*LSB-really large!!$$

3.8 Input stage-sampling

/*Rs, Cs-sampling parasitics

/* No change, due to calibration

$$\text{Sampling parasitics: } R_{sw} = 1.2 \text{ k}\Omega \quad C_h = 8 \text{ pF}$$

$$\text{Sampling time: } T_{sample} = 75 \text{ ns}$$

$$\text{Conversion time: } T_{conv} = 250 \text{ ns}$$

6.8.2.3 ADC Input Model

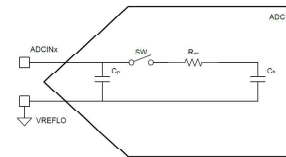


Figure 6-1. ADC Input Model

Sampling loss (due to finite samplin time)

$$\text{Sampling parasitic time constant: } T_{sp} = 9.6 \text{ ns}$$

$$\text{Settling factor during sampling: } 1 - \left(e^{-\frac{T_{sample}}{T_{sp}}} \right) = 9.996 \cdot 10^{-1}$$

$$\text{Sampling loss(fractional) } loss_s := \left(e^{-\frac{T_{sample}}{T_{sp}}} \right) = 0.0405\%$$

$$loss_s \frac{3.3 \text{ V}}{LSB_cal} = 3.314$$

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/*of sampled value-prportional with the amplitude

/* 3*LSB @full scale, negligible?

Note: all of sampled sub-circuit attached by 10 -15nF so sampledcharge loss calculation is not necessary

3.9 Input stage AMP-Gain and offset

$$\text{Gain Error: } E_{G_cal} := 0 \cdot LSB_cal$$

$$\text{Offset Error: } E_{O_cal} := 0 \cdot LSB_cal$$

$$\text{Input leak current: } I_{leak} := 1.2 \text{ }\mu\text{A}$$

- ADC conversion parameters:

/*TUE-Total Unadjusted Error, INL, DNL

3.10 Digitizing error params

$$\text{Differential Non-linearity } DNL_cal := 1 \cdot LSB_cal$$

$$\text{Integral Non-linearity } INL_cal := 2 \cdot LSB_cal$$

$$TUE/*TUE-Total Unadjusted Error \quad \text{Not defined separately}$$

3.11 ADC resolution-By amplitude

$$ADC_{bit} = 12$$

$$ADC_{resolution} = 4.095 \cdot 10^{-3}$$

$$LSB_cal := \frac{VREF_{cal_nom}}{2^{ADC_{bit}} - 1} = 0.403 \text{ mV} \quad /*most ADC parameters are expressed in LSB$$

4.MCU ADC working range and accuracy calculations

[Home](#)

4.2 ADC Input voltage range:

$$V_{REF_{1V8_min}} = 1.787 \text{ V}$$

$$V_{REF_{1V8_max}} = 1.813 \text{ V}$$

$$V_{in_ADC_max} = \frac{32}{18} \cdot V_{REF_{1V8_min}} = 3.178 \text{ V}$$

Limit max:

Limit max:

$$V_{3V3_LV_nom} = 3.3 \text{ V}$$

Result:

$$V_{in_ADC_max} = 3.178 \text{ V}$$

Note: in case of 3.3V , ADC input voltage range can be failed

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6.8.2 Analog to Digital Converter Characteristics

This section describes the Analog to Digital Converter electrical characteristics required to ensure proper device operation.

6.8.2.1 Analog-to-Digital Converter (ADC)
over operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REF_{min}}$		1.71	1.8	1.89	(V)
Input Conversion Range (V_{IN+} , V_{IN-})	Must be < VDDA33	0		$32/18 \cdot V_{REF_{min}}$	(V)

4.3. Final accuracy:

MCU ADC accuracy without offset calibration

VREF error:

$$E_{V_{REF_{1V8}}} = 12.6 \text{ mV}$$

$$\frac{E_{V_{REF_{1V8}}}}{LSB} = 28.665$$

Integral Non-linearity

$$INL = 0.879 \text{ mV}$$

$$\frac{INL}{LSB} = 2 \quad \frac{DNL}{LSB} = 1$$

Differential Non-linearity

$$DNL = 0.44 \text{ mV}$$

Gain Error:

$$E_G = 2.198 \text{ mV}$$

$$\frac{E_G}{LSB} = 5$$

Offset Error:

$$E_O = 1.758 \text{ mV}$$

$$\frac{E_O}{LSB} = 4$$

$$E_{ADC_TOTAL} := \sqrt{E_{V_{REF_{1V8}}}^2 + INL^2 + DNL^2 + E_G^2 + E_O^2} = 12.948 \text{ mV}$$

$$\frac{E_{ADC_TOTAL}}{LSB} = 29 \quad /*LSB$$

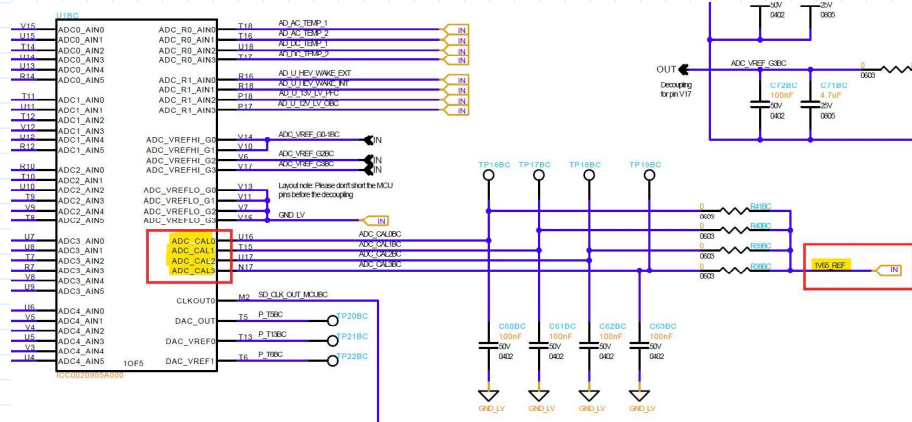
+Calculate leakage current for external circuit analysis

5.MCU ADC accuracy after calibration

Calibration procedure isof MCU ADC within the board is not clear for the author at this moment

[Home](#)

Supposing calibration will be executed on room temperature 25C



OPERATIONAL VOLTAGE REFERENCE TOLERANCE:

$$tol_{VREF_V8} = 0.7\%$$

Parameter	Value	Unit
Total DC output voltage accuracy, including voltage references, DC load and line regulation, process and temperature	0.7%	

CALIBRATION VOLTAGE REFERENCE TOLERANCE:

$$tol_{SH_REG} = 0.7\%$$

Reference voltage tolerances at 25°C	0.5% for TLV431B
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+Calculate leakage current for external circuit analysis

6.SUMMARY

WITHOUT CALIBRATION:

$$\frac{E_{ADC_TOTAL}}{LSB} = 29 \quad /*LSB$$

WITH CALIBRATION:

$$\frac{E_{ADC_CAL_TOTAL}}{LSB} = ? \quad /*LSB$$

+Calculate leakage current for external circuit analysis

FOR SUPPORT TEAM:

PLEASE DESCRIBE THE CALIBRATION PROCEDURE AND PARAMETERS!

HELP ME TO FIND THE ADC ACCURACY AFTER THE CALIBRATION!