3.Components

Home

MCU ADC as sub-component

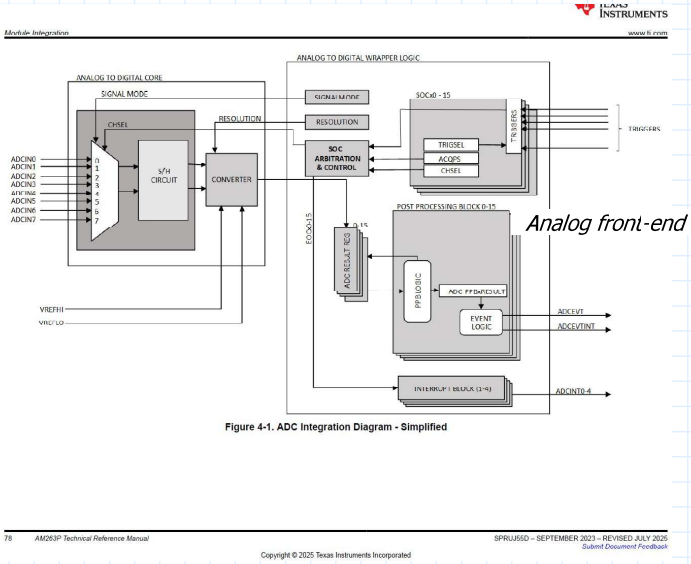
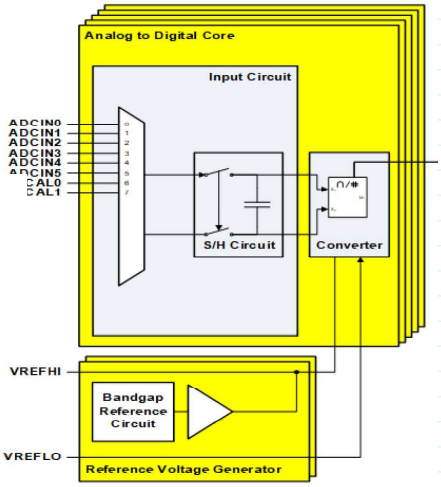


Figure 4-1. ADC Integration Diagram - Simplified

Analog front-end



MCU man. type: Texas Instruments: **AM263P4AFONFZCZRQ1**

AM263P4, AM263P2, AM263P4-Q1, AM263P2-Q1
SPRSP81D – OCTOBER 2023 – REVISED MAY 2025
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6.8.2 Analog to Digital Converter Characteristics

This section describes the Analog to Digital Converter electrical characteristics required to ensure proper device operation.

6.8.2.1 Analog-to-Digital Converter (ADC)

over operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REFHI}		1.71	1.8	1.89	V
Input Conversion Range (Vin+, Vin-)	Must be < VDDA33	0		$32/18 \times V_{REFHI}$	V
Power-up time				500	µs
Gain error		–5	±3	5	LSBs
Offset error		–4	±2	4	LSBs
Channel-to-channel gain error			±4		LSBs
Channel-to-channel offset error			±2		LSBs
ADC-to-ADC gain error	Same reference group		±4		LSBs
ADC-to-ADC offset error	Same reference group		±2		LSBs
DNL	Controlled environment to minimize input noise	–1	±0.5	1	LSBs
INL	Controlled environment to minimize input noise	–2	±1.0	2	LSBs
SNR	Controlled environment to minimize input noise		68		dB
ENOB (Synchronous Operation)			11		bits
ENOB (Asynchronous Operation)			9.7		bits
ADC-to-ADC isolation	Synchronous operation	–10		10	LSBs
V_{REFHI} input current			400		µA
Conversion time				250	ns
Parasitic Input Capacitance (C_p)(1)			7		pF
Sample/Hold Resistance (R_{on})(1)				1.2	kΩ
Sample/Hold Capacitance (C_h)(1)				8	pF
Input Leakage		–1.2	0.1	1.2	µA
Power supply (VDDA33)		3.13	3.3	3.46	V
Power supply (VDDA18)		1.71	1.8	1.89	V
Power Consumption (VDDA33)			200		µA
Power Consumption (VDDA18)			700		µA
Maximum ADCCLK frequency	With 50% duty cycle. Minimum pulse width must be maintained at 7.5ns		50	66.667	MHz
Sample time		75			ns

(1) See *ADC Input Model*

from the reference manual:

7.5.2.18 ADC Calibration

During the fabrication and test process, Texas Instruments calibrates the gain, offset, and linearity of the ADCs. These trim settings are stored in TI reserved OTP memory.

- Calibration information is stored in TOP_CTRL registers and copied to ADC registers ADCINLTRIM1-6 (offsets 0xE0-0xF4) during power up.

7.5.2.18.1 ADC Zero Offset Calibration

ADC offset error is determined and calibrated during factory testing. However, the user still has the option to perform offset calibration if the end application specifically requires this. This section describes how to perform offset calibration using internal VREFLO connection for single-ended operation.

Zero offset error is defined as the difference from 0 that occurs when converting a voltage at VREFLO. The zero offset error can be positive or negative. To correct this error, an adjustment of equal magnitude and opposite polarity is written into the ADCOFFTRIMx register. The value contained in this register is applied before the results are available in the ADC result registers. This operation is fully contained within the ADC core, so the timing of the results is not affected, and the full dynamic range of the ADC is maintained for any trim value.

Note

Regardless of the converter resolution, the size of each ADCOFFTRIMx step is (VREFHI-VREFLO)/ 65536.

Use the following procedure to re-calibrate the ADC offset in 12-bit single-ended mode:

1. Set ADCOFFTRIMx to +112 steps (0x70). This adds an artificial offset to account for negative offset that can reside in the ADC core.
2. Perform some multiple of 16 conversions on VREFLO (internal connection), accumulating the results (for example, 32 × 16 conversions = 512 conversions). Use the maximum value of ACQPS to make sure longer settling time to account for parasitic impedance of internal VREFLO connections.
3. Divide the accumulated result by the multiple of 16 (for example, for 512 conversions, divide by 32).
4. Set ADCOFFTRIMx to 112 – result from step 3.

7.5.2.19 ADC Timings

The process of converting an analog voltage to a digital value is broken down into an S+H phase and a conversion phase. The ADC sample and hold circuits (S+H) are clocked by SYSCLK while the ADC conversion process is clocked by ADCCLK. ADCCLK is generated by dividing down SYSCLK based on the PRESCALE field in the ADCCTL2 register.

The S+H duration is the value of the ACQPS field of the SOC being converted, plus one, times the SYSCLK period. The user must make sure that this duration exceeds both 1 ADCCLK period and the minimum S+H duration specified in the data sheet. The conversion time is approximately 10.5 ADCCLK cycles. See the timing diagrams and tables in Section 7.5.2.19.1 for exact timings.