new SOC PHY MII connections

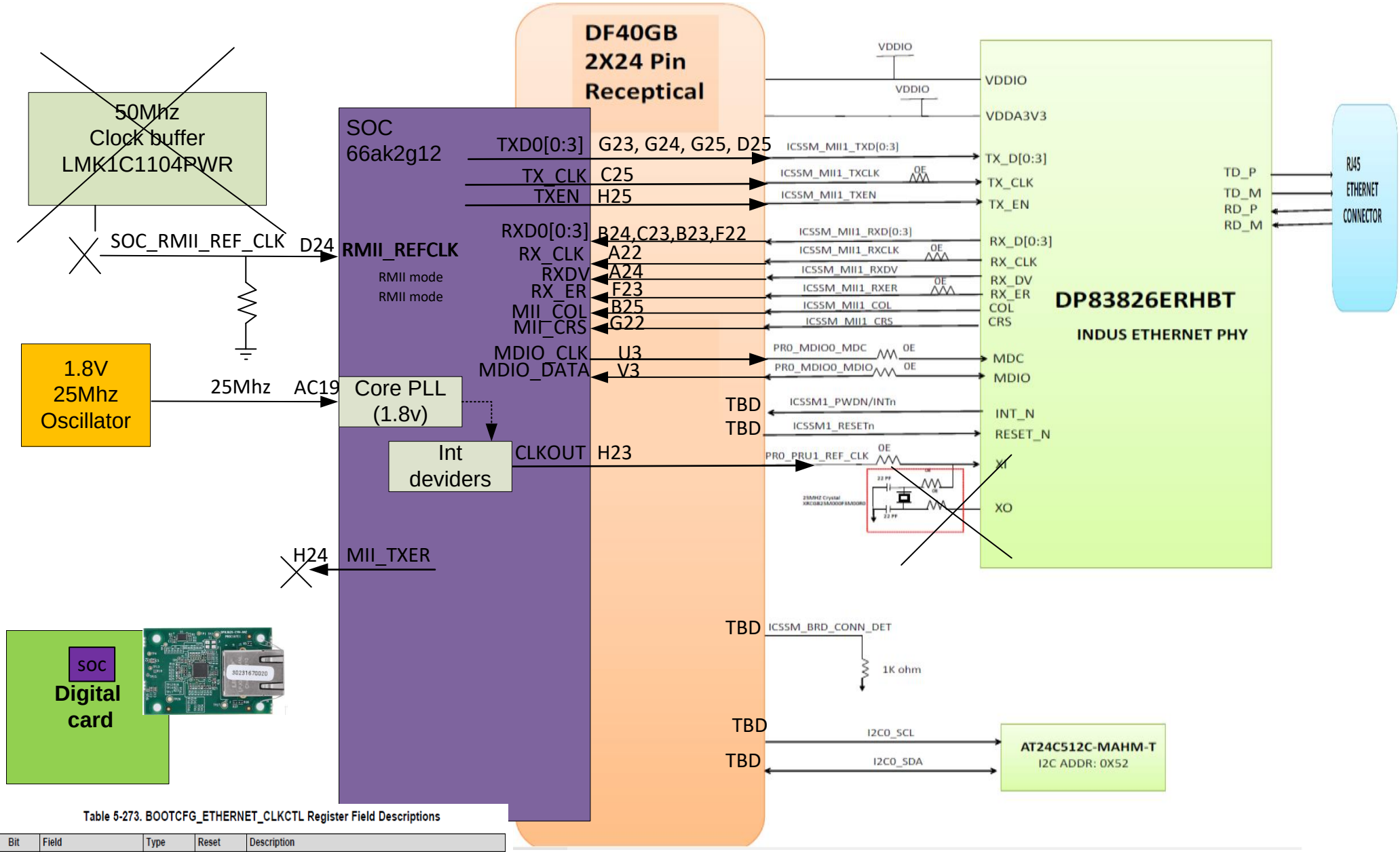

Table 5-273. BOOTCFG_ETHERNET_CLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	RMII_MII_CLKOUT_EN	RW	0h	BOOTROM code will set this bit based on the BOOTMODE selection 0 - CLKOUT pin is disabled 1 - CLKOUT pin is enabled
1	RMII_MII_CLKSEL	RW	0h	BOOTROM code will set this bit based on the BOOTMODE selection 0 - RMII_CLK will drive the CLKOUT pin 1 - MII_CLK will drive the CLKOUT pin
0	RESERVED	R	0h	Reserved

TBD=TO BE DESIGNED