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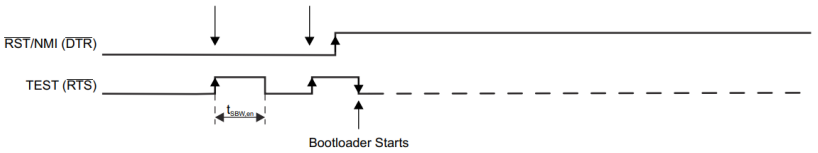
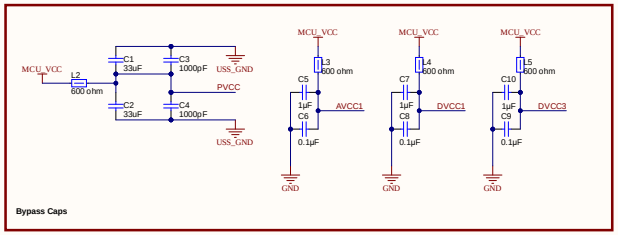
REVISION	DESCRIPTION	DATE	APPROVED

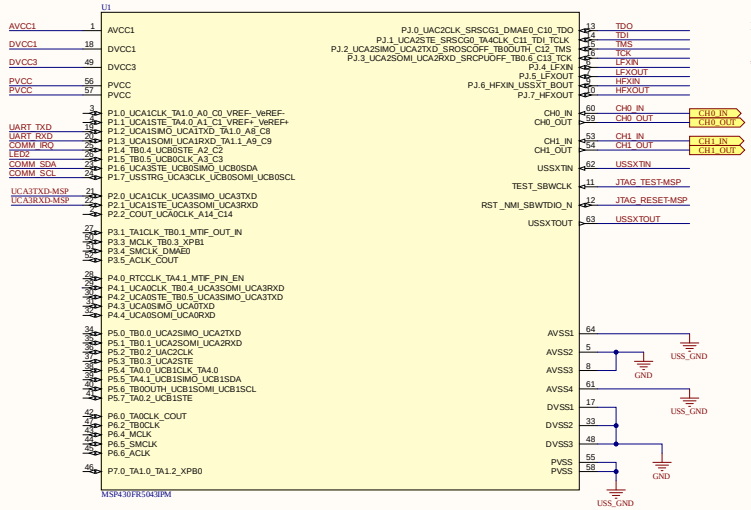
The BSL program execution starts when the TEST pin has received a minimum of two rising edges (low-to-high transitions) and if TEST is high while $\overline{RST}$/NMI rises from low to high (BSL entry method, see Figure 3-2). This level transition triggering improves BSL startup reliability. The first high level of the TEST pin must be at least $t_{SBW, En}$ (see the device-specific data sheet for $t_{SBW, En}$ parameter).

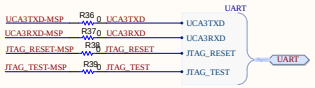


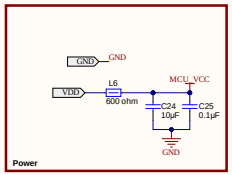
A. The recommended minimum time for pin states is 250 ns.

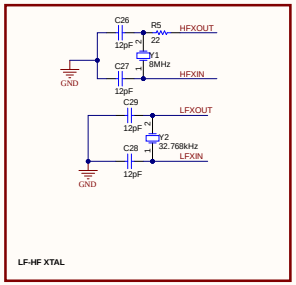
Figure 3-2. BSL Entry Sequence at Shared JTAG Pins

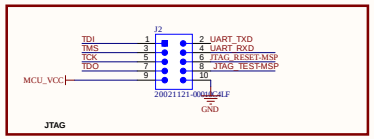


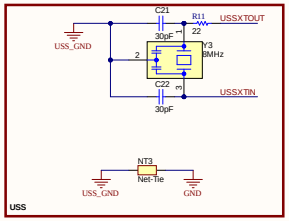




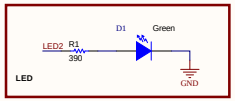


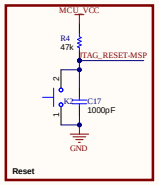






A resonator also consumes less current than a crystal.





APPROVALS	DATE
ENG: Eddie LaCost	
DSN:	
CHK: Not shown in title block	
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: Altium — Not in version control
DOCUMENT REVISION: Not in version control
DESIGN ITEM: Not in version control
TITLE
SIZE: C
CAGE CODE
DWG NO.
REV: ItemRevision not interpreted
SCALE:
FILE NAME: MSP430FR5043IPM.SchDoc
SHEET 2 OF 6

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