

K2G ICE EVM

V 1.0

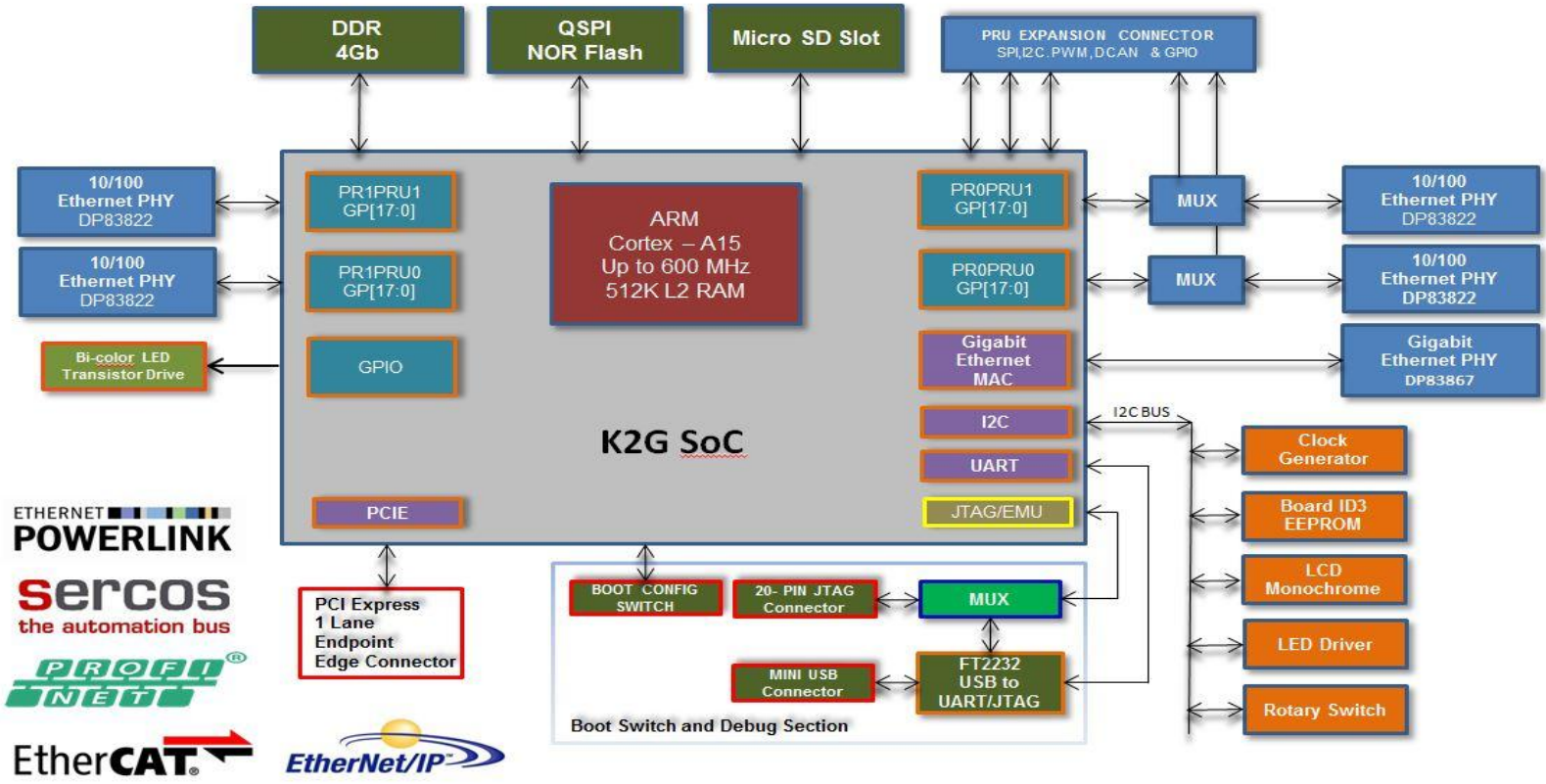
- See the Hardware Implementation Document for Design Details
- See the Hardware User Guide for Board Details
- See the PCB Build Specification for PCB Design Details

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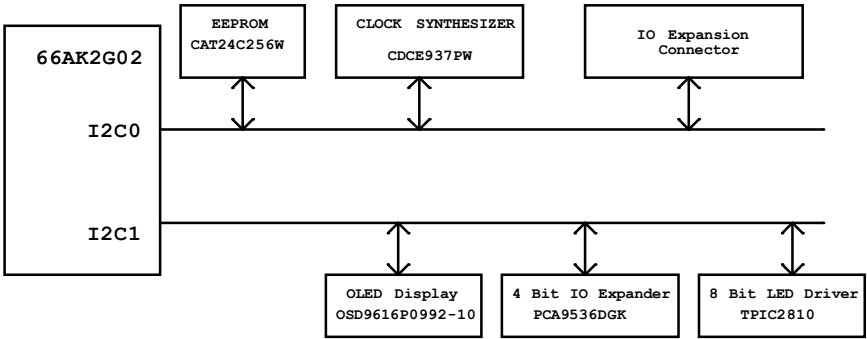
REVISION HISTORY

| VER # | DATE | DESCRIPTION OF CHANGES | AUTHOR |
|-------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|
| 0.1 | 10th FEB 2017 | R501 DNI'd from BOOTCMPLT signal (Page 06) Part number updated for Screws H9-H12 with RoHS and REACH compliant parts (Page 29) Part number updated for Screws H13-H16 with RoHS and REACH compliant parts (Page 29) | Mistral Design Team |
| 0.2 | 8th MAR 2017 | Power Cord H20 removed from Kit Content | Mistral Design Team |
| 1.0 | 8th MAR 2017 | Baselined for Production RevD | Mistral Design Team |
| | | | |

K2G ICE - INDUSTRIAL COMMUNICATION ENGINE SYSTEM BLOCK DIAGRAM

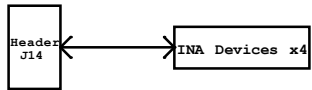


I2C TREE

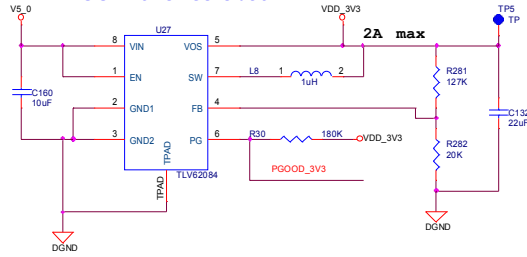


I2C ADDRESS TABLE

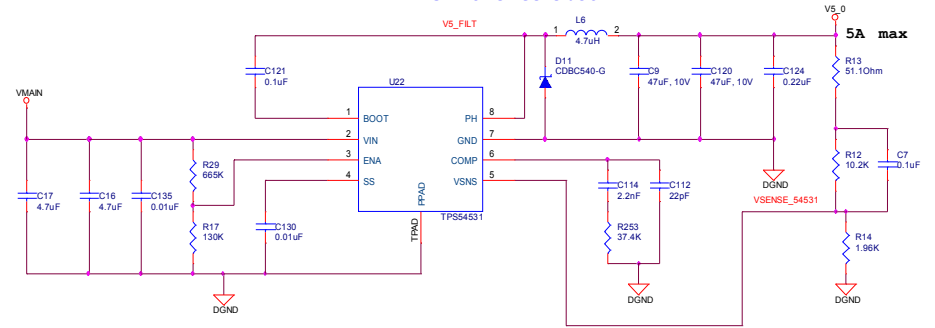
| I2C DEVICES | 7 BIT ADDRESS |
|-------------------|------------------------|
| EEPROM | 0x50 |
| OLED Display | 0x3C |
| INA Devices | 0x40, 0x41, 0x43, 0x44 |
| 4 Bit IO Expander | 0x41 |
| 8 Bit LED Driver | 0x6x |
| CLOCK SYNTHESIZER | 0x6D |



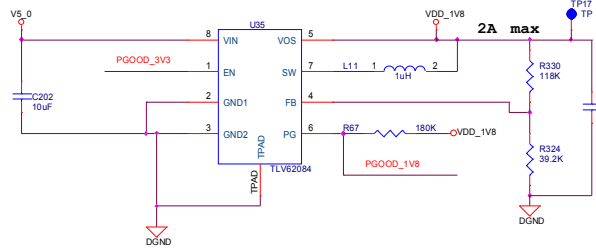
3.3V Power Generation



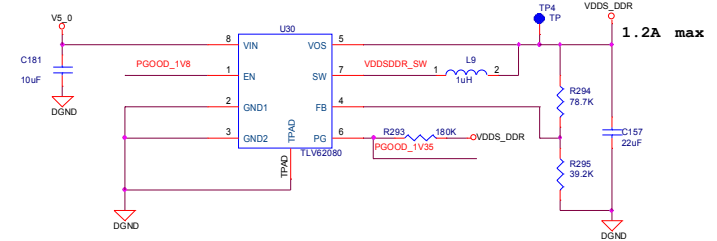
24V - 5V Power Generation



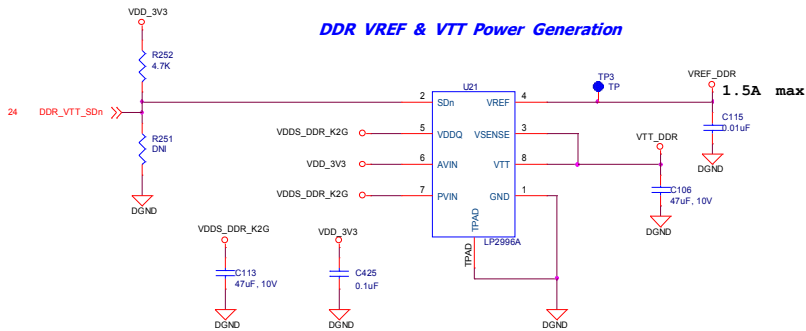
1.8V Power Generation



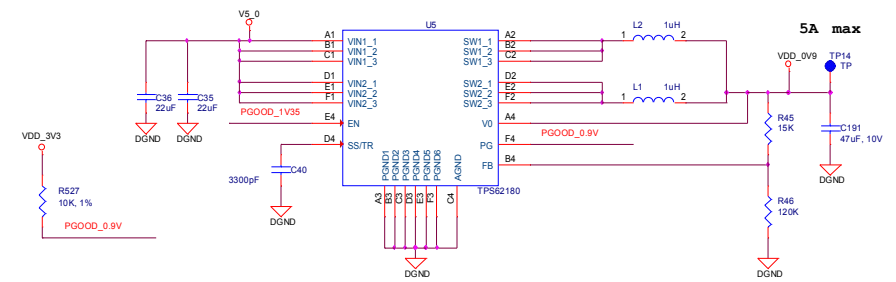
DDR3L 1.35V Power Generation



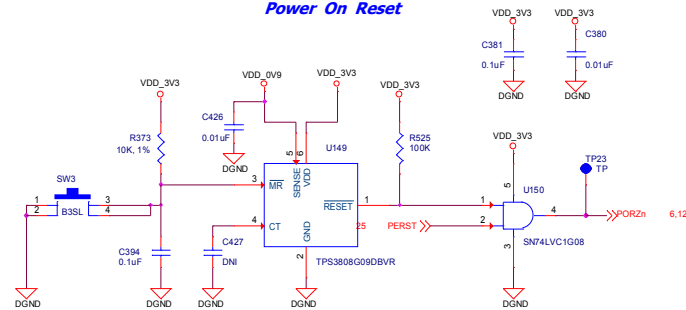
DDR VREF & VTT Power Generation



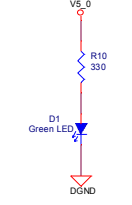
0.9V Power Generation



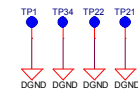
Power On Reset



Power On LED

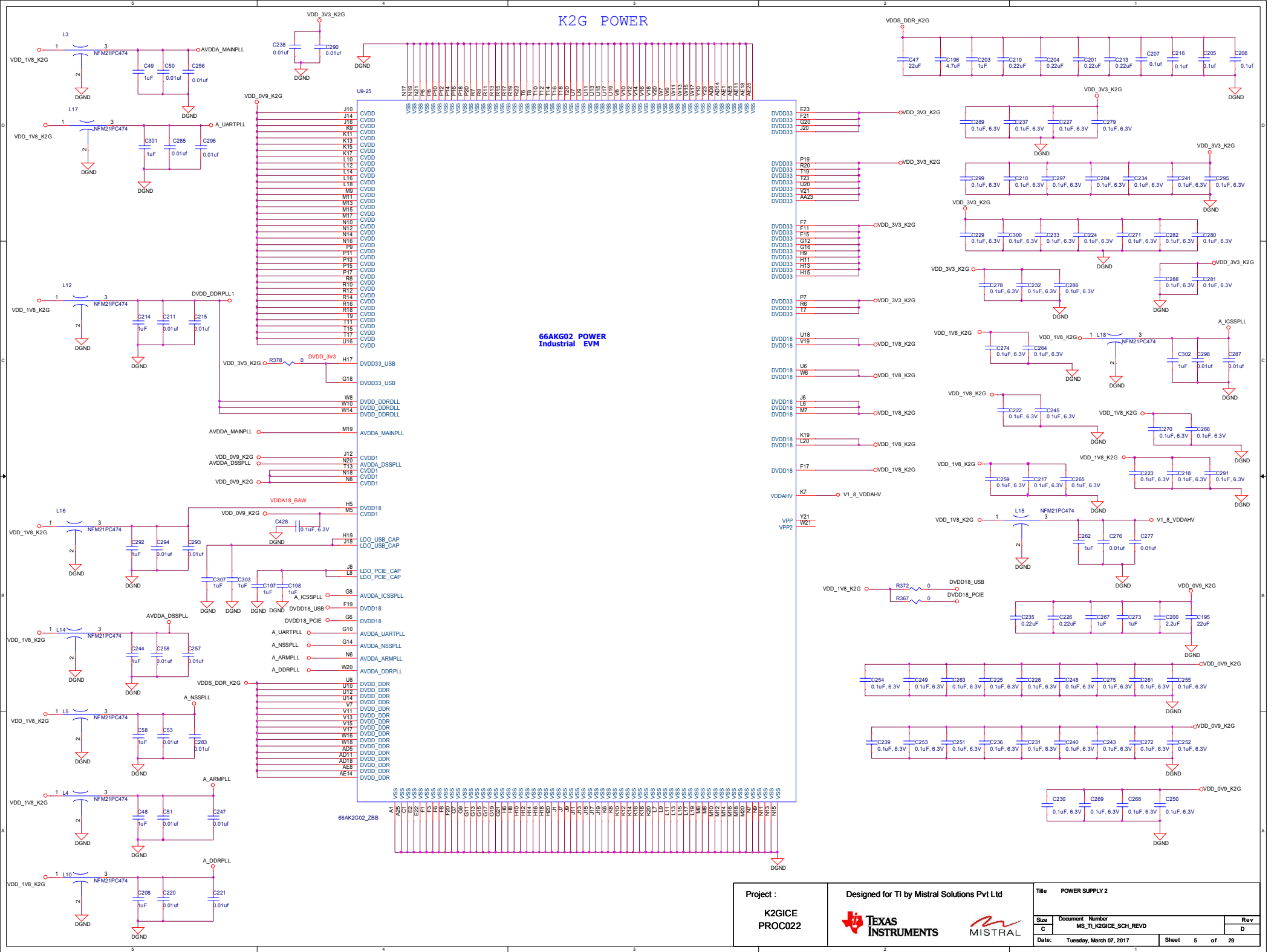


GROUND PROBING POINTS



| | | | |
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| K2GICE PROC022 |   | Size | Document Number |
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| | | Date: | Tuesday, March 07, 2017 |
| | | Sheet | 4 of 29 |

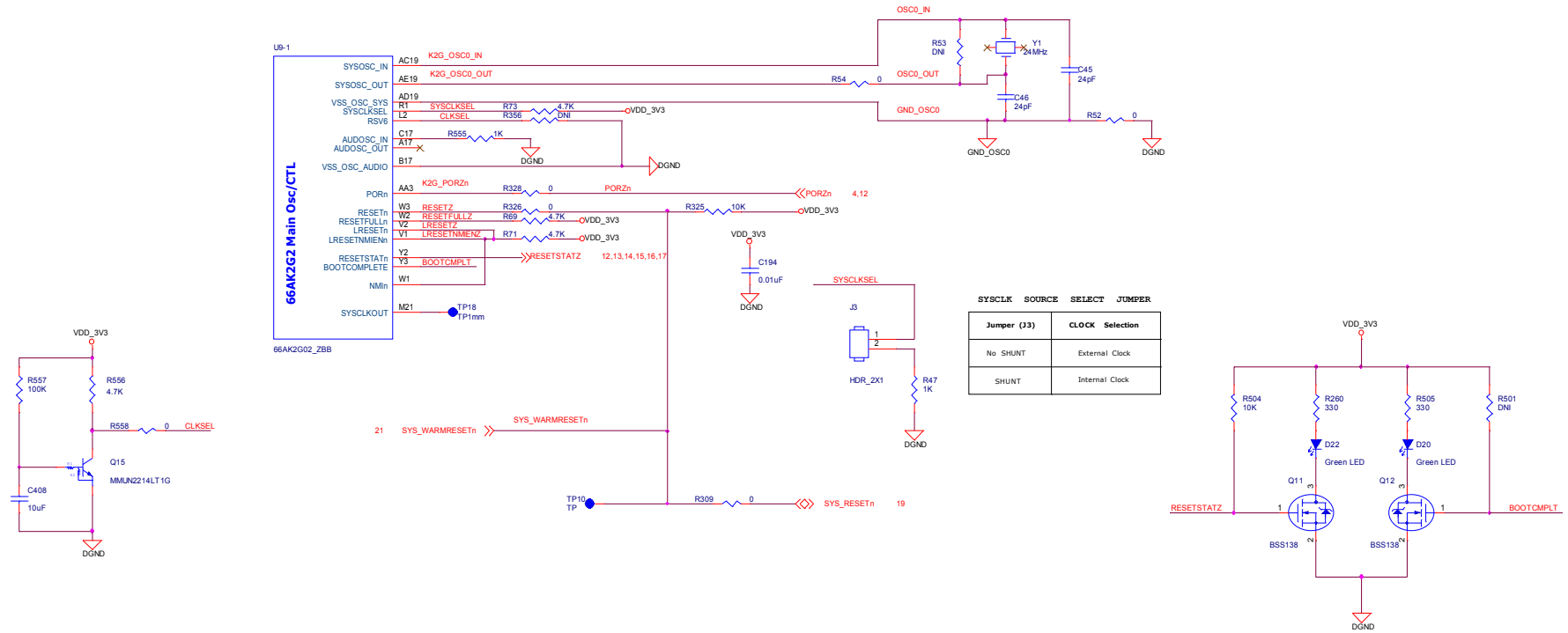
K2G POWER



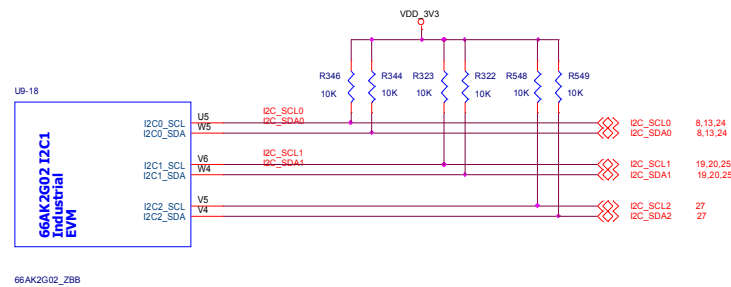
66AKG02_POWER Industrial EVB

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| | | Date: | Tuesday, March 07, 2017 |
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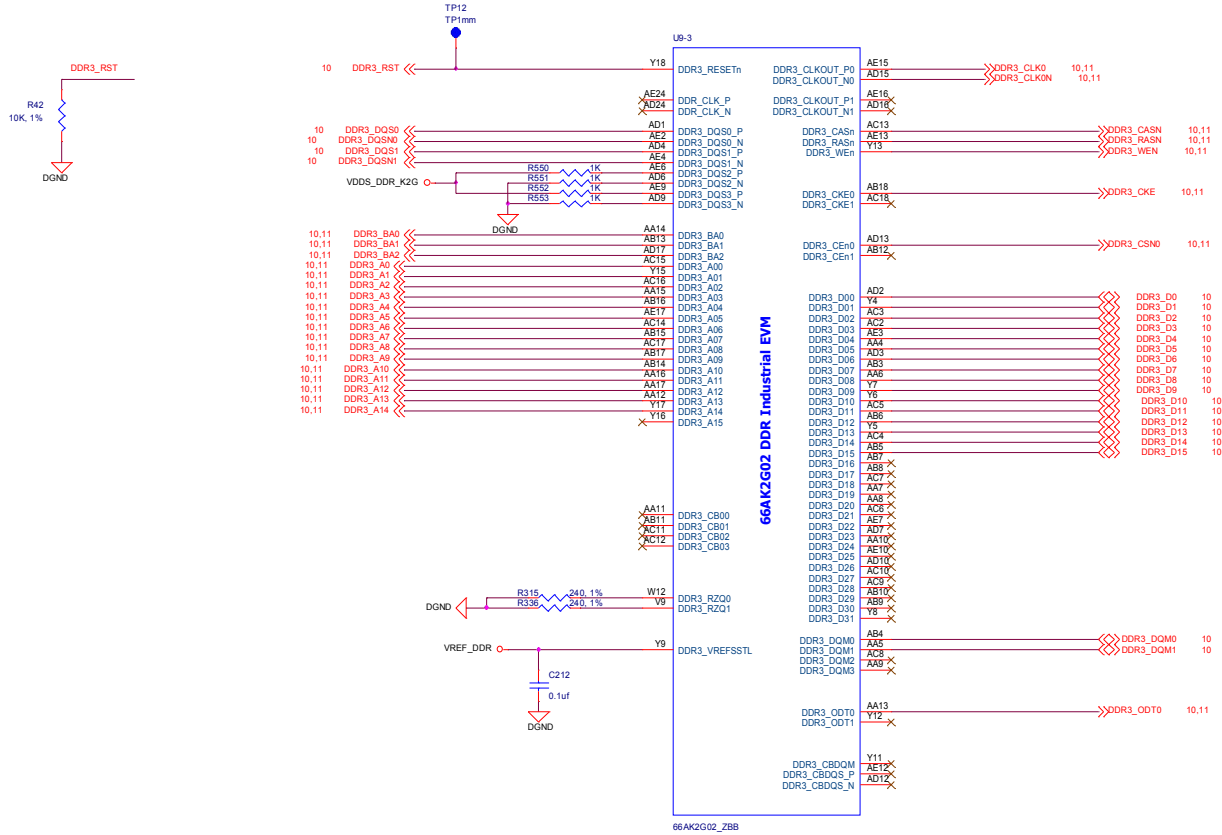
K2G CLOCK & RESET



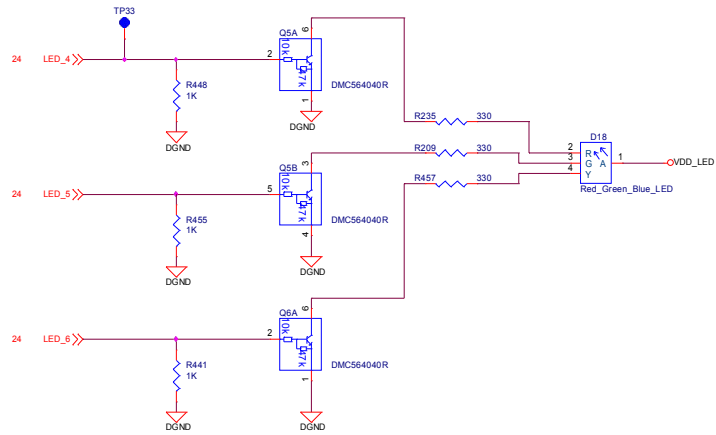
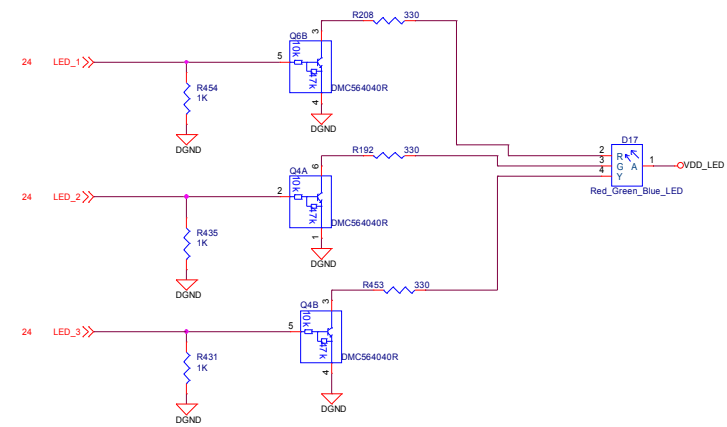
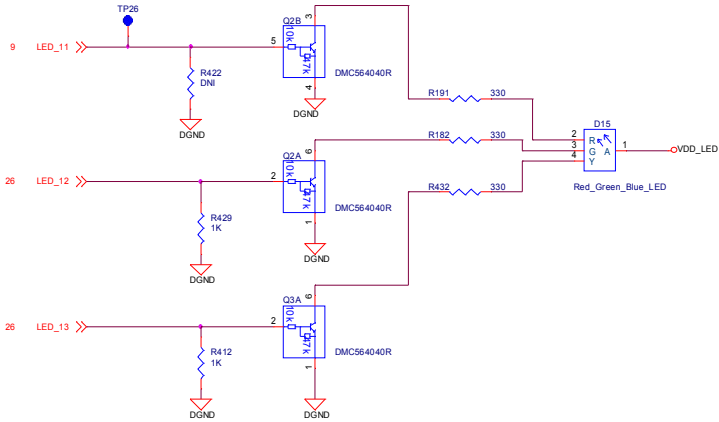
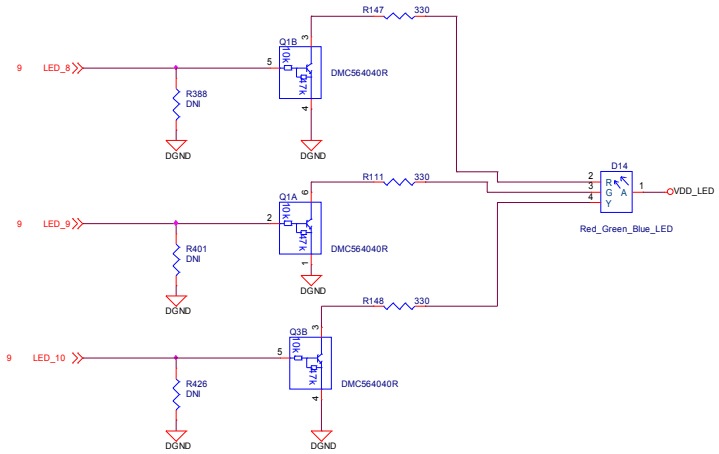
I2C



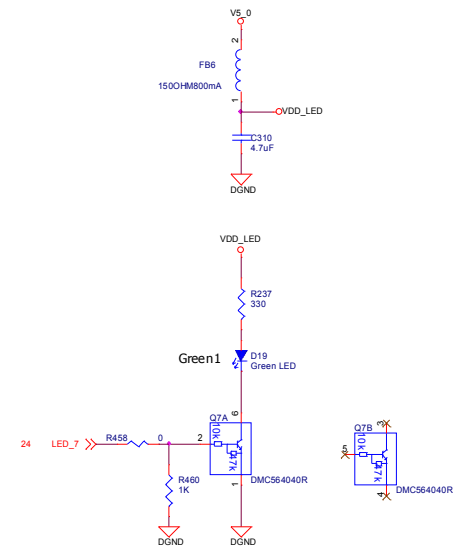
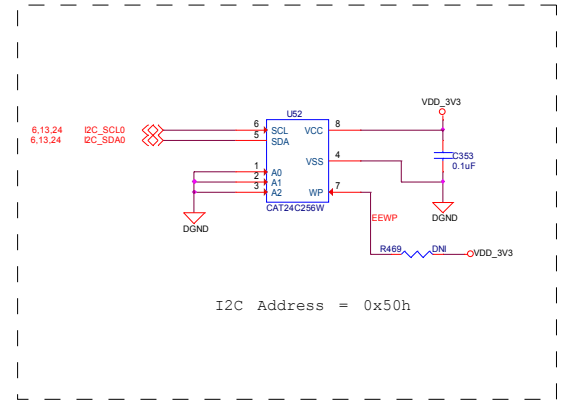
DDR3L INTERFACE



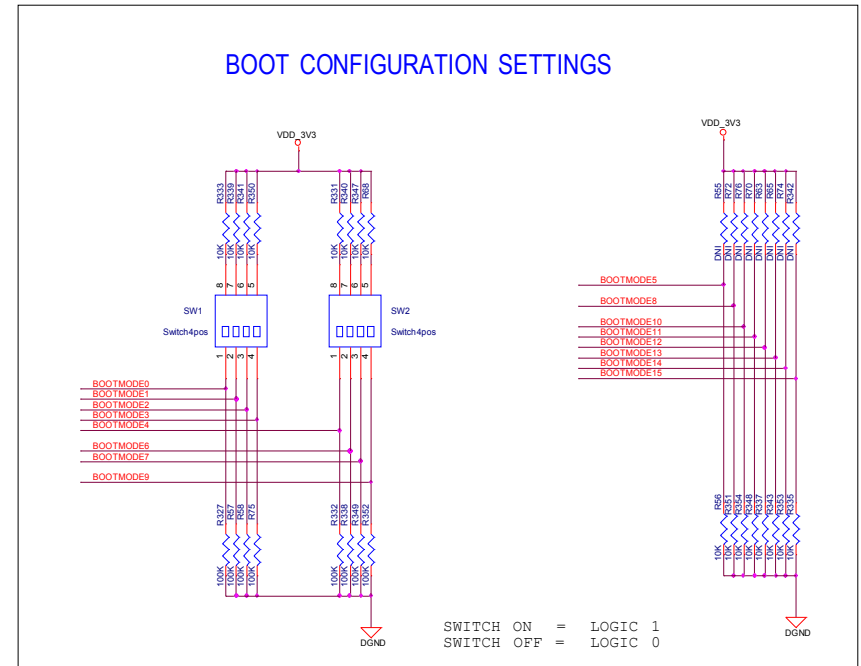
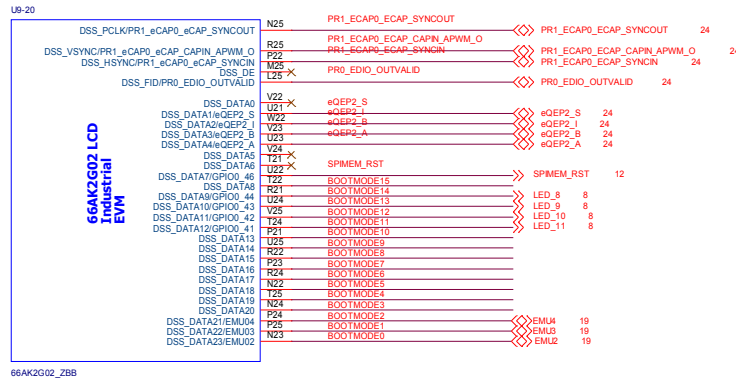
ETHERNET LEDS



BOARD ID EEPROM



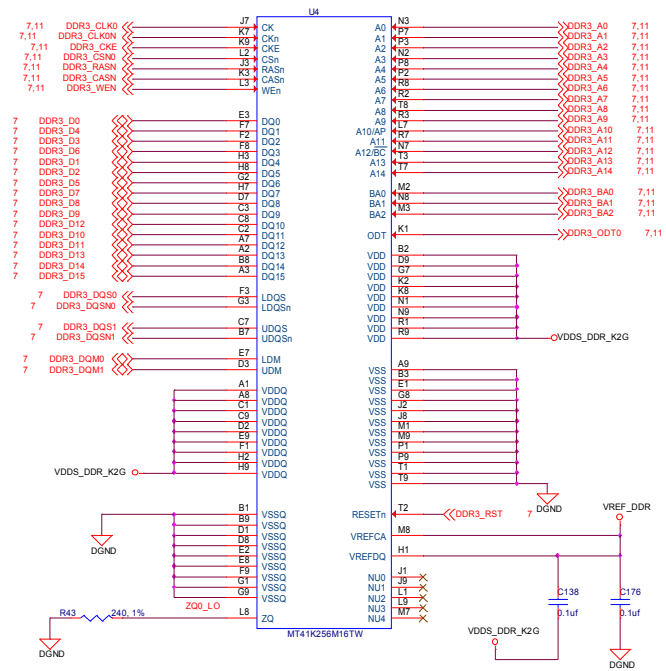
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| C | MS_TI_K2GICE_SCH_REV D | | | D | |
| Date: | Tuesday, March 07, 2017 | Sheet | 8 | of 29 | |



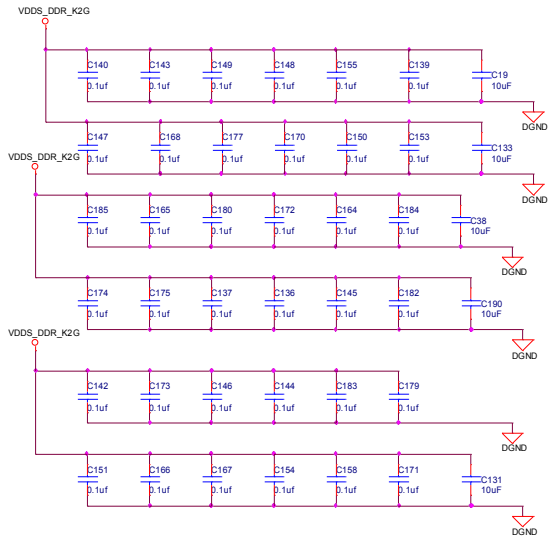
BOOT MODES SUPPORTED

1. QSPI48
2. QSPI96
3. SD CARD
4. EMULATOR
5. PCIe

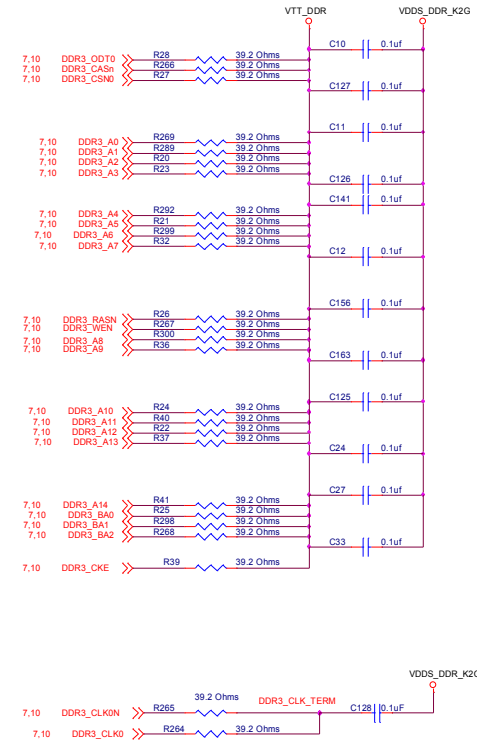
DDR3L



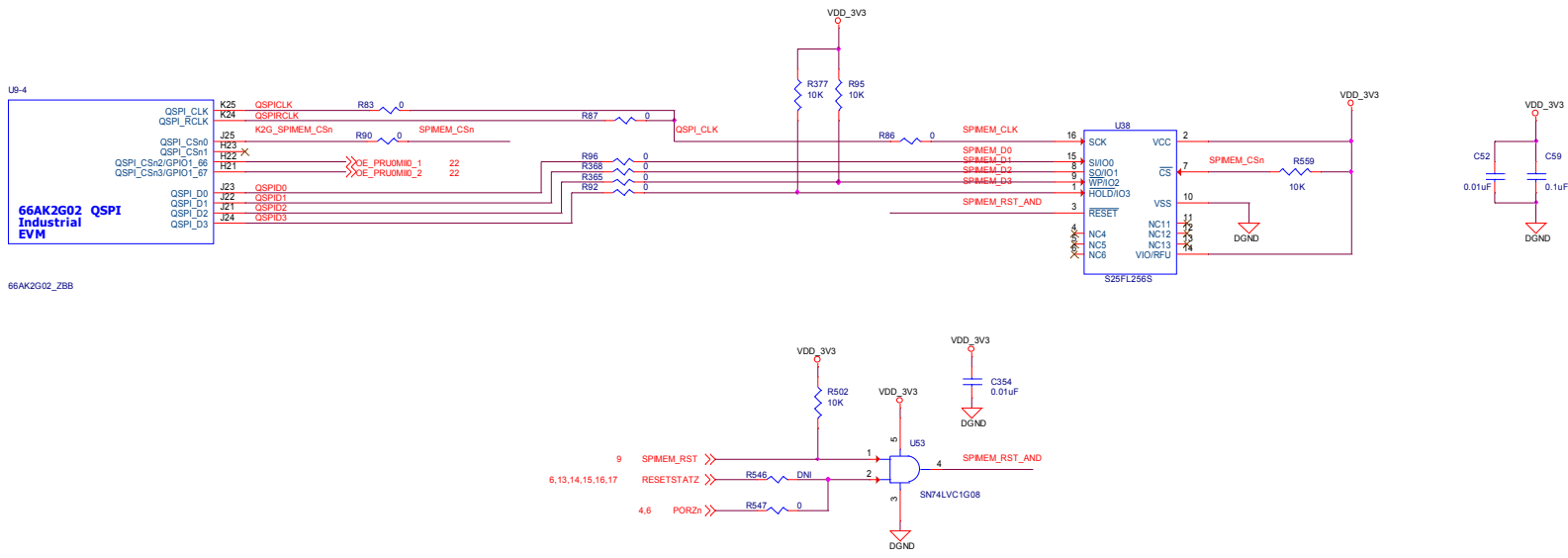
DDR3 SECTION DE-CAPS



DDR3 SECTION TERMINATIONS



QSPI Flash

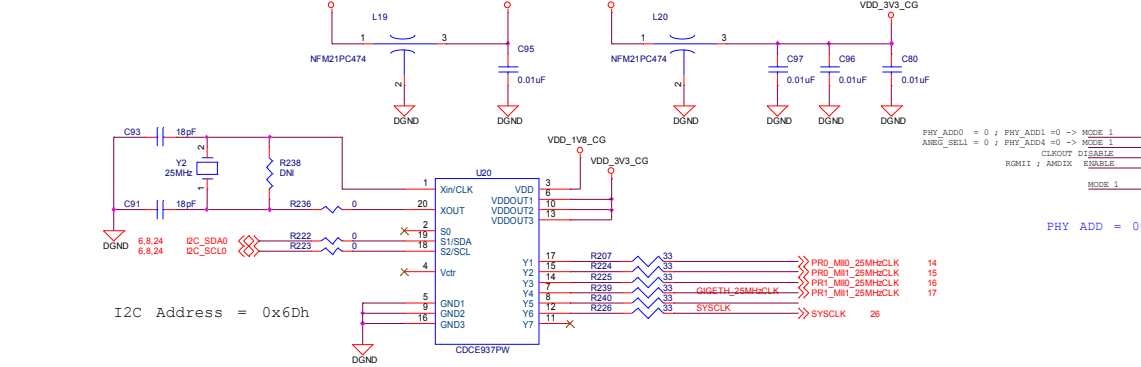
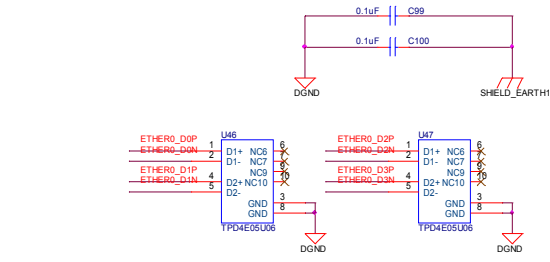
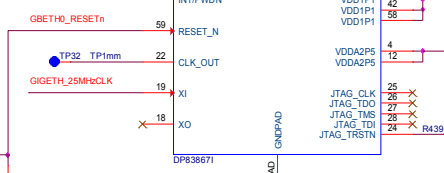
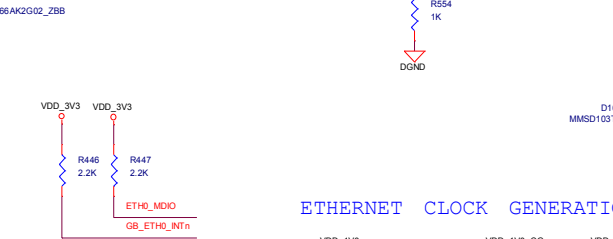
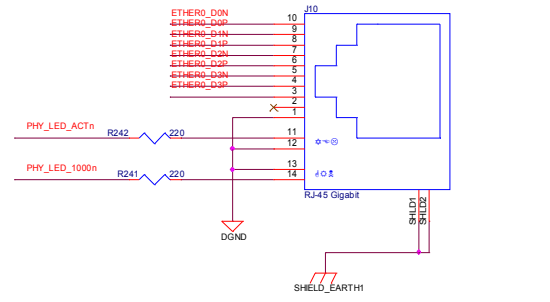
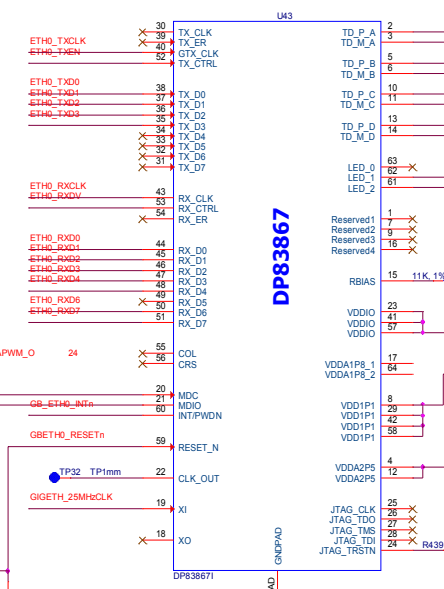
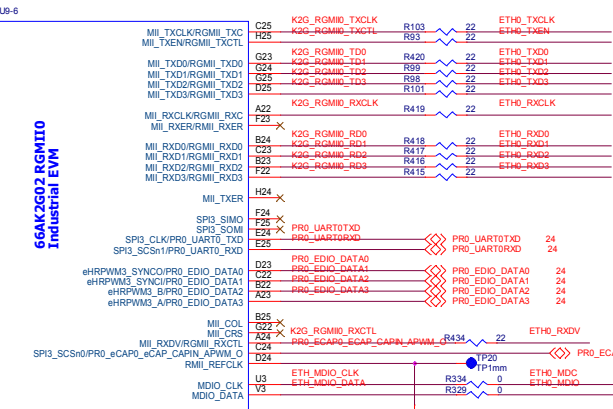


66AK2G02 QSPI Industrial EVM

66AK2G02_ZBB

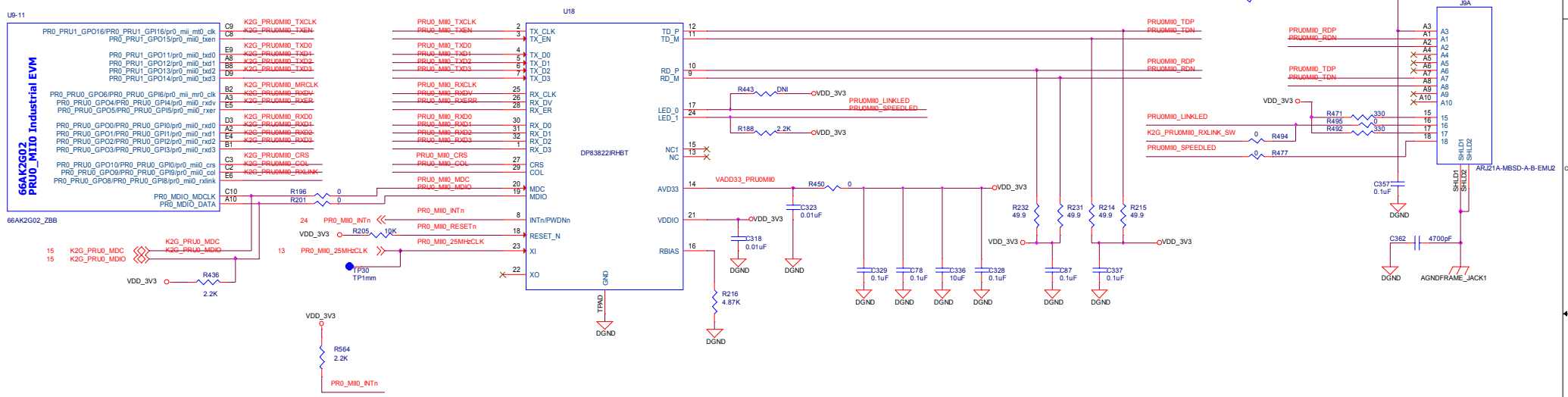
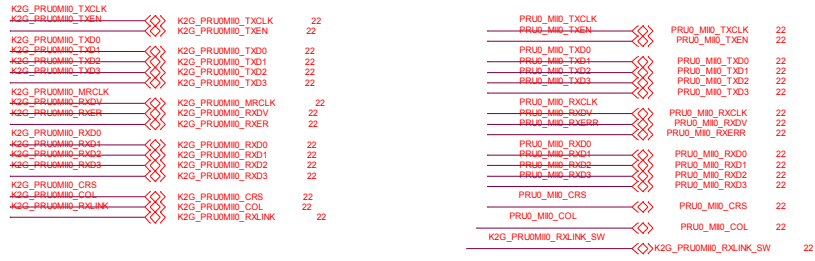
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| Date: Tuesday, March 07, 2017 | Sheet: 12 | of: 29 | | | |

GIGABIT ETHERNET

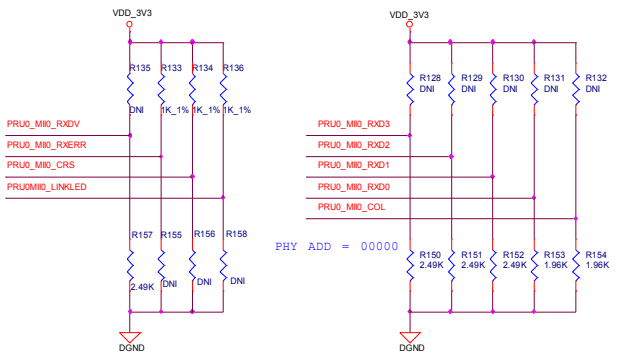


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| C | | | | D |
| Date: | Tuesday, March 07, 2017 | Sheet | 13 | of 29 |

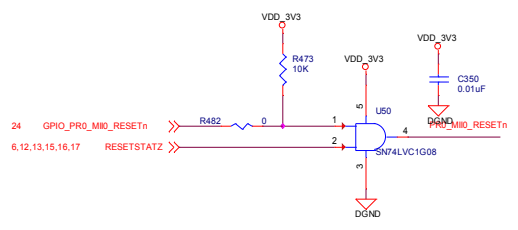




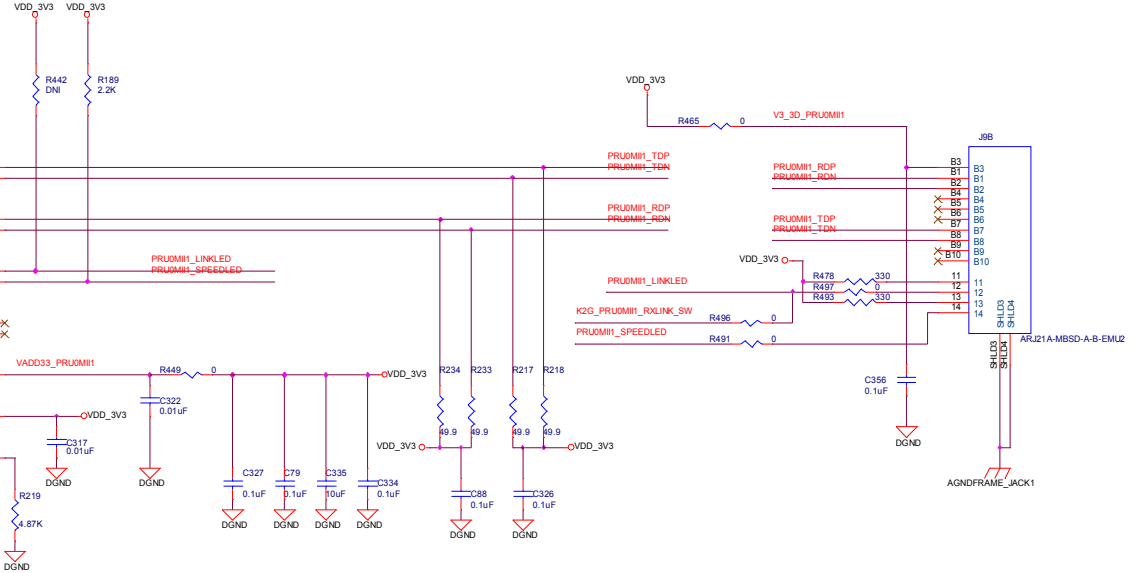
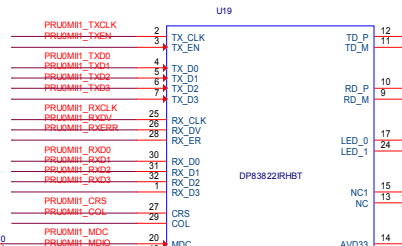
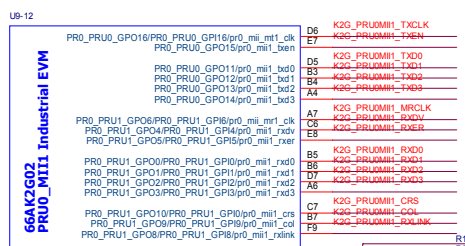
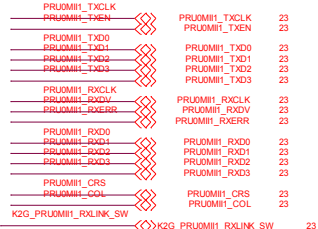
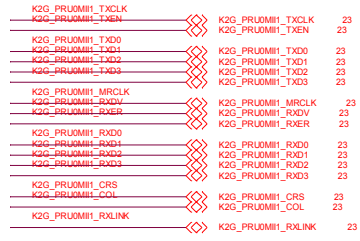
RESISTOR STRAPPING



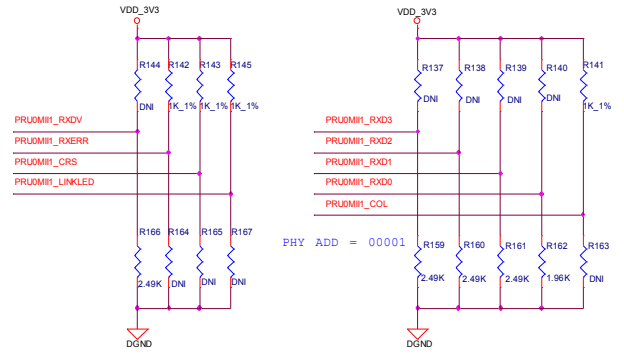
ETHERNET RESET



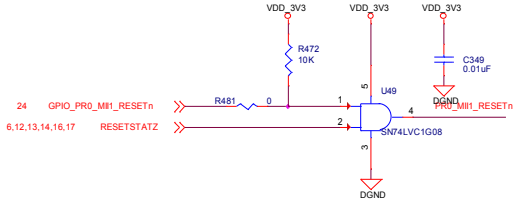
ETHERNET 1



RESISTOR STRAPPING

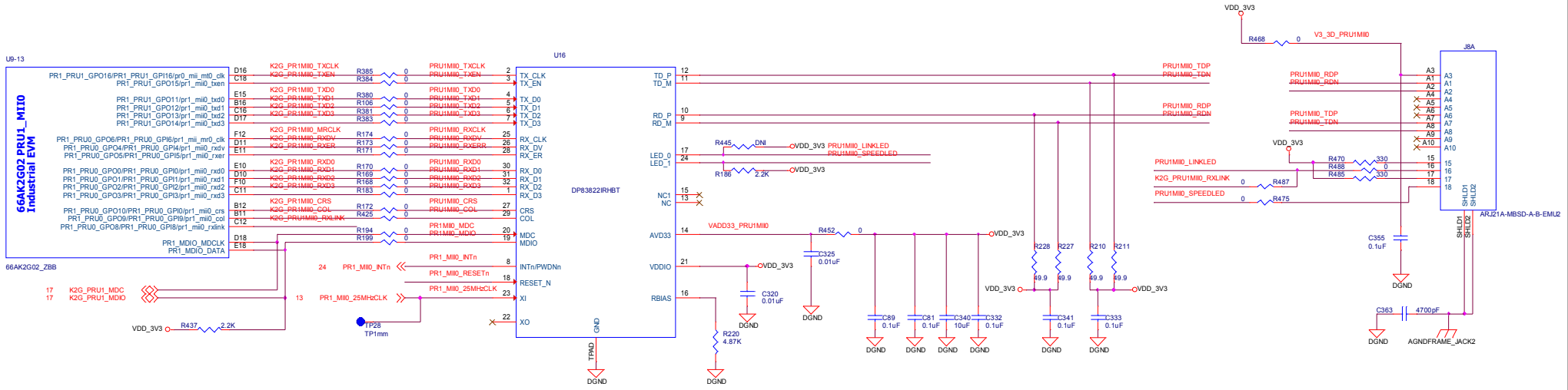


ETHERNET RESET



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| K2GICE PROC022 | TEXAS INSTRUMENTS | Size | Document Number |
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| | | Date: | Tuesday, March 07, 2017 |
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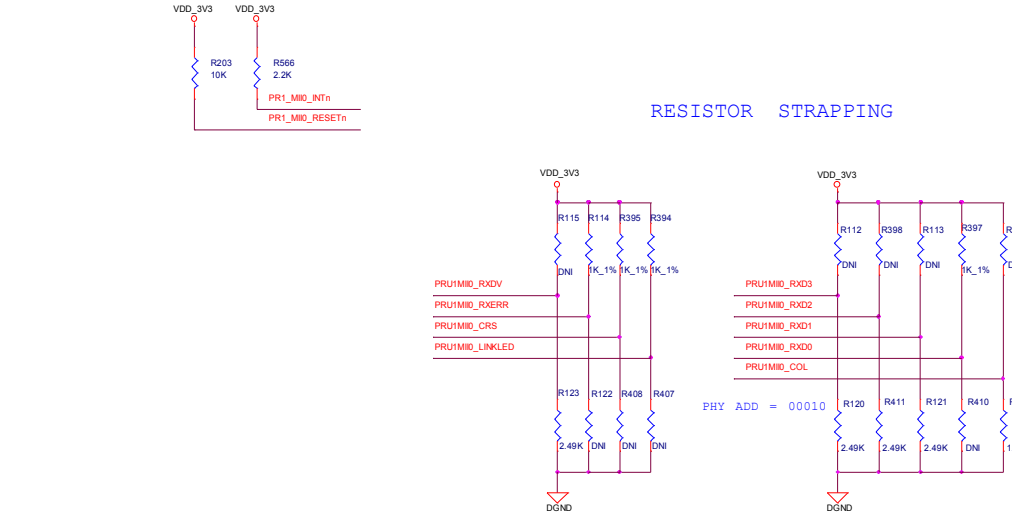
ETHERNET 2



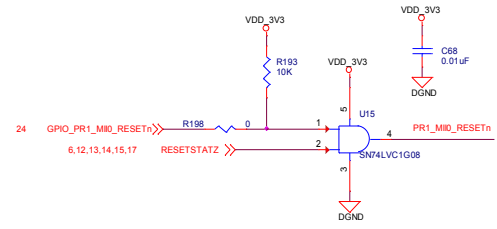
66AK2G02 PRU1_MII0 Industrial EVM

UB-13

RESISTOR STRAPPING

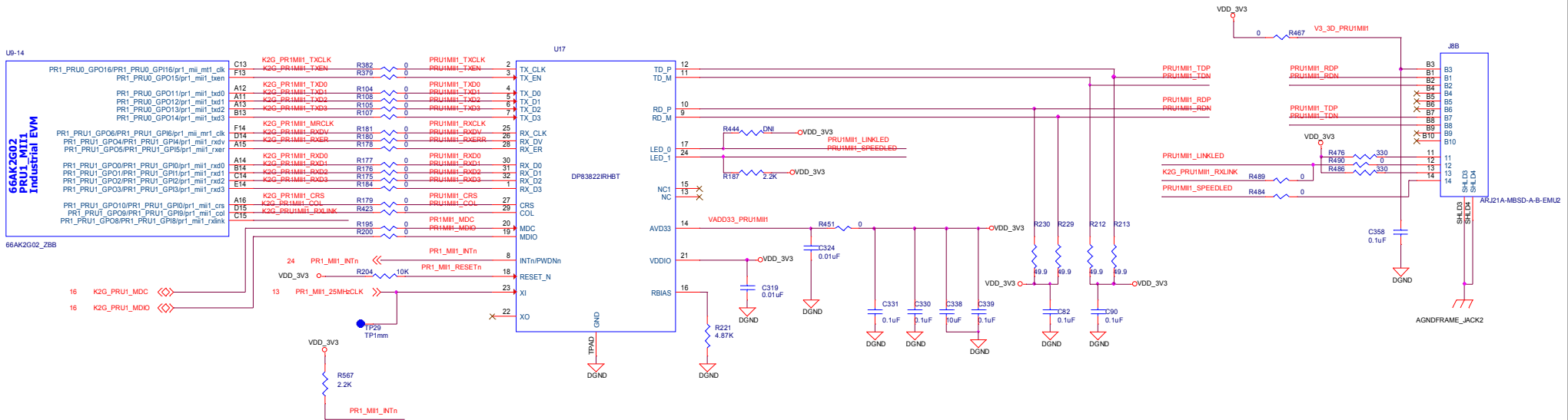


ETHERNET RESET

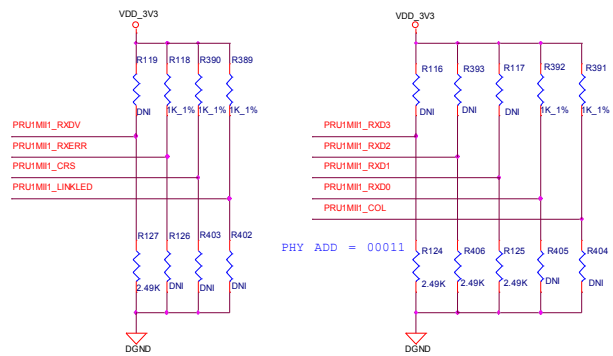


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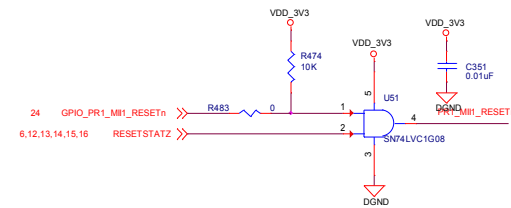
ETHERNET 3



RESISTOR STRAPPING



ETHERNET RESET



Project :
K2GICE
PROC022

Designed for TI by Mistral Solutions Pvt Ltd



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Size: Document Number
C: MS_TI_K2GICE_SCH_REV D

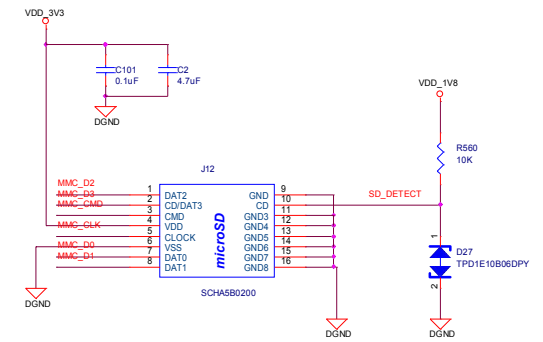
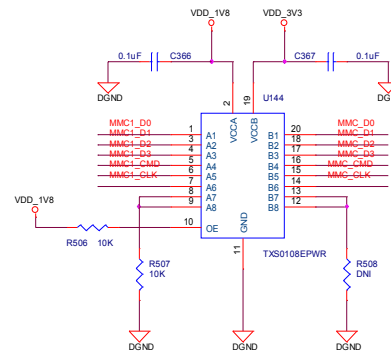
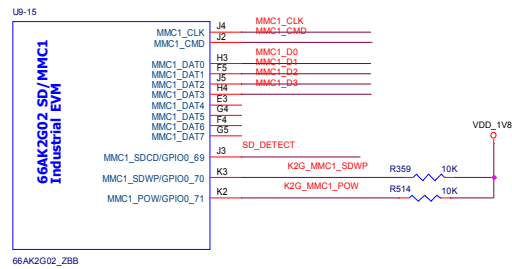
Date: Tuesday, March 07, 2017

Rev: D

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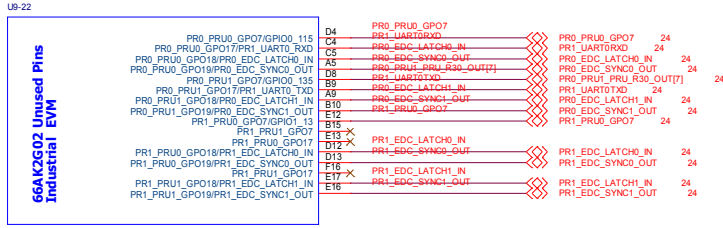
SD/MMC1 Port

SD/MMC1 1.8V to 3.3V VOLTAGE TRANSLATION

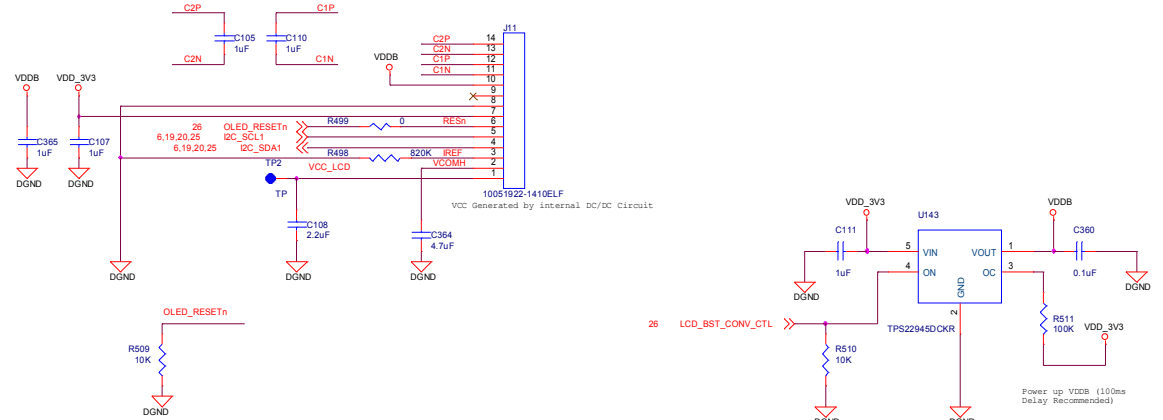


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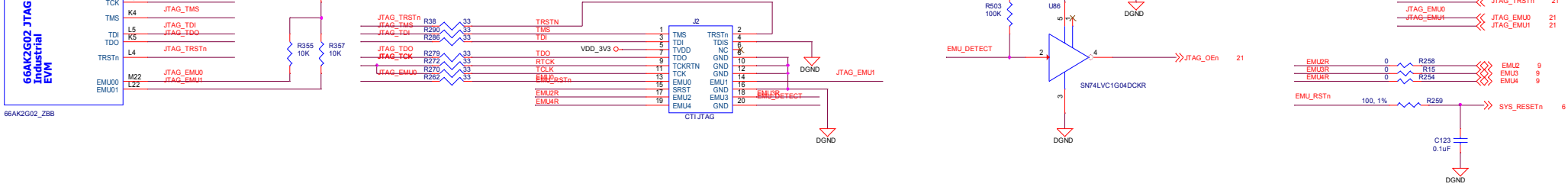
SMART REFLEX & MISC



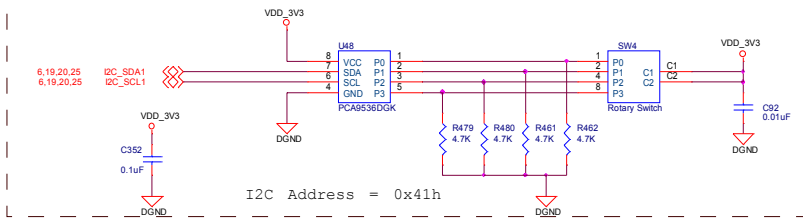
MONOCHROME LCD INTERFACE



U9-19

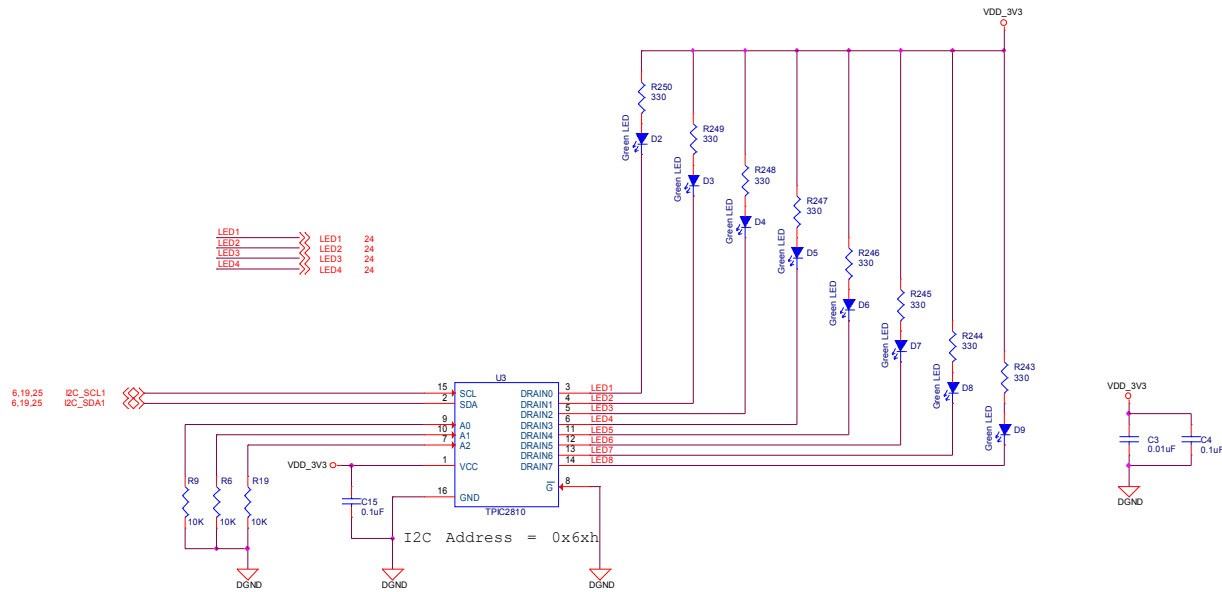


ROTARY SWITCH - INDUSTRIAL ETHERNET SLAVE ADDRESS SELECTOR

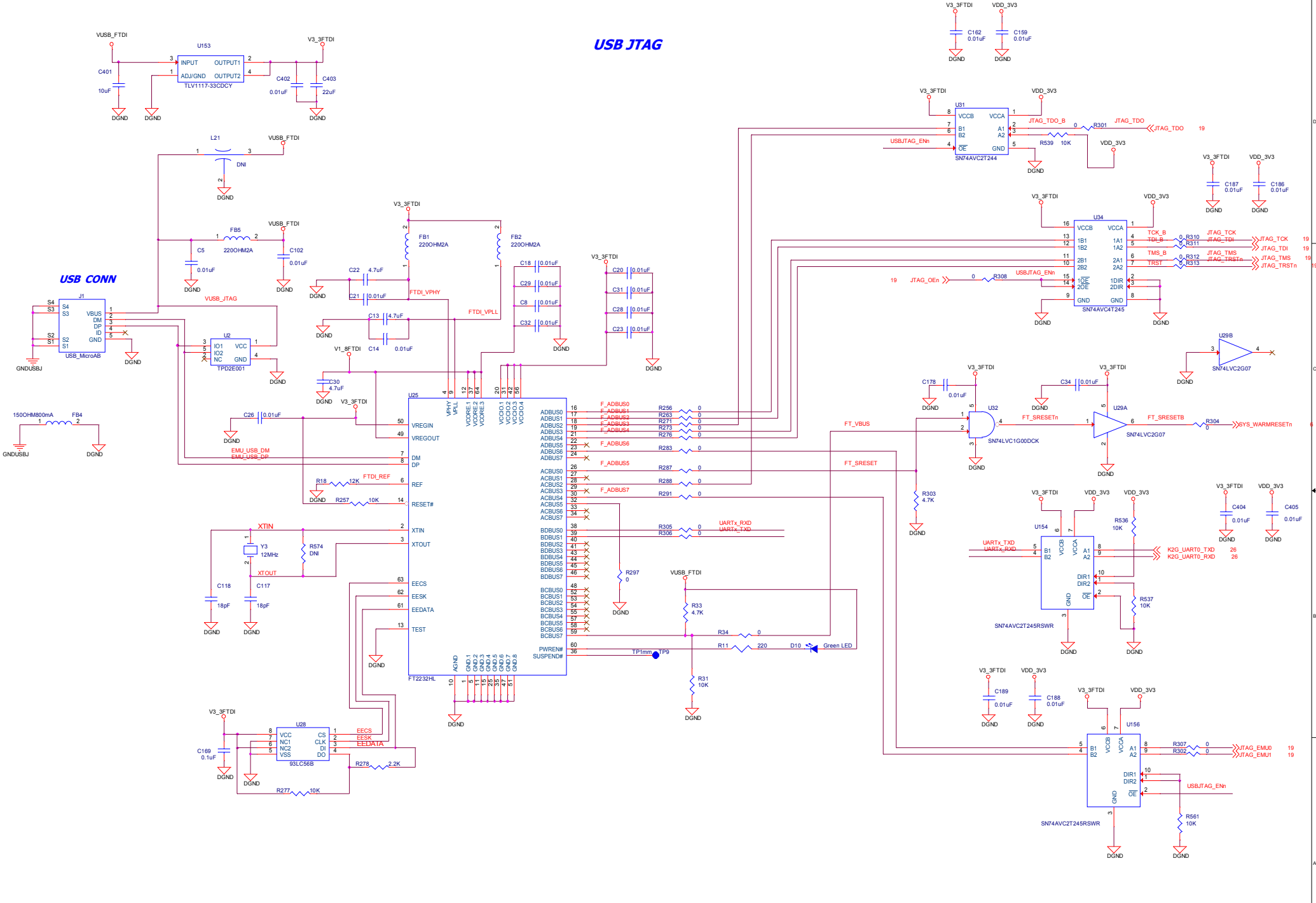


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| K2GICE | | Size | Document Number |
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INDUSTRIAL OUTPUT LEDES

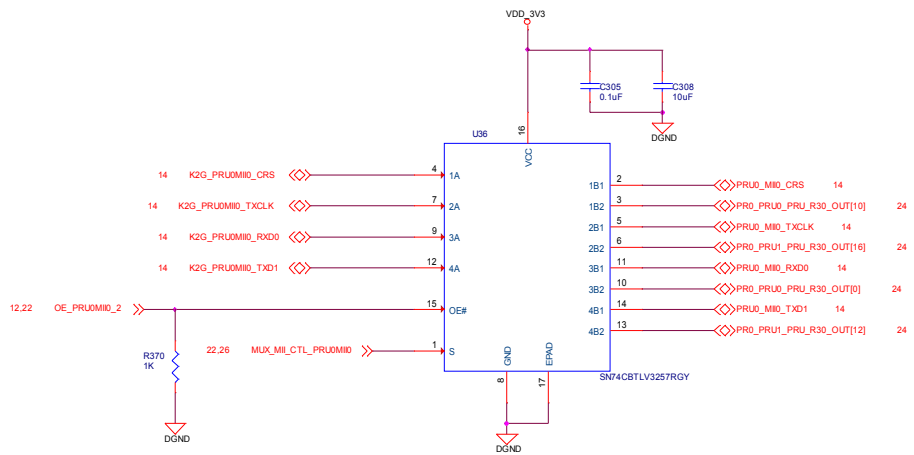
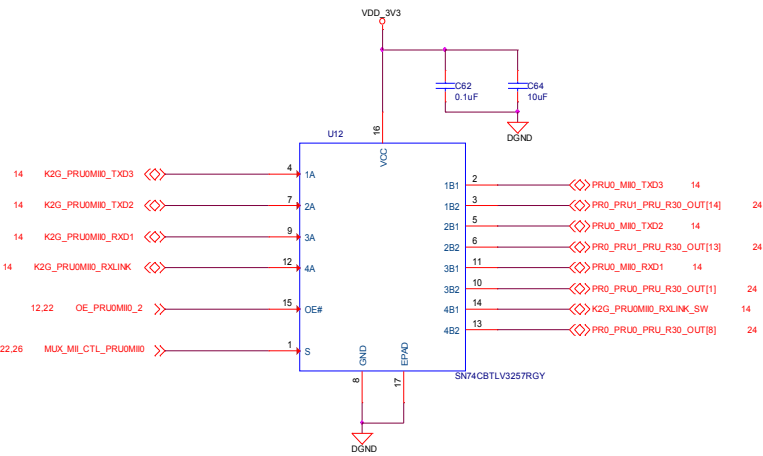
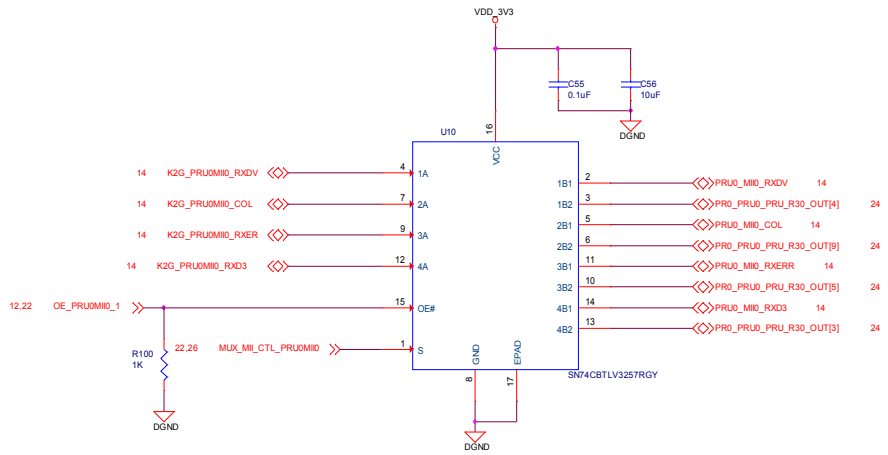
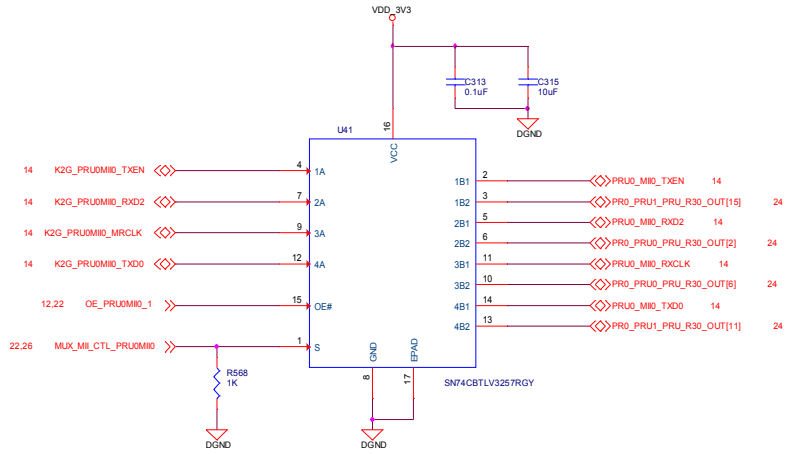


USB JTAG



| Project : K2GICE PROC022 | | Designed for TI by Mistral Solutions Pvt Ltd | | Title: USB JTAG | | | | | | | | | | | |
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| Size | Document Number | Rev | | | | | | | | | | | | | |
| C | MS_TL_K2GICE_SCH_REV D | D | | | | | | | | | | | | | |
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MUX/DEMUX 1



Project :
K2GICE
PROC022

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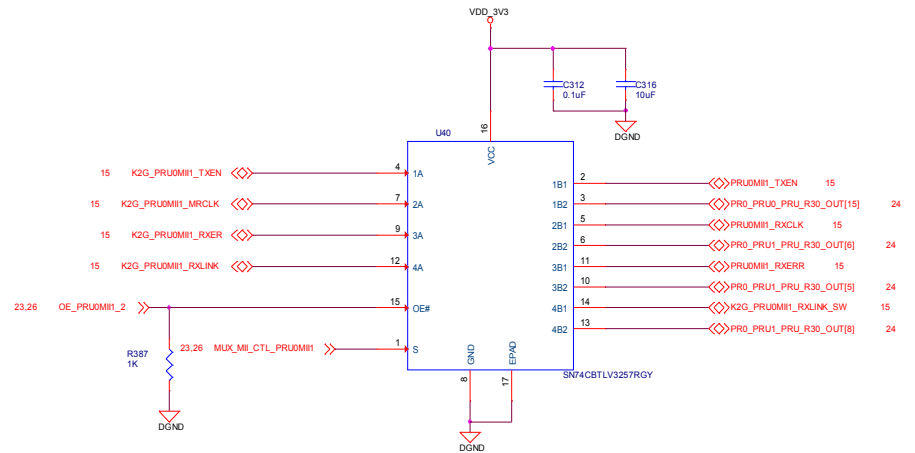
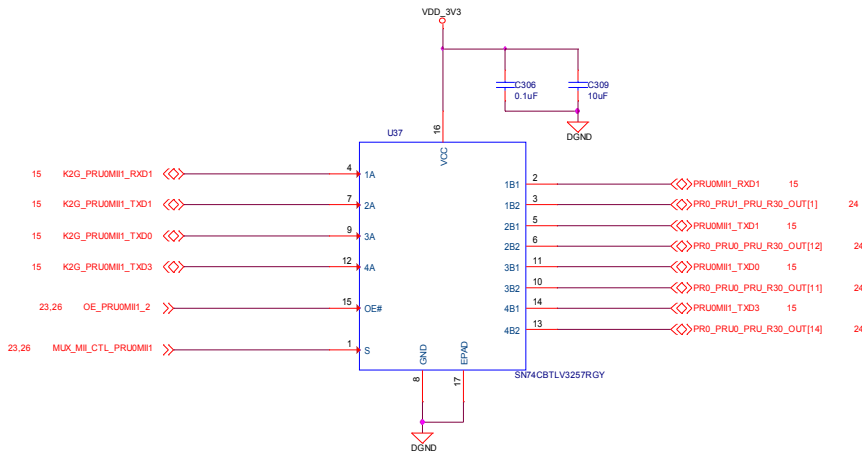
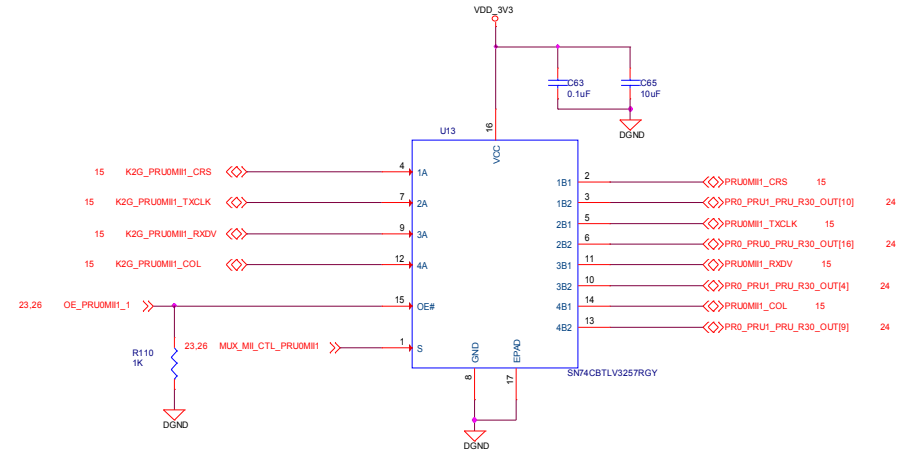
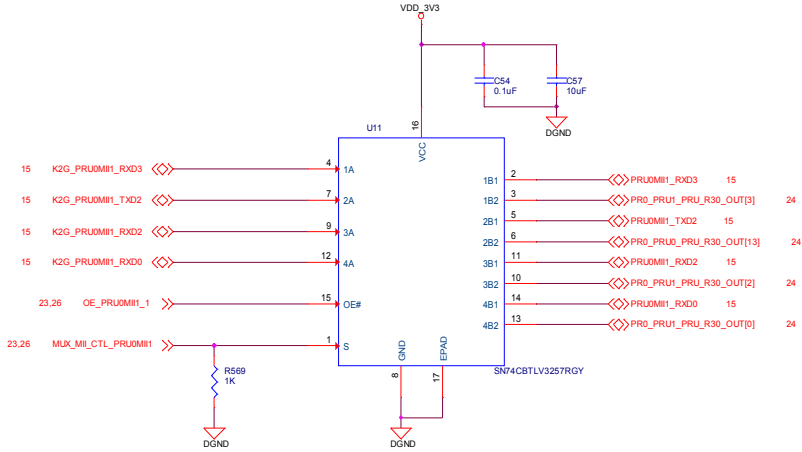
Title MUX_DEMUX1

| | | |
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| Size | Document Number | Rev |
| C | MS_TL_K2GICE_SCH_REV D | D |

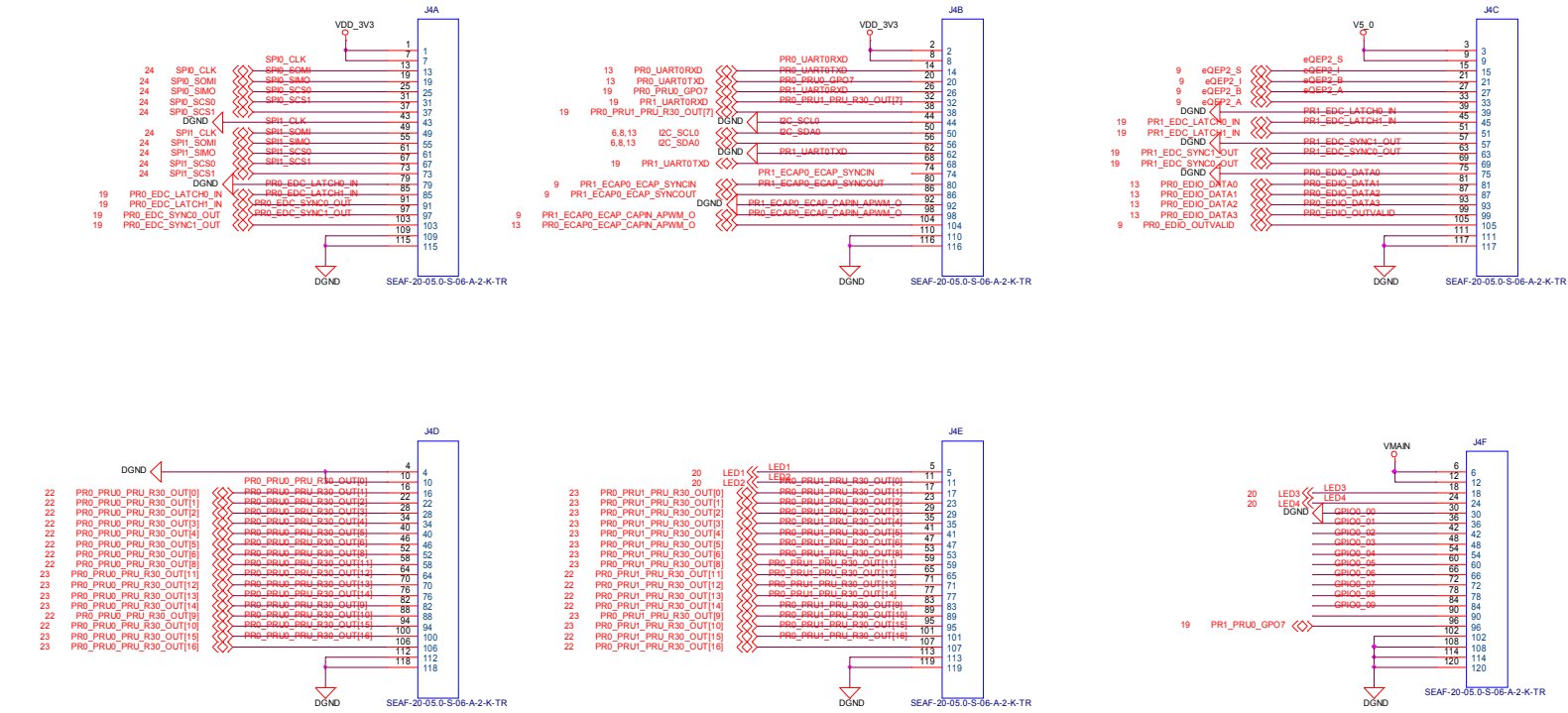
Date: Tuesday, March 07, 2017

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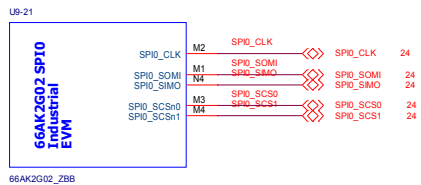
MUX DEMUX 2



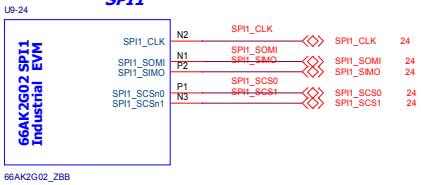
EXPANSION CONNECTOR



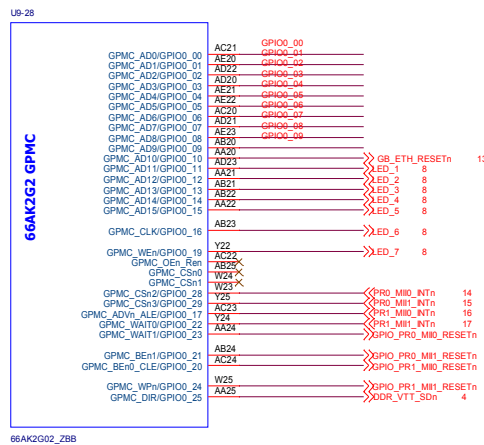
SPI0



SPI1



GPIO EXPANSION



Project :



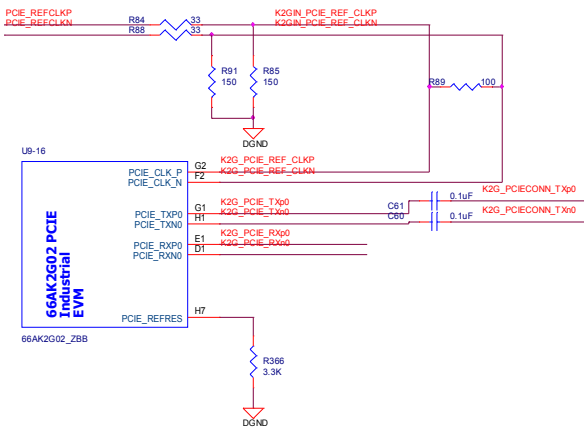
Designed for TI by Mistral Solutions Pvt Ltd



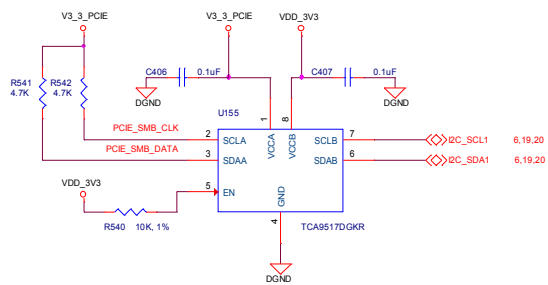
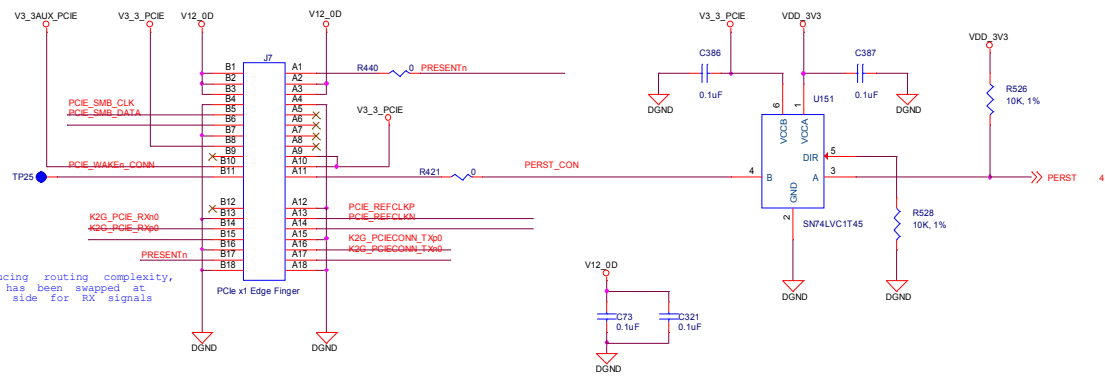
Title EXPANSION_HEADER

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|------|------------------------|-----|
| C | MS_TI_K2GICE_SCH_REV D | D |

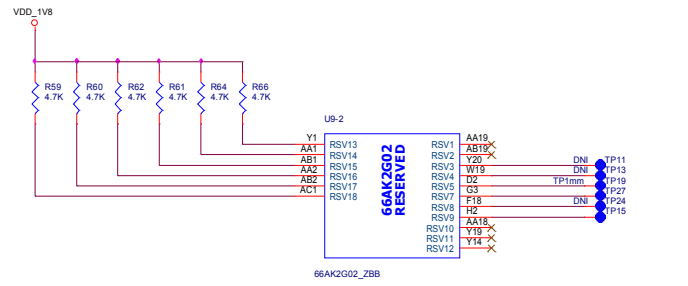
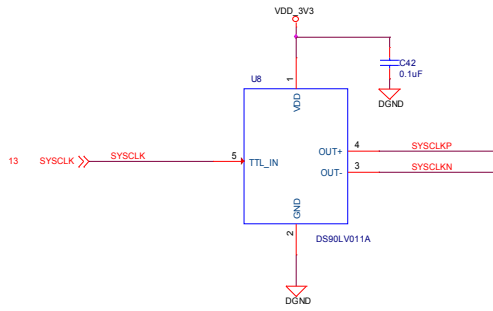
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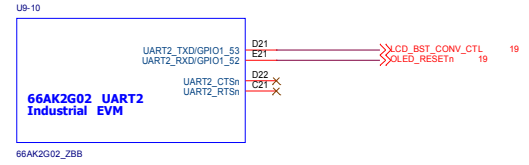
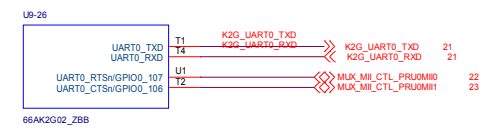
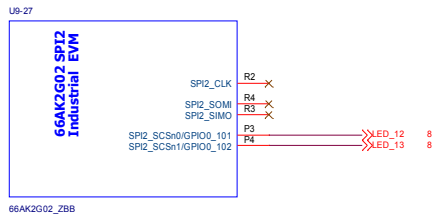
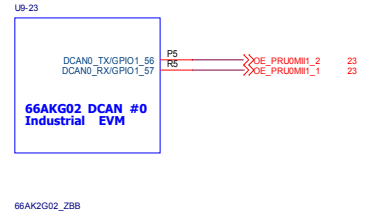
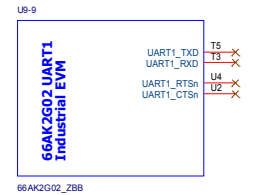
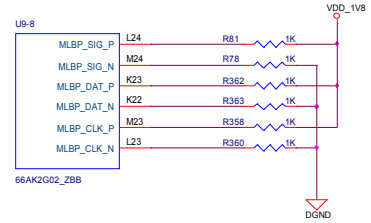
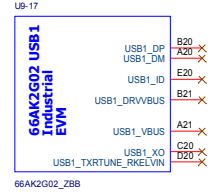
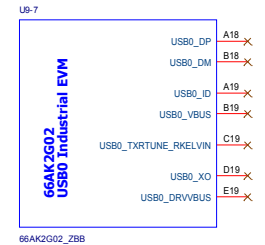
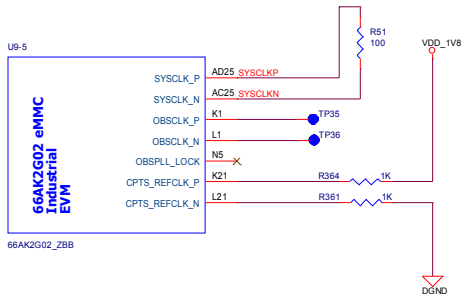
PCIe Edge Fingers



| | | | | | |
|----------------------------------------|-----------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--------------------------|--|
| Project : K2GICE PROC022 | | Designed for TI by Mistral Solutions Pvt Ltd   | | Title: PCIe x1 CONNECTOR | |
| Size: C | Document Number: MS_TL_K2GICE_SCH_REV D | Rev: D | | | |
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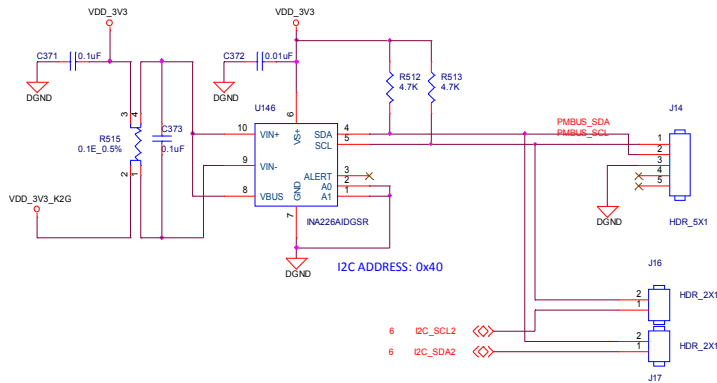


GPIOs / UNUSED PINS

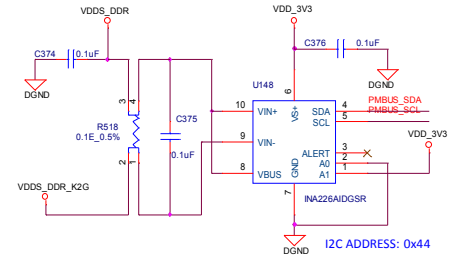
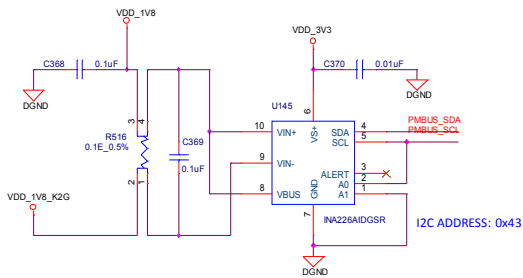
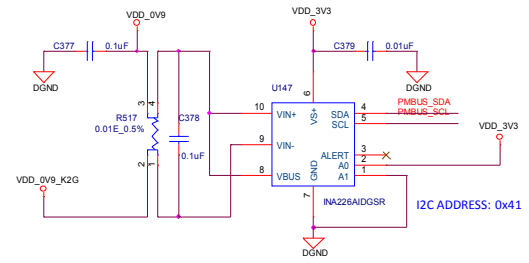


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| Project : K2GICE PROC022 | | Designed for TI by Mistral Solutions Pvt Ltd   | | Title: GPIOs | |
| Size | Document Number | | | Rev | |
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INA DEVICES



Note :- Put the Shut to J16 & J17 for connecting INA devices to the Processor



Project :

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PROC022

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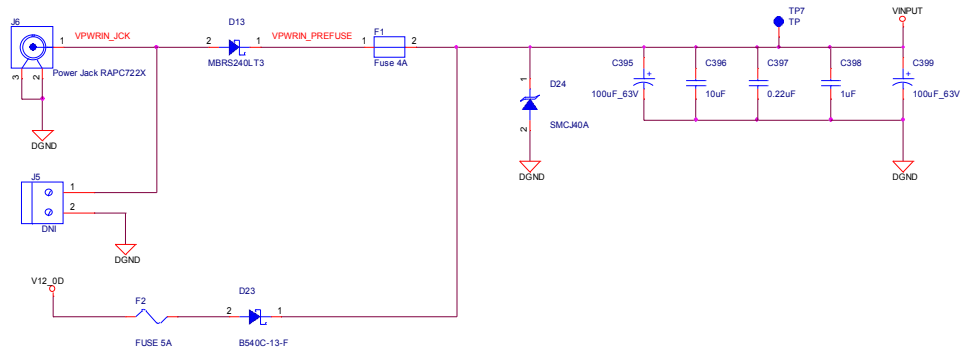
Title CURRENT MEASUREMENT

Size Document Number
C MS_TI_K2GICE_SCH_REV D

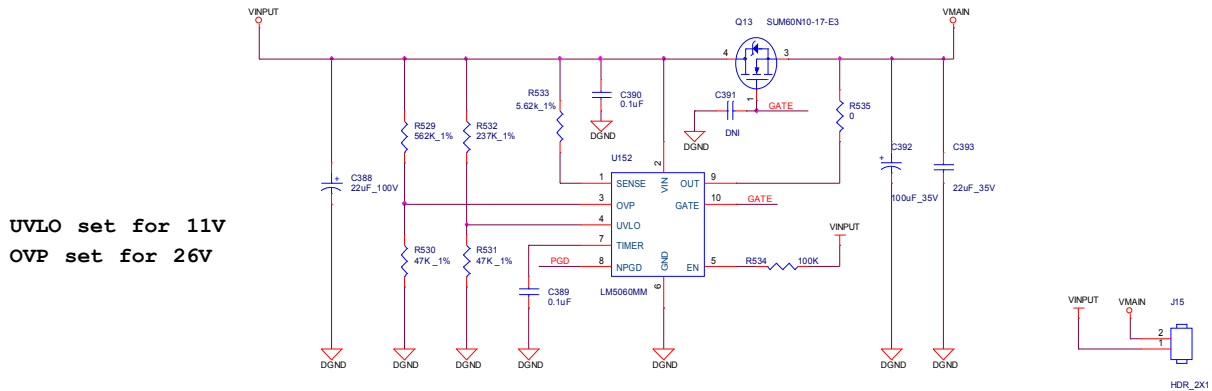
Date: Tuesday, March 07, 2017

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Main 24VDC & PCIe 12DC Power Input

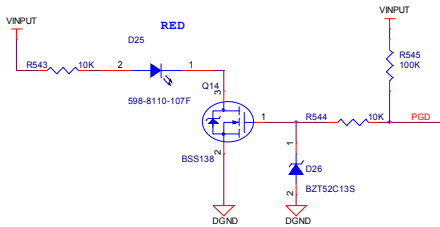


Over Voltage Protection Circuit



UVLO set for 11V
OVP set for 26V

Fault Indication



| Condition | LED Status (D25) |
|---------------------------------|------------------|
| VININPUT between 11 to 26V | OFF |
| VININPUT above 26V or below 11V | ON |

Note:- When fault is indicated ,set to proper voltage and power cycle the board.

Project :
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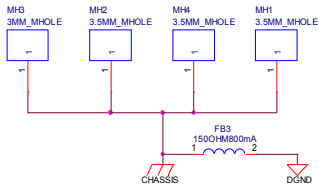
Title POWER ORING & OVP CIRCUIT

Size Document Number
C MS_TL_K2GICE_SCH_REV D
Date: Tuesday, March 07, 2017

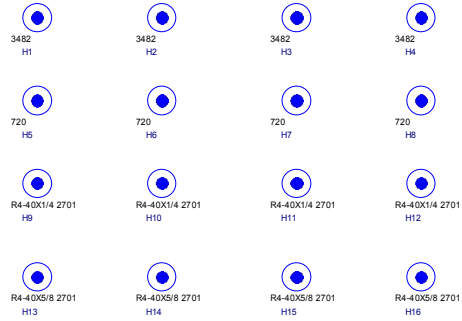
Rev D
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HARDWARE SCHEMATICS

MOUNTING HOLES



STANDOFFS

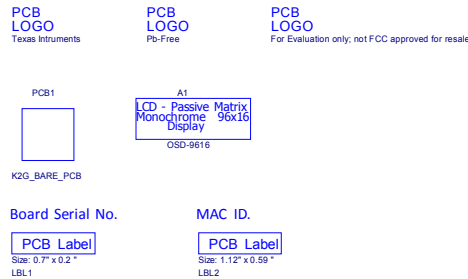


SHUNT SHOULD BE PLACED ON J3 FOR INTERNAL SYSCCLK SOURCE SELECT

FIDUCIALS



LOGOs & LABELS



KIT CONTENTS



Label Assembly Note

Z21 The boards and components must be baked before assembly

Label Assembly Note

Z22 Provide serial numbers to the assembled boards for identification

Label Assembly Note

Z23 Please carry out the cold points check verification and provide the report for each assembled board

Label Assembly Note

Z24 The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

Label Assembly Note

Z25 All MSL components should be baked as per JEDEC standard

Label Assembly Note

Z26 PCB should be baked at 120 degree for 8 hours

Label Assembly Note

Z27 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Label Assembly Note

Z28 These assemblies are ESD sensitive, ESD precautions shall be observed.

Label Assembly Note

Z29 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Project :

K2GICE
PROC022

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Title HARDWARE SCHEMATICS

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