

1.35V DDR3L SDRAM

MT41K512M4 – 64 Meg x 4 x 8 banks
MT41K256M8 – 32 Meg x 8 x 8 banks
MT41K128M16 – 16 Meg x 16 x 8 banks

Description

DDR3L SDRAM (1.35V) is a low voltage version of the DDR3 SDRAM (1.5V). Unless stated otherwise, DDR3L SDRAM meet the functional and timing specifications listed in the equivalent density DDR3 SDRAM data sheet located on www.micron.com.

Features

- $V_{DD} = V_{DDQ} = 1.35V$ (1.283–1.45V)
- Backward-compatible to $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode

- T_C of 0°C to +95°C
 - 64ms, 8192-cycle refresh at 0°C to +85°C
 - 32ms at +85°C to +95°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

Options

- Configuration
 - 512 Meg x 4
 - 256 Meg x 8
 - 128 Meg x 16
- FBGA package (Pb-free) – x4, x8
 - 78-ball (8mm x 10.5mm) Rev. H, M, K
 - 78-ball FBGA (9mm x 11.5mm) Rev. D
- FBGA package (Pb-free) – x16
 - 96-ball FBGA (9mm x 14mm) Rev. D
 - 96-ball FBGA (8mm x 14mm) Rev. K
- Timing – cycle time
 - 1.25ns @ CL = 11 (DDR3-1600)
 - 1.5ns @ CL = 9 (DDR3-1333)
 - 1.875ns @ CL = 7 (DDR3-1066)
- Revision

Marking

512M4
256M8
128M16

DA
HX

HA
JT

-125
-15E
-187E

:D/ :H/ :K/ :
M

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target t_{RCD} - t_{RP} -CL	t_{RCD} (ns)	t_{RP} (ns)	CL (ns)
-125 ^{1, 2}	1600	11-11-11	13.75	13.75	13.75
-15E ¹	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Notes: 1. Backward compatible to 1066, CL = 7 (-187E).

2. Backward compatible to 1333, CL = 9 (-15E).

Table 2: Addressing

Parameter	512 Meg x 4	256 Meg x 8	128 Meg x 16
Configuration	64 Meg x 4 x 8 banks	32 Meg x 8 x 8 banks	16 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row address	32K A[14:0]	32K A[14:0]	16K A[13:0]
Bank address	8 BA[2:0]	8 BA[2:0]	8 BA[2:0]
Column address	2K A[11, 9:0]	1K A[9:0]	1K A[9:0]

Ball Assignments and Descriptions

Figure 1: 78-Ball FBGA – x4, x8 Ball Assignments (Top View)

	1	2	3	4	5	6	7	8	9
A	 V _{SS}	 V _{DD}	 NC				 NF, NF/TDQS#	 V _{SS}	 V _{DD}
B	 V _{SS}	 V _{SSQ}	 DQ0				 DM, DM/TDQS	 V _{SSQ}	 V _{DDQ}
C	 V _{DDQ}	 DQ2	 DQS				 DQ1	 DQ3	 V _{SSQ}
D	 V _{SSQ}	 NF, DQ6	 DQS#				 V _{DD}	 V _{SS}	 V _{SSQ}
E	 V _{REFDQ}	 V _{DDQ}	 NF, DQ4				 NF, DQ7	 NF, DQ5	 V _{DDQ}
F	 NC	 V _{SS}	 RAS#				 CK	 V _{SS}	 NC
G	 ODT	 V _{DD}	 CAS#				 CK#	 V _{DD}	 CKE
H	 NC	 CS#	 WE#				 A10/AP	 ZQ	 NC
J	 V _{SS}	 BA0	 BA2				 NC	 V _{REFCA}	 V _{SS}
K	 V _{DD}	 A3	 A0				 A12/BC#	 BA1	 V _{DD}
L	 V _{SS}	 A5	 A2				 A1	 A4	 V _{SS}
M	 V _{DD}	 A7	 A9				 A11	 A6	 V _{DD}
N	 V _{SS}	 RESET#	 A13				 A14	 A8	 V _{SS}

- Notes:
1. Ball descriptions listed in Table 3 (page 5) are listed as "x4, x8" if unique; otherwise, x4 and x8 are the same.
 2. A comma separates the configuration; a slash defines a selectable function.
Example: D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3).

Figure 2: 96-Ball FBGA – x16 Ball Assignments (Top View)

	1	2	3	4	5	6	7	8	9
A	 V _{DDQ}	 DQ13	 DQ15				 DQ12	 V _{DDQ}	 V _{SS}
B	 V _{SSQ}	 V _{DD}	 V _{SS}				 UDQS#	 DQ14	 V _{SSQ}
C	 V _{DDQ}	 DQ11	 DQ9				 UDQS	 DQ10	 V _{DDQ}
D	 V _{SSQ}	 V _{DDQ}	 UDM				 DQ8	 V _{SSQ}	 V _{DD}
E	 V _{SS}	 V _{SSQ}	 DQ0				 LDM	 V _{SSQ}	 V _{DDQ}
F	 V _{DDQ}	 DQ2	 LDQS				 DQ1	 DQ3	 V _{SSQ}
G	 V _{SSQ}	 DQ6	 LDQS#				 V _{DD}	 V _{SS}	 V _{SSQ}
H	 V _{REFDQ}	 V _{DDQ}	 DQ4				 DQ7	 DQ5	 V _{DDQ}
J	 NC	 V _{SS}	 RAS#				 CK	 V _{SS}	 NC
K	 ODT	 V _{DD}	 CAS#				 CK#	 V _{DD}	 CKE
L	 NC	 CS#	 WE#				 A10/AP	 ZQ	 NC
M	 V _{SS}	 BA0	 BA2				 NC	 V _{REFCA}	 V _{SS}
N	 V _{DD}	 A3	 A0				 A12/BC#	 BA1	 V _{DD}
P	 V _{SS}	 A5	 A2				 A1	 A4	 V _{SS}
R	 V _{DD}	 A7	 A9				 A11	 A6	 V _{DD}
T	 V _{SS}	 RESET#	 A13				 NC	 A8	 V _{SS}

Notes: 1. Ball descriptions listed in Table 4 (page 7) are listed as "x16."

2. A comma separates the configuration; a slash defines a selectable function.

Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions

Symbol	Type	Description
A[14:13], A12/BC#, A11, A10/AP, A[9:0]	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA} . A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop).
BA[2:0]	Input	Bank address inputs: BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA} .
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA} .
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA} .
DM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REFDQ} . DM has an optional use as TDQS on the x8 device.
ODT	Input	On-die termination: ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA} .
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA} .
RESET#	Input	Reset: RESET# is an active LOW CMOS input referenced to V_{SS} . The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times V_{\text{DDQ}}$ and DC LOW $\leq 0.2 \times V_{\text{DDQ}}$. RESET# assertion and deassertion are asynchronous.

Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions (Continued)

Symbol	Type	Description
DQ[3:0]	I/O	Data input/output: Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to V_{REFDQ} .
DQ[7:0]	I/O	Data input/output: Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to V_{REFDQ} .
DQS, DQS#	I/O	Data strobe: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	I/O	Termination data strobe: Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
V_{DD}	Supply	Power supply: 1.35V, 1.283–1.45V operational; compatible to 1.5V operation.
V_{DDQ}	Supply	DQ power supply: 1.35V, 1.283–1.45V operational; compatible with 1.5V operation.
V_{REFCA}	Supply	Reference voltage for control, command, and address: V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	Reference voltage for data: V_{REFDQ} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	DQ ground: Isolated on the device for improved noise immunity.
ZQ	Reference	External reference ball for output drive calibration: This ball is tied to an external 240 Ω resistor (R_{ZQ}), which is tied to V_{SSQ} .
NC	–	No connect: These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	No function: When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

Table 4: 96-Ball FBGA – x16 Ball Descriptions

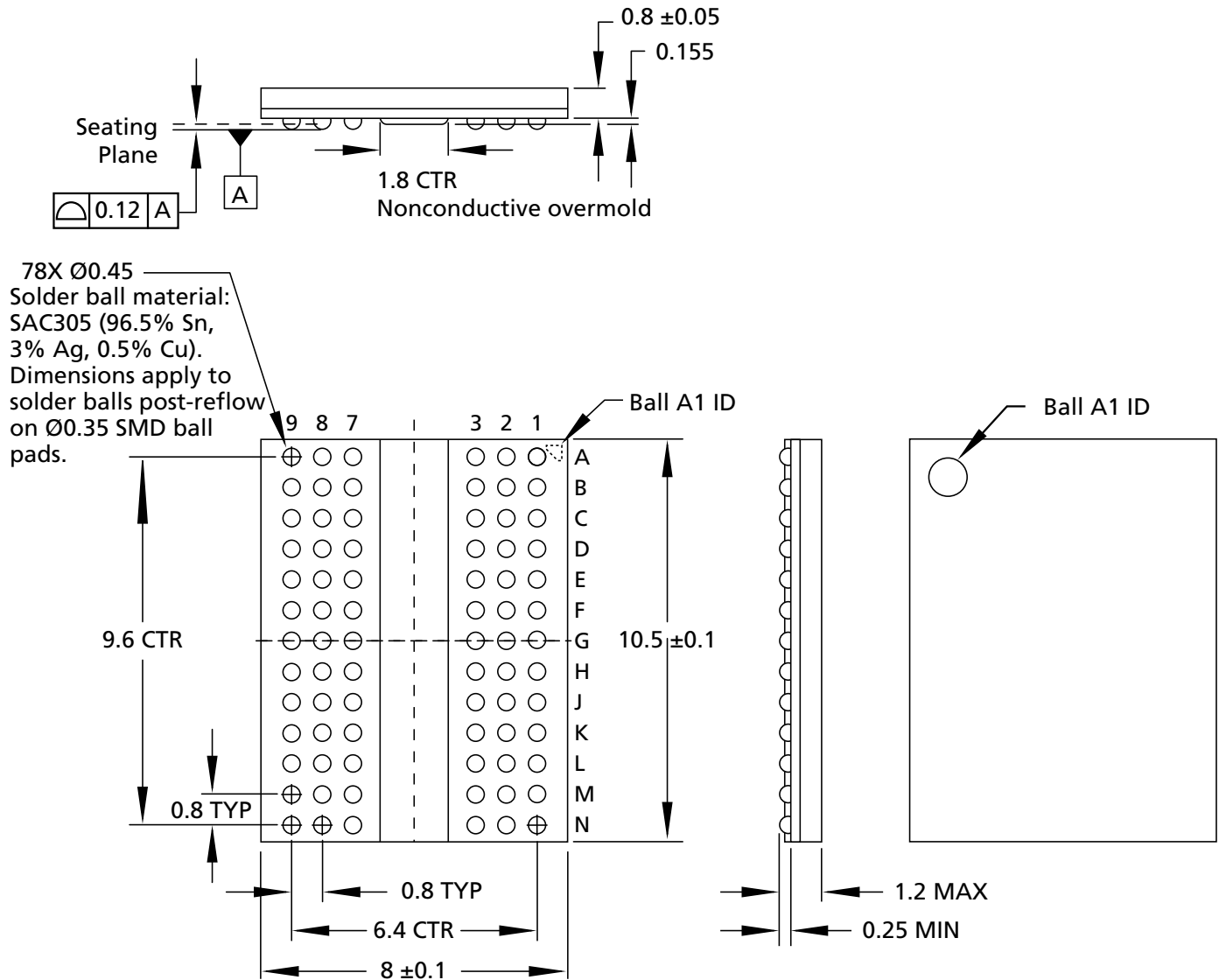
Symbol	Type	Description
A13, A12/BC#, A11, A10/AP, A[9:0]	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA} . A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop).
BA[2:0]	Input	Bank address inputs: BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA} .
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (LDQS, LDQS#, UDQS, UDQS#) is referenced to the crossings of CK and CK#.
CKE	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA} .
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA} .
LDM	Input	Input data mask: LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and LDQS balls. LDM is referenced to V_{REFDQ} .
ODT	Input	On-die termination: ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA} .
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA} .
RESET#	Input	Reset: RESET# is an active LOW CMOS input referenced to V_{SS} . The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times V_{\text{DDQ}}$ and DC LOW $\leq 0.2 \times V_{\text{DDQ}}$. RESET# assertion and deassertion are asynchronous.

Table 4: 96-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
UDM	Input	Input data mask: UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with the input data during a write access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and UDQS balls. UDM is referenced to V_{REFDQ} .
DQ[7:0]	I/O	Data input/output: Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to V_{REFDQ} .
DQ[15:8]	I/O	Data input/output: Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to V_{REFDQ} .
LDQS, LDQS#	I/O	Lower byte data strobe: Output with read data. Edge-aligned with read data. Input with write data. LDQS is center-aligned to write data.
UDQS, UDQS#	I/O	Upper byte data strobe: Output with read data. Edge-aligned with read data. Input with write data. UDQS is center-aligned to write data.
V_{DD}	Supply	Power supply: 1.35V, 1.283–1.45V operational; compatible to 1.5V operation.
V_{DDQ}	Supply	DQ power supply: 1.35V, 1.283–1.45V operational; compatible with 1.5V operation.
V_{REFCA}	Supply	Reference voltage for control, command, and address: V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	Reference voltage for data: V_{REFDQ} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	DQ ground: Isolated on the device for improved noise immunity.
ZQ	Reference	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (R_{ZQ}), which is tied to V_{SSQ} .
NC	–	No connect: These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

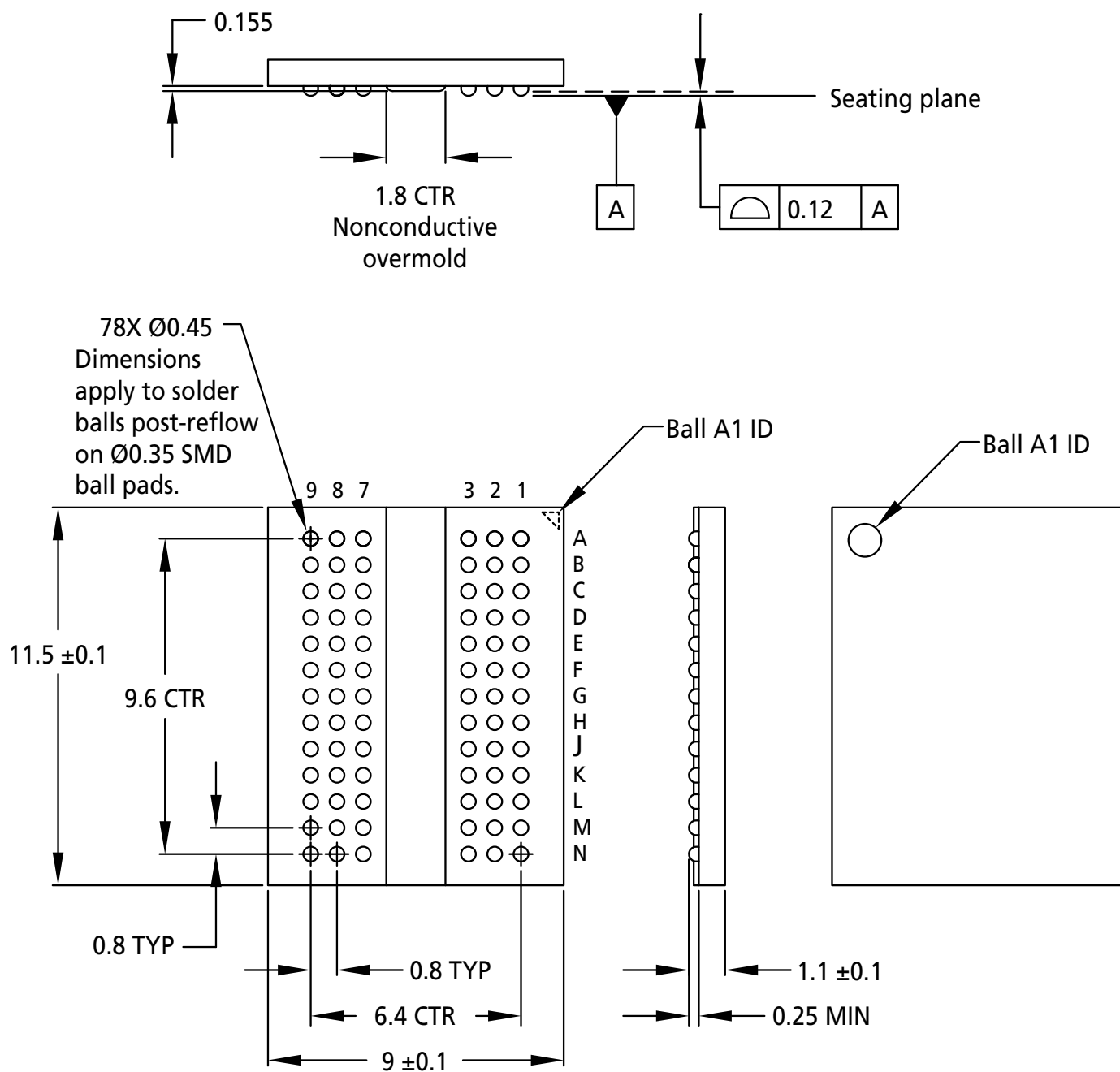
Package Dimensions

Figure 3: 78-Ball FBGA – x4, x8; Die Rev. H, M, K (DA)



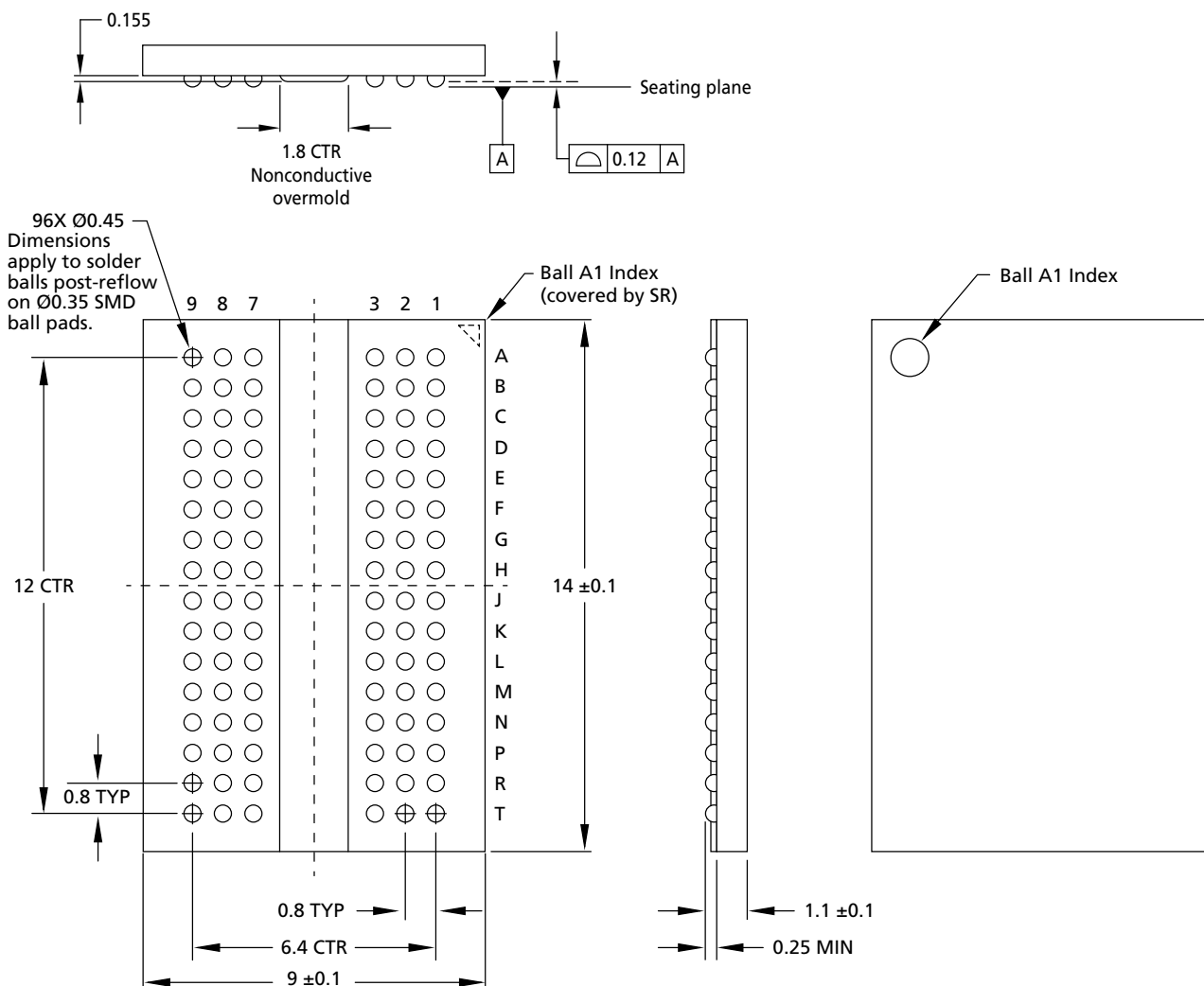
Note: 1. All dimensions are in millimeters.

Figure 4: 78-Ball FBGA – x4, x8; Die Rev. D (HX)



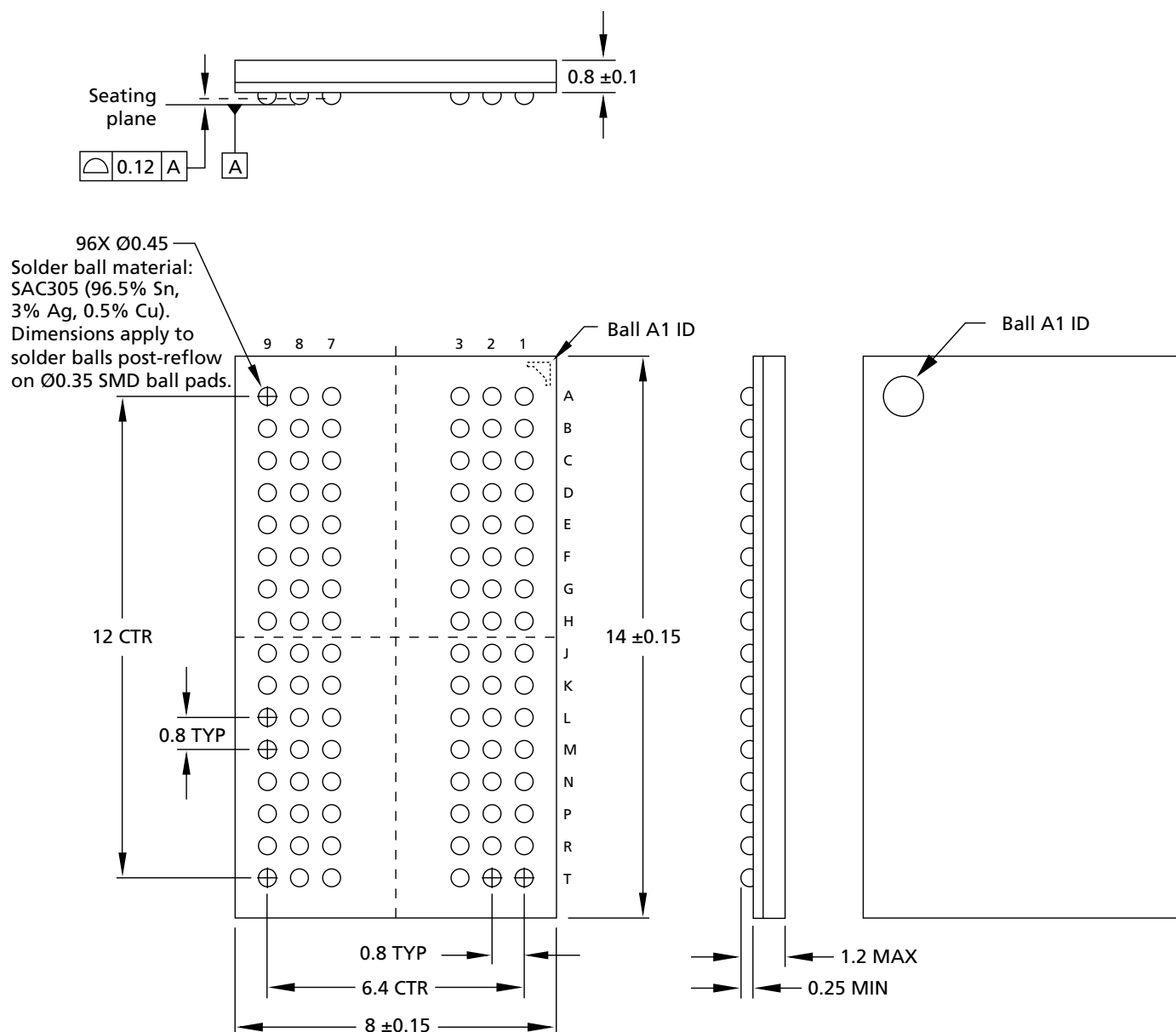
- Notes:
1. All dimensions are in millimeters.
 2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 5: 96-Ball FBGA – x16; Die Rev. D (HA)



Note: 1. All dimensions are in millimeters.

Figure 6: 96-Ball FBGA – x16; Die Rev. K (JT)



Note: 1. All dimensions are in millimeters.

Electrical Characteristics – I_{DD} Specifications

Table 5: I_{DD} Maximum Limits – Die Rev. D

Speed Bin		DDR3L-800	DDR3L-1066	DDR3L-1333	Units
I _{DD}	Width				
I _{DD0}	x4, 8	70	75	85	mA
	x16	85	90	100	mA
I _{DD1}	x4, 8	92	95	100	mA
	x16	122	125	130	mA
I _{DD2P0} (Slow)	All	12	12	12	mA
I _{DD2P1} (Fast)	x4, 8	22	25	30	mA
	x16	27	30	35	mA
I _{DD2Q}	All	27	30	35	mA
I _{DD2N}	All	28	32	37	mA
I _{DD2NT}	x4, 8	37	40	45	mA
	x16	52	55	60	mA
I _{DD3P}	x4, 8	27	30	35	mA
	x16	32	35	40	mA
I _{DD3N}	All	32	35	40	mA
I _{DD4R}	x4	110	125	145	mA
	x8	125	140	160	mA
	x16	160	200	245	mA
I _{DD4W}	x4	120	135	155	mA
	x8	130	145	165	mA
	x16	170	210	255	mA
I _{DD5B}	All	185	190	200	mA
I _{DD6}	All	12	12	12	mA
I _{DD6ET}	All	15	15	15	mA
I _{DD7}	x4, 8	290	335	385	mA
	x16	330	375	425	mA
I _{DD8}	All	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	mA

Table 6: I_{DD} Maximum Limits – Die Rev. H

Speed Bin		DDR3L-1066	DDR3L-1333	DDR3L-1600	Unit
I _{DD}	Width				
I _{DD0}	x4, 8	65	70	75	mA
I _{DD1}	x4, 8	85	90	95	mA
I _{DD2P0} (Slow)	x4, 8	12	12	12	mA
I _{DD2P1} (Fast)	x4, 8	27	32	37	mA
I _{DD2Q}	x4, 8	32	37	42	mA
I _{DD2N}	x4, 8	34	38	43	mA
I _{DD2NT}	x4, 8	42	47	52	mA
I _{DD3P}	x4, 8	37	42	47	mA
I _{DD3N}	x4, 8	42	47	52	mA
I _{DD4R}	x4	110	125	140	mA
	x8	125	140	155	mA
I _{DD4W}	x4	110	125	140	mA
	x8	125	140	155	mA
I _{DD5B}	x4, 8	180	185	190	mA
I _{DD6}	x4, 8	12	12	12	mA
I _{DD6ET}	x4, 8	15	15	15	mA
I _{DD7}	x4, 8	225	240	255	mA
I _{DD8}	x4, 8	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	mA



2Gb: x4, x8, x16 DDR3L SDRAM Electrical Characteristics – I_{DD} Specifications

Table 7: I_{DD} Maximum Limits – Die Rev. M

Speed Bin		DDR3L-1066	DDR3L-1333	DDR3L-1600	Unit
I _{DD}	Width				
I _{DD0}	x4, 8	50	55	60	mA
I _{DD1}	x4, 8	65	70	75	mA
I _{DD2P0} (Slow)	x4, 8	12	12	12	mA
I _{DD2P1} (Fast)	x4, 8	23	28	33	mA
I _{DD2Q}	x4, 8	23	28	33	mA
I _{DD2N}	x4, 8	25	30	35	mA
I _{DD2NT}	x4, 8	30	35	40	mA
I _{DD3P}	x4, 8	37	42	47	mA
I _{DD3N}	x4, 8	42	47	52	mA
I _{DD4R}	x4	95	110	125	mA
	x8	110	125	140	mA
I _{DD4W}	x4	85	100	115	mA
	x8	95	110	125	mA
I _{DD5B}	x4, 8	180	185	190	mA
I _{DD6}	x4, 8	12	12	12	mA
I _{DD6ET}	x4, 8	15	15	15	mA
I _{DD7}	x4, 8	190	205	220	mA
I _{DD8}	x4, 8	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	mA

Table 8: I_{DD} Maximum Limits – Die Rev. K

Speed Bin		DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3-1866	Units
I _{DD}	Width					
I _{DD0}	x4, x8	36	38	39	40	mA
	x16	43	45	46	48	mA
I _{DD1}	x4	43	47	49	52	mA
	x8	46	50	52	54	mA
	x16	58	63	65	68	mA
I _{DD2P0} (Slow)	All	12	12	12	12	mA
I _{DD2P1} (Fast)	All	14	14	14	14	mA
I _{DD2Q}	All	20	20	20	20	mA
I _{DD2N}	All	21	21	21	21	mA
I _{DD2NT}	x4, x8	26	29	31	33	mA
	x16	30	33	34	36	mA
I _{DD3P}	All	21	21	21	21	mA
I _{DD3N}	x4,x8	28	30	32	34	mA
	x16	30	33	34	36	mA
I _{DD4R}	x4	64	78	90	100	mA
	x8	68	82	94	104	mA
	x16	88	108	128	148	mA
I _{DD4W}	x4	69	81	93	105	mA
	x8	73	85	97	108	mA
	x16	99	119	138	156	mA
I _{DD5B}	All	107	109	110	112	mA
I _{DD6}	All	12	12	12	12	mA
I _{DD6ET}	All	15	15	15	15	mA
I _{DD7}	x4, 8	121	150	156	164	mA
	x16	152	172	195	219	mA
I _{DD8}	All	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	mA

Electrical Specifications

Table 9: Input/Output Capacitance

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Capacitance Parameters	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single-end I/O: DQ, DM	C_{IO}	1.5	2.5	1.5	2.5	1.5	2.3	1.5	2.2	1.5	2.1	pF
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	1.5	2.5	1.5	2.5	1.5	2.3	1.5	2.2	1.5	2.1	pF
Inputs (CTRL, CMD, ADDR)	C_I	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF

Table 10: DC Electrical Characteristics and Operating Conditions – 1.35V Operation

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1, 2, 3, 4
I/O supply voltage	V_{DDQ}	1.283	1.35	1.45	V	1, 2, 3, 4

- Notes:
1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of $V_{DD}/V_{DDQ}(t)$ over a very long period of time (for example, 1 sec).
 2. If the maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
 3. Under these supply voltages, the device operates to this DDR3L specification.
 4. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3 operation (see Figure 7 (page 29)).

Table 11: DC Electrical Characteristics and Operating Conditions – 1.5V Operation

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1, 2, 3
I/O supply voltage	V_{DDQ}	1.425	1.5	1.575	V	1, 2, 3

- Notes:
1. If the minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
 2. Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifications under the same speed timings as defined for this device.
 3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3L operation (see Figure 7 (page 29)).

Table 12: Input Switching Conditions – Command and Address

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	DDR3L-1866	Units
Input high AC voltage: Logic 1	$V_{IH(AC160)min}^1$	160	160	–	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}^1$	135	135	135	mV
Input high AC voltage: Logic 1	$V_{IH(AC125)min}^1$	–	–	125	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC125)min}^1$	–	–	–125	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)min}^1$	–135	–135	–135	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)min}^1$	–160	–160	–	mV

Note: 1. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

For example, for DDR3L-800, two input AC levels are defined: $V_{IH(AC160),min}$ and $V_{IH(AC135),min}$ (corresponding $V_{IL(AC160),min}$ and $V_{IL(AC135),min}$). For DDR3L-800, the address/command inputs must use either $V_{IH(AC160),min}$ with $t_{IS(AC160)}$ of 215ps or $V_{IH(AC135),min}$ with $t_{IS(AC135)}$ of 365ps; independently, the data inputs may use either $V_{IH(AC160),min}$ or $V_{IH(AC135),min}$.

Table 13: Input Switching Conditions – DQ and DM

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	DDR3L-1866	Units
Input high AC voltage: Logic 1	$V_{IH(AC160)min}^1$	160	160	–	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}^1$	135	135	135	mV
Input high AC voltage: Logic 1	$V_{IH(AC125)min}^1$	–	–	130	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC125)min}^1$	–	–	–130	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)min}^1$	–135	–135	–135	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)min}^1$	–160	–160	–	mV

Note: 1. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

For example, for DDR3L-800, two input AC levels are defined: $V_{IH(AC160),min}$ and $V_{IH(AC135),min}$ (corresponding $V_{IL(AC160),min}$ and $V_{IL(AC135),min}$). For DDR3L-800, the data inputs must use either $V_{IH(AC160),min}$ with $t_{IS(AC160)}$ of 90ps or $V_{IH(AC135),min}$ with $t_{IS(AC135)}$ of 140ps; independently, the address/command inputs may use either $V_{IH(AC160),min}$ or $V_{IH(AC135),min}$.

Table 14: Differential Input Operating Conditions (CK, CK# and DQS, DQS#)

Parameter/Condition	Symbol	Min	Max	Units
Differential input logic high – slew	$V_{IH,diff(AC)slew}$	180	N/A	mV
Differential input logic low – slew	$V_{IL,diff(AC)slew}$	N/A	-180	mV
Differential input logic high	$V_{IH,diff(AC)}$	$2 \times (V_{IH(AC)} - V_{REF})$	V_{DD}/V_{DDQ}	mV
Differential input logic low	$V_{IL,diff(AC)}$	V_{SS}/V_{SSQ}	$2 \times (V_{IL(AC)} - V_{REF})$	mV
Single-ended high level for strobes	V_{SEH}	$V_{DDQ}/2 + 160$	V_{DDQ}	mV
Single-ended high level for CK, CK#		$V_{DD}/2 + 160$	V_{DD}	mV
Single-ended low level for strobes	V_{SEL}	V_{SSQ}	$V_{DDQ}/2 - 160$	mV
Single-ended low level for CK, CK#		V_{SS}	$V_{DD}/2 - 160$	mV

Table 15: Minimum Required Time t_{DVAC} for CK/CK#, DQS/DQS# Differential for AC Ringback

Slew Rate (V/ns)	DDR3L-800/1066/1333/1600		DDR3L-1866		
	t_{DVAC} at 320mV (ps)	t_{DVAC} at 270mV (ps)	t_{DVAC} at 270mV (ps)	t_{DVAC} at 250mV (ps)	t_{DVAC} at 260mV (ps)
>4.0	189	201	163	168	176
4.0	189	201	163	168	176
3.0	162	179	140	147	154
2.0	109	134	95	105	111
1.8	91	119	80	91	97
1.6	69	100	62	74	78
1.4	40	76	37	52	55
1.2	Note1	44	5	22	24
1.0	Note1	Note1	Note1	Note1	Note1
<1.0	Note1	Note1	Note1	Note1	Note1

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(ac)}$ level and Falling input signal shall become equal to or less than $V_{IL(ac)}$ level.

Table 16: R_{TT} Effective Impedance

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [9, 6, 2]	R _{TT}	Resistor	V _{OUT}	Min	Nom	Max	Units
0, 1, 0	120Ω	R _{TT,120PD240}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/1
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/1
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/1
		R _{TT,120PU240}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/1
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/1
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/1
	120Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/2
0, 0, 1	60Ω	R _{TT,60PD120}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/2
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/2
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/2
		R _{TT,60PU120}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/2
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/2
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/2
	60Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/4
0, 1, 1	40Ω	R _{TT,40PD80}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/3
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/3
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/3
		R _{TT,40PU80}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/3
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/3
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/3
	40Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/6
1, 0, 1	30Ω	R _{TT,30PD60}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/4
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/4
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/4
		R _{TT,30PU60}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/4
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/4
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/4
	30Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/8
1, 0, 0	20Ω	R _{TT,20PD40}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/6
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/6
		R _{TT,20PU40}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/6
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/6
	20Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/12

Table 17: Reference Settings for ODT Timing Measurements

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Measured Parameter	$R_{TT,nom}$ Setting	$R_{TT(WR)}$ Setting	V_{SW1}	V_{SW2}
t_{AON}	RZQ/4 (60 Ω)	N/A	50mV	100mV
	RZQ/12 (20 Ω)	N/A	100mV	200mV
t_{AOF}	RZQ/4 (60 Ω)	N/A	50mV	100mV
	RZQ/12 (20 Ω)	N/A	100mV	200mV
t_{AONPD}	RZQ/4 (60 Ω)	N/A	50mV	100mV
	RZQ/12 (20 Ω)	N/A	100mV	200mV
t_{AOFPD}	RZQ/4 (60 Ω)	N/A	50mV	100mV
	RZQ/12 (20 Ω)	N/A	100mV	200mV
t_{ADC}	RZQ/12 (20 Ω)	RZQ/2 (20 Ω)	200mV	250mV

Table 18: 34 Ω Driver Impedance Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [5, 1]	R _{ON}	Resistor	V _{OUT}	Min	Nom	Max ¹	Units
0, 1	34.3Ω	R _{ON,34PD}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/7
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/7
		R _{ON,34PU}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/7
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/7
Pull-up/pull-down mismatch (MM _{PUPD})			V _{IL(AC)} to V _{IH(AC)}	−10	N/A	10	%

Note: 1. A larger maximum limit will result in slightly lower minimum currents.

Table 19: 40 Ω Driver Impedance Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [5, 1]	R _{ON}	Resistor	V _{OUT}	Min	Nom	Max ¹	Units
0, 0	40Ω	R _{ON,40PD}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/6
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/6
		R _{ON,40PU}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/6
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/6
Pull-up/pull-down mismatch (MM _{PUPD})		V _{IL(AC)} to V _{IH(AC)}	−10	N/A	10	%	

Note: 1. A larger maximum limit will result in slightly lower minimum currents.

Table 20: Single-Ended Output Driver Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Parameter/Condition	Symbol	Min	Max	Units
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.09 \times V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.09 \times V_{DDQ}$	SRQ_{se}	1.75	6	V/ns

Table 21: Differential Output Driver Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Parameter/Condition	Symbol	Min	Max	Units
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.18 \times V_{DDQ}$ and $V_{OH,diff(AC)} = 0.18 \times V_{DDQ}$	SRQ_{diff}	3.5	12	V/ns
Output differential crosspoint voltage	$V_{OX(AC)}$	$V_{REF} - 135$	$V_{REF} + 135$	mV

Table 22: Electrical Characteristics and AC Operating Conditions

Note 1 applies to base timing specifications

Parameter		Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
DQ Input Timing													
Data setup time to DQS, DQS#	Base (specification)	^t _{DS} (AC160)	90	–	40	–	N/A	–	N/A	–	N/A	–	ps
	V _{REF} @ 1 V/ns		250	–	200	–	N/A	–	N/A	–	N/A	–	ps
Data setup time to DQS, DQS#	Base (specification)	^t _{DS} (AC135)	140	–	90	–	45	–	25	–	N/A	–	ps
	V _{REF} @ 1 V/ns		275	–	225	–	180	–	160	–	N/A	–	ps
Data hold time from DQS, DQS#	Base (specification)	^t _{DH} (DC90)	160	–	110	–	75	–	55	–	N/A	–	ps
	V _{REF} @ 1 V/ns		250	–	200	–	165	–	145	–	N/A	–	ps
Data setup time to DQS, DQS#	Base (specification)	^t _{DS} (AC130)	N/A	–	N/A	–	N/A	–	N/A	–	70	–	ps
	V _{REF} @ 2 V/ns		N/A	–	N/A	–	N/A	–	N/A	–	135	–	ps
Data hold time from DQS, DQS#	Base (specification)	^t _{DH} (DC90)	N/A	–	N/A	–	N/A	–	N/A	–	75	–	ps
	V _{REF} @ 2 V/ns		N/A	–	N/A	–	N/A	–	N/A	–	110	–	ps
Command and Address Timing													
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	^t _{IS} (AC160)	215	–	140	–	80	–	60	–	N/A	–	ps
	V _{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	N/A	–	ps
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	^t _{IS} (AC135)	365	–	290	–	205	–	185	–	65	–	ps
	V _{REF} @ 1 V/ns		500	–	425	–	340	–	320	–	200	–	ps

Table 22: Electrical Characteristics and AC Operating Conditions (Continued)

Note 1 applies to base timing specifications

Parameter		Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	$t_{IS}^{(AC125)}$	N/A	–	N/A	–	N/A	–	N/A	–	150	–	ps
	V_{REF} @ 1 V/ns		N/A	–	N/A	–	N/A	–	N/A	–	275	–	ps
CTRL, CMD, ADDR hold from CK, CK#	Base (specification)	$t_{IH}^{(DC90)}$	285	–	210	–	150	–	130	–	110	–	ps
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	200	–	ps

- Notes: 1. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC160),min}$ and $V_{IH(AC135),min}$ (corresponding $V_{IL(AC160),min}$ and $V_{IL(AC135),min}$). For DDR3-800, the address/command inputs must use either $V_{IH(AC160),min}$ with $t_{IS(AC160)}$ of 215ps or $V_{IH(AC135),min}$ with $t_{IS(AC135)}$ of 365ps; independently, the data inputs must use either $V_{IH(AC160),min}$ with $t_{DS(AC160)}$ of 90ps or $V_{IH(AC135),min}$ with $t_{DS(AC135)}$ of 140ps.

2. When DQ single-ended slew rate is 1V/ns, the DQS differential slew rate is 2V/ns; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns;

Table 23: Derating Values for t_{IS}/t_{IH} – AC160/DC90-Based

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
2.0	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	–1	–3	–1	–3	–1	–3	7	5	15	13	23	21	31	31	39	47
0.8	–3	–8	–3	–8	–3	–8	5	1	13	9	21	17	29	27	37	43
0.7	–5	–13	–5	–13	–5	–13	3	–5	11	3	19	11	27	21	35	37
0.6	–8	–20	–8	–20	–8	–20	0	–12	8	–4	16	4	24	14	32	30
0.5	–20	–30	–20	–30	–20	–30	–12	–22	–4	–14	4	–6	12	4	20	20
0.4	–40	–45	–40	–45	–40	–45	–32	–37	–24	–29	–16	–21	–8	–11	0	5

Table 24: Derating Values for t_{IS}/t_{IH} – AC135/DC90-Based

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
2.0	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	2	–3	2	–3	2	–3	10	5	18	13	26	21	34	31	42	47
0.8	3	–8	3	–8	3	–8	11	1	19	9	27	17	35	27	43	43
0.7	6	–13	6	–13	6	–13	14	–5	22	3	30	11	38	21	46	37
0.6	9	–20	9	–20	9	–20	17	–12	25	–4	33	4	41	14	49	30
0.5	5	–30	5	–30	5	–30	13	–22	21	–14	29	–6	37	4	45	20
0.4	–3	–45	–3	–45	–3	–45	6	–37	14	–29	22	–21	30	–11	38	5

Table 25: Derating Values for t_{IS}/t_{IH} – AC125/DC90-Based

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
2.0	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	3	–3	3	–3	3	–3	11	5	19	13	27	21	35	31	43	47
0.8	6	–8	6	–8	6	–8	14	1	22	9	30	17	38	27	46	43
0.7	10	–13	10	–13	10	–13	18	–5	26	3	34	11	42	21	50	37
0.6	16	–20	16	–20	16	–20	24	–12	32	–4	40	4	48	14	56	30
0.5	15	–30	15	–30	15	–30	23	–22	31	–14	39	–6	47	4	55	20
0.4	13	–45	13	–45	13	–45	21	–37	29	–29	37	–21	45	–11	53	5

Table 26: Minimum Required Time t_{VAC} Above $V_{IH(AC)}$ (Below $V_{IL(AC)}$) for Valid ADD/CMD Transition

Slew Rate (V/ns)	DDR3L-800/1066/1333/1600		DDR3L-1866	
	t_{VAC} at 160mV (ps)	t_{VAC} at 135mV (ps)	t_{VAC} at 135mV (ps)	t_{VAC} at 125mV (ps)
>2.0	70	209	200	205
2.0	53	198	200	205
1.5	47	194	178	184
1.0	35	186	133	143
0.9	31	184	118	129
0.8	26	181	99	111
0.7	20	177	75	89
0.6	12	171	43	59
0.5	Note 1	164	Note 1	18
<0.5	Note 1	164	Note 1	18

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(ac)}$ level and Falling input signal shall become equal to or less than $V_{IL(ac)}$ level.

Table 27: Derating Values for t_{DS}/t_{DH} – AC160/DC90-Based

$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
2.0	80	45	80	45	80	45										
1.5	53	30	53	30	53	30	61	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			–1	–3	–1	–3	7	5	15	13	23	21				
0.8					–3	–8	5	1	13	9	21	17	29	27		
0.7							–3	–5	11	3	19	11	27	21	35	37
0.6									8	–4	16	4	24	14	32	30
0.5											4	6	12	4	20	20
0.4													–8	–11	0	5

Table 28: Derating Values for t_{DS}/t_{DH} – AC135/DC90-Based

$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
2.0	68	45	68	45	68	45										
1.5	45	30	45	30	45	30	53	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			2	–3	2	–3	10	5	18	13	26	21				
0.8					3	–8	11	1	19	9	27	17	35	27		
0.7							14	–5	22	3	30	11	38	21	46	37
0.6									25	–4	33	4	41	14	49	30
0.5											39	–6	37	4	45	20
0.4													30	–11	38	5

Table 29: Derating Values for t_{DS}/t_{DH} – AC130/DC100-Based at 2V/ns

Shaded cells indicate slew rate combinations not supported

Δ ^t DS, Δ ^t DH Derating (ps) – AC/DC-Based																									
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate																								
	8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		
	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	
	t ^{DS}	t ^{DH}	t ^{DS}	t ^{DH}	t ^{DS}	t ^{DH}	t ^{DS}	t ^{DH}	t ^{DS}	t ^{DH}	t ^{DS}	t ^{DH}	t ^{DS}	t ^{DH}	t ^{DS}	t ^{DH}	t ^{DS}	t ^{DH}	t ^{DS}	t ^{DH}	t ^{DS}	t ^{DH}	t ^{DS}	t ^{DH}	
4.0	33	23	33	23	33	23																			
3.5	28	19	28	19	28	19	28	19																	
3.0	22	15	22	15	22	15	22	15	22	15															
2.5			13	9	13	9	13	9	13	9	13	9													
2.0					0	0	0	0	0	0	0	0	0	0											
1.5							-22	-15	-22	-15	-22	-15	-22	-15	-14	-7									
1.0									-65	-45	-65	-45	-65	-45	-57	-37	-49	-29							
0.9											-62	-48	-62	-48	-54	-40	-46	-32	-38	-24					
0.8													-61	-53	-53	-45	-45	-37	-37	-29	-29	-19			
0.7															-49	-50	-41	-42	-33	-34	-25	-24	-17	-8	
0.6																	-37	-49	-29	-41	-21	-31	-13	-15	
0.5																			-31	-51	-23	-41	-15	-25	
0.4																					-28	-56	-20	-40	

Table 30: Minimum Required Time t_{VAC} Above $V_{IH(AC)}$ (Below $V_{IL(AC)}$) for Valid DQTransition

Slew Rate (V/ns)	t_{VAC} at 160mV (ps)	t_{VAC} at 135mV (ps)	t_{VAC} at 130mV (ps)
>2.0	165	113	95
2.0	165	113	95
1.5	138	90	73
1.0	85	45	30
0.9	67	30	16
0.8	45	11	Note1
0.7	16	Note1	–
0.6	Note1	Note1	–
0.5	Note1	Note1	–
<0.5	Note1	Note1	–

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(ac)}$ level and Falling input signal shall become equal to or less than $V_{IL(ac)}$ level.

Initialization

If the SDRAM is powered up and initialized for the 1.35V operating voltage range, voltage can be increased to the 1.5V operating range provided that:

- Just prior to increasing the 1.35V operating voltages, no further commands are issued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.5V operating voltages are stable prior to issuing new commands, other than NOPs or COMMAND INHIBITs.
- The DLL is reset and relocked after the 1.5V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed. t_{ZQinit} must be satisfied after the 1.5V operating voltages are stable and prior to any READ command.

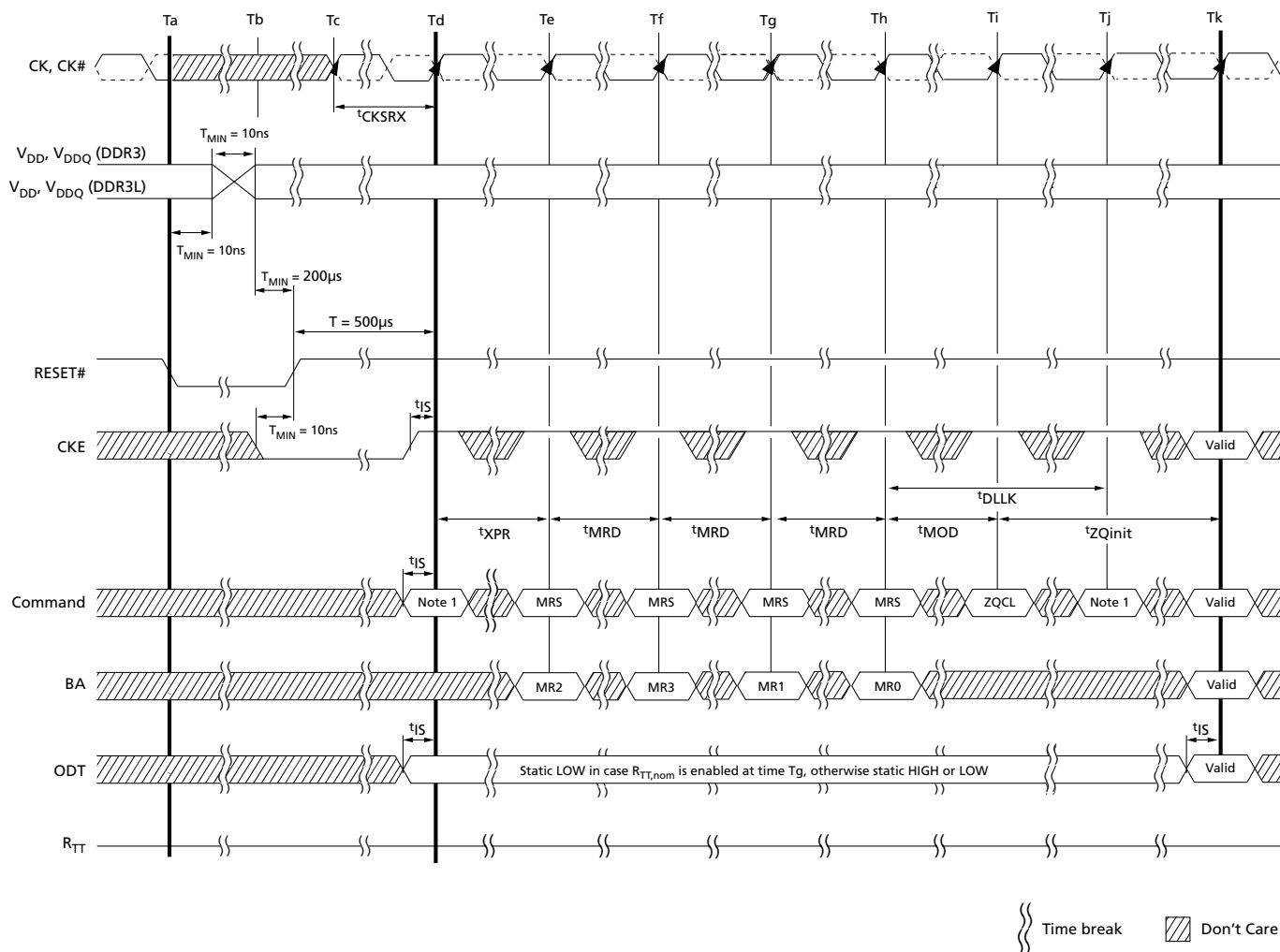
If the SDRAM is powered up and initialized for the 1.5V operating voltage range, voltage can be reduced to the 1.35V operation range provided that:

- Just prior to reducing the 1.5V operating voltages, no further commands are issued, other than NOPs or COMMAND INHIBITs, and all banks are in the precharge state.
- The 1.35V operating voltages are stable prior to issuing new commands, other than NOPs or COMMAND INHIBITs.
- The DLL is reset and relocked after the 1.35V operating voltages are stable and prior to any READ command.
- The ZQ calibration is performed. t_{ZQinit} must be satisfied after the 1.35V operating voltages are stable and prior to any READ command.

V_{DD} Voltage Switching

After the DDR3L DRAM is powered up and initialized, the power supply can be altered between the DDR3L and DDR3 levels, provided the sequence in Figure 7 is maintained.

Figure 7: V_{DD} Voltage Switching



Note: 1. From time point Td until Tk, NOP or DES commands must be applied between MRS and ZQCL commands.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.