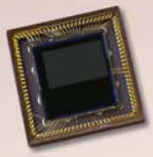
OmniVision



datasheet

PRODUCT SPECIFICATION

1/3" CMOS 720p wide dynamic range (WDR)
high definition (HD) image sensor

OV10633/OV10133

CMOS 720p wide dynamic range (WDR) high definition (HD) image sensor

datasheet (CLGA)
PRODUCT SPECIFICATION

version 2.0
november 2011

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- surveillance

ordering information

- **OV10633-C96A** (color, lead-free)
  96-pin CLGA
- **OV10133-C96A** (b&w, lead-free)
  96-pin CLGA

features

- support for image sizes: HD 720p (1280x720), WVGA (752x480), VGA (640x480), 600x400, CIF (352x288), QVGA (320x240)
- support for output formats: YUV and separated and combined RAW
- parallel DVP interface
- high sensitivity
- automatic exposure/gain
- horizontal and vertical windowing capability
- auto white balance control
- aperture/gamma correction
- serial camera control bus (SCCB) for register programming
- low power consumption
- external frame sync capability
- 50/60 Hz flicker cancellation
- defective pixel correction

key specifications (typical)

- **active array size:** 1280 x 720
- **power supply:**
  analog: 3.14~3.47V
  core: 1.6~1.7V
  I/O: 1.7~3.6V
- **power requirements:**
  active: 532 mW typical @ 3.3V AVDD, 1.65V DVDD, and 1.8V DOVDD
  standby: 480 µW typical @ 3.3V AVDD, 1.65V DVDD, and 1.8V DOVDD
- **temperature range:**
  operating:-20°C to 70°C junction temperature (see **table 8-2**)
  stable image: 0°C to 50°C junction temperature (see **table 8-2**)
- **output interfaces:** 10-bit parallel DVP
- **output formats:** up to 18-bit combined raw, separated 10-bit raw, 8-/10-bit YUV422
- **lens size:** 1/3"
- **lens chief ray angle:** 9° (see **figure 10-2**)
- **input clock frequency:** 6 ~ 27 MHz
- **scan mode:** progressive
- **shutter:** rolling shutter
- **maximum exposure interval:** 838 t_{ROW}
- **maximum image transfer rate:** 30 fps full resolution
- **sensitivity:** 3650 mV/Lux-sec
- **max S/N ratio:** 39 dB
- **dynamic range:** 115 dB
- **pixel size:** 4.2 µm x 4.2 µm
- **dark current:** 2.5 mV/s @ 50°C junction temperature
- **image area:** 5510.4 µm x 3418.8 µm
- **package dimensions:** 11 mm x 11 mm

table of contents

1 signal descriptions **1-1**

2 system level description **2-1**

2.1 overview 2-1

2.2 architecture 2-1

2.3 format and frame rate 2-4

2.4 I/O control 2-4

2.5 system clock control 2-5

2.6 serial camera control bus (SCCB) interface 2-6

2.6.1 data transfer protocol 2-6

2.6.2 message format 2-6

2.6.3 read / write operation 2-7

2.6.4 SCCB timing 2-10

2.7 standby 2-11

2.8 power on timing 2-11

2.9 system control 2-12

3 pixel array structure **3-1**

4 image sensor core digital functions **4-1**

4.1 mirror and flip 4-1

4.2 test pattern 4-2

4.2.1 color bar 4-2

4.2.2 square 4-5

4.2.3 random data 4-5

4.2.4 transparent effect 4-5

4.2.5 rolling bar effect 4-5

4.3 image cropping and windowing 4-7

4.4 AEC/AGC algorithms 4-9

4.4.1 position weight 4-9

4.4.2 exposure/gain control 4-15

4.5 black level calibration (BLC) 4-25

4.5.1 overview 4-25

4.5.2 coarse BLC 4-25

4.5.3 fine BLC 4-25

4.5.4 trigger methods 4-25

5 image sensor processor digital functions 5-1
5.1 DSP top level control 5-1
5.2 LENC 5-3
5.3 auto white balance (AWB) 5-6
5.3.1 simple AWB 5-8
5.3.2 CT WB 5-8
5.3.3 CT AWB calibration 5-8
5.3.4 AWB control 5-14
5.3.5 AWB stable range and gain range 5-15
5.4 de-noise (DNS) 5-16
5.5 color interpolation (CIP) 5-20
5.6 color matrix (CMX) 5-26
5.7 auto color saturation 5-28
5.8 combine 5-29
5.9 normalize 5-32
5.10 tone_mapping 5-33
5.11 OTP memory read/write 5-35
5.11.1 procedure to read OTP content 5-35
5.11.2 procedure to program OTP content 5-35
5.11.3 power supply requirement for OTP memory programming 5-35
5.12 group control 5-36
5.13 windowing cropping and sub-sampling 5-37
5.14 white/black pixel cancellation (WBC) 5-37
6 image sensor output interface digital functions 6-1
6.1 temperature sensor 6-1
6.1.1 overview 6-1
6.1.2 output mode 6-1
6.2 embedded line 6-2
6.2.1 overview 6-2
6.3 DVP timing 6-3
6.3.1 DVP setup/hold time 6-5

7 register tables 7-1
7.1 system control [0x0100 - 0x3049] 7-1
7.2 analog control [0x3600 - 0x3633] 7-7
7.3 sensor control [0x3700 - 0x374F] 7-8
7.4 timing control [0x3800 - 0x3844] 7-10
7.5 OTP control [0x3D00 - 0x3D1F] 7-12
7.6 BLC functions [0x4000 - 0x5D30] 7-15
7.7 AEC control [0x3503 - 0x5C17] 7-23
7.8 ISP control [0x5000 - 0x5044] 7-43
7.9 LENC control [0x5080 - 0x50B8] 7-45
7.10 white/black pixel cancellation [0x5180 - 0x51A3] 7-48
7.11 VAP control [0x5900 - 0x5910] 7-49
7.12 AWB control [0x5100 - 0x5D1B] 7-50
7.13 DNS control [0x5210 - 0x5256] 7-57
7.14 CIP control [0x5280 - 0x52E1] 7-60
7.15 CMX control [0xC318 - 0xC347] 7-68
7.16 LLF control [0x5380 - 0x538A] 7-70
7.17 combine control [0x5400 - 0x5C6F] 7-71
7.18 NMLZ control [0x5480 - 0x5C78] 7-78
7.19 TMAP control [0x5500 - 0x5CFB] 7-79
7.20 FC control [0x4200 - 0x4203] 7-87
7.21 format control [0x4300 - 0x4309] 7-87
7.22 VFIFO control [0x4600 - 0x4639] 7-88
7.23 DVP control [0x4700 - 0x470D] 7-91
7.24 temperature sensor control [0x6706 - 0x6721] 7-92
7.25 embedded line control [0x6800 - 0x6807] 7-93
7.26 group writer [0x6F00 - 0x6F1F] 7-94
8 operating specifications 8-1
8.1 absolute maximum ratings 8-1
8.2 functional temperature 8-1
8.3 DC characteristics 8-2
8.4 AC characteristics 8-3
9 mechanical specifications 9-1
9.1 physical specifications 9-1
9.2 IR reflow specifications 9-2

10 optical specifications **10-1**
10.1 sensor array center 10-1
10.2 lens chief ray angle (CRA) 10-2
10.3 spectrum response curve 10-3

list of figures

figure 1-1	pin diagram	1-4
figure 2-1	OV10633/OV10133 block diagram	2-2
figure 2-2	OV10633/OV10133 reference schematic	2-3
figure 2-3	PLL control diagram	2-5
figure 2-4	message type	2-6
figure 2-5	SCCB single read from random location	2-7
figure 2-6	SCCB single read from current location	2-7
figure 2-7	SCCB sequential read from random location	2-8
figure 2-8	SCCB sequential read from current location	2-8
figure 2-9	SCCB single write to random location	2-9
figure 2-10	SCCB sequential write to random location	2-9
figure 2-11	SCCB interface timing	2-10
figure 2-12	power on timing diagram	2-11
figure 3-1	sensor array region color filter layout	3-1
figure 4-1	mirror and flip samples	4-1
figure 4-2	color bar types	4-2
figure 4-3	color, black and white square bars	4-5
figure 4-4	transparent effect	4-5
figure 4-5	rolling bar effect	4-5
figure 4-6	frame structure diagram	4-7
figure 4-7	position window diagram	4-10
figure 4-8	position weight diagram	4-14
figure 4-9	AEC/AGC target/range diagram	4-16
figure 5-1	LENC coefficient versus sensor gain	5-3
figure 5-2	RAW domain DNS - long	5-16
figure 5-3	RAW domain DNS - short	5-16
figure 5-4	auto color saturation graph	5-28
figure 6-1	DVP timing diagram	6-3
figure 6-2	DVP setup/hold time diagram	6-5
figure 9-1	package specifications	9-1
figure 9-2	IR reflow ramp rate requirements	9-2
figure 10-1	sensor array center	10-1

figure 10-2 chief ray angle (CRA) 10-2
figure 10-3 spectrum response curve diagram 10-3

list of tables

table 1-1 signal descriptions 1-1
table 2-1 DVP supported formats and frame rates 2-4
table 2-2 driving capability and direction control for I/O pads 2-4
table 2-3 SCCB interface timing specifications 2-10
table 2-4 power on timing 2-11
table 2-5 system control registers 2-12
table 4-1 mirror and flip function control 4-1
table 4-2 enter/exit color bar settings 4-3
table 4-3 test pattern registers 4-6
table 4-4 format related registers 4-7
table 4-5 position window control registers 4-10
table 4-6 AEC position weight registers 4-14
table 4-7 AEC target/range control registers 4-16
table 4-8 BLC control functions 4-25
table 5-1 DSP top registers 5-1
table 5-2 LENC control registers 5-3
table 5-3 AWB registers 5-6
table 5-4 AWB long calibration registers 5-8
table 5-5 AWB short calibration registers 5-11
table 5-6 AWB control registers 5-14
table 5-7 AWB range registers 5-15
table 5-8 DNS control registers 5-17
table 5-9 CIP control registers 5-20
table 5-10 CMX control registers 5-26
table 5-11 auto color saturation control registers 5-29
table 5-12 combine control registers 5-29
table 5-13 normalize control registers 5-32
table 5-14 tone_mapping registers 5-33
table 5-15 group control registers 5-36
table 5-16 WINC control registers 5-37
table 5-17 WBC control registers 5-37
table 6-1 TPM control 6-1

table 6-2 embedded line control 6-2
table 6-3 DVP timing specifications 6-3
table 6-4 DVP setup/hold time 6-5
table 7-1 system control registers 7-1
table 7-2 analog control registers 7-7
table 7-3 sensor control 7-8
table 7-4 timing control 7-10
table 7-5 OTP control 7-12
table 7-6 BLC control functions 7-15
table 7-7 AEC control registers 7-23
table 7-8 ISP control registers 7-43
table 7-9 LENC control registers 7-45
table 7-10 white/black pixel cancellation registers 7-48
table 7-11 VAP control registers 7-49
table 7-12 AWB control registers 7-50
table 7-13 DNS control registers 7-57
table 7-14 CIP control registers 7-60
table 7-15 CMX control registers 7-68
table 7-16 LLF control registers 7-70
table 7-17 combine control registers 7-71
table 7-18 NMLZ control registers 7-78
table 7-19 TMAP control registers 7-79
table 7-20 FC control 7-87
table 7-21 format control 7-87
table 7-22 VFIFO control 7-88
table 7-23 DVP control 7-91
table 7-24 temperature sensor control (TPM) 7-92
table 7-25 embedded line control registers (EMB) 7-93
table 7-26 group writer registers 7-94
table 8-1 absolute maximum ratings 8-1
table 8-2 functional temperature 8-1
table 8-3 DC characteristics (-20°C < TJ < 70°C) 8-2
table 8-4 AC characteristics (TA = 25°C, VDD-A = 3.3V, VDD-IO = 1.8V) 8-3
table 8-5 timing characteristics 8-3
table 9-1 reflow conditions 9-2

table 10-1 CRA versus image height plot 10-2

1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV10633/OV10133 image sensor. The package information is shown in section 9.

table 1-1 signal descriptions (sheet 1 of 4)

pin number	signal name	pin type	description
A1	NC	–	no connect
A2	DVDD	power	1.5V power
A3	SDA	I/O	SCCB interface data
A4	D2	I/O	video data output[2]
A5	DOGND	ground	I/O ground
A6	D8	I/O	video data output[8]
A7	HREF	I/O	video output horizontal signal
A8	D3	I/O	video data output[3]
A9	DOVDD	power	1.7 ~ 3.6V power
A10	NC	–	no connect
B1	NC	–	no connect
B2	PVDD	power	PLL analog power
B3	DOVDD	power	1.7 ~ 3.6V power
B4	SCL	input	SCCB interface input clock
B5	D4	I/O	video data output[4]
B6	D7	I/O	video data output[7]
B7	DVDD	power	1.5V power
B8	D1	I/O	video data output[1]
B9	DVDD	power	1.5V power
B10	NC	–	no connect
C1	AGND	ground	analog ground
C2	NC	–	no connect
C3	AVDD	power	3.3V power
C4	D0	I/O	video data output[0]
C5	D6	I/O	video data output[6]

table 1-1 signal descriptions (sheet 2 of 4)

pin number	signal name	pin type	description
C6	D9	I/O	video data output[9]
C7	DOGND	ground	I/O ground
C8	PCLK	I/O	video output clock
C9	NC	–	no connect
C10	DVDD	power	1.5V power
D1	NC	–	no connect
D2	DVDD	power	1.5V power
D3	NC	–	no connect
D4	XVCLK	input	system clock input
D5	DOGND	ground	I/O ground
D6	D5	I/O	video data output[5]
D7	AGND	ground	analog ground
D8	NC	–	no connect
D9	DOGND	ground	I/O ground
D10	NC	–	no connect
E1	NC	–	no connect
E2	NC	–	no connect
E3	NC	–	no connect
E4	DOGND	ground	I/O ground
E7	NC	–	no connect
E8	DOGND	ground	I/O ground
E9	NC	–	no connect
E10	DVDD	power	1.5V power
F1	NC	–	no connect
F2	NC	–	no connect
F3	NC	–	no connect
F4	NC	–	no connect
F7	NC	–	no connect
F8	NC	–	no connect
F9	NC	–	no connect

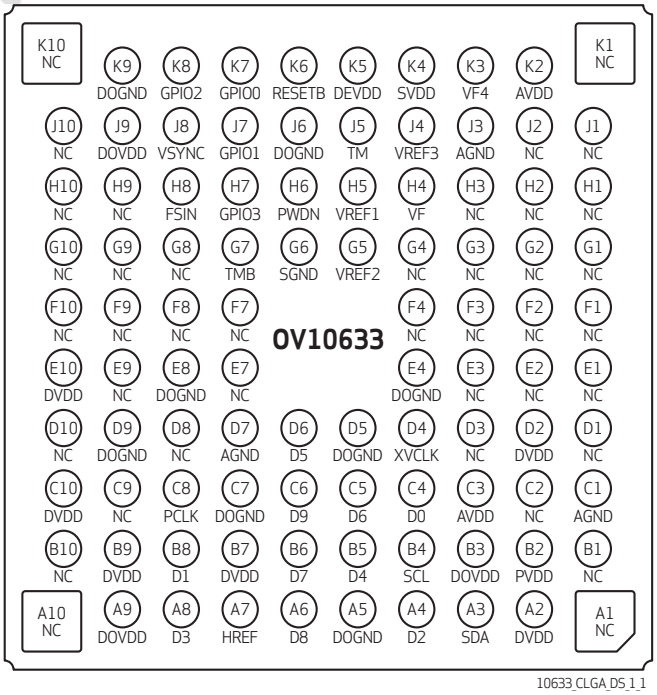
table 1-1 signal descriptions (sheet 3 of 4)

pin number	signal name	pin type	description
F10	NC	–	no connect
G1	NC	–	no connect
G2	NC	–	no connect
G3	NC	–	no connect
G4	NC	–	no connect
G5	VREF2	reference	internal reference
G6	SGND	ground	sensor array ground
G7	TMB	input	test mode (active low)
G8	NC	–	no connect
G9	NC	–	no connect
G10	NC	–	no connect
H1	NC	–	no connect
H2	NC	–	no connect
H3	NC	–	no connect
H4	VF	reference	internal reference
H5	VREF1	reference	internal reference (connect to AGND)
H6	PWDN	input	input (active high with pull-down resistor)
H7	GPIO3	I/O	general purpose IO3
H8	FSIN	I/O	frame sync input
H9	NC	–	no connect
H10	NC	–	no connect
J1	NC	–	no connect
J2	NC	–	no connect
J3	AGND	ground	analog ground
J4	VREF3	reference	internal reference
J5	TM	input	test mode (active high)
J6	DOGND	ground	I/O ground
J7	GPIO1/SCCBID1	I/O	general purpose IO1/ SCCBID1
J8	VSYNC	I/O	vertical signal video output
J9	DOVDD	power	1.7 ~ 3.6V power

table 1-1 signal descriptions (sheet 4 of 4)

pin number	signal name	pin type	description
J10	NC	–	no connect
K1	NC	–	no connect
K2	AVDD	power	3.3V power
K3	VF4	reference	internal reference
K4	SVDD	power	3.3V power
K5	DEVDD	power	analog power
K6	RESETB	input	reset input (active low with internal pull-up resistor)
K7	GPIO0/SCCBIO0	I/O	general purpose IO0/ SCCBID0
K8	GPIO2/SCCBID2	I/O	general purpose IO2/ SCCBID2
K9	DOGND	ground	I/O ground
K10	NC	–	no connect

figure 1-1 pin diagram



10633_CLGA_DS_1_1

2 system level description

2.1 overview

The OV10633 (color) and OV10133 (b&w) image sensors are low voltage, high performance 1/3-inch 1 Megapixel CMOS image sensors that provide the full functionality of a single chip 1280x720 camera using OmniPixel3-HS™ technology in a small footprint package. It provides full-frame, sub-sampled and windowed images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV10633/OV10133 has an image array capable of operating at up to 30 frames per second (fps) in full resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, white balance, defective pixel canceling, etc., are programmable through the SCCB interface. In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

2.2 architecture

The OV10633/OV10133 sensor core generates stream pixel data at a constant frame rate, indicated by HREF, VSYNC, and PCLK.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC.

figure 2-1 OV10633/OV10133 block diagram

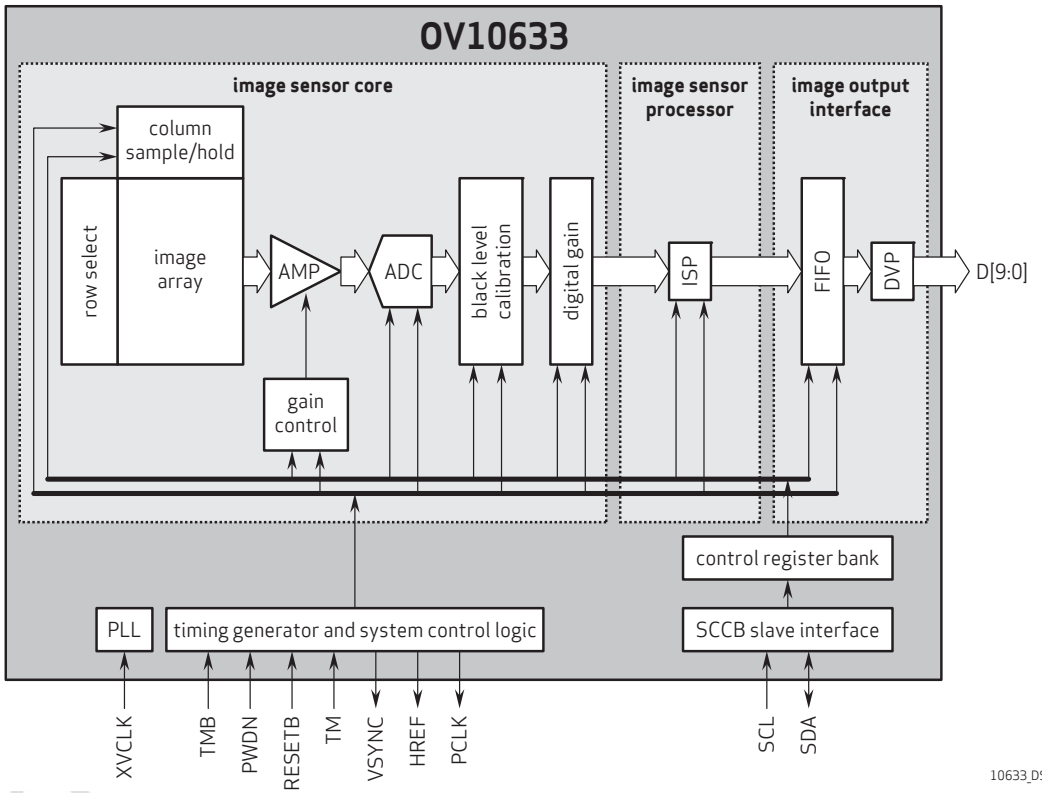
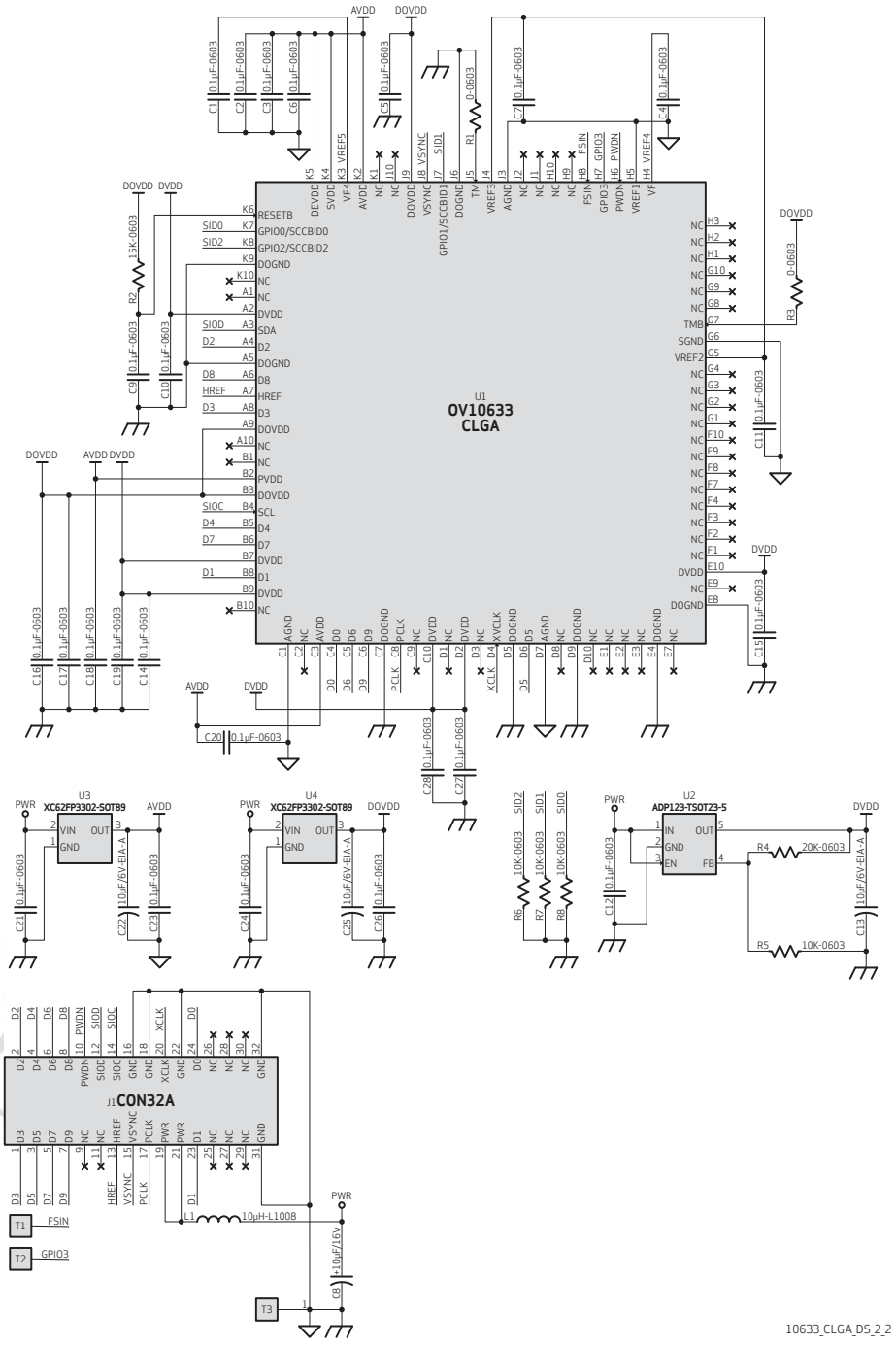


figure 2-2 OV10633/OV10133 reference schematic



2.3 format and frame rate

The OV10633/OV10133 supports 12-/18-bit raw RGB.

table 2-1 DVP supported formats and frame rates

format	resolution	frame rate	mode
HD 720p	1280 x 720	30 fps	cropping
WVGA	752 x 480	30 fps	cropping
VGA	640 x 480	30 fps	cropping
600 x 400	600 x 400	60 fps	skipping, cropping
CIF	352 x 288	60 fps	skipping, cropping
QVGA	320 x 240	60 fps	skipping, cropping
any size		30 fps	cropping, windowing

2.4 I/O control

The OV10633/OV10133 I/O pad direction and driving capability can be easily adjusted. **table 2-2** lists the driving capability and direction control registers of the I/O pads.

table 2-2 driving capability and direction control for I/O pads (sheet 1 of 2)

function	register	R/W	description
output drive capability control	0x3011	RW	Bit[7:6]: output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
D[9:0] I/O control	0x3000[1:0], 0x3001[7:0]	RW	input/output selection for the D[9:0] pins 0: input 1: output
D[9:0] output select	0x300E[1:0], 0x300F[7:0]	RW	output selection for the D[9:0] pins 0: video data output 1: register-controlled value, refer to registers {0x3008[1:0], 0x3009[7:0]} and {0x3008[1:0], 0x3001[7:0]}
D[9:0] output value	0x3008[1:0], 0x3009[7:0]	RW	D[9:0] output value
VSYNC I/O control	0x3002	RW	Bit[7]: input/output selection for the VSYNC pin 0: input 1: output

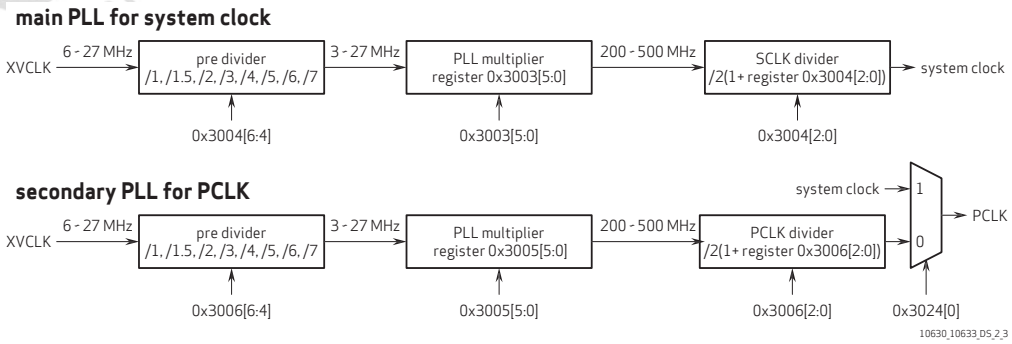
table 2-2 driving capability and direction control for I/O pads (sheet 2 of 2)

function	register	R/W	description
VSYNC output select	0x3010	RW	Bit[7]: output selection for the VSYNC pin 0: vertical sync output 1: register-controlled value, refer to register 0x300D[7] and 0x3002[7]
VSYNC output value	0x300D	RW	Bit[7]: VSYNC output value
HREF I/O control	0x3002	RW	Bit[6]: input/output selection for the HREF pin 0: input 1: output
HREF output select	0x3010	RW	Bit[6]: output selection for the HREF pin 0: horizontal reference output 1: register-controlled value, refer to register 0x300D[6] and 0x3002[6]
HREF output value	0x300D	RW	Bit[6]: HREF output value
PCLK I/O control	0x3002	RW	Bit[5]: input/output selection for the PCLK pin 0: input 1: output
PCLK output select	0x3010	RW	Bit[5]: output selection for the PCLK pin 0: pixel clock output 1: register-controlled value, refer to register 0x300D[5] and 0x3002[5]
PCLK output value	0x300D	RW	Bit[5]: PCLK output value

2.5 system clock control

The PLL inside the device generates a maximum 96 MHz system clock from a 6~27 MHz input clock. A programmable clock divider is needed to generate different frame rate timing.

figure 2-3 PLL control diagram



2.6 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.6.1 data transfer protocol

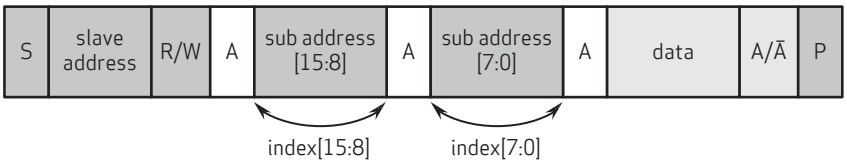
The data transfer of the OV10633/OV10133 follows the SCCB protocol.

2.6.2 message format

The OV10633/OV10133 supports the message format shown in **figure 2-4**. The 7-bit I2C slave device address is 0x30 | SCCBID[2:0], where SCCBID[2:0] is from pin GPIO/SCCBID[2:0]. The repeated START (Sr) condition is not shown in **figure 2-5**, but is shown in **figure 2-6** and **figure 2-7**.

figure 2-4 message type

message type: 16-bit sub-address, 8-bit data, and 7-bit slave address



	from slave to master	S	START condition	A	acknowledge
	from master to slave	P	STOP condition	Ā	negative acknowledge
	direction depends on operation	Sr	repeated START condition		

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2.6.3 read / write operation

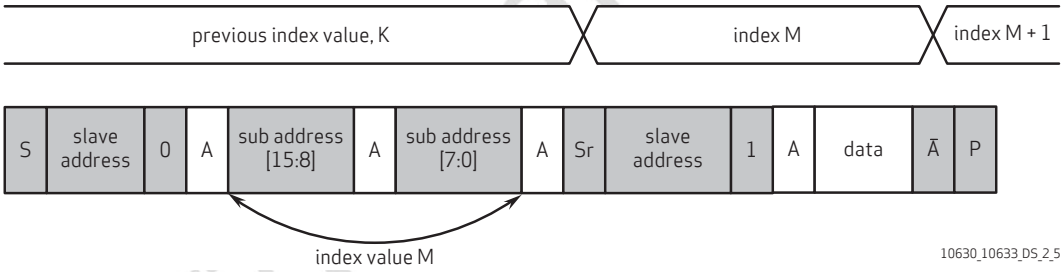
The OV10633/OV10133 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

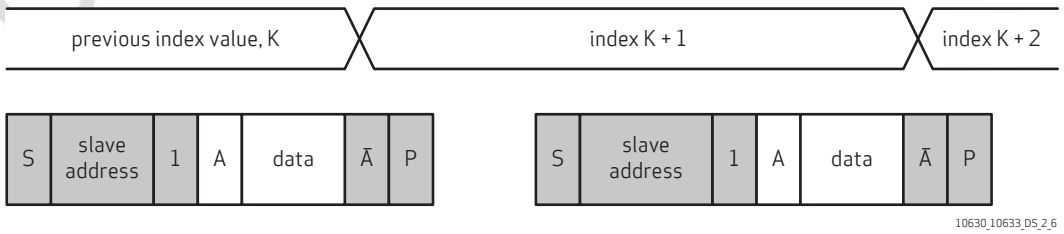
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 2-5**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-5 SCCB single read from random location



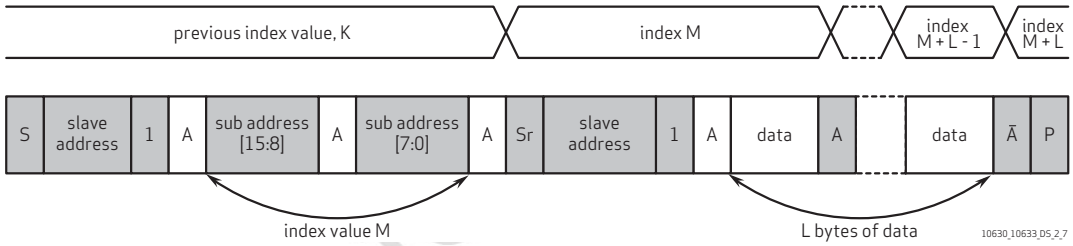
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 2-6**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-6 SCCB single read from current location



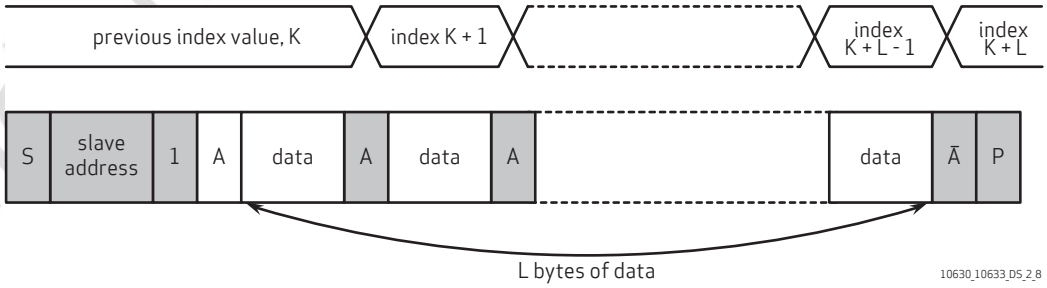
The sequential read from a random location is illustrated in **figure 2-7**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-7 SCCB sequential read from random location



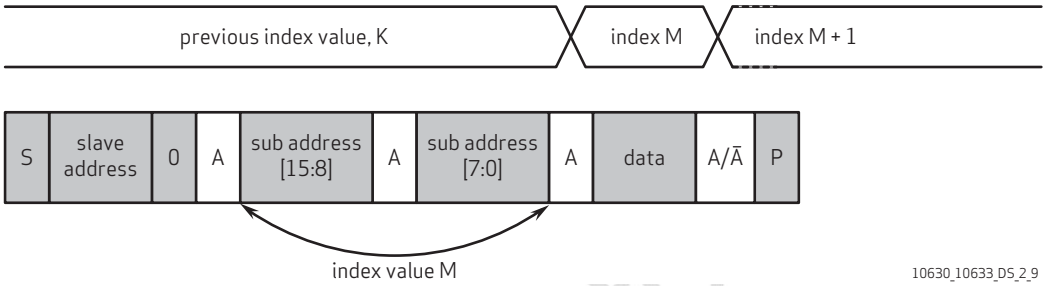
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation. as shown in **figure 2-8**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-8 SCCB sequential read from current location



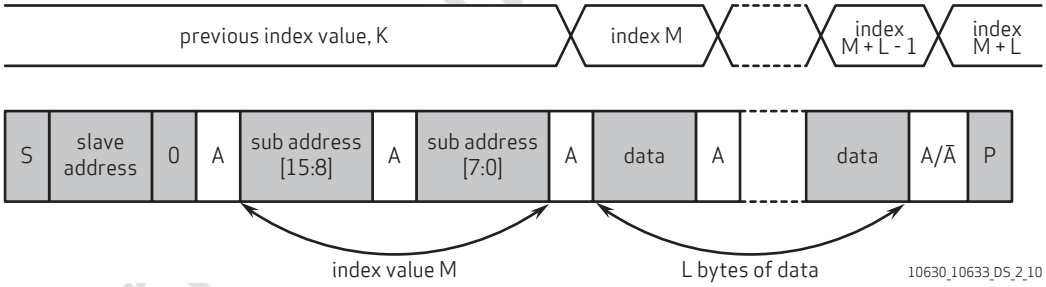
The write operation to a random location is illustrated in **figure 2-9**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-9 SCCB single write to random location



The sequential write is illustrated in **figure 2-10**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-10 SCCB sequential write to random location



2.6.4 SCCB timing

figure 2-11 SCCB interface timing

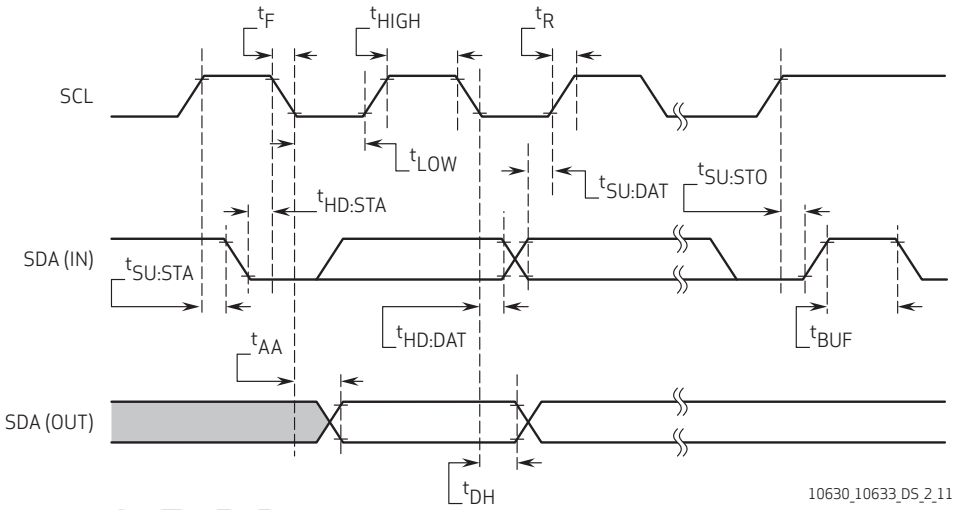


table 2-3 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			400	KHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400KHz mode

b. timing measurement shown at the beginning of the rising edge or the end of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the end of rising edge or the beginning of the falling edge signifies 90%

2.7 standby

To initiate hardware standby mode, the PWDN pin must be tied to high. When this occurs, the OV10633/OV10133 internal device clock is halted and all internal counters are reset and registers are maintained.

2.8 power on timing

figure 2-12 power on timing diagram

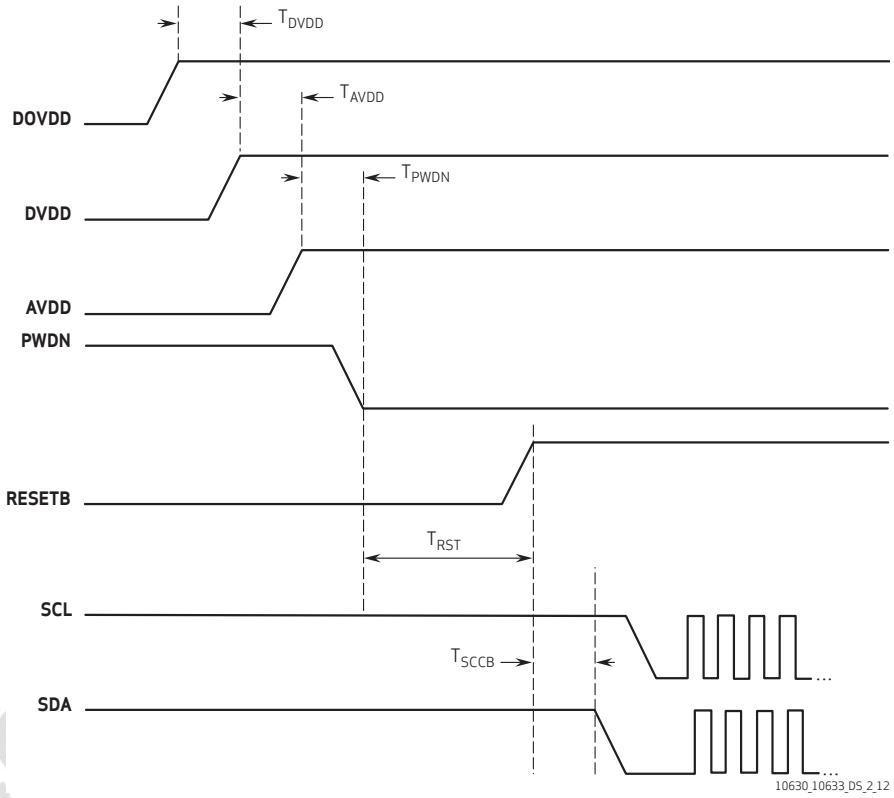


table 2-4 power on timing

parameter	min	max	unit
T_{DVDD}	>0	10	ms
T_{AVDD}	>0	n/a	ms
T_{PWDN}	>1	n/a	ms
T_{RST}	>200	n/a	µs
T_{SCCB}	>2048	n/a	XVCLK cycles

2.9 system control

table 2-5 system control registers

address	register name	default value	R/W	description
0x0100	STREAM MODE	0x00	RW	Bit[7:1]: Not used Bit[0]: Turn on video stream after power up, always set to "1" 0: Not used 1: Stream on
0x0103	SOFTWARE RESET	0x00	RW	Software Reset will Auto Clear by Itself to 0x00

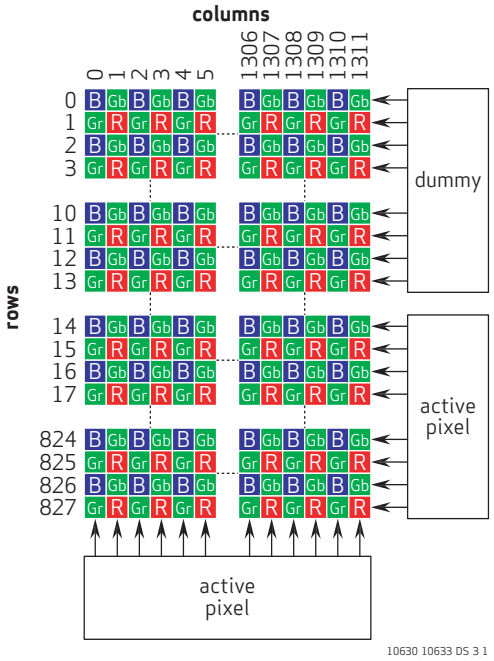
3 pixel array structure

The OV10633/OV10133 sensor has an image array of 1312 columns by 828 rows. figure 3-1 shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 828 rows, 814 rows are active rows and can be output. The other rows are used for black level calibration and interpolation.

The sensor array design is based on a read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



4 image sensor core digital functions

4.1 mirror and flip

The OV10633/OV10133 provides mirror mode, which reverses the sensor data read-out order horizontally, and flip mode which reverses it vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

10630_10633_DS_4_1

table 4-1 mirror and flip function control

function	register	description
mirror	0x381D	Bit[1:0]: mirror ON/OFF select 00: horizontal mirror OFF 01: not allowed 10: not allowed 11: horizontal mirror ON
flip	0x381C	Bit[7:6]: flip ON/OFF select 00: vertical flip OFF 01: not allowed 10: not allowed 11: vertical flip ON

4.2 test pattern

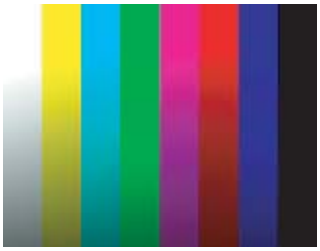
For testing purposes, the OV10633/OV10133 offers one type of analog test pattern and three types of digital test patterns. The analog test pattern is a color bar which is controlled by register 0x370A[2]. The three types of digital test patterns are color bar, square and random data. Also, the OV10633/OV10133 also offers two digital effects: transparent effect and rolling bar effect. The output type of digital test pattern is controlled by the test_pattern_type register (0x503E[1:0]). The digital test pattern function is controlled by register 0x503D[7].

4.2.1 color bar

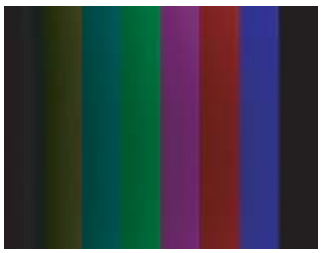
There are four types of color bars shown in **figure 4-2**.

figure 4-2 color bar types

color bar type 1
0x503D[5:4]=2'b00



color bar type 2
0x503D[5:4]=2'b01



color bar type 3
0x503D[5:4]=2'b10

color bar type 4
0x503D[5:4]=2'b11

10630_10633_DS_4_2

table 4-2 enter/exit color bar settings (sheet 1 of 2)

enter settings[a]	exit settings[b]
60 5120 01	60 5120 00
60 56d0 01	60 56d0 00
60 5300 01	60 5300 01
60 5301 00	60 5301 00
60 5302 00	60 5302 00
60 5303 00	60 5303 0e
60 5304 00	60 5304 00
60 5305 00	60 5305 0e
60 5306 00	60 5306 00
60 5307 00	60 5307 36
60 5308 01	60 5308 00
60 5309 00	60 5309 d9
60 530a 00	60 530a 00
60 530b 00	60 530b 0f
60 530c 00	60 530c 00
60 530d 00	60 530d 2c
60 530e 00	60 530e 00
60 530f 00	60 530f 59
60 5310 01	60 5310 00
60 5311 00	60 5311 7b
60 5312 00	60 5312 00
60 5313 00	60 5313 22
60 5314 01	60 5314 00
60 5315 00	60 5315 d5
60 5316 00	60 5316 00
60 5317 00	60 5317 13
60 5318 00	60 5318 00
60 5319 00	60 5319 18
60 531a 00	60 531a 00

table 4-2 enter/exit color bar settings (sheet 2 of 2)

enter settings[a]	exit settings[b]
60 531b 00	60 531b 26
60 531c 01	60 531c 00
60 531d 00	60 531d dc
60 531e 00	60 531e 00
60 531f 00	60 531f 02
60 5320 00	60 5320 00
60 5321 00	60 5321 24
60 5322 00	60 5322 00
60 5323 00	60 5323 56
60 5324 01	60 5324 00
60 5325 00	60 5325 85
60 5326 00	60 5326 00
60 5327 00	60 5327 20
60 c2ea 80	60 c2ea 7a
60 c2eb 80	60 c2eb 90
60 5000 79	60 5000 ff

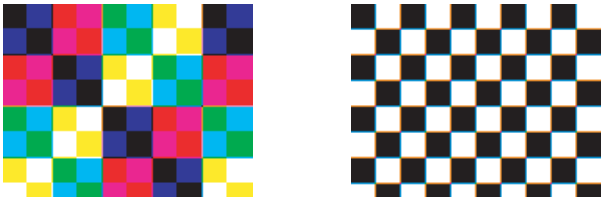
a. before enabling color bar, use these settings

b. after turning off color bar, use these settings to return to normal mode

4.2.2 square

There are two types of square test patterns: color square and black-white square.

figure 4-3 color, black and white square bars



10630_10633_DS_4_3

4.2.3 random data

There are two types of random data test patterns: frame-changing and frame-fixed random data.

4.2.4 transparent effect

figure 4-4 is an example which shows a transparent color bar image.

figure 4-4 transparent effect

10630_10633_DS_4_4

4.2.5 rolling bar effect

figure 4-5 is an example which shows a rolling bar on color bar image.

figure 4-5 rolling bar effect

10630_10633_DS_4_5

table 4-3 test pattern registers

address	register name	default value	R/W	description
0x370A	SENSOR REG0A	0x00	RW	Bit[2]: Analog color bar enable 0: Disable 1: Enable
0x503D	ISP CTRL3D	0x00	RW	Bit[7]: Digital test pattern enable 0: Disable 1: enable Bit[5:4]: Color bar type (see **figure 4-2**) Bit[2]: Rolling horizontal bar in color bar test pattern 0: Disable rolling bar 1: Enable rolling bar Bit[1:0]: Debug control Changing this value is not allowed
0x503E	ISP CTRL3E	0x00	RW	Bit[7:4]: Seed of random number Initial seed for random data pattern Bit[3]: B&W square test pattern enable 0: Output square is color square 1: Output square is black-white square Bit[2]: Transparent enable mode 0: Disable 1: Enable Bit[1:0]: Test pattern type 00: Color bar 01: Random data 10: Square 11: Not allowed

4.3 image cropping and windowing

An image cropping area is defined by four parameters: H_crop_start, H_crop_end, V_crop_start, V_crop_end; windowing area is defined by four parameters, horizontal start (H_win_off), horizontal width (H_output_size), vertical start (V_win_off), and vertical height (V_output_size). By properly setting the parameters, any portion within the sense array size can be cropped as a visible area. This cropping is achieved by simply masking the pixels outside the cropping window; thus, it will not affect original timings. It will also not conflict with the flip and mirror functions.

The OV10633/OV10133 can:

- support any size vertical crop
- support three size horizontal crop: 1312, 768 and 656
- support WDR mode
- support non-WDR mode
- support mirror and flip mode
- support any size windowing

figure 4-6 frame structure diagram

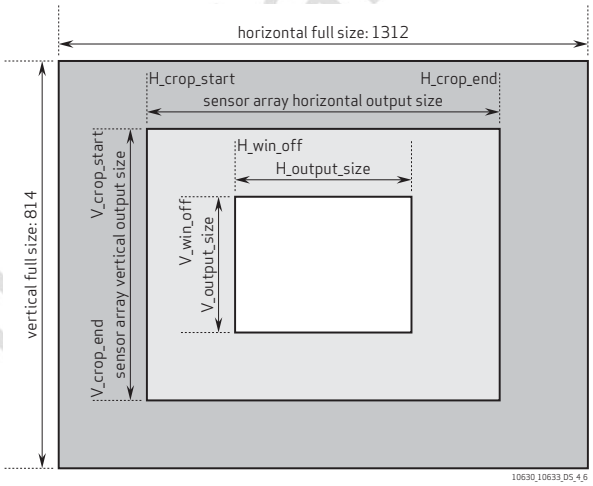


table 4-4 format related registers (sheet 1 of 2)

address	default value	R/W	description
0x3621	0x03	RW	Bit[4:3]: Horizontal crop mode select 00: Full size 01: Horizontal crop to 768 10: Horizontal crop to 656
0x3802	0x00	RW	Vertical Crop Start Address High Byte
0x3803	0x00	RW	Vertical Crop Start Address Low Byte

table 4-4 format related registers (sheet 2 of 2)

address	default value	R/W	description
0x3806	0x05	RW	Vertical Crop End Address High Byte
0x3807	0x0F	RW	Vertical Crop End Address Low Byte
0x3808	0x05	RW	DVP Horizontal Output Size High Byte
0x3809	0x00	RW	DVP Horizontal Output Size Low Byte
0x380A	0x03	RW	DVP Vertical Output Size High Byte
0x380B	0x20	RW	DVP Vertical Output Size Low Byte
0x380C	0x07	RW	Line Length High Byte
0x380D	0x70	RW	Line Length Low Byte
0x380E	0x03	RW	Frame Length High Byte
0x380F	0x48	RW	Frame Length Low Byte
0x3810	0x00	RW	Horizontal ISP Window Offset High Byte
0x3811	0x00	RW	Horizontal ISP Window Offset Low Byte
0x3812	0x00	RW	Vertical ISP Window Offset High Byte
0x3813	0x00	RW	Vertical ISP Window Offset Low Byte
0x381C	0x00	RW	Bit[0]: Vertical sub-sample in array
0x5005	0x08	RW	Bit[7]: Vertical sub-sample in ISP Bit[0]: VAP enable
0x3007	0x01	RW	Bit3:0]: DVP PCLK divider Used when ISP horizontal sub-sample
0x4600	0x00	RW	Bit[2]: VFIFO 2 bytes input 0: Raw10 mode 1: Other mode
0x4300	0x00	RW	Bit[7:4]: Output format select 0x3: YUV mode 0xF: RAW mode Others: Not allowed

4.4 AEC/AGC algorithms

In the OV10633/OV10133, the exposure/gain control is designed to adjust the weighted frame average to a user defined range. The weight of each pixel includes three parts: position weight, combination weight and luminance weight. Instead of using the whole frame, the statistic window can be defined manually with the left-top corner {0x5601[2:0], 0x5602}, {0x5603[1:0], 0x5604}, width {0x5605[2:0], 0x5606} and height {0x5607[1:0], 0x5608}. The pixels outside of the window will not be included in the weighted average.

There are three target modes: AA, AB and ABC mode. This is defined by the target mode register 0xC450[1:0].

The AEC/AGC algorithms supports WDR mode and non-WDR mode. Register 0xC454[0] must be set to 1 for non-WDR mode and 0 for WDR mode.

In non-WDR mode, the sensor only uses one sub-pixel. In WDR mode, the AEC/AGC needs to determine the exposure and the gain for the two sub-pixels. It supports auto ratio mode, fixed ratio mode and geometric proportion mode.

Auto ratio mode means the long exposure/short exposure ratio changes automatically according to the scene. It supports all modes (AA,AB and ABC). To enable auto ratio mode, the fixed ratio mode register 0xC456[0] and the geometric proportion mode register 0xC457[0] must be set to 0.

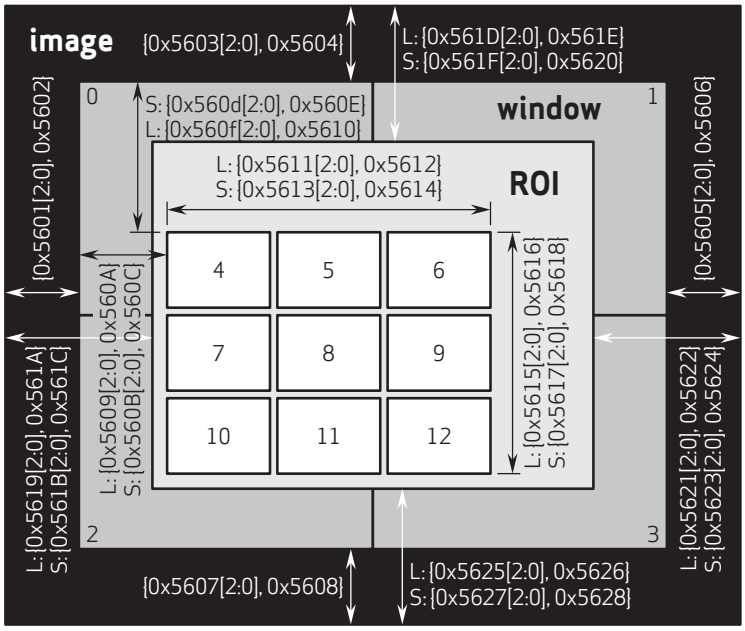
Fixed ratio mode means the long exposure/short exposure ratio is fixed regardless of the scene. It supports all modes (AA, AB and ABC). To enable fixed ratio mode, register 0xC456[0] should be set to 1. The fixed ratio can be set by register 0xC490. In this mode, the geometric proportion mode register 0xC457[0] should be set to 0.

Geometric proportion mode works only in AB or ABC modes. This means that the relationship between the stable range of AB or ABC frame is fixed. The fixed relationship can be adjusted by registers 0xC492 and 0xC493. In geometric proportion mode, the register 0xC457[0] must be set to be 1.

4.4.1 position weight

The position weight is decided by the position of the pixel, which also includes two independent parts: the windowing weight and the region of interest (ROI) weight. The windowing weight function divides the statistic window into 13 windows as shown in **figure 4-7** and each window has a weight defined by one of registers 0x562E~0x5647. Also, the size and position of the center 3×3 windows can be defined with registers 0x5609~0x5618. The ROI weight is determined by whether the pixel is within the ROI region which is defined with the registers 0x5619~0x5628. The weight of pixels, which are in ROI region is defined with register 0x562A (for long exposure channel) or 0x562C (for short exposure channel). The weight of other pixels is defined with register 0x562B (for long exposure channel) and 0x562D (for short exposure channel). The long ROI shift (0x5629[5:3]) and short ROI shift (0x5629[2:0]) control the precision of the long ROI weight and the short ROI weight, separately.

figure 4-7 position window diagram



10630_10633_DS_4_7

table 4-5 position window control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5600	AEC CTRL00	0x01	RW	Bit[1:0]: Sampling 0x: 2 10: 4 11: 8
0x5601	AEC CTRL01	0x00	RW	Bit[2:0]: Statwinleft[10:8] Horizontal start point of outer 4-zone statistic window
0x5602	AEC CTRL02	0x00	RW	Bit[7:0]: Statwinleft[7:0] Horizontal start point of outer 4-zone statistic window
0x5603	AEC CTRL03	0x00	RW	Bit[1:0]: Statwintop[9:8] Vertical start point of outer 4-zone statistic window
0x5604	AEC CTRL04	0x00	RW	Bit[7:0]: Statwintop[7:0] Vertical start point for statistic image
0x5605	AEC CTRL05	0x00	RW	Bit[2:0]: Statwinright[10:8] Horizontal end point of outer 4-zone statistic window

table 4-5 position window control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5606	AEC CTRL06	0x00	RW	Bit[7:0]: Statwinright[7:0] Horizontal end point of outer 4-zone statistic window
0x5607	AEC CTRL07	0x00	RW	Bit[1:0]: Statwinbottom[9:8] Vertical end point of outer 4-zone statistic window
0x5608	AEC CTRL08	0x00	RW	Bit[7:0]: Statwinbottom[7:0] Vertical end point of outer 4-zone statistic window
0x5609	AEC CTRL09	0x00	RW	Bit[2:0]: winleft_l[10:8] Horizontal start point of inner 9-zone window long exposure sub-pixel
0x560A	AEC CTRL0A	0x64	RW	Bit[7:0]: winleft_l[7:0] Horizontal start point of inner 9-zone window long exposure sub-pixel
0x560B	AEC CTRL0B	0x00	RW	Bit[2:0]: winleft_s[10:8] Horizontal start point of inner 9-zone window short exposure sub-pixel
0x560C	AEC CTRL0C	0x64	RW	Bit[7:0]: winleft_s[7:0] Horizontal start point of inner 9-zone window short exposure sub-pixel
0x560D	AEC CTRL0D	0x00	RW	Bit[1:0]: wintop_l[9:8] Vertical start point of inner 9-zone window long exposure sub-pixel
0x560E	AEC CTRL0E	0x4B	RW	Bit[7:0]: wintop_l[7:0] Vertical start point of inner 9-zone window long exposure sub-pixel
0x560F	AEC CTRL0F	0x00	RW	Bit[1:0]: wintop_s[9:8] Vertical start point of inner 9-zone window short exposure sub-pixel
0x5610	AEC CTRL10	0x4B	RW	Bit[7:0]: wintop_s[7:0] Vertical start point of inner 9-zone window short exposure sub-pixel
0x5611	AEC CTRL11	0x00	RW	Bit[2:0]: winwidth_l[10:8] Horizontal width of inner 9-zone window long exposure sub-pixel
0x5612	AEC CTRL12	0xC8	RW	Bit[7:0]: winwidth_l[7:0] Horizontal width of inner 9-zone window long exposure sub-pixel

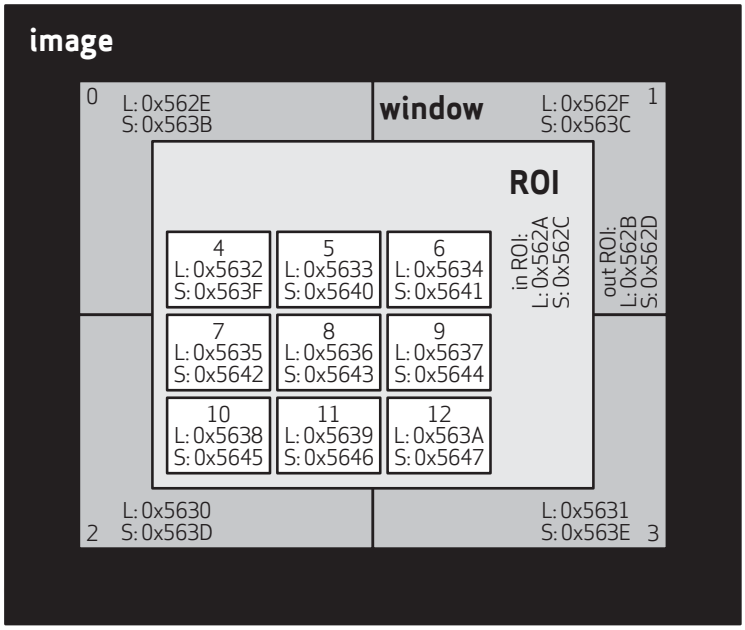
table 4-5 position window control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5613	AEC CTRL13	0x00	RW	Bit[2:0]: winwidth_s[10:8] Horizontal width of inner 9-zone window short exposure sub-pixel
0x5614	AEC CTRL14	0xC8	RW	Bit[7:0]: winwidth_s[7:0] Horizontal width of inner 9-zone window short exposure sub-pixel
0x5615	AEC CTRL15	0x00	RW	Bit[1:0]: winheight_l[9:8] Vertical width of inner 9-zone window long exposure sub-pixel
0x5616	AEC CTRL16	0x96	RW	Bit[7:0]: winheight_l[7:0] Vertical width of inner 9-zone window long exposure sub-pixel
0x5617	AEC CTRL17	0x00	RW	Bit[1:0]: winheight_s[9:8] Vertical width of inner 9-zone window long exposure sub-pixel
0x5618	AEC CTRL18	0x96	RW	Bit[7:0]: winheight_s[7:0] Vertical width of inner 9-zone window long exposure sub-pixel
0x5619	AEC CTRL19	0x00	RW	Bit[2:0]: roileft_l[10:8] Horizontal start point for ROI for long exposure sub-pixel
0x561A	AEC CTRL1A	0x00	RW	Bit[7:0]: roileft_l[7:0] Horizontal start point for ROI for long exposure sub-pixel
0x561B	AEC CTRL1B	0x00	RW	Bit[2:0]: roileft_s[10:8] Horizontal start point for ROI for short exposure sub-pixel
0x561C	AEC CTRL1C	0x00	RW	Bit[7:0]: roileft_s[7:0] Horizontal start point for ROI for short exposure sub-pixel
0x561D	AEC CTRL1D	0x00	RW	Bit[1:0]: roitop_l[9:8] Vertical start point for ROI for long exposure sub-pixel
0x561E	AEC CTRL1E	0x00	RW	Bit[7:0]: roitop_l[7:0] Vertical start point for ROI for long exposure sub-pixel
0x561F	AEC CTRL1F	0x00	RW	Bit[1:0]: roitop_s[9:8] Vertical start point for ROI for short exposure sub-pixel

table 4-5 position window control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5620	AEC CTRL20	0x00	RW	Bit[7:0]: roitop_s[7:0] Vertical start point for ROI for short exposure sub-pixel
0x5621	AEC CTRL21	0x00	RW	Bit[2:0]: roiright_l[10:8] Horizontal end point for ROI for long exposure sub-pixel
0x5622	AEC CTRL22	0x00	RW	Bit[7:0]: roiright_l[7:0] Horizontal end point for ROI for long exposure sub-pixel
0x5623	AEC CTRL23	0x00	RW	Bit[2:0]: roiright_s[10:8] Horizontal end point for ROI for short exposure sub-pixel
0x5624	AEC CTRL24	0x00	RW	Bit[7:0]: roiright_s[7:0] Horizontal end point for ROI for short exposure sub-pixel
0x5625	AEC CTRL25	0x00	RW	Bit[1:0]: roibottom_l[9:8] Vertical end point for ROI for long exposure sub-pixel
0x5626	AEC CTRL26	0x00	RW	Bit[7:0]: roibottom_l[7:0] Vertical end point for ROI for long exposure sub-pixel
0x5627	AEC CTRL27	0x00	RW	Bit[1:0]: roibottom_s[9:8] Vertical end point for ROI for short exposure sub-pixel
0x5628	AEC CTRL28	0x00	RW	Bit[7:0]: roibottom_s[7:0] Vertical end point for ROI for short exposure sub-pixel
0x5629	AEC CTRL29	0x00	RW	Bit[5:3]: r_roishift_l Bit[2:0]: r_roishift_s

figure 4-8 position weight diagram



10630_10633_DS_4_8

table 4-6 AEC position weight registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3621	ANA_ARRAY1	0x03	RW	Bit[4:3]: Horizontal crop mode select 00: Full size 01: Horizontal crop to 768 10: Horizontal crop to 656
0x562A	AEC CTRL2A	0x01	RW	ROIweightl0 for Long Exposure Sub-pixel
0x562B	AEC CTRL2B	0x01	RW	ROIweightl1 for Long Exposure Sub-pixel
0x562C	AEC CTRL2C	0x01	RW	ROIweights0 for Long Exposure Sub-pixel
0x562D	AEC CTRL2D	0x01	RW	ROIweights1 for Long Exposure Sub-pixel
0x562E	AEC CTRL2E	0x01	RW	Weightl0 for Long Exposure Sub-pixel
0x562F	AEC CTRL2F	0x01	RW	Weightl1 for Long Exposure Sub-pixel
0x5630	AEC CTRL30	0x01	RW	Weightl2 for Long Exposure Sub-pixel
0x5631	AEC CTRL31	0x01	RW	Weightl3 for Long Exposure Sub-pixel
0x5632	AEC CTRL32	0x01	RW	Weightl4 for Long Exposure Sub-pixel

table 4-6 AEC position weight registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5633	AEC CTRL33	0x01	RW	WeightI5 for Long Exposure Sub-pixel
0x5634	AEC CTRL34	0x01	RW	WeightI6 for Long Exposure Sub-pixel
0x5635	AEC CTRL35	0x01	RW	WeightI7 for Long Exposure Sub-pixel
0x5636	AEC CTRL36	0x01	RW	WeightI8 for Long Exposure Sub-pixel
0x5637	AEC CTRL37	0x01	RW	WeightI9 for Long Exposure Sub-pixel
0x5638	AEC CTRL38	0x01	RW	WeightIa for Long Exposure Sub-pixel
0x5639	AEC CTRL39	0x01	RW	WeightIb for Long Exposure Sub-pixel
0x563A	AEC CTRL3A	0x01	RW	WeightIc for Long Exposure Sub-pixel
0x563B	AEC CTRL3B	0x01	RW	Weights0 for Short Exposure Sub-pixel
0x563C	AEC CTRL3C	0x01	RW	Weights1 for Short Exposure Sub-pixel
0x563D	AEC CTRL3D	0x01	RW	Weights2 for Short Exposure Sub-pixel
0x563E	AEC CTRL3E	0x01	RW	Weights3 for Short Exposure Sub-pixel
0x563F	AEC CTRL3F	0x01	RW	Weights4 for Short Exposure Sub-pixel
0x5640	AEC CTRL40	0x01	RW	Weights5 for Short Exposure Sub-pixel
0x5641	AEC CTRL41	0x01	RW	Weights6 for Short Exposure Sub-pixel
0x5642	AEC CTRL42	0x01	RW	Weights7 for Short Exposure Sub-pixel
0x5643	AEC CTRL43	0x01	RW	Weights8 for Short Exposure Sub-pixel
0x5644	AEC CTRL44	0x01	RW	Weights9 for Short Exposure Sub-pixel
0x5645	AEC CTRL45	0x01	RW	Weightsa for Short Exposure Sub-pixel
0x5646	AEC CTRL46	0x01	RW	Weightsb for Short Exposure Sub-pixel
0x5647	AEC CTRL47	0x01	RW	Weightsc for Short Exposure Sub-pixel

4.4.2 exposure/gain control

Both long and short exposure are controlled by the same algorithm, which estimates the new exposure based on the weighted average of current frame. Long exposure can change freely in the whole range. Short exposure, however, is limited by the new estimated dynamic range and long exposure.

The AEC/AGC adjustment step is calculated by the distance between current weighted average and the target. When the current weighted average is far from the stable range, the exposure will adjust by big steps to quickly bring the image to stable range. When the current weighted average is close to the stable range, the exposure will adjust by small steps to avoid flickering.

In the OV10633/OV10133, the exposure time and gain changes every two frames. In the end of first frame, the new exposure time and gain will be estimated and the exposure time registers will be updated afterward. The gain registers will be updated at the end of the second frame. So, the third frame will be the result of new exposure and gain.

figure 4-9 AEC/AGC target/range diagram

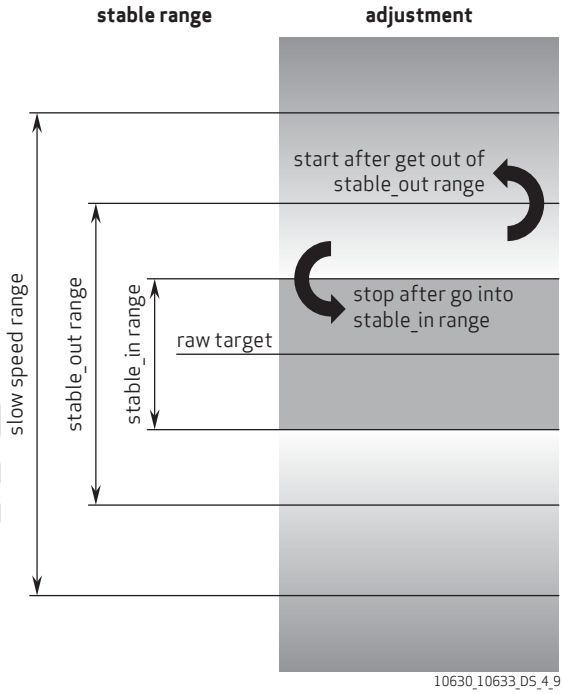


table 4-7 AEC target/range control registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x5648	AEC CTRL48	0x01	RW	Minwl for Long Exposure Sub-pixel
0x5649	AEC CTRL49	0x01	RW	Minws for Short Exposure Sub-pixel
0x564A	AEC CTRL4A	0x00	RW	Bit[1:0]: Maxwl[9:8] for long exposure sub-pixel
0x564B	AEC CTRL4B	0x20	RW	Bit[7:0]: Maxwl[7:0] for long exposure sub-pixel
0x564C	AEC CTRL4C	0x01	RW	Bit[1:0]: Maxws[9:8] for short exposure sub-pixel

table 4-7 AEC target/range control registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x564D	AEC CTRL4D	0x00	RW	Bit[7:0]: Maxws[7:0] for short exposure sub-pixel
0x566C	AEC CTRL6C	0x00	RW	Bit[0]: r_his_en
0x566D	AEC CTRL6D	0x00	RW	r_his_addr
0x566E	AEC CTRL6E	–	R	Bit[6:0]: r_his_data[14:8]
0x566F	AEC CTRL6F	–	R	Bit[7:0]: r_his_data[7:0]
0x56D0	AEC CTRLD0	0x00	RW	Bit[2:0]: r_man_en
0x56D1	AEC CTRLD1	0x00	RW	Bit[1:0]: r_cameragain_l_m[9:8]
0x56D2	AEC CTRLD2	0x10	RW	Bit[7:0]: r_cameragain_l_m[7:0]
0x56D3	AEC CTRLD3	0x00	RW	Bit[1:0]: r_cameragain_s_m[9:8]
0x56D4	AEC CTRLD4	0x10	RW	Bit[7:0]: r_cameragain_s_m[7:0]
0x56D5	AEC CTRLD5	0x00	RW	Bit[7:0]: r_exp_l_m[31:24]
0x56D6	AEC CTRLD6	0x00	RW	Bit[7:0]: r_exp_l_m[23:16]
0x56D7	AEC CTRLD7	0x00	RW	Bit[7:0]: r_exp_l_m[15:8]
0x56D8	AEC CTRLD8	0x00	RW	Bit[7:0]: r_exp_l_m[7:0]
0x56D9	AEC CTRLD9	0x00	RW	Bit[7:0]: r_exp_s_m[31:24]
0x56DA	AEC CTRLDA	0x00	RW	Bit[7:0]: r_exp_s_m[23:16]
0x56DB	AEC CTRLDB	0x00	RW	Bit[7:0]: r_exp_s_m[15:8]
0x56DC	AEC CTRLDC	0x00	RW	Bit[7:0]: r_exp_s_m[7:0]
0x56DF	AEC CTRLDF	0x02	RW	Bit[2:0]: r_digigain_l_m[10:8]
0x56E0	AEC CTRLE0	0x00	RW	Bit[7:0]: r_digigain_l_m[7:0]
0x56E1	AEC CTRLE1	0x02	RW	Bit[2:0]: r_digigain_s_m[10:8]
0x56E2	AEC CTRLE2	0x00	RW	Bit[7:0]: r_digigain_s_m[7:0]
0x56E3	AEC CTRLE3	0x00	RW	Bit[0]: r_exp_ctrl
0x56E4	AEC CTRLE4	0x00	RW	Bit[3:0]: r_exp_l_f[11:8]
0x56E5	AEC CTRLE5	0x00	RW	Bit[7:0]: r_exp_l_f[7:0]
0x56E6	AEC CTRLE6	0x00	RW	Bit[3:0]: r_exp_s_f[11:8]
0x56E7	AEC CTRLE7	0x00	RW	Bit[7:0]: r_exp_s_f[7:0]
0x56E8	AEC CTRLE8	0x00	RW	Bit[0]: r_snrgain_l_m[8]

table 4-7 AEC target/range control registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x56E9	AEC CTRLE9	0x00	RW	Bit[7:0]: r_snrgain_l_m[7:0]
0x56EA	AEC CTRLEA	0x00	RW	Bit[0]: r_snrgain_s_m[8]
0x56EB	AEC CTRLEB	0x00	RW	Bit[7:0]: r_snrgain_s_m[7:0]
0xC2F0	S_MANUAL_EXP11	0x34	RW	Bit[7:0]: manual_expo11[15:8]
0xC2F1	S_MANUAL_EXP11	0x00	RW	Bit[7:0]: manual_expo11[7:0]
0xC2F2	S_MANUAL_EXP12	0x06	RW	Bit[7:0]: manual_expo12[15:8]
0xC2F3	S_MANUAL_EXP12	0x80	RW	Bit[7:0]: manual_expo12[7:0]
0xC2F4	S_MANUAL_EXP21	0x34	RW	Bit[7:0]: manual_expo21[15:8]
0xC2F5	S_MANUAL_EXP21	0x00	RW	Bit[7:0]: manual_expo21[7:0]
0xC2F6	S_MANUAL_EXP22	0x06	RW	Bit[7:0]: manual_expo22[15:8]
0xC2F7	S_MANUAL_EXP22	0x80	RW	Bit[7:0]: manual_expo22[7:0]
0xC2F8	S_MANUAL_EXP31	0x34	RW	Bit[7:0]: manual_expo31[15:8]
0xC2F9	S_MANUAL_EXP31	0x00	RW	Bit[7:0]: manual_expo31[7:0]
0xC2FA	S_MANUAL_EXP32	0x06	RW	Bit[7:0]: manual_expo32[15:0]
0xC2FB	S_MANUAL_EXP22	0x80	RW	Bit[7:0]: manual_expo32[7:0]
0xC2FC	S_MANUAL_GAIN11	0x10	RW	Bit[7:0]: manual_gain11[15:8]
0xC2FD	S_MANUAL_GAIN11	0x18	RW	Bit[7:0]: manual_gain11[7:0]
0xC2FE	S_MANUAL_GAIN12	0x10	RW	Bit[7:0]: manual_gain12[15:8]
0xC2FF	S_MANUAL_GAIN12	0x18	RW	Bit[7:0]: manual_gain12[7:0]
0xC300	S_MANUAL_GAIN21	0x10	RW	Bit[7:0]: manual_gain21[15:8]
0xC301	S_MANUAL_GAIN21	0x18	RW	Bit[7:0]: manual_gain21[7:0]
0xC302	S_MANUAL_GAIN22	0x10	RW	Bit[7:0]: manual_gain22[15:8]
0xC303	S_MANUAL_GAIN22	0x18	RW	Bit[7:0]: manual_gain22[7:0]
0xC304	S_MANUAL_GAIN31	0x10	RW	Bit[7:0]: manual_gain31[15:8]
0xC305	S_MANUAL_GAIN31	0x18	RW	Bit[7:0]: manual_gain31[7:0]
0xC306	S_MANUAL_GAIN32	0x10	RW	Bit[7:0]: manual_gain32[15:8]
0xC307	S_MANUAL_GAIN32	0x18	RW	Bit[7:0]: manual_gain32[7:0]

table 4-7 AEC target/range control registers (sheet 4 of 9)

address	register name	default value	R/W	description
0xC308	S_MANUAL_EN	0x00	RW	Bit[0]: manual_en 0: Disable 1: Enable
0xC309	S_MANUAL_MODE	0x00	RW	Bit[2]: targetc_manual_en 0: Disable 1: Enable Bit[1]: targetb_manual_en 0: Disable 1: Enable Bit[0]: targeta_manual_en 0: Disable 1: Enable
0xC30A	S_MANUAL_DONE	0x00	RW	Bit[1:0]: manual_done 00: Write protected 01: Write valid once 10: Write valid always
0xC450	TARGET_NUM	0x01	RW	Bit[1:0]: Target number 01: AA mode 10: AB mode 11: ABC mode
0xC451	HW_STOP_EN	0x00	RW	Bit[0]: HW stop frame enable (for AB/ABC mode, blanking time is not enough) 0: Duplicate setting for next frame 1: Stop next frame
0xC452	LS_SENS_RATIO_1	0x04	RW	Bit[7:0]: L/S sensitivity ratio[15:8]
0xC453	LS_SENS_RATIO_2	0x00	RW	Bit[7:0]: L/S sensitivity ratio[7:0]
0xC454	NONWDR_EN	0x00	RW	Bit[0]: Non-WDR mode 0: Disable 1: Enable
0xC455	NONWDR_SWITCH	0x00	RW	Bit[0]: Non-WDR mode switch to combine long mode when being stabled 0: Disable 1: Enable
0xC456	FIXED_RATIO_EN	0x00	RW	Bit[0]: Fixed ratio mode 0: Disable 1: Enable
0xC457	GP_MODE_EN	0x00	RW	Bit[0]: Geometric proportion mode 0: Disable 1: Enable

table 4-7 AEC target/range control registers (sheet 5 of 9)

address	register name	default value	R/W	description
0xC458	NIGHT_MODE_EN	0x00	RW	Bit[0]: Night mode 0: Disable 1: Enable
0xC459	NIGHT_MODE_CTRL	0x00	RW	Bit[0]: Only insert frame when in night mode 0: Disable 1: Enable
0xC45A	FRACTAL_EXP_EN	0x01	RW	Bit[0]: Allow fractal exposure 0: Disable 1: Enable
0xC45B	NONLINEAR_GAIN_EN	0x01	RW	Bit[0]: Non linear gain mode 0: Disable 1: Enable
0xC45C	MANU_GAMMA_EN	0x00	RW	Bit[0]: Manual gamma mode 0: Disable 1: Enable
0xC45D	HOLD_BAND_EN	0x00	RW	Bit[0]: Hold band mode 0: Disable 1: Enable
0xC45E	BAND_FILTER_FLAG	0x00	RW	Bit[1:0]: Light source type 00: Frequency is zero or very high 01: 60Hz 10: 50Hz 11: Not valid
0xC45F	BAND_FILTER_EN	0x00	RW	Bit[0]: Banding filter 0: Disable 1: Enable
0xC460	BAND_FILTER_SHORT	0x00	RW	Bit[0]: Short banding filter 0: Disable 1: Enable
0xC461	LESS_1BAND_EN	0x01	RW	Bit[0]: Less than one band exposure mode 0: Disable 1: Enable
0xC462	LESS_1BAND_SHORT	0x01	RW	Bit[0]: Less than one band exposure for short 0: Disable 1: Enable
0xC463	WDR_GAIN_LIMIT_EN	0x01	RW	Bit[0]: WDR gain limitation enable 0: Disable 1: Enable

table 4-7 AEC target/range control registers (sheet 6 of 9)

address	register name	default value	R/W	description
0xC464	LOG_TARGET_11	0x88	RW	Bit[7:0]: Log target 1[15:8]
0xC465	LOG_TARGET_12	0x00	RW	Bit[7:0]: Log target 1[7:0]
0xC466	LOG_TARGET_21	0x8A	RW	Bit[7:0]: Log target 2[15:8]
0xC467	LOG_TARGET_22	0x00	RW	Bit[7:0]: Log target 2[7:0]
0xC468	LOG_TARGET_31	0x86	RW	Bit[7:0]: Log target 3[15:8]
0xC469	LOG_TARGET_32	0x00	RW	Bit[7:0]: Log target 3[7:0]
0xC46A	TARGET_LONG_1	0x40	RW	Target of Raw Data for Long 1
0xC46B	TARGET_LONG_2	0x50	RW	Target of Raw Data for Long 2
0xC46C	TARGET_LONG_3	0x30	RW	Target of Raw Data for Long 3
0xC46D	TARGET_SHORT_1	0x50	RW	Target of Raw Data for Short 1
0xC46E	TARGET_SHORT _2	0x60	RW	Target of Raw Data for Short 2
0xC46F	TARGET_SHORT _3	0x40	RW	Target of Raw Data for Short 3
0xC470	SLOW_RANGE_LONG	0x20	RW	Slow Range for Long Exposure
0xC471	SLOW_RANGE_SHORT	0x20	RW	Slow Range for Short Exposure
0xC472	STABLE_RANGE_IN	0x04	RW	Range Become Stable from Unstable
0xC473	STABLE_RANGE_OUT	0x08	RW	Range Become Unstable from Stable
0xC474	FAST_STEP_LONG	0x0A	RW	Fast AEC Adjustment Step for Long Exposure
0xC475	FAST_STEP_SHORT	0x0A	RW	Fast AEC Adjustment Step for Short Exposure
0xC476	SLOW_STEP_LONG	0x08	RW	Slow AEC Adjustment Step for Long Exposure
0xC477	SLOW_STEP_SHORT	0x08	RW	Slow AEC Adjustment Step for Short Exposure
0xC478	MAX_FAST_RATIO	0x40	RW	Max Fast Adjustment Ratio
0xC479	MAX_SLOW_RATIO	0x02	RW	Max Slow Adjustment Ratio
0xC47A	MAX_FRACTAL_EXP	0x0B	RW	Max Fractal Exposure (X/16)
0xC47B	MIN_FRACTAL_EXP	0x04	RW	Min Fractal Exposure (X/16)
0xC47C	MAX_SHORT_LE_1	0x34	RW	Bit[7:0]: Max short light exposure[31:24]
0xC47D	MAX_SHORT_LE_2	0x80	RW	Bit[7:0]: Max short light exposure[23:16]

table 4-7 AEC target/range control registers (sheet 7 of 9)

address	register name	default value	R/W	description
0xC47E	MAX_SHORT_LE_3	0x00	RW	Bit[7:0]: Max short light exposure[15:8]
0xC47F	MAX_SHORT_LE_4	0x00	RW	Bit[7:0]: Max short light exposure[7:0]
0xC480	MAX _GAIN_LONG_1	0x00	RW	Bit[1:0]: Max gain for long[9:8]
0xC481	MAX _GAIN_LONG_2	0x80	RW	Bit[7:0]: Max gain for long[7:0]
0xC482	MAX_GAIN_SHORT_1	0x00	RW	Bit[1:0]: Max gain for short[9:8]
0xC483	MAX_GAIN_SHORT_1	0x80	RW	Bit[7:0]: Max gain for short[7:0]
0xC484	MIN_ GAIN_LONG_1	0x00	RW	Bit[1:0]: Min gain for long[9:8]
0xC485	MIN_ GAIN_LONG_2	0x10	RW	Bit[7:0]: Min gain for long[7:0]
0xC486	MIN_GAIN_SHORT_1	0x00	RW	Bit[1:0]: Min gain for short[9:8]
0xC487	MIN_GAIN_SHORT_2	0x10	RW	Bit[7:0]: Min gain for short[7:0]
0xC488	MAX_EXP_LONG_1	0x34	RW	Bit[7:0]: Max exposure for long[15:8]
0xC489	MAX_EXP_LONG_2	0x00	RW	Bit[7:0]: Max exposure for long[7:0]
0xC48A	MAX_EXP_SHORT_1	0x34	RW	Bit[7:0]: Max exposure for short[15:8]
0xC48B	MAX_EXP_SHORT_2	0x00	RW	Bit[7:0]: Max exposure for short[7:0]
0xC48C	MIN_EXP_LONG_1	0x00	RW	Bit[7:0]: Min exposure for long[15:8]
0xC48D	MIN_EXP_LONG_2	0x04	RW	Bit[7:0]: Min exposure for long[7:0]
0xC48E	MIN_EXP_SHORT_1	0x00	RW	Bit[7:0]: Min exposure for short[15:8]
0xC48F	MIN_EXP_ SHORT_2	0x04	RW	Bit[7:0]: Min exposure for short[7:0]
0xC490	FIXED_RATIO	0x01	RW	Fixed Ratio, Value+1
0xC491	NIGHT_MODE_STEP	0x0C	RW	AEC Adjustment Step in Night Mode
0xC492	GP_MODE_RATIO_B2A	0x20	RW	B/A Ratio in Gp Mode
0xC493	GP_MODE_RATIO_C2A	0x08	RW	C/A Ratio in Gp Mode
0xC494	WDR_GAIN_STEP	0x04	RW	WDR Gain Adjustment Step
0xC495	EXP_RATIO_STEP	0x20	RW	L/S Ratio Change Step
0xC496	GAMMA_STEP	0x04	RW	Gamma Adjustment Step

table 4-7 AEC target/range control registers (sheet 8 of 9)

address	register name	default value	R/W	description
0xC497	MIN_SATU_LEVEL	0x08	RW	Min Saturate Level for Short
0xC498	MIN_GAMMA_LIST_11	0x02	RW	Bit[7:0]: Min gamma list 1[15:8]
0xC499	MIN_GAMMA_LIST_12	0x00	RW	Bit[7:0]: Min gamma list 1[7:0]
0xC49A	MIN_GAMMA_LIST_21	0x02	RW	Bit[7:0]: Min gamma list 2[15:8]
0xC49B	MIN_GAMMA_LIST_22	0x00	RW	Bit[7:0]: Min gamma list 2[7:0]
0xC49C	MIN_GAMMA_LIST_31	0x02	RW	Bit[7:0]: Min gamma list 3[15:8]
0xC49D	MIN_GAMMA_LIST_32	0x00	RW	Bit[7:0]: Min gamma list 3[7:0]
0xC49E	MAX_GAMMA_LIST_11	0x02	RW	Bit[7:0]: Max gamma list 1[15:8]
0xC49F	MAX_GAMMA_LIST_12	0x60	RW	Bit[7:0]: Max gamma list 1[7:0]
0xC4A0	MAX_GAMMA_LIST_21	0x04	RW	Bit[7:0]: Max gamma list 2[15:8]
0xC4A1	MAX_GAMMA_LIST_22	0x00	RW	Bit[7:0]: Max gamma list 2[7:0]
0xC4A2	MAX_GAMMA_LIST_31	0x05	RW	Bit[7:0]: Max gamma list 3[15:8]
0xC4A3	MAX_GAMMA_LIST_32	0x00	RW	Bit[7:0]: Max gamma list 3[7:0]
0xC4A4	DR_LIST_11	0x00	RW	Bit[7:0]: Dynamic range list 1[15:8]
0xC4A5	DR_LIST_12	0x10	RW	Bit[7:0]: Dynamic range list 1[7:0]
0xC4A6	DR_LIST_21	0x00	RW	Bit[7:0]: Dynamic range list 2[15:8]
0xC4A7	DR_LIST_22	0x80	RW	Bit[7:0]: Dynamic range list 2[7:0]
0xC4A8	DR_LIST_31	0x02	RW	Bit[7:0]: Dynamic range list 3[15:8]
0xC4A9	DR_LIST_32	0x00	RW	Bit[7:0]: Dynamic range list 3[7:0]
0xC4AA	BAND_VALUE_60HZ_1	0x0D	RW	Bit[7:0]: Band filter value for 60Hz[15:8]
0xC4AB	BAND_VALUE_60HZ_2	0x20	RW	Bit[7:0]: Band filter value for 60Hz[7:0]

table 4-7 AEC target/range control registers (sheet 9 of 9)

address	register name	default value	R/W	description
0xC4AC	BAND_VALUE_50HZ_1	0x0F	RW	Bit[7:0]: Band filter value for 50Hz[15:8]
0xC4AD	BAND_VALUE_50HZ_2	0xC0	RW	Bit[7:0]: Band filter value for 50Hz[7:0]
0xC4AE	LINEAR_EXP_START_1	0x00	RW	Bit[7:0]: Linear exposure start point[15:8]
0xC4AF	LINEAR_EXP_START_2	0x80	RW	Bit[7:0]: Linear exposure start point[7:0]
0xC4B0	PRE_CHARGE_WIDTH	0x08	RW	Pixel Timing Control
0xC4B1	MIN_DR_RATIO	0x02	RW	Min Dynamic Ratio
0xC4B2	MAX_DR_RATIO_1	0x01	RW	Bit[7:0]: Max dynamic ratio[15:8]
0xC4B3	MAX_DR_RATIO_2	0x00	RW	Bit[7:0]: Max dynamic ratio[7:0]
0xC514	SENSOR_CLK_RATIO_1	0x04	RW	Bit[7:0]: Sensor clock ratio[15:8]
0xC515	SENSOR_CLK_RATIO_2	0x00	RW	Bit[7:0]: Sensor clock ratio[7:0]
0xC516	NON_WDR_STEP	0x08	RW	Non-WDR Ratio Adjustment Step
0xC518	VTS_ADDR_1	0x03	RW	Bit[7:0]: VTS[15:8]
0xC519	VTS_ADDR_2	0x48	RW	Bit[7:0]: VTS[7:0]
0xC51A	HTS_ADDR_1	0x07	RW	Bit[7:0]: HTS[15:8]
0xC51B	HTS_ADDR_2	0x70	RW	Bit[7:0]: HTS[7:0]
0x5A00~0x5A03	AEC_R	–	R	Debug Information for AEC control

4.5 black level calibration (BLC)

4.5.1 overview

The OV10633/OV10133 calibrate the black level of active pixels using optically shielded pixels.

4.5.2 coarse BLC

The dark current changes with the temperature. At high temperature, the dark current may be out of fine BLC range. The coarse BLC cancels the majority of the dark current to make sure the remaining dark current is within the fine BLC range.

4.5.3 fine BLC

The fine BLC subtracts the output value of the optical black pixel from the active pixel.

4.5.4 trigger methods

The BLC including, coarse and fine BLC, is initiated by the following conditions:

- system reset
- gain change
- exposure change
- temperature change
- format change

The BLC can manually be triggered by setting the register trig_man (0x4003[7]) from 0 to 1.

table 4-8 BLC control functions (sheet 1 of 3)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x01	RW	Bit[0]: BLC enable 0: Disable 1: Enable
0x4001	START LINE	0x04	RW	Bit[5:0]: Start black line Start line for calculating normal offsets
0x4002	BLC CTRL02	0xC5	RW	Bit[7]: Trigger BLC when format change 0: Change of format will not trigger BLC 1: Change of format will trigger BLC Bit[6]: BLC manual mode enable 0: Use the manual offsets for BLC 1: Use the calculated offsets for BLC Bit[5:0]: rest_frame_num Number indicates how many frames BLC will be updated continuously when the BLC is reset

table 4-8 BLC control functions (sheet 2 of 3)

address	register name	default value	R/W	description
0x4003	BLC CTRL03	0x08	RW	Bit[7]: BLC manual trigger BLC will update manual_frame_num frames continuously, refer to register BLC CTRL03[5:0] when this register changes from 0 to 1 Bit[6]: BLC freeze 0: BLC running 1: BLC freeze Bit[5:0]: manual_frame_num Number of frames BLC will be updated continuously when BLC is manually triggered by register BLC CTRL03[7]
0x4004	LINE NUM	0x08	RW	Bit[5:0]: line_num Line number specifies the black lines used in offsets calculation
0x4008	LONG BLC TARGET	0x10	RW	Bit[7:0]: Target black level for long exposure channel BLC target for long exposure channel
0x4009	SHORT BLC TARGET	0x10	RW	Bit[7:0]: Target black level for short exposure channel BLC target for short exposure channel
0x4050~ 0x4051	BLC CTRL5	–	RW	BLC Control Changing these registers is not allowed

table 4-8 BLC control functions (sheet 3 of 3)

address	register name	default value	R/W	description
0x4055	BLC CTRL55	0xFF	RW	Bit[7]: Debug control Changing this value is not allowed Bit[6]: BLC temperature trigger enable for short exposure channel 0: Temperature change does not trigger BLC 1: Temperature change triggers BLC Bit[5]: BLC exposure trigger enable for short exposure channel 0: Exposure change does not trigger BLC 1: Exposure change triggers BLC Bit[4]: BLC gain trigger enable for short exposure channel 0: Gain change does not trigger BLC 1: Gain change triggers BLC Bit[3]: Debug control Changing this value is not allowed Bit[2]: BLC temperature trigger enable for long exposure channel 0: Temperature change does not trigger BLC 1: Temperature change triggers BLC Bit[1]: BLC exposure trigger enable for long exposure channel 0: Exposure change does not trigger BLC 1: Exposure change triggers BLC Bit[0]: BLC gain trigger enable for long exposure channel 0: gain change does not trigger BLC 1: gain change triggers BLC

5 image sensor processor digital functions

5.1 DSP top level control

Each individual DSP blocks can be enabled/disabled by a register however, each image format requires a specific on/off control for each block. Please refer to reference settings.

table 5-1 DSP top registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP RW00	0xFF	RW	Bit[7]: Color matrix enable Bit[6]: Color interpolation enable Bit[5]: Denoise enable Bit[4]: white defect pixel correction enable Bit[3]: Black defect pixel correction enable Bit[2]: AWB statistic enable Bit[1]: AWB gain enable Bit[0]: Lens shading correction enable
0x5001	ISP RW01	0xBF	RW	Bit[7]: Data and its weight synchronization enable Bit[6]: Black/white mode enable Bit[5]: Dark level filter enable Bit[4]: Buffer control enable Bit[3]: AEC enable Bit[2]: Tone mapping enable Bit[1]: Normalize enable Bit[0]: Long-short combination enable
0x5002	ISP RW02	0xFE	RW	Bit[3]: Digital gain enable Bit[2]: Window border cut enable Bit[1]: Dithering enable Bit[0]: Internal long/short sequence 0: LSLS 1: SLSL
0x5004	ISP RW04	0x14	RW	Bit[4]: Auto window enable 0: Manually set image window for DSP blocks 1: Automatically handle image window Bit[3:0]: Dummy line number for ISP

table 5-1 DSP top registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5005	ISP RW05	0x08	RW	Bit[7]: Vertical sub-sampling enable 0: Disable 1: Enable Bit[6]: Lens shading correction center option 0: Manually set by register 1: Automatically set based on image window Bit[5]: Output row in drop mode of sub-sampling 0: First row 1: Second row Bit[4]: Output column in drop mode of sub-sampling 0: First pair 1: Second pair Bit[3]: Average enable in non-drop mode of sub-sampling 0: Sum 1: Average Bit[2]: Green/Y channel sub-sampling mode 0: Non-drop 1: Drop Bit[1]: RB/UV channel sub-sampling mode 0: Non-drop 1: Drop Bit[0]: Sub-sampling mode enable 0: Full resolution 1: Sub-sampling

5.2 LENC

The main purpose of the LENC algorithm is compensate for non-uniform illumination due to the lens. Fall off from the radius of each pixel to the lens center this algorithm calculates again for each pixel. It then corrects each pixel with the calculated gain to compensate for the lens fall off.

figure 5-1 LENC coefficient versus sensor gain

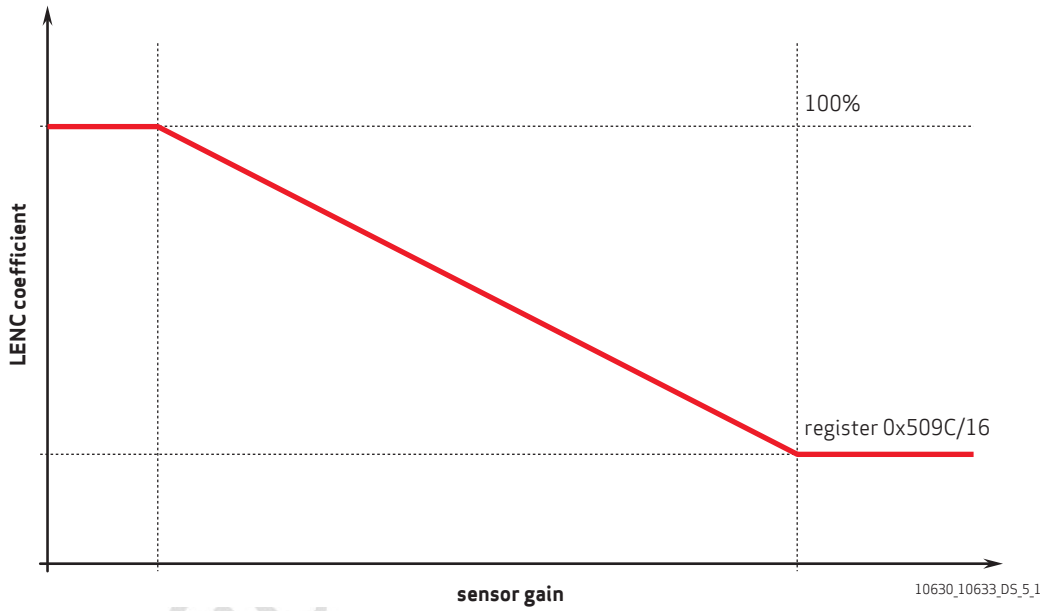


table 5-2 LENC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5080	LENC CTRL0	0x10	RW	Bit[6]: Gain manual mode enable 0: Use auto gain 1: Use manual gain set by user Bit[5]: Auto LENC switch enable 0: LENC gain adjust according to sensor gain 1: LENC gain is fixed Bit[4:0]: Manual gain input
0x5081	LENC CTRL1	0x00	RW	Bit[2:0]: long_red_x0[10:8]
0x5082	LENC CTRL2	0x00	RW	Bit[7:0]: long_red_x0[7:0]
0x5083	LENC CTRL3	0x00	RW	Bit[1:0]: long_red_y0[9:8]

table 5-2 LENC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5084	LENC CTRL4	0x00	RW	Bit[7:0]: long_red_y0[7:0]
0x5085	LENC CTRL5	0x00	RW	Bit[6:0]: long_red_a1
0x5086	LENC CTRL6	0x01	RW	Bit[3:0]: long_red_a2
0x5087	LENC CTRL7	0x00	RW	Bit[7]: long_red_sign Bit[6:0]: long_red_b1
0x5088	LENC CTRL8	0x01	RW	Bit[3:0]: long_red_b2
0x5089	LENC CTRL9	0x00	RW	Bit[2:0]: long_grn_x0[10:8]
0x508A	LENC CTRL10	0x00	RW	Bit[7:0]: long_grn_x0[7:0]
0x508B	LENC CTRL11	0x00	RW	Bit[1:0]: long_grn_y0[9:8]
0x508C	LENC CTRL12	0x00	RW	Bit[7:0]: long_grn_y0[7:0]
0x508D	LENC CTRL13	0x00	RW	Bit[6:0]: long_grn_a1
0x508E	LENC CTRL14	0x01	RW	Bit[3:0]: long_grn_a2
0x508F	LENC CTRL15	0x00	RW	Bit[7]: long_grn_sign Bit[6:0]: long_grn_b1
0x5090	LENC CTRL16	0x01	RW	Bit[3:0]: long_grn_b2
0x5091	LENC CTRL17	0x00	RW	Bit[2:0]: long_blu_x0[10:8]
0x5092	LENC CTRL18	0x00	RW	Bit[7:0]: long_blu_x0[7:0]
0x5093	LENC CTRL19	0x00	RW	Bit[1:0]: long_blu_y0[9:8]
0x5094	LENC CTRL20	0x00	RW	Bit[7:0]: long_blu_y0[7:0]
0x5095	LENC CTRL21	0x00	RW	Bit[6:0]: long_blu_a1
0x5096	LENC CTRL22	0x01	RW	Bit[3:0]: long_blu_a2
0x5097	LENC CTRL23	0x0	RW	Bit[7]: long_blu_sign Bit[6:0]: long_blu_b1
0x5098	LENC CTRL24	0x01	RW	Bit[3:0]: long_blu_b2
0x509C	LENC CTRL28	0x00	RW	Bit[4:0]: Min LENC gain
0x509D	LENC CTRL29	0x00	RW	Bit[0]: Sensor gain1[8] (must less than 0x200)
0x509E	LENC CTRL30	0x00	RW	Bit[7:0]: Sensor gain1[7:0]
0x509F	LENC CTRL31	0x00	RW	Bit[0]: Sensor gain2[8] (must less than 0x200)
0x50A0	LENC CTRL32	0x00	RW	Bit[7:0]: Sensor gain2[7:0]
0x50A1	LENC CTRL33	0x00	RW	Bit[2:0]: short_red_x0[10:8]

table 5-2 LENC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x50A2	LENC CTRL34	0x00	RW	Bit[7:0]: short_red_x0[7:0]
0x50A3	LENC CTRL35	0x00	RW	Bit[1:0]: short_red_y0[9:8]
0x50A4	LENC CTRL36	0x00	RW	Bit[7:0]: short_red_y0[7:0]
0x50A5	LENC CTRL37	0x00	RW	Bit[6:0]: short_red_a1
0x50A6	LENC CTRL38	0x01	RW	Bit[3:0]: short_red_a2
0x50A7	LENC CTRL39	0x00	RW	Bit[7]: short_red_sign Bit[6:0]: short_red_b1
0x50A8	LENC CTRL40	0x01	RW	Bit[3:0]: short_red_b2
0x50A9	LENC CTRL41	0x00	RW	Bit[2:0]: short_grn_x0[10:8]
0x50AA	LENC CTRL42	0x00	RW	Bit[7:0]: short_grn_x0[7:0]
0x50AB	LENC CTRL43	0x00	RW	Bit[1:0]: short_grn_y0[9:8]
0x50AC	LENC CTRL44	0x00	RW	Bit[7:0]: short_grn_y0[7:0]
0x50AD	LENC CTRL45	0x00	RW	Bit[6:0]: short_grn_a1
0x50AE	LENC CTRL46	0x01	RW	Bit[3:0]: short_grn_a2
0x50AF	LENC CTRL47	0x00	RW	Bit[7]: short_grn_sign Bit[6:0]: short_grn_b1
0x50B0	LENC CTRL48	0x01	RW	Bit[3:0]: short_grn_b2
0x50B1	LENC CTRL49	0x00	RW	Bit[2:0]: short_blu_x0[10:8]
0x50B2	LENC CTRL50	0x00	RW	Bit[7:0]: short_blu_x0[7:0]
0x50B3	LENC CTRL51	0x00	RW	Bit[1:0]: short_blu_y0[9:8]
0x50B4	LENC CTRL52	0x00	RW	Bit[7:0]: short_blu_y0[7:0]
0x50B5	LENC CTRL53	0x00	RW	Bit[6:0]: short_blu_a1
0x50B6	LENC CTRL54	0x01	RW	Bit[3:0]: short_blu_a2
0x50B7	LENC CTRL55	0x00	RW	Bit[7]: short_blu_sign Bit[6:0]: short_blu_b1
0x50B8	LENC CTRL56	0x01	RW	Bit[3:0]: short_blu_b2

5.3 auto white balance (AWB)

The raw R,G and B values of a white object detected by the image sensor vary with the spectrum of light source. The spectrum of light source is usually described by "color temperature", which is the surface temperature of black body radiating equivalent spectrum. The white balance process applies different gain on each color channel to make the white object rendered white in the image.

The OV10630 builds the AWB algorithm to automatically adjust the gain of each channel to achieve white balance. There are two kinds of AWB: Color Temperature (CT) based AWB and simple gray world AWB. CT AWB is based on the color temperature of the scene, which is based on G/R and G/B ratios. Simple AWB calculates the gains based on scene simple statistics of the final image.

For OV10630, AWB gets two sets of statistics separately from long and short channels. It can work in four modes: separated mode, long channel mode, short channel mode and combination mode. In separated mode, the two channels may apply different AWB gain. In other modes, they apply same AWB gain. Based on the two sets of statistics, the AWB will estimate two sets of AWB gain at first. In long or short channel mode, the two channels apply one of the two sets. In combination mode, a weighted average of the two sets of statistics is used to estimate the AWB gain. In separate mode, the two channels will apply the two sets of AWB gain respectively.

table 5-3 AWB registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP RW00	0x01	RW	Bit[2]: AWB statistics enable 0: Disable 1: Enable Bit[1]: AWB gain enable 0: Disable 1: Enable
0x5120	GAIN AWB CTRL32	0x00	RW	Bit[0]: awb_gain_manual_en 0: Reserved 1: AWB gain adjusted by user
0xC4B8	CT_AWB_EN	0x01	RW	Bit[0]: Color temperature based AWB 0: Disable 1: Enable
0x5100	GAIN AWB CTRL0	0x00	RW	Bit[1:0]: manual_gain_b_long[9:8]
0x5101	GAIN AWB CTRL1	0x80	RW	Bit[7:0]: manual_gain_b_long[7:0]
0x5102	GAIN AWB CTRL2	0x00	RW	Bit[1:0]: manual_gain_gb_long[9:8]
0x5103	GAIN AWB CTRL3	0x80	RW	Bit[7:0]: manual_gain_gb_long[7:0]
0x5104	GAIN AWB CTRL4	0x00	RW	Bit[1:0]: manual_gain_gr_long[9:8]
0x5105	GAIN AWB CTRL5	0x80	RW	Bit[7:0]: manual_gain_gr_long[7:0]
0x5106	GAIN AWB CTRL6	0x00	RW	Bit[1:0]: manual_gain_r_long[9:8]

table 5-3 AWB registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5107	GAIN AWB CTRL7	0x80	RW	Bit[7:0]: manual_gain_r_long[7:0]
0x5110	GAIN AWB CTRL16	0x00	RW	Bit[1:0]: manual_gain_b_short[9:8]
0x5111	GAIN AWB CTRL17	0x80	RW	Bit[7:0]: manual_gain_b_short[7:0]
0x5112	GAIN AWB CTRL18	0x00	RW	Bit[1:0]: manual_gain_gb_short[9:8]
0x5113	GAIN AWB CTRL19	0x80	RW	Bit[7:0]: manual_gain_gb_short[7:0]
0x5114	GAIN AWB CTRL20	0x00	RW	Bit[1:0]: manual_gain_gr_short[9:8]
0x5115	GAIN AWB CTRL21	0x80	RW	Bit[7:0]: manual_gain_gr_short[7:0]
0x5116	GAIN AWB CTRL22	0x00	RW	Bit[1:0]: manual_gain_r_short[9:8]
0x5117	GAIN AWB CTRL23	0x80	RW	Bit[7:0]: manual_gain_r_short[7:0]

5.3.1 simple AWB

Simple AWB algorithm is based on the gray world assumption, meaning the sensor will make the R, G and B average of all pixels equal to each other by adjusting the gain of each color channel.

5.3.2 CT WB

CT AWB algorithm adjusts R, G and B gain based on the color temperature of the ambient light. It will make the R, G and B channel average of gray pixels equal to each other by adjusting the gain of each color channel.

5.3.3 CT AWB calibration

To identify the gray pixels over the color temperature range, the characteristics of a gray object must be calibrated first using the target lens.

table 5-4 AWB long calibration registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5589	AWB_M_X	0x40	RW	Bit[7:0]: AWB_M_X[7:0] X characteristics of gray object in middle color temperature range. When AWB_M_X increases, gray will shift toward blue in low color temperature light, or red in high color temperature light. When AWB_M_X decreases, gray will shift toward yellow in low color temperature light, or cyan in high color temperature light. If AWB_M_X is too big or too small, the AWB algorithm may fail to identify the gray object and the result is not stable and unpredictable.
0x558A	AWB_M_Y	0x40	RW	Bit[7:0]: AWB_M_Y[7:0] Y characteristics of gray object in middle color temperature range. When AWB_M_Y increases, gray will shift toward blue in low color temperature light, or red in high color temperature light. When AWB_M_Y decreases, gray will shift toward yellow in low color temperature light, or cyan in high color temperature light. If AWB_M_Y is too big or too small, the AWB algorithm will fail to identify the gray object and the result is not stable and unpredictable

table 5-4 AWB long calibration registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5586	AWB_M_RNG	0x10	RW	Bit[7:0]: AWB_M_RNG[7:0] Tolerance of AWB_M_X and AWB_M_Y in middle color temperature range. Too small tolerance results in unstable AWB, while too great tolerance results in inaccurate AWB.
0x5587	AWB CTRL10	0x10	RW	Bit[7:0]: AWB_L_XRNG[7:0] Tolerance of AWB_L_X in low color temperature range, where AWB_L_X is the X characteristics of gray object in low color temperature range. Too small tolerance results in unstable AWB, while too great tolerance results in inaccurate AWB. The typical value ranges from 0x08~0x18.
0x5588	AWB_H_YRNG	0x10	RW	Bit[7:0]: AWB_H_YRNG[7:0] Tolerance of AWB_H_Y in low color temperature range, where AWB_H_Y is the Y characteristics of gray object in high color temperature range. Too small tolerance results in unstable AWB, while too great tolerance results in inaccurate white balance. The typical value ranges from 0x08~0x10.
0x558B	AWB_L_K	0x00	RW	Bit[7:0]: AWB_L_K K characteristics of gray object in low color temperature range When AWB_L_K increases/decreases, the gray color will slightly shift toward yellow/blue respectively in low color temperature range. In general, AWB_L_K should be no less than 0x80

table 5-4 AWB long calibration registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x558C	AWB_H_K	0x00	RW	Bit[7:0]: AWB_H_K K characteristics of gray object in high color temperature range When AWB_H_K increases/decreases, the gray color will slightly shift toward cyan/red respectively in high color temperature range.
0x558D	AWB_H_LMT	0x00	RW	Bit[7:0]: AWB_H_LMT[7:0] Lower limit of AWB_H_X, where AWB_H_X is the X characteristics of gray object in high color temperature range. Smaller AWB_H_LMT covers greater upper limit of color temperature, however also results in less accurate white balance
0x558E	AWB_L_LMT	0x00	RW	Bit[7:0]: AWB_L_LMT[7:0] Lower limit of AWB_L_Y, where AWB_L_Y is the Y characteristics of gray object in low color temperature range. Smaller AWB_L_LMT covers smaller lower limit of color temperature, however also results in less accurate white balance.
0x558F	AWB_DBG1	0x20	RW	Bit[7:0]: AWB_DBG1 Debug control register, not effective in normal usage.
0x5590	AWB_DBG2	0x20	RW	Bit[7:0]: AWB_DBG2 Debug control register, not effective in normal usage
0x5591	AWB_DATA_ULMT	0xFF	RW	Bit[7:0]: AWB_DATA_ULMT Pixels with output value greater than AWB_DATA_ULMT are excluded in the AWB statistics
0x5592	AWB_DATA_LLMT	0x00	RW	Bit[7:0]: AWB_DATA_LLMT Pixels with output value smaller than AWB_DATA_LLMT are excluded in the AWB statistics

table 5-5 AWB short calibration registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x55A2	AWB_M_X	0x40	RW	Bit[7:0]: AWB_M_X[7:0] X characteristics of gray object in middle color temperature range. When AWB_M_X increases, gray will shift toward blue in low color temperature light, or red in high color temperature light. When AWB_M_X decreases, gray will shift toward yellow in low color temperature light, or cyan in high color temperature light. If AWB_M_X is too big or too small, the AWB algorithm may fail to identify the gray object and the result is not stable and unpredictable.
0x55A3	AWB_M_Y	0x40	RW	Bit[7:0]: AWB_M_Y[7:0] Y characteristics of gray object in middle color temperature range. When AWB_M_Y increases, gray will shift toward blue in low color temperature light, or red in high color temperature light. When AWB_M_Y decreases, gray will shift toward yellow in low color temperature light, or cyan in high color temperature light. If AWB_M_Y is too big or too small, the AWB algorithm will fail to identify the gray object and the result is not stable and unpredictable
0x559F	AWB_M_RNG	0x10	RW	Bit[7:0]: AWB_M_RNG[7:0] Tolerance of AWB_M_X and AWB_M_Y in middle color temperature range. Too small tolerance results in unstable AWB, while too great tolerance results in inaccurate AWB.

table 5-5 AWB short calibration registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x55A0	AWB_L_XRNG	0x10	RW	Bit[7:0]: AWB_L_XRNG[7:0] Tolerance of AWB_L_X in low color temperature range, where AWB_L_X is the X characteristics of gray object in low color temperature range. Too small tolerance results in unstable AWB, while too great tolerance results in inaccurate AWB. The typical value ranges from 0x08~0x18.
0x55A1	AWB_H_YRNG	0x10	RW	Bit[7:0]: AWB_H_YRNG[7:0] Tolerance of AWB_H_Y in low color temperature range, where AWB_H_Y is the Y characteristics of gray object in high color temperature range. Too small tolerance results in unstable AWB, while too great tolerance results in inaccurate white balance. The typical value ranges from 0x08~0x10.
0x55A4	AWB_L_K	0x00	RW	Bit[7:0]: AWB_L_K K characteristics of gray object in low color temperature range When AWB_L_K increases/decreases, the gray color will slightly shift toward yellow/blue respectively in low color temperature range. In general, AWB_L_K should be no less than 0x80
0x55A5	AWB_H_K	0x00	RW	Bit[7:0]: AWB_H_K K characteristics of gray object in high color temperature range When AWB_H_K increases/decreases, the gray color will slightly shift toward cyan/red respectively in high color temperature range.

table 5-5 AWB short calibration registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x55A6	AWB_H_LMT	0x00	RW	Bit[7:0]: AWB_H_LMT[7:0] Lower limit of AWB_H_X, where AWB_H_X is the X characteristics of gray object in high color temperature range. Smaller AWB_H_LMT covers greater upper limit of color temperature, however also results in less accurate white balance
0x55A7	AWB_L_LMT	0x00	RW	Bit[7:0]: AWB_L_LMT[7:0] Lower limit of AWB_L_Y, where AWB_L_Y is the Y characteristics of gray object in low color temperature range. Smaller AWB_L_LMT covers smaller lower limit of color temperature, however also results in less accurate white balance.
0x55A8	AWB_DBG1	0x20	RW	Bit[7:0]: AWB_DBG1 Debug control register, not effective in normal usage
0x55A9	AWB_DBG2	0x20	RW	Bit[7:0]: AWB_DBG2 Debug control register, not effective in normal usage
0x55AA	AWB_DATA_ULMT	0xFF	RW	Bit[7:0]: AWB_DATA_ULMT pixels with output value greater than AWB_DATA_ULMT are excluded in the AWB statistics
0x55AB	AWB_DATA_LLMT	0x00	RW	Bit[7:0]: AWB_DATA_LLMT pixels with output value smaller than AWB_DATA_LLMT are excluded in the AWB statistics

5.3.4 AWB control

table 5-6 AWB control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5581	AWB CT CTRL1	0x5B	RW	Bit[7:6]: Gain adjustment step in normal zone (current gain is close to target value) Bit[5:4]: Gain adjustment step in fast zone (current gain is far away from target value) Bit[3:2]: Scale of AWB_L_K and AWB_H_K for long exposure, it is usually set to 2'b01 00: 2x 01: 4x 10: 8x 11: Not allowed Bit[1:0]: AWB debug mode Changing these registers is not recommended.
0x5582	AWB CT CTRL2	0x11	RW	Bit[7:4]: AWB update rate in normal zone Color gain will be adjust every AWB_update[7:4] + 1 frames in normal zone Bit[3:0]: AWB update rate in fast zone Color gain will be adjust every AWB_update[7:4] + 1 frames in fast zone
0x5583	AWB CT CTRL3	0x10	RW	Bit[7:6]: Scale of AWB_L_K and AWB_H_K for short exposure, it is usually set to 2'b01 00: 2x 01: 4x 10: 8x 11: Not allowed Bit[4]: Fast adjustment enable in simple AWB mode 0: Disable, AWB speed is slow 1: Enable, AWB adjustment is fast for fast scene change Bit[3:2]: AWB statistics window selection 00: Full image 01: Exclude 8 rows and columns at each image boundary 10: Exclude 1/8 of total rows and columns at each image boundary 11: Exclude 1/4 of total rows and columns at each image boundary Bit[1:0]: AWB debug control Changing these registers is not recommended

table 5-6 AWB control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5584	AWB CT CTRL4	0x25	RW	Bit[5]: Green channel gain enable 0: Only adjust red and blue channel gain 1: Adjust red, green and blue channel gain Green channel gain must be enabled to avoid false color of bright object in reddish or bluish light. Changing other register bits is not recommended

5.3.5 AWB stable range and gain range

From an unstable state, the AWB algorithm will stop to adjust the AWB gain when the difference between each channel is no more than threshold AWB_STABLE_RNG_In[3:0]. From a stable state, the AWB algorithm will start to adjust gain once the difference between each channel is greater than threshold AWB_STABLE_RNG_OUT[3:0].

The R, G and B gain can be further limited by register MAX_AWB_GAIN.

table 5-7 AWB range registers

address	register name	default value	R/W	description
0x5585	AWB_STABLE_RNG	0x24	RW	Bit[7:4]: AWB_stable_rng_in[3:0] AWB will adjust the gain of each color channel until the difference between each channel is no more than AWB_stable_rng_in[3:0] Bit[3:0]: AWB_stable_rng_out[3:0] AWB will start to adjust the gain once the difference between each channel is greater than AWB_stable_rng_out[3:0]
0xC2E6	MAX_AWB_GAIN1	0x01	RW	Bit[7:0]: Maximum gain MSB of R/G/B channel
0xC2E7	MAX_AWB_GAIN2	0x7F	RW	Bit[7:0]: Maximum gain LSB of R/G/B channel

5.4 de-noise (DNS)

The DNS block uses a low pass filter to remove white noise in each color channel and white noise between Gb and Gr. Control parameters are separate for long and short exposures. Difference below threshold is treated as noise and will be smoothed. Difference than threshold is treated as edge and will be preserved. The low pass filter is adaptive to the gain value.

figure 5-2 RAW domain DNS - long

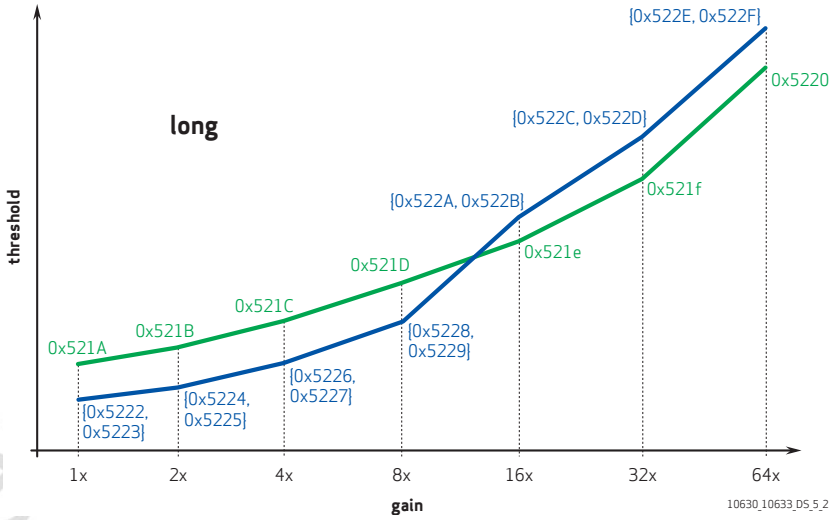


figure 5-3 RAW domain DNS - short

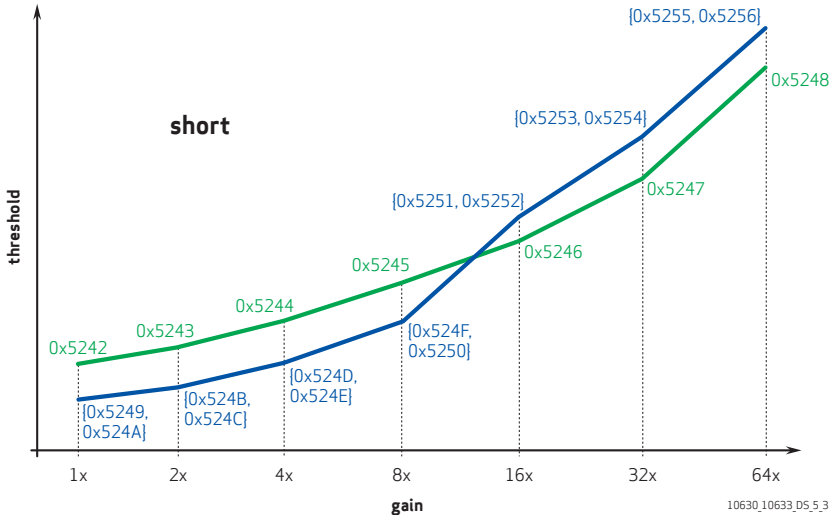


table 5-8 DNS control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP RW00	0xFF	RW	Bit[5]: dns_en
0x5210	DNS CTRL10	0x04	RW	Bit[3:0]: noise_y_a for long exposure sub-pixel
0x5211	DNS CTRL11	0x08	RW	Bit[4:0]: noise_uv_a for long exposure sub-pixel
0x5212	DNS CTRL12	0x00	RW	Bit[0]: dns_manual for long exposure sub-pixel
0x5213	DNS CTRL13	0x02	RW	noise_y for Long Exposure Sub-pixel
0x5214	DNS CTRL14	0x00	RW	Bit[0]: noise_u[8] for long exposure sub-pixel
0x5215	DNS CTRL15	0x02	RW	Bit[7:0]: noise_u[7:0] for long exposure sub-pixel
0x5216	DNS CTRL16	0x00	RW	Bit[0]: noise_v[8] for long exposure sub-pixel
0x5217	DNS CTRL17	0x02	RW	Bit[7:0]: noise_v[7:0] for long exposure sub-pixel
0x5218	DNS CTRL18	0x06	RW	dns_edgethre for Long Exposure Sub-pixel
0x5219	DNS CTRL19	0x04	RW	Bit[3:0]: dns_gbgr_extra[3:0] for long exposure sub-pixel
0x521A	DNS CTRL20	0x02	RW	noise_y_list_0 for Long Exposure Sub-pixel
0x521B	DNS CTRL21	0x04	RW	noise_y_list_1 for Long Exposure Sub-pixel
0x521C	DNS CTRL22	0x08	RW	noise_y_list_2 for Long Exposure Sub-pixel
0x521D	DNS CTRL23	0x14	RW	noise_y_list_3 for Long Exposure Sub-pixel
0x521E	DNS CTRL24	0x1E	RW	noise_y_list_4 for Long Exposure Sub-pixel
0x521F	DNS CTRL25	0x28	RW	noise_y_list_5 for Long Exposure Sub-pixel
0x5220	DNS CTRL26	0x32	RW	noise_y_list_6_l for Long Exposure Sub-pixel
0x5221	DNS CTRL27	0x00	RW	Bit[0]: dns_dummy[0] for long exposure sub-pixel

table 5-8 DNS control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5222	DNS CTRL28	0x00	RW	Bit[0]: noise_uv_list_0[8] for long exposure sub-pixel
0x5223	DNS CTRL29	0x02	RW	Bit[7:0]: noise_uv_list_0[7:0] for long exposure sub-pixel
0x5224	DNS CTRL30	0x00	RW	Bit[0]: noise_uv_list_1[8] for long exposure sub-pixel
0x5225	DNS CTRL31	0x04	RW	Bit[7:0]: noise_uv_list_1[7:0] for long exposure sub-pixel
0x5226	DNS CTRL32	0x00	RW	Bit[0]: noise_uv_list_2[8] for long exposure sub-pixel
0x5227	DNS CTRL33	0x0C	RW	Bit[7:0]: noise_uv_list_2[7:0] for long exposure sub-pixel
0x5228	DNS CTRL34	0x00	RW	Bit[0]: noise_uv_list_3[8] for long exposure sub-pixel
0x5229	DNS CTRL35	0x28	RW	Bit[7:0]: noise_uv_list_3[7:0] for long exposure sub-pixel
0x522A	DNS CTRL36	0x00	RW	Bit[0]: noise_uv_list_4[8] for long exposure sub-pixel
0x522B	DNS CTRL37	0x32	RW	Bit[7:0]: noise_uv_list_4[7:0] for long exposure sub-pixel
0x522C	DNS CTRL38	0x00	RW	Bit[0]: noise_uv_list_5[8] for long exposure sub-pixel
0x522D	DNS CTRL39	0x3C	RW	Bit[7:0]: noise_uv_list_5[7:0] for long exposure sub-pixel
0x522E	DNS CTRL40	0x00	RW	Bit[0]: noise_uv_list_6[8] for long exposure sub-pixel
0x522F	DNS CTRL41	0x4C	RW	Bit[7:0]: noise_uv_list_6[7:0] for long exposure sub-pixel
0x5238	DNS CTRL50	0x04	RW	Bit[3:0]: noise_y_a for short exposure sub-pixel
0x5239	DNS CTRL51	0x08	RW	Bit[4:0]: noise_uv_a for short exposure sub-pixel
0x523A	DNS CTRL52	0x00	RW	Bit[0]: dns_manual for short exposure sub-pixel
0x523B	DNS CTRL53	0x02	RW	noise_y for Short Exposure Sub-pixel
0x523C	DNS CTRL54	0x00	RW	Bit[0]: noise_u[8] for short exposure sub-pixel

table 5-8 DNS control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x523D	DNS CTRL55	0x02	RW	Bit[7:0]: noise_u[7:0] for short exposure sub-pixel
0x523E	DNS CTRL56	0x00	RW	Bit[0]: noise_v[8] for short exposure sub-pixel
0x523F	DNS CTRL57	0x02	RW	Bit[7:0]: noise_v[7:0] for short exposure sub-pixel
0x5240	DNS CTRL58	0x06	RW	dns_edgethre for Short Exposure Sub-pixel
0x5241	DNS CTRL59	0x04	RW	Bit[3:0]: dns_gbgr_extra[3:0] for short exposure sub-pixel
0x5242	DNS CTRL60	0x02	RW	noise_y_list_0 for Short Exposure Sub-pixel
0x5243	DNS CTRL61	0x04	RW	noise_y_list_1 for Short Exposure Sub-pixel
0x5244	DNS CTRL62	0x08	RW	noise_y_list_2 for Short Exposure Sub-pixel
0x5245	DNS CTRL63	0x14	RW	noise_y_list_3 for Short Exposure Sub-pixel
0x5246	DNS CTRL64	0x1E	RW	noise_y_list_4 for Short Exposure Sub-pixel
0x5247	DNS CTRL65	0x28	RW	noise_y_list_5 for Short Exposure Sub-pixel
0x5248	DNS CTRL66	0x32	RW	noise_y_list_6 for Short Exposure Sub-pixel
0x5249	DNS CTRL67	0x00	RW	Bit[0]: noise_uv_list_0[8] for short exposure sub-pixel
0x524A	DNS CTRL68	0x02	RW	Bit[7:0]: noise_uv_list_0[7:0] for short exposure sub-pixel
0x524B	DNS CTRL69	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_1[8] for short exposure sub-pixel
0x524C	DNS CTRL70	0x04	RW	Bit[7:0]: noise_uv_list_1[7:0] for short exposure sub-pixel
0x524D	DNS CTRL71	0x00	RW	Bit[0]: noise_uv_list_2[8] for short exposure sub-pixel
0x524E	DNS CTRL72	0x0C	RW	Bit[7:0]: noise_uv_list_2[7:0] for short exposure sub-pixel

table 5-8 DNS control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x524F	DNS CTRL73	0x00	RW	Bit[0]: noise_uv_list_3[8] for short exposure sub-pixel
0x5250	DNS CTRL74	0x28	RW	Bit[7:0]: noise_uv_list_3[7:0] for short exposure sub-pixel
0x5251	DNS CTRL75	0x00	RW	Bit[0]: noise_uv_list_4[8] for short exposure sub-pixel
0x5252	DNS CTRL76	0x32	RW	Bit[7:0]: noise_uv_list_4[7:0] for short exposure sub-pixel
0x5253	DNS CTRL77	0x00	RW	Bit[0]: noise_uv_list_5[8] for short exposure sub-pixel
0x5254	DNS CTRL78	0x3C	RW	Bit[7:0]: noise_uv_list_5[7:0] for short exposure sub-pixel
0x5255	DNS CTRLI79	0x00	RW	Bit[0]: noise_uv_list_6[8] for short exposure sub-pixel
0x5256	DNS CTRLI80	0x4C	RW	Bit[7:0]: noise_uv_list_6[7:0] for short exposure sub-pixel

5.5 color interpolation (CIP)

CIP block interpolates raw R,G,B pixels to RGB space. It also contains the sharpen function.

table 5-9 CIP control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5000	ISP RW00	1'b1	RW	Bit[6]: cip_en
0x5280	CIP CTRL00	0x00	RW	Bit[1:0]: min_gain[9:8] for long exposure Min_gain is used in CIP_start module and is used to judge in which range the current sensor is in
0x5281	CIP CTRL01	0x10	RW	Bit[7:0]: min_gain[7:0] for long exposure Min_gain is used in CIP_start module and is used to judge in which range the current sensor is in
0x5282	CIP CTRL02	0x00	RW	Bit[1:0]: max_gain[9:8] for long exposure Max_gain is used in CIP_start module and is used to judge in which range the current sensor is in

table 5-9 CIP control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x5283	CIP CTRL03	0x80	RW	Bit[7:0]: max_gain[7:0] for long exposure Max_gain is used in CIP_start module and is used to judge in which range the current sensor is in
0x5284	CIP CTRL04	0x00	RW	Bit[0]: min_noise[8] for long exposure min_noise is used for calculating int_noise in auto mode
0x5285	CIP CTRL05	0x10	RW	Bit[7:0]: min_noise[7:0] for long exposure min_noise is used for calculating int_noise in auto mode
0x5286	CIP CTRL06	0x01	RW	Bit[1:0]: noise_slope[9:8] for long exposure Slope value used for calculating int_noise in auto mode
0x5287	CIP CTRL07	0x00	RW	Bit[7:0]: noise_slope[7:0] for long exposure Slope value used for calculating int_noise in auto mode
0x5288	CIP CTRL08	0x10	RW	Bit[7:0]: unsharpen_mask0 for long exposure UnSharpenMask0 used in some filters as multipliers
0x5289	CIP CTRL09	0x30	RW	Bit[7:0]: unsharpen_mask1 for long exposure UnSharpenMask0 used in some filters as multipliers
0x528A	CIP CTRL0A	0x10	RW	Bit[1]: man_en for long exposure Enable manual mode Bit[0]: anti_aliasing for long exposure Enable anti-aliasing
0x528B	CIP CTRL0B	0x02	RW	Bit[3:0]: combine_alpha[3:0] for long exposure Combine coefficients for U, V and H components
0x528C	CIP CTRL0C	0x00	RW	Bit[4:0]: min_sharpen[4:0] for long exposure Min_sharpen is used for sharpen_p calculation in auto mode
0x528D	CIP CTRL0D	0x10	RW	Bit[5:0]: max_sharpen[5:0] for long exposure Max_sharpen is used for sharpen_p calculation in auto mode
0x528E	CIP CTRL0E	0x10	RW	Bit[5:0]: min_sharpen_tp[5:0] for long exposure Min_sharpen_tp is used for sharpen_tp computation in auto mode
0x528F	CIP CTRL0F	0x60	RW	Bit[7:0]: max_sharpen_tp[7:0] for long exposure Max_sharpen_tp is used for sharpen_tp computation in auto mode

table 5-9 CIP control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x5290	CIP CTRL10	0x20	RW	Bit[5:0]: min_sharpen_tm[5:0] for long exposure Min_sharpen_tm is used for sharpen_tm computation in auto mode
0x5291	CIP CTRL11	0x60	RW	Bit[7:0]: max_sharpen_tm[7:0] for long exposure Max_sharpen_tm is used for sharpen_tm computation in auto mode
0x5292	CIP CTRL12	0x40	RW	Bit[7:0]: sharpen_tya[7:0] for long exposure Threshold used for the function of adaptive sharpen
0x5293	CIP CTRL13	0x10	RW	Bit[4:0]: sharpen_alpha[4:0] for long exposure Sharpen_alpha is used for calculating sharpen_m after sharpen_p is obtained
0x5294	CIP CTRL14	0x06	RW	Bit[5:0]: mthre[5:0] for long exposure Threshold for medium frequency signals
0x5295	CIP CTRL15	0x08	RW	Bit[5:0]: hthre[5:0] for long exposure Threshold for high frequency signals
0x5297	CIP CTRL17	0x06	RW	Bit[3:0]: hfreq_coef[3:0] for long exposure Coefficients for high frequency signals
0x5298	CIP CTRL18	0x00	RW	Bit[1:0]: efreq_coef[1:0] for long exposure Coefficients for E frequency signals
0x5299	CIP CTRL19	0x08	RW	Bit[5:0]: lthre[5:0] for long exposure Threshold for low frequency signals
0x529A	CIP CTRL1A	0x00	RW	Bit[1:0]: man_int_noise[9:8] for long exposure int_noise is input only in manual mode and is used as threshold in some filters
0x529B	CIP CTRL1B	0x30	RW	Bit[7:0]: man_int_noise[7:0] for long exposure int_noise is input only in manual mode and is used as threshold in some filters
0x529C	CIP CTRL1C	0x00	RW	Bit[0]: man_inv_noise[8] for long exposure inv_noise is input only in manual mode and is used as threshold in some filters
0x529D	CIP CTRL1D	0x55	RW	Bit[7:0]: man_inv_noise[7:0] for long exposure inv_noise is input only in manual mode and is used as threshold in some filters
0x529E	CIP CTRL1E	0x08	RW	Bit[5:0]: man_sharpen_p[5:0] for long exposure sharpen_p is input only in manual mode and is used for the function of adaptive sharpen

table 5-9 CIP control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x529F	CIP CTRL1F	0x08	RW	Bit[6:0]: man_sharpen_m[6:0] for long exposure sharpen_m is input only in manual mode and is used for the function of adaptive sharpen
0x52A0	CIP CTRL20	0x06	RW	Bit[7:0]: man_sharpen_tp[7:0] for long exposure sharpen_tp is input only in manual mode and is used for the function of adaptive sharpen
0x52A1	CIP CTRL21	0x08	RW	Bit[7:0]: man_sharpen_tm[7:0] for long exposure sharpen_tm is input only in manual mode and is used for the function of adaptive sharpen
0x52C0	CIP CTRL40	0x00	RW	Bit[1:0]: min_gain[9:8] for short exposure Min_gain is used in CIP_start module and is used to judge in which range the current sensor is in
0x52C1	CIP CTRL41	0x10	RW	Bit[7:0]: min_gain[7:0] for short exposure Min_gain is used in CIP_start module and is used to judge in which range the current sensor is in
0x52C2	CIP CTRL42	0x00	RW	Bit[1:0]: max_gain[9:8] for short exposure Max_gain is used in CIP_start module and is used to judge in which range the current sensor is in
0x52C3	CIP CTRL43	0x80	RW	Bit[7:0]: max_gain[7:0] for short exposure Max_gain is used in CIP_start module and is used to judge in which range the current sensor is in
0x52C4	CIP CTRL44	0x00	RW	Bit[0]: min_noise[8] for short exposure min_noise used for calculating int_noise in auto mode
0x52C5	CIP CTRL45	0x10	RW	Bit[7:0]: min_noise[7:0] for short exposure min_noise used for calculating int_noise in auto mode
0x52C6	CIP CTRL46	0x01	RW	Bit[1:0]: noise_slope[9:8] for short exposure Slope value used for calculating int_noise in auto mode
0x52C7	CIP CTRL47	0x00	RW	Bit[7:0]: noise_slope[7:0] for short exposure Slope value used for calculating int_noise in auto mode

table 5-9 CIP control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x52C8	CIP CTRL48	0x10	RW	Bit[7:0]: unsharpen_mask0 for short exposure UnSharpenMask0 used in some filters as multipliers
0x52C9	CIP CTRL49	0x30	RW	Bit[7:0]: unsharpen_mask1 for short exposure UnSharpenMask0 used in some filters as multipliers
0x52CA	CIP CTRL4A	0x01	RW	Bit[1]: man_en for short exposure Enable manual mode Bit[0]: anti_aliasing for short exposure Enable anti-aliasing
0x52CB	CIP CTRL4B	0x02	RW	Bit[3:0]: combine_alpha[3:0] for short exposure Combine coefficients for U, V and H components
0x52CC	CIP CTRL4C	0x00	RW	Bit[4:0]: min_sharpen[4:0] for short exposure Min_sharpen is used for sharpen_p calculation in auto mode
0x52CD	CIP CTRL4D	0x00	RW	Bit[5:0]: max_sharpen[5:0] for short exposure Max_sharpen is used for sharpen_p calculation in auto mode
0x52CE	CIP CTRL4E	0x10	RW	Bit[5:0]: min_sharpen_tp[5:0] for short exposure Min_sharpen_tp is used for sharpen_tp computation in auto mode
0x52CF	CIP CTRL4F	0x60	RW	Bit[7:0]: max_sharpen_tp[7:0] for short exposure Max_sharpen_tp is used for sharpen_tp computation in auto mode
0x52D0	CIP CTRL50	0x20	RW	Bit[5:0]: min_sharpen_tm[5:0] for short exposure Min_sharpen_tm is used for sharpen_tm computation in auto mode
0x52D1	CIP CTRL51	0x60	RW	Bit[7:0]: max_sharpen_tm[7:0] for short exposure Max_sharpen_tm is used for sharpen_tm computation in auto mode
0x52D2	CIP CTRL52	0x40	RW	Bit[7:0]: sharpen_tya[7:0] for short exposure Threshold used for the function of adaptive sharpen
0x52D3	CIP CTRL53	0x10	RW	Bit[4:0]: sharpen_alpha[4:0] for short exposure Sharpen_alpha is used for calculating sharpen_m after sharpen_p is obtained
0x52D4	CIP CTRL54	0x06	RW	Bit[5:0]: mthre[5:0] for short exposure Threshold for medium frequency signals

table 5-9 CIP control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x52D5	CIP CTRL55	0x08	RW	Bit[5:0]: hthre[5:0] for short exposure Threshold for high frequency signals
0x52D7	CIP CTRL57	0x06	RW	Bit[3:0]: hfreq_coef[3:0] for short exposure Coefficients for high frequency signals
0x52D8	CIP CTRL58	0x00	RW	Bit[1:0]: efreq_coef[1:0] for short exposure Coefficients for E frequency signals
0x52D9	CIP CTRL59	0x08	RW	Bit[5:0]: lthre[5:0] for short exposure Threshold for low frequency signals
0x52DA	CIP CTRL5A	0x00	RW	Bit[1:0]: man_int_noise[9:8] for short exposure int_noise is input only in manual mode and is used as threshold in some filters
0x52DB	CIP CTRL5B	0x30	RW	Bit[7:0]: man_int_noise[7:0] for short exposure int_noise is input only in manual mode and is used as threshold in some filters
0x52DC	CIP CTRL5C	0x00	RW	Bit[0]: man_inv_noise[8] for short exposure inv_noise is input only in manual mode and is used as threshold in some filters
0x52DD	CIP CTRL5D	0x55	RW	Bit[7:0]: man_inv_noise[7:0] for short exposure inv_noise is input only in manual mode and is used as threshold in some filters
0x52DE	CIP CTRL5E	0x08	RW	Bit[5:0]: man_sharpen_p[5:0] for short exposure sharpen_p is input only in manual mode and is used for the function of adaptive sharpen
0x52DF	CIP CTRL5F	0x08	RW	Bit[6:0]: man_sharpen_m[6:0] for short exposure sharpen_m is input only in manual mode and is used for the function of adaptive sharpen
0x52E0	CIP CTRL60	0x06	RW	Bit[7:0]: man_sharpen_tp[7:0] for short exposure sharpen_tp is input only in manual mode and is used for the function of adaptive sharpen
0x52E1	CIP CTRL61	0x08	RW	Bit[7:0]: man_sharpen_tm[7:0] for short exposure sharpen_tm is input only in manual mode and is used for the function of adaptive sharpen

5.6 color matrix (CMX)

The main purpose of Color Matrix (CMX) is color correction.

$$\begin{bmatrix} \{0xC318, 0xC319\} & \{0xC31A, 0xC31B\} & \{0xC31C, 0xC31D\} \\ \{0xC31E, 0xC31F\} & \{0xC320, 0xC321\} & \{0xC322, 0xC323\} \\ \{0xC324, 0xC325\} & \{0xC326, 0xC327\} & \{0xC328, 0xC329\} \\ \{0xC32A, 0xC32B\} & \{0xC32C,0xC32D\} & \{0xC32E, 0xC32F\} \end{bmatrix} = 256 \times \begin{bmatrix} 0.114 & 0.587 & 0.299 \\ 0.5 & -0.331 & -0.169 \\ -0.056 & 0.278 & -0.222 \\ -0.081 & -0.419 & 0.5 \end{bmatrix} \times [CCM]\ long$$

$$\begin{bmatrix} \{0xC330, 0xC331\} & \{0xC332, 0xC333\} & \{0xC334, 0xC335\} \\ \{0xC336, 0xC337\} & \{0xC338, 0xC339\} & \{0xC33A, 0xC33B\} \\ \{0xC33C, 0xC33D\} & \{0xC33E, 0xC33F\} & \{0xC340, 0xC341\} \\ \{0xC342, 0xC343\} & \{0xC344, 0xC345\} & \{0xC346, 0xC347\} \end{bmatrix} = 256 \times \begin{bmatrix} 0.114 & 0.587 & 0.299 \\ 0.5 & -0.331 & -0.169 \\ -0.056 & -0.278 & -0.222 \\ -0.081 & -0.419 & 0.5 \end{bmatrix} \times [CCM]\ short$$

table 5-10 CMX control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	1'b1	RW	Bit[7]: cmx_en 0: Disable CMX 1: Enable CMX
0xC318	COLOR_MATRIX_L_1_1	0x00	RW	Long Color Matrix 1[15:8]
0xC319	COLOR_MATRIX_L_1_2	0x3C	RW	Long Color Matrix 1[7:0]
0xC31A	COLOR_MATRIX_L_2_1	0x00	RW	Long Color Matrix 2[15:8]
0xC31B	COLOR_MATRIX_L_2_2	0xA9	RW	Long Color Matrix 2[7:0]
0xC31C	COLOR_MATRIX_L_3_1	0x00	RW	Long Color Matrix 3[15:8]
0xC31D	COLOR_MATRIX_L_3_2	0x1B	RW	Long Color Matrix 3[7:0]
0xC31E	COLOR_MATRIX_L_4_1	0x00	RW	Long Color Matrix 4[15:8]
0xC31F	COLOR_MATRIX_L_4_2	0xD6	RW	Long Color Matrix 4[7:0]
0xC320	COLOR_MATRIX_L_5_1	0xFF	RW	Long Color Matrix 5[15:8]
0xC321	COLOR_MATRIX_L_5_2	0x3C	RW	Long Color Matrix 5[7:0]
0xC322	COLOR_MATRIX_L_6_1	0xFF	RW	Long Color Matrix 6[15:8]
0xC323	COLOR_MATRIX_L_6_2	0xEE	RW	Long Color Matrix 6[7:0]
0xC324	COLOR_MATRIX_L_7_1	0xFF	RW	Long Color Matrix 7[15:8]
0xC325	COLOR_MATRIX_L_7_2	0xE9	RW	Long Color Matrix 7[7:0]
0xC326	COLOR_MATRIX_L_8_1	0x00	RW	Long Color Matrix 8[15:8]
0xC327	COLOR_MATRIX_L_8_2	0x4C	RW	Long Color Matrix 8[7:0]

table 5-10 CMX control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0xC328	COLOR_MATRIX_L_9_1	0xFF	RW	Long Color Matrix 9[15:8]
0xC329	COLOR_MATRIX_L_9_2	0xCB	RW	Long Color Matrix 9[7:0]
0xC32A	COLOR_MATRIX_L_10_1	0xFF	RW	Long Color Matrix 10[15:8]
0xC32B	COLOR_MATRIX_L_10_2	0xDD	RW	Long Color Matrix 10[7:0]
0xC32C	COLOR_MATRIX_L_11_1	0xFF	RW	Long Color Matrix 11[15:8]
0xC32D	COLOR_MATRIX_L_11_2	0xB5	RW	Long Color Matrix 11[7:0]
0xC32E	COLOR_MATRIX_L_12_1	0x00	RW	Long Color Matrix 12[15:8]
0xC32F	COLOR_MATRIX_L_12_2	0x6E	RW	Long Color Matrix 12[7:0]
0xC330	COLOR_MATRIX_S_1_1	0x00	RW	Short Color Matrix 1[15:8]
0xC331	COLOR_MATRIX_S_1_2	0x29	RW	Short Color Matrix 1[7:0]
0xC332	COLOR_MATRIX_S_2_1	0x00	RW	Short Color Matrix 2[15:8]
0xC333	COLOR_MATRIX_S_2_2	0xB1	RW	Short Color Matrix 2[7:0]
0xC334	COLOR_MATRIX_S_3_1	0x00	RW	Short Color Matrix 3[15:8]
0xC335	COLOR_MATRIX_S_3_2	0x26	RW	Short Color Matrix 3[7:0]
0xC336	COLOR_MATRIX_S_4_1	0x00	RW	Short Color Matrix 4[15:8]
0xC337	COLOR_MATRIX_S_4_2	0xC2	RW	Short Color Matrix 4[7:0]
0xC338	COLOR_MATRIX_S_5_1	0xFF	RW	Short Color Matrix 5[15:8]
0xC339	COLOR_MATRIX_S_5_2	0x54	RW	Short Color Matrix 5[7:0]
0xC33A	COLOR_MATRIX_S_6_1	0xFF	RW	Short Color Matrix 6[15:8]
0xC33B	COLOR_MATRIX_S_6_2	0xEA	RW	Short Color Matrix 6[7:0]
0xC33C	COLOR_MATRIX_S_7_1	0xFF	RW	Short Color Matrix 7[15:8]
0xC33D	COLOR_MATRIX_S_7_2	0xE8	RW	Short Color Matrix 7[7:0]
0xC33E	COLOR_MATRIX_S_8_1	0x00	RW	Short Color Matrix 8[15:8]
0xC33F	COLOR_MATRIX_S_8_2	0x4E	RW	Short Color Matrix 8[7:0]
0xC340	COLOR_MATRIX_S_9_1	0xFF	RW	Short Color Matrix 9[15:8]
0xC341	COLOR_MATRIX_S_9_2	0xCA	RW	Short Color Matrix 9[7:0]
0xC342	COLOR_MATRIX_S_10_1	0xFF	RW	Short Color Matrix 10[15:8]
0xC343	COLOR_MATRIX_S_10_2	0xE5	RW	Short Color Matrix 10[7:0]

table 5-10 CMX control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0xC344	COLOR_MATRIX_S_11_1	0xFF	RW	Short Color Matrix 11[15:8]
0xC345	COLOR_MATRIX_S_11_2	0xA8	RW	Short Color Matrix 11[7:0]
0xC346	COLOR_MATRIX_S_12_1	0x00	RW	Short Color Matrix 12[15:8]
0xC347	COLOR_MATRIX_S_12_2	0x73	RW	Short Color Matrix 12[7:0]

5.7 auto color saturation

The auto color saturation block can adjust the color saturation level based on the sensor gain. Thus in low light, with high gain the color saturation can be reduced to effectively receive scene spatial noise. In bright conditions, with lower gain, color saturation can be at an increased level.

figure 5-4 auto color saturation graph

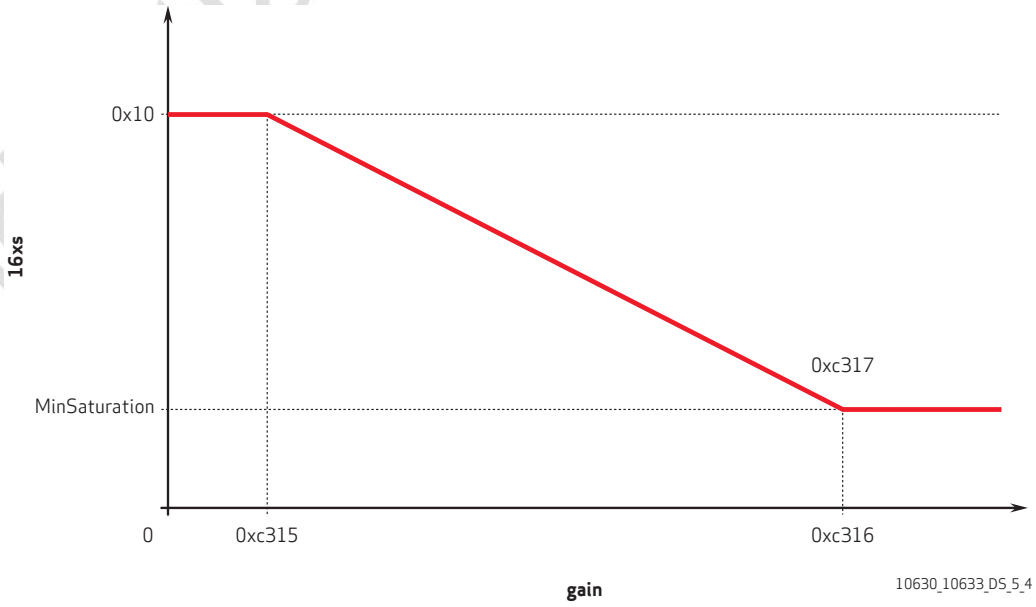


table 5-11 auto color saturation control registers

address	register name	default value	R/W	description
0xC314	SATURATION_ADJ_EN	0x01	RW	Auto adjust color saturation in low light condition: 0: Disabled 1: Enabled
0xC315	SATURATION_MINGAIN	0x7F	RW	Min Gain To Adjust Color Saturation
0xC316	SATURATION_MAXGAIN	0xFF	RW	Max Gain To Adjust Color Saturation
0xC317	SATURATION_MINTHRE	0x0B	RW	Min Threshold When Adjusting Color Saturation

5.8 combine

The main purposes of the combine block is to combine the long exposure and short exposure channel into one channel.

table 5-12 combine control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5001	ISP RW01	1'b1	RW	Bit[0]: Combine enable 0: Disable 1: Enable
0x5400	COMB CTRL0	0x0F	RW	Bit[3]: Dark boost enable 0: Dark boost disable 1: Dark boost enable Bit[2]: combine_uv_weight enable 0: Combine without UV weight 1: Combine with UV weight Bit[1]: color_diff_compensate enable 0: Compensate disable 1: Compensate enable Bit[0]: Compensate error enable 0: Compensate error disable 1: Compensate error enable
0x5401	COMB CTRL1	0x05	RW	Bit[3:0]: comb_thre_s0 Threshold1 of short channel
0x5402	COMB CTRL2	0x08	RW	Bit[3:0]: comb_thre_s1 Threshold2 of short channel
0x5403	COMB CTRL3	0x0A	RW	Bit[3:0]: comb_thre_s2 Threshold3 of short channel

table 5-12 combine control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5404	COMB CTRL4	0x09	RW	Bit[3:0]: comb_thre_l0 Threshold1 of long channel
0x5405	COMB CTRL5	0x0A	RW	Bit[3:0]: comb_thre_l1 Threshold2 of long channel
0x5406	COMB CTRL6	0x0A	RW	Bit[3:0]: comb_thre_l2 Threshold3 of long channel
0x5407	COMB CTRL7	0x05	RW	Bit[3:0]: comb_uv_thre_s0 UV threshold1 of short channel
0x5408	COMB CTRL8	0x08	RW	Bit[3:0]: comb_uv_thre_s1 UV threshold2 of short channel
0x5409	COMB CTRL9	0x0A	RW	Bit[3:0]: comb_uv_thre_s2 UV threshold3 of short channel
0x540A	COMB CTRL10	0x09	RW	Bit[3:0]: comb_uv_thre_l0 UV threshold1 of long channel
0x540B	COMB CTRL11	0x0A	RW	Bit[3:0]: comb_uv_thre_l1 UV threshold2 of long channel
0x540C	COMB CTRL12	0x0A	RW	Bit[3:0]: comb_uv_thre_l2 UV threshold3 of long channel
0x540D	COMB CTRL13	0x80	RW	comb_weight00
0x540E	COMB CTRL14	0x80	RW	comb_weight01
0x540F	COMB CTRL15	0x60	RW	comb_weight02
0x5410	COMB CTRL16	0x40	RW	comb_weight03
0x5411	COMB CTRL17	0x80	RW	comb_weight10
0x5412	COMB CTRL18	0x80	RW	comb_weight11
0x5413	COMB CTRL19	0x20	RW	comb_weight12
0x5414	COMB CTRL20	0x10	RW	comb_weight13
0x5415	COMB CTRL21	0x80	RW	comb_weight20
0x5416	COMB CTRL22	0x80	RW	comb_weight21
0x5417	COMB CTRL23	0x00	RW	comb_weight22
0x5418	COMB CTRL24	0x00	RW	comb_weight23
0x5419	COMB CTRL25	0x80	RW	comb_weight30
0x541A	COMB CTRL26	0x80	RW	comb_weight31
0x541B	COMB CTRL27	0x00	RW	comb_weight32

table 5-12 combine control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x541C	COMB CTRL28	0x00	RW	comb_weight33
0x541D	COMB CTRL29	0x80	RW	comb_uv_weight00
0x541E	COMB CTRL30	0x80	RW	comb_uv_weight01
0x541F	COMB CTRL31	0x80	RW	comb_uv_weight02
0x5420	COMB CTRL32	0x80	RW	comb_uv_weight03
0x5421	COMB CTRL33	0x80	RW	comb_uv_weight10
0x5422	COMB CTRL34	0x80	RW	comb_uv_weight11
0x5423	COMB CTRL35	0x60	RW	comb_uv_weight12
0x5424	COMB CTRL36	0x40	RW	comb_uv_weight13
0x5425	COMB CTRL37	0x80	RW	comb_uv_weight20
0x5426	COMB CTRL38	0x80	RW	comb_uv_weight21
0x5427	COMB CTRL39	0x00	RW	comb_uv_weight22
0x5428	COMB CTRL40	0x00	RW	comb_uv_weight23
0x5429	COMB CTRL41	0x80	RW	comb_uv_weight30
0x542A	COMB CTRL42	0x80	RW	comb_uv_weight31
0x542B	COMB CTRL43	0x00	RW	comb_uv_weight32
0x542C	COMB CTRL44	0x00	RW	comb_uv_weight33
0x542D	COMB CTRL45	0x3C	RW	Debug Mode for Combine Bit[5:2]: Fixed value for RO register Bit[1]: Debug mode 2 (EOF to VSYNC fixed value, other zero) Bit[0]: Debug mode 1 (always fixed value)
0xC4B4	CUT_BL_EN	0x01	RW	Bit[0]: Cut black level 0: Disable 1: Enable
0xC4B5	DARKBOOST_AUTO_EN	0x01	RW	Bit[0]: Dark boost auto switch 0: Disable 1: Enable
0xC4B6	AUTO_LOW_LEVEL_EN	0x01	RW	Bit[0]: Auto low level 0: Disable 1: Enable
0xC4BC	MAX_CURVE_GAIN_1	0x00	RW	Bit[7:0]: Max curve gain[15:8]
0xC4BD	MAX_CURVE_GAIN_2	0x90	RW	Bit[7:0]: Max curve gain[7:0]

table 5-12 combine control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0xC4BE	MANUAL_GAMMA_1	0x02	RW	Bit[7:0]: Manual gamma[15:8]
0xC4BF	MANUAL_GAMMA_2	0x00	RW	Bit[7:0]: Manual gamma[7:0]
0xC4C0	DB_GAIN_THRE_11	0x00	RW	Bit[7:0]: Dark boost gain threshold 1[15:8]
0xC4C1	DB_GAIN_THRE_12	0x20	RW	Bit[7:0]: Dark boost gain threshold 1[7:0]
0xC4C2	DB_GAIN_THRE_21	0x00	RW	Bit[7:0]: Dark boost gain threshold 2[15:8]
0xC4C3	DB_GAIN_THRE_22	0x80	RW	Bit[7:0]: Dark boost gain threshold 2[7:0]
0xC4C4	DB_AMT	0x10	RW	Dark Boost Amount
0xC4C5	DB_AMT_MIN	0x00	RW	Min Dark Boost Amount
0xC4C6	DB_AMT_MAX	0x10	RW	Max Dark Boost Amount
0xC4C7	ERROR_STEP	0x04	RW	Combine Error Compensation Step
0xC4C8	DB_MAX_GAMMA_1	0x03	RW	Bit[7:0]: Max dark boost gamma[15:8]
0xC4C9	DB_MAX_GAMMA_2	0xA0	RW	Bit[7:0]: Max dark boost gamma[7:0]
0xC4CA	DARK_TONE_WIDTH_1	0x10	RW	Bit[7:0]: Dark boost tone width[15:8]
0xC4CB	DARK_TONE_WIDTH_2	0x00	RW	Bit[7:0]: Dark boost tone width[7:0]

5.9 normalize

Normalize module is designed to adjust the image contrast. Normalize supports auto and manual mode. In manual mode, the normalize algorithm uses the manual input high level and low level. In auto mode, the algorithm will automatically update the low level and high levels.

table 5-13 normalize control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP_CTRL1	1'b1	R/W	Bit[1]: Normalize enable 0: Disable normalize 1: Enable normalize
0x5480	NORM RW00	0x21	RW	Bit[4:0]: Step
0x5481	NORM RW01	0x10	RW	Bit[6:0]: max_low_level 16 ~ 127
0x5482	NORM RW02	0xF8	RW	Bit[7:0]: min_low_level -128 to -16, complementary code

table 5-13 normalize control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5483	NORM RW03	0x04	RW	Bit[6:0]: ps_thres[14:8]
0x5484	NORM RW04	0x00	RW	Bit[7:0]: ps_thres[7:0]

5.10 tone_mapping

The tone-mapping module further adjusts the histogram and contrast.

table 5-14 tone_mapping registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	1'b1	R/W	Bit[2]: tone_mapping enable 0: Disable tone_mapping 1: Enable tone_mapping
0x5500	TOMP RW00	0x03	RW	Bit[2:0]: edge_thre 000: 16 001: 32 010: 64 011: 128 100: 256 101: 512
0x5501	TOMP RW01	0x3A	RW	Bit[5]: h_dark_en Bit[4]: uv_dark_en Bit[3:2]: h_dark_thre 00: 16 01: 32 10: 48 11: 64 Bit[1:0]: uv_dark_thre 00: 16 01: 32 10: 48 11: 64
0x5502	TOMP RW02	0x00	RW	Bit[0]: curve_step[8]
0x5503	TOMP RW03	0x40	RW	Bit[7:0]: curve_step[7:0]
0x5504	TOMP RW04	0xC6	RW	Bit[7:4]: max_alpha Bit[3:0]: min_alpha
0x5505	TOMP RW05	0x00	RW	Bit[3:0]: alpha
0x5506	TOMP RW06	0x00	RW	Bit[6:0]: min_dynamic_range[14:8]

table 5-14 tone_mapping registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5507	TOMP RW07	0x40	RW	Bit[7:0]: min_dynamic_range[7:0]
0x5508	TOMP RW08	0x04	RW	Bit[6:0]: max_dynamic_range[14:8]
0x5509	TOMP RW09	0x00	RW	Bit[7:0]: max_dynamic_range[7:0]
0x550A	TOMP RW10	0x00	RW	Bit[7:0]: dbg_ctrl_0
0x550B	TOMP RW11	0x00	RW	Bit[7:0]: dbg_ctrl_1
0x550C	TOMP RW12	0x00	RW	Bit[7:0]: dbg_ctrl_2
0x550D	TOMP RW13	0x00	RW	Bit[7:1]: Not used Bit[0]: dbg_sram_freeze
0x550E	TOMP RW14	0x00	RW	Bit[7:0]: dbg_addr
0xC4E4	CONTRAST_CURVE_1	0x10	RW	Contrast Curve 1
0xC4E5	CONTRAST_CURVE_2	0x20	RW	Contrast Curve 2
0xC4E6	CONTRAST_CURVE_3	0x30	RW	Contrast Curve 3
0xC4E7	CONTRAST_CURVE_4	0x40	RW	Contrast Curve 4
0xC4E8	CONTRAST_CURVE_5	0x50	RW	Contrast Curve 5
0xC4E9	CONTRAST_CURVE_6	0x60	RW	Contrast Curve 6
0xC4EA	CONTRAST_CURVE_7	0x70	RW	Contrast Curve 7
0xC4EB	CONTRAST_CURVE_8	0x80	RW	Contrast Curve 8
0xC4EC	CONTRAST_CURVE_9	0x90	RW	Contrast Curve 9
0xC4ED	CONTRAST_CURVE_10	0xA0	RW	Contrast Curve 10
0xC4EE	CONTRAST_CURVE_11	0xB0	RW	Contrast Curve 11
0xC4EF	CONTRAST_CURVE_12	0xC0	RW	Contrast Curve 12
0xC4F0	CONTRAST_CURVE_13	0xD0	RW	Contrast Curve 13
0xC4F1	CONTRAST_CURVE_14	0xE0	RW	Contrast Curve 14
0xC4F2	CONTRAST_CURVE_15	0xF0	RW	Contrast Curve 15
0xC4F3	CURVE_STEP	0x80	RW	Curve Adjustment Step
0xC4F4	CURVE_MIN_DR_1	0x00	RW	Bit[7:0]: Curve min dynamic range[15:8]
0xC4F5	CURVE_MIN_DR_2	0x20	RW	Bit[7:0]: Curve min dynamic range[7:0]
0xC4F6	CURVE_MAX_DR_1	0x02	RW	Bit[7:0]: Curve max dynamic range[15:8]
0xC4F7	CURVE_MAX_DR_2	0x00	RW	Bit[7:0]: Curve max dynamic range[7:0]
0xC4F8	CURVE_MIN_ALPHA	0x00	RW	Min Curve Alpha

table 5-14 tone_mapping registers (sheet 3 of 3)

address	register name	default value	R/W	description
0xC4F9	CURVE_MAX_ALPHA	0x0A	RW	Max Curve Alpha

5.11 OTP memory read/write

Since the OTP memory can only be programmed once, the user should be very careful while accessing the OTP.

5.11.1 procedure to read OTP content

1. Clear software buffer which is to receive the OTP content.
2. Start video streaming if not yet started.
3. Clear register buffer 0x3D00~0x3D0F to 0x00.
4. Set register 0x3D10 to 0x00.
5. Set register 0x3D10 to 0x01.
6. Wait 15ms.
7. Read register 0x3D00~0x3D0F and set to the software buffer.

The OTP read operation is performed to read back the information stored in OTP memory, to verify the OTP memory is blank before programming data into it, or to verify OTP content after programming data into it.

Verifying the OTP content at the last step of camera module testing is highly recommended in case the OTP content is accidently overwritten during the module testing.

5.11.2 procedure to program OTP content

1. Follow the above **procedure to read OTP content** to make sure the OTP is blank.
2. Program the intended OTP content to its corresponding register buffer, and clear unused register buffers to 0
   For OmniVision - registers 0x3D05~0x3D0F must be clear to 0x00 before initiating the OTP programming command.
   For customer - registers 0x3D00~0x3D0F must be clear to 0x00 before initiating the OTP programming command.
3. Read back registers 0x3D00~0x3D0F to make sure they contain the correct data to program to OTP memory, and 0 for all other bits.
4. Set register 0x3D10 to 0x00 to reset OTP functionality.
5. Write 0x02 to register 0x3D10 to initiate OTP programming.
6. Wait 15ms. Any register access during this period is prohibited.
7. Follow the above **procedure to read OTP content** to read back the OTP content.
8. Compare the OTP content read back to the intended OTP content.

5.11.3 power supply requirement for OTP memory programming

The OTP memory is programmed using the analog power. The AVDD voltage for OTP programming must be 2.5V ± 10%. The power supply should be able to provide extra 50mA for OTP programming.

5.12 group control

The OV10630/OV10131 supports up to four groups. Each group can have up to 256 registers. For group operation, you must first record the group, then write the related register values, and last, set record end.

table 5-15 group control registers

address	register name	default value	R/W	description
0x6F00	GROUP WRITER COMMAND	0x00	RW	Bit[7:6]: Operation code 00: Group record end 01: Group launch (only once) 10: Group launch (ABC mode) 11: Group record start In ABC mode, group0 is for frame A, group1 is for frame B and group2 is for frame C. The three groups launch periodically. Bit[5:4]: Group ID Bit[3:2]: Chip debug Bit[1:0]: Group write function enable, must be 2'b11
0xCFF2	GROUP TABLE0H	0xDD	RW	Group Table0 Start Address HSB
0xCFF3	GROUP TABLE0L	0x00	RW	Group Table0 Start Address HSB
0xCFF6	GROUP TABLE1H	0xDD	RW	Group Table1 Start Address HSB
0xCFF7	GROUP TABLE1L	0x80	RW	Group Table1 Start Address HSB
0xCFFA	GROUP TABLE2H	0xDE	RW	Group Table2 Start Address HSB
0xCFFB	GROUP TABLE2L	0x00	RW	Group Table2 Start Address HSB
0xCFFE	GROUP TABLE3H	0xDE	RW	Group Table3 Start Address HSB
0xCFFF	GROUP TABLE3L	0x80	RW	Group Table3 Start Address HSB

5.13 windowing cropping and sub-sampling

table 5-16 WINC control registers

address	register name	default value	R/W	description
0x5002	ISP CTRL02	1'b1	RW	Bit[2]: winc_en 0: Disable window cropping 1: Enable window cropping
0x5005	ISP RW05	0x08	RW	Bit[7]: vap_v_sel Bit[5]: vap_second_line Bit[4]: vap_second_pix Bit[3]: vap_mean Bit[2:1]: vap_drop Bit[0]: vap_en

5.14 white/black pixel cancellation (WBC)

This block corrects the white and black defect pixel.

table 5-17 WBC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP RW00	2'b11	RW	Bit[4]: White defect pixel correction enable 0: Disable 1: Enable Bit[3]: Black defect pixel correction enable 0: Disable 1: Enable
0x5180	WBC CTRL00	0x1C	RW	Bit[7:0]: Debug mode for long exposure sub-pixel
0x5181	WBC CTRL01	0x13	RW	Bit[4]: Debug mode Bit[1:0]: Option for padding the boundary pixel for long exposure sub-pixel
0x5182~ 0x5191	DEBUG CONTROL	–	RW	WBC Debug Control for Long Exposure Sub-pixel
0x5192	WBC CTRL12	0x1C	RW	Bit[7:0]: Debug mode for short exposure sub-pixel

table 5-17 WBC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5193	WBC CTRL13	0x13	RW	Bit[4]: Debug mode Bit[1:0]: Option for padding the boundary pixel for short exposure sub-pixel
0x5194~ 0x51A3	DEBUG CONTROL	–	RW	WBC Debug Control for Short Exposure Sub-pixel

6 image sensor output interface digital functions

6.1 temperature sensor

6.1.1 overview

The temperature sensor can detect current temperature. The temperature can cover from -40ºC to +105ºC. This module needs a 1-3 MHz clock divided from XVCLK. IF XVCLK is 24 MHz, 0x6706[3:0] needs to be programmed to 8.

6.1.2 output mode

There are two other simple ways to get the temperature. One is {0x6715, 0x6717} where 0x6715[7] is the sign bit and the other 15 bits are the absolute value. The other way is using register 0x6719. If register 0x6719 is larger than 0xC0, it is a negative value. If 0x6719 is smaller than 0xC0, it is a positive value.

When {0x6715, 0x6717} is used register 0x6707 can be used to stall the temperature calculation in order to get the consistent value from these two registers.

table 6-1 TPM control

address	register name	default value	R/W	description
0x6706	TPM_CTRL0	0x78	RW	Bit[7:4]: Reserved Bit[3:0]: Module clock divider
0x6707	TPM_STALL	0x00	RW	Bit[0]: tpm_stall
0x6710~ 0x6714	TPM_DB_NUM	–	R	Debug Information for TPM Control
0x6715	TPM_01	–	R	Bit[7]: Sign Bit[6:0]: TPM o1[14:8] Temperature high byte
0x6716	TPM_DB_NUM	–	R	Debug Information for TPM Control
0x6717	TPM_01	–	R	Bit[7:0]: TPM o1[7:0] Temperature low byte
0x6718	TPM_DB_NUM	–	R	Debug Information for TPM Control
0x6719	TPM_02	–	R	If 0x6719 < 192, temperature = 0x6719 If 0x6719 ≥ 192, temperature = -(256-0x6719)
0x6720~ 0x6721	TPM_DB_NUM	–	R	Debug Information for TPM Control

6.2 embedded line

6.2.1 overview

Embedded line contains register values. The embedded lines is prefixed to the normal image data. The line length of the embedded line is the same as the normal image line. Embedded line only contains register value that are followed with a 0x369 tag (10-bit) or 0xDA tag (8-bit). The 8-bit register values are output D[9:2].

Only the last embedded line contains valid register data for each frame. The other embedded line is a dummy line used to make an even number of lines per frame.

table 6-2 embedded line control

address	register name	default value	R/W	description
0x6800	EMB_LINE_EN	0x00	RW	Bit[0]: emb_line enable
0x6801	EMB_LINE_TAG	0xDA	RW	Bit[7:0]: emb_line tag[9:2]
0x6802	EMB_LINE_TAG	0x01	RW	Bit[1:0]: emb_line tag[1:0]
0x6803	EMB_LINE_SOF_CTRL	0x11	RW	Bit[7:4]: s2h_width Bit[3:0]: sof_width
0x6804	EMB_SIZE_MANU_EN	0x00	RW	Bit[0]: emb_size manual enable
0x6805	EMB_SIZE_MANU	0x04	RW	Bit[7:0]: emb_size[15:8]
0x6806	EMB_SIZE_MANU	0x00	RW	Bit[7:0]: emb_size[7:0]
0x6807	EMB_MASK_EN	0x01	RW	Bit[0]: emb_line mask enable

6.3 DVP timing

figure 6-1 DVP timing diagram

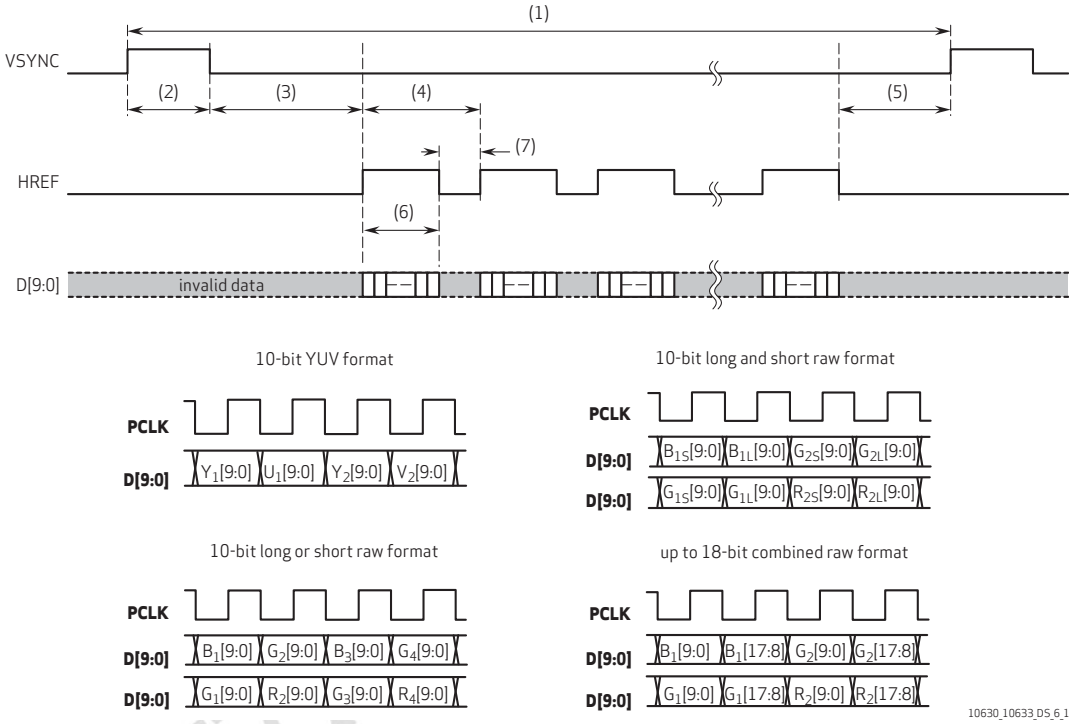


table 6-3 DVP timing specifications[a] (sheet 1 of 3)

resolution	parameter	format			
		YUV	combined RAW	long and short RAW	long or short RAW
1280x720	(1) frame period	748 lines	748 lines	748 lines	748 lines
	(2) VSYNC width	128.5 t_p	128.5 t_p	128.5 t_p	257 t_p
	(3) VSYNC to HREF	28760.5 t_p	28752.5 t_p	25154.5 t_p	25223 t_p
	(4) line period	1782 t_p	1782 t_p	1782 t_p	1782 t_p
	(5) HREF to VSYNC	21007 t_p	21015 t_p	24613 t_p	24416 t_p
	(6) active pixel	1280 t_p	1280 t_p	1280 t_p	1280 t_p
	(7) horizontal blanking	502 t_p	502 t_p	502 t_p	502 t_p

table 6-3 DVP timing specifications[a] (sheet 2 of 3)

resolution	parameter	format			
		YUV	combined RAW	long and short RAW	long or short RAW
752x480	(1) frame period	520 lines	520 lines	520 lines	520 lines
	(2) VSYNC width	128.5 t_p	128.5 t_p	128.5 t_p	257 t_p
	(3) VSYNC to HREF	20660.5 t_p	20746.5 t_p	18148.5 t_p	18021t_p
	(4) line period	1282 t_p	1282 t_p	1282 t_p	1282 t_p
	(5) HREF to VSYNC	30491 t_p	30405 t_p	33003 t_p	33002 t_p
	(6) active pixel	752 t_p	752 t_p	752 t_p	752 t_p
	(7) horizontal blanking	530 t_p	530 t_p	530 t_p	530 t_p
640x480	(1) frame period	520 lines	520 lines	520 lines	520 lines
	(2) VSYNC width	128.5 t_p	128.5 t_p	128.5 t_p	257 t_p
	(3) VSYNC to HREF	20636.5 t_p	20694.5 t_p	18096.5 t_p	17969 t_p
	(4) line period	1282 t_p	1282 t_p	1282 t_p	1282 t_p
	(5) HREF to VSYNC	30515 t_p	30457 t_p	33055 t_p	33054 t_p
	(6) active pixel	640 t_p	640 t_p	640 t_p	640 t_p
	(7) horizontal blanking	642 t_p	642 t_p	642 t_p	642 t_p
640x400	(1) frame period	438 lines			
	(2) VSYNC width	128.5 t_p			
	(3) VSYNC to HREF	14701 t_p			
	(4) line period	914 t_p			
	(5) HREF to VSYNC	19902.5 t_p			
	(6) active pixel	640 t_p			
	(7) horizontal blanking	274 t_p			
352x288	(1) frame period	328 lines			
	(2) VSYNC width	128.5 t_p			
	(3) VSYNC to HREF	9748 t_p			
	(4) line period	618 t_p			
	(5) HREF to VSYNC	14443.5 t_p			
	(6) active pixel	352 t_p			
	(7) horizontal blanking	256 t_p			

table 6-3 DVP timing specifications[a] (sheet 3 of 3)

resolution	parameter	format			
		YUV	combined RAW	long and short RAW	long or short RAW
320x240	(1) frame period	280 lines			
	(2) VSYNC width	128.5 t_p			
	(3) VSYNC to HREF	7040 t_p			
	(4) line period	440 t_p			
	(5) HREF to VSYNC	10431.5 t_p			
	(6) active pixel	320 tp			
	(7) horizontal blanking	120 t_p			

a. these parameters change with register settings

6.3.1 DVP setup/hold time

figure 6-2 DVP setup/hold time diagram

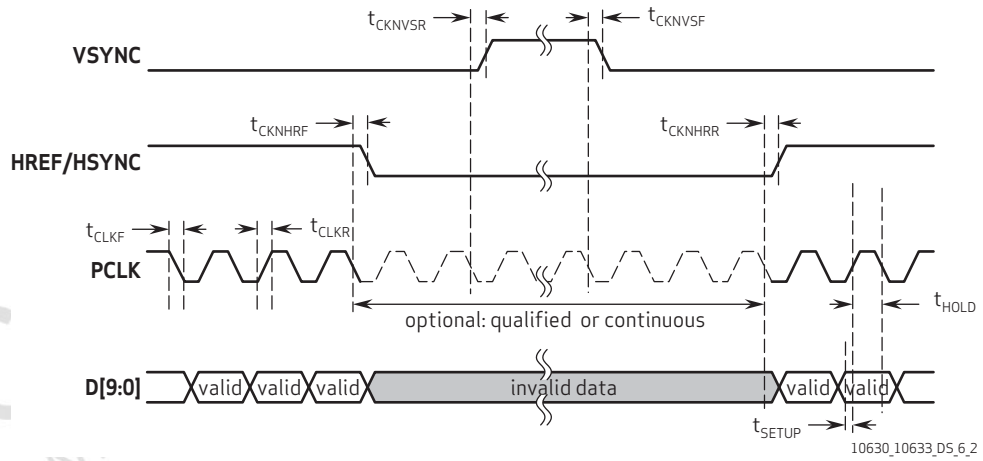


table 6-4 DVP setup/hold time[ab] (sheet 1 of 2)

symbol	parameter	min	typ	max	unit
t_{CKNVSR}	PCLK falling edge to VSYNC rising edge delay	–	0.5	1	ns
t_{CKNVSF}	PCLK falling edge to VSYNC falling edge delay	–	1	1.5	ns

table 6-4 DVP setup/hold time[ab] (sheet 2 of 2)

symbol	parameter	min	typ	max	unit
t_{CKNHRF}	PCLK falling edge to HREF falling edge delay	–	0	1	ns
t_{CKNHRR}	PCLK falling edge to HREF rising edge delay	–	-0.5	0.5	ns
t_{CLKF}	PCLK fall time		1.2	2.5	ns
t_{CLKR}	PLCK rise time		1.8	3.5	ns
t_{SETUP}	data setup time	3	4	–	ns
t_{HOLD}	data hold time	3	5	–	ns

a. measured at 1.8V DOVDD and 96 MHz PCLK, with 2x drive strength and 10 pF loading

b. timing measurement shown at the beginning of the rising edge or end of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the end of the rising edge or the beginning of the falling edge signifies 90%

7 register tables

The following table provides a preliminary description of the device control registers contained in the OV10633/OV10133. The 7-bit I2C slave device address is 0x30 | SCCBID[2:0], where SCCBID[2:0] is from pin GPIO/SCCBID[2:0].

7.1 system control [0x0100 - 0x3049]

table 7-1 system control registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x0100	STREAM MODE	0x00	RW	Bit[7:1]: Not used Bit[0]: Turn on video stream after power up, always set to "1" 0: Not used 1: Stream on
0x0103	SOFTWARE RESET	0x00	RW	Software Reset will Auto Clear by Itself to 0x00
0x3000	SC_CMMN_PAD_OEN0	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: io_y_oen[9:8]
0x3001	SC_CMMN_PAD_OEN1	0x00	RW	Bit[7:4]: io_y_oen[7:0] Bit[3:0]: Not used
0x3002	SC_CMMN_PAD_OEN2	0x00	RW	Bit[7]: io_vsync_oen Bit[6]: io_href_oen Bit[5]: io_pclk_oen Bit[4]: Reserved Bit[3]: io_strobe_oen Bit[2]: io_sda_oen Bit[1]: io_gpio1_oen Bit[0]: io_gpio0_oen
0x3003	SC_CMMN_PLL_CTRL0	0x20	RW	Bit[7:6]: SCLK PLL cp[1:0] Bit[5:0]: SCLK PLL multi
0x3004	SC_CMMN_PLL_CTRL1	0x00	RW	Bit[7]: Bypass SCLK PLL Bit[6:4]: SCLK PLL pre div Bit[3]: SCLK PLL cp[2] Bit[2:0]: SCLK PLL sdiv
0x3005	SC_CMMN_PLL_CTRL2	0x20	RW	Bit[7:6]: PCLK PLL cp[1:0] Bit[5:0]: PCLK PLL multi
0x3006	SC_CMMN_PLL_CTRL3	0x00	RW	Bit[7]: Bypass PCLK PLL Bit[6:4]: PCLK PLL pre div Bit[3]: PCLK PLL cp[2] Bit[2:0]: PCLK PLL sdiv
0x3007	SC_CMMN_PCLK_DIV_CTRL	0x01	RW	Bit[7:0]: Chip debug
0x3008	SC_CMMN_PAD_OUT0	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: io_y_o[9:8]

table 7-1 system control registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x3009	SC_CMMN_PAD_OUT1	0x00	RW	Bit[7:0]: io_y_o[7:0]
0x300A	PID	0xA6	R	Product ID Number MSB (Read only)
0x300B	VER	0x30	R	Product ID Number LSB (Read only)
0x300C	SC_CMMN_SCCB_ID	0x60	RW	Bit[7:1]: SCCB ID Bit[0]: SCCB ID select 0: {sccb_id[7:4],gpio_i[3:1]} 1: sccb_id[7:1]
0x300D	SC_CMMN_PAD_OUT2	0x00	RW	Bit[7]: io_vsync_o Bit[6]: io_href_o Bit[5]: io_pclk_o Bit[4:0]: Reserved
0x300E	SC_CMMN_PAD_SEL0	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: io_y_sel[9:8]
0x300F	SC_CMMN_PAD_SEL1	0x00	RW	Bit[7:0]: io_y_sel[7:0]
0x3010	SC_CMMN_PAD_SEL2	0x00	RW	Bit[7]: io_vsync_sel Bit[6]: io_href_sel Bit[5]: io_pclk_sel Bit[4:0]: Reserved
0x3011	SC_CMMN_PAD	0x02	RW	Bit[7:6]: Pad drive strength Bit[5:0]: Reserved
0x3012	SC_CMMN_SENSOR_GATE_CTRL	0x00	RW	Bit[7]: Sensor gate BLC enable Bit[6]: Sensor gate ISP enable Bit[5]: Not used Bit[4]: Sensor gate VFIFO enable Bit[3]: Sensor gate DVP enable Bit[2:1]: Not used Bit[0]: Sensor gate OTP enable
0x3016~ 0x3019	SC_CMMN_CTRL	–	RW	Bit[7:0]: Chip debug
0x301A	SC_CMMN_CLKRST0	0x70	RW	Bit[7:6]: Reserved Bit[5]: sclk_ac Bit[4]: sclk_tc Bit[3:2]: Reserved Bit[1]: rst_ac Bit[0]: rst_tc

table 7-1 system control registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x301B	SC_CMMN_CLKRST1	0xB4	RW	Bit[7]: sclk_blc Bit[6]: sclk_isp Bit[5]: Chip debug Bit[4]: sclk_vfifo Bit[3]: rst_blc Bit[2]: rst_isp Bit[1]: Chip debug Bit[0]: rst_vfifo
0x301C	SC_CMMN_CLKRST2	0xF0	RW	Bit[7]: pclk_dvp Bit[6]: Chip debug Bit[5]: sclk_cif Bit[4]: sclk_otp Bit[3]: rst_dvp Bit[2]: Chip debug Bit[1]: rst_cif Bit[0]: rst_otp
0x301D	SC_CMMN_CLKRST3	0xB4	RW	Bit[7]: sclk2x_isp Bit[6:5]: Chip debug Bit[4]: sclk_aec_pk Bit[3]: Not used Bit[2:1]: Chip debug Bit[0]: rst_aec_pk
0x301E	SC_CMMN_CLKRST4	0xF0	RW	Bit[7:6]: Chip debug Bit[5]: pclk_vfifo Bit[4:2]: Chip debug Bit[1:0]: Reserved
0x301F	SC_CMMN_FREX_RST_MASK0	0x00	RW	Bit[7:0]: Reserved
0x3020	SC_CMMN_CLOCK_SEL	0x0B	RW	Bit[7]: Not used Bit[6:4]: Chip debug Bit[3:0]: Reserved
0x3021	SC_CMMN_MISC_CTRL	0x03	RW	Bit[7]: pclk_inv enable Bit[6]: sclk_inv enable Bit[5]: sclk2x_inv enable Bit[4:1]: Reserved Bit[0]: cen_global_o
0x3022	SC_CMMN_CORE_CTRL	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Chip debug

table 7-1 system control registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x3023	SC_CMMN_CORE_CTRL	0x00	RW	Bit[7:6]: Chip debug Bit[5]: bist_en Bit[4]: CLK switch 0: Switch all clock to pad clock 1: Switch from pad clock to all clock Bit[3]: Not used Bit[2:0]: Chip debug
0x3024	SC_CMMN_CORE_CTRL	0x04	RW	Bit[7:6]: Not used Bit[5:4]: RAW mode 00: Long 01: Short 10: Long, short 11: combined Bit[3]: Debug mode Bit[2:1]: YUV mode 00: WDR 01: Long 10: Short 11: Not allowed Bit[0]: PCLK PLL disable 0: PCLK from secondary PLL 1: PCLK from system clock
0x3025	SC_CMMN_CORE_CTRL1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Debug control
0x3028	NOT USED	–	–	Not Used
0x3029	SC_CMMN_BIST_EN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Debug control
0x302A	SC_CMMN_SB_ID	0xF2	RW	Chip Subversion ID
0x302B	SC_CMMN_RS232_ID	0xFE	RW	Chip Debug
0x302C	SC_CMMN_PWDN_CTRL1	0x00	RW	Bit[7]: gate_pad_clk_man Bit[6:5]: Reserved Bit[4]: rst_ana_man Bit[3]: gate_dig1_man Bit[2]: rst_dig1_man Bit[1]: gate_dig2_man Bit[0]: rst_dig2_man

table 7-1 system control registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x302D	SC_CMMN_PWDN_CTRL2	0x2F	RW	Bit[7:4]: Not used Bit[3]: Rst dig1 enable when PWDN Bit[2]: Rst dig2 enable when PWDN Bit[1]: Rst ISP enable when PWDN Bit[0]: PWDN and power up sequence enable
0x302E	SC_CMMN_FSIN_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: FSIN enable
0x302F	SC_CMMN_GPIO01	0x88	RW	Bit[7]: gpio0_sel Bit[6]: gpio0_dir Bit[5]: gpio0_out Bit[4]: gpio0_in, read only Bit[3]: gpio1_sel Bit[2]: gpio1_dir Bit[1]: gpio1_out Bit[0]: gpio1_in, read only
0x3030	SC_CMMN_GPIO23	0x80	RW	Bit[7]: gpio2_sel Bit[6]: gpio2_dir Bit[5]: gpio2_out Bit[4]: gpio2_in, read only Bit[3]: gpio3_sel Bit[2]: gpio3_dir Bit[1]: gpio3_out Bit[0]: gpio3_in, read only
0x3031	SC_CMMN_GPIO45	0x00	RW	Bit[7]: gpio4_sel Bit[6]: gpio4_dir Bit[5]: gpio4_out Bit[4]: gpio4_in, read only Bit[3]: gpio5_sel Bit[2]: gpio5_dir Bit[1]: gpio5_out Bit[0]: gpio5_in, read only

table 7-1 system control registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x3032	SC_CMMN_PUMP_CLK_SEL	0x44	RW	Bit[7]: Not used Bit[6:4]: n_pump_ck_sel 000: pll_sclk_i 001: pll_sclk_i/2 010: pll_sclk_i/4 011: pll_sclk_i/8 100: Pad clock 101: Pad clock/2 110: Pad clock/4 111: Not used Bit[2:0]: p_pump_clk_sel 000: pll_pclk_i 001: pll_pclk_i/2 010: pll_pclk_i/4 011: pll_pclk_i/8 100: Pad clock 101: Pad clock/2 110: Pad clock/4 111: Not used
0x3033	SC_CMMN_SCLK2X_SEL	0x08	RW	Bit[7:4]: Not used Bit[3:2]: System clock select 00: Reserved 01: system clock/2 10: system clock/4 11: Reserved Bit[1:0]: Reserved
0x3038	SC_CMMN_MAN_ID	–	R	Manufacturer ID High Byte
0x3039	SC_CMMN_MAN_ID	–	R	Manufacturer ID Low Byte
0x303C	SC_CMMN_PWDN	–	R	Bit[7:1]: Not used Bit[0]: Power down signal from PAD
0x303D~ 0x303E	RSVD	–	–	Reserved
0x3040	SC_SOC_CLKRST5	0xF0	RW	Bit[7]: sclk_isp_fc Bit[6]: sclk_fc Bit[5]: Reserved Bit[4]: sclk_fmt Bit[3]: rst_isp_fc Bit[2]: rst_fc Bit[1]: Reserved Bit[0]: rst_fmt
0x3041	SC_SOC_CLKRST6	0xF0	RW	Bit[7:6]: Chip debug Bit[5]: sclk_intr_reg Bit[4:2]: Chip debug Bit[1]: rst_intr_reg Bit[0]: Chip debug

table 7-1 system control registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x3042	SC_SOC_CLKRST7	0xF9	RW	Bit[7]: sclk_wb Bit[6]: sclk_dr Bit[5]: sclk_mp Bit[4]: sclk_ct Bit[3]: rst_wb Bit[2]: rst_dr Bit[1]: rst_mp Bit[0]: rst_ct
0x3043	SC_SOC_FREX_RST_MASK1	0xF0	RW	Bit[7:0]: Reserved
0x3044	SC_SOC_MC_DIV	0x01	RW	Bit[7:0]: Reserved
0x3045	SC_SOC_PWDN_CTRL_SOC	0x01	RW	Bit[7:1]: Not used Bit[0]: Enable SRB when PWDN
0x3046	SC_SOC_TIMEOUT	0x00	RW	Bit[7:1]: Not used Bit[0]: Timeout counter enable
0x3047	SC_SOC_CLKRST8	0x70	RW	Bit[7:0]: Chip debug
0x3048	SC_SOC_SNR_GATE_CTRL	0x00	RW	Bit[7:0]: Chip debug
0x3049	SC_SOC_SNR_GATE_CTRL	0x00	RW	Bit[7:0]: Chip debug

7.2 analog control [0x3600 - 0x3633]

table 7-2 analog control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3600	ANA_ADC1	0x54	RW	ADC Control 1
0x3601	ANA_ADC2	0x03	RW	ADC Control 2
0x3602	ANA_ADC3	0x2F	RW	ADC Control 3
0x3603	ANA_ADC4	0x00	RW	ADC Control 4
0x3610	ANA_ANALOG1	0x2C	RW	Analog Control 1
0x3611	ANA_ANALOG2	0x66	RW	Analog Control 2
0x3612	ANA_ANALOG3	0xE8	RW	Analog Control 3
0x3613	ANA_ANALOG4	0x01	RW	Analog Control 4
0x3614	ANA_ANALOG5	0x00	RW	Analog Control 5
0x3615	ANA_ANALOG6	0x00	RW	Analog Control 6

table 7-2 analog control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3616~ 0x3618	ANA_ANALOG7	0x00	RW	Chip Debug
0x3620	ANA_ARRAY2	0x88	RW	Array Readout Control 2
0x3621	ANA_ARRAY1	0x03	RW	Array Readout Control 1
0x3630	ANA_PWC1	0x00	RW	Power/Reference Control 1
0x3631	ANA_PWC2	0x14	RW	Power/Reference Control 2
0x3632	ANA_PWC3	0x40	RW	Power/Reference Control 3
0x3633	ANA_PWC4	0xBA	RW	Power/Reference Control 4

7.3 sensor control [0x3700 - 0x374F]

table 7-3 sensor control (sheet 1 of 3)

address	register name	default value	R/W	description
0x3700	SENSOR_REG00	0x22	RW	Timing Control 1
0x3701	SENSOR_CTRL01	0x28	RW	Timing Control 2
0x3702	SENSOR_RSTGOLOW	0x20	RW	Timing Control 3
0x3703	SENSOR HLDWIDTH	0x32	RW	Timing Control 4
0x3704	SENSOR_TXWIDTH	0x32	RW	Timing Control 5
0x3705	SENSOR_REG05	0x61	RW	Timing Control 6
0x3706	SENSOR_REG06	0x11	RW	Debug Control
0x3707	SENSOR_REG7	0x03	RW	Timing Control 7
0x3708	SENSOR_REG8	0x00	RW	Timing Control 8
0x3709	SENSOR_REG9	0x28	RW	Timing Control 9
0x370A	SENSOR_REGA	0x00	RW	Timing Control 10
0x370B	SENSOR_REGB	0x11	RW	Timing Control 11
0x370C	SENSOR_REGC	0x07	RW	Timing Control 12
0x370D	SENSOR_REGD	0x00	RW	Timing Control 13

table 7-3 sensor control (sheet 2 of 3)

address	register name	default value	R/W	description
0x370E~ 0x370F	SENSOR RSVD	0x00	RW	Chip Debug
0x3710	SENSOR_REG10	0x33	RW	Timing Control 14
0x3712	SENSOR_RSTYZ_ GOLOW	0x00	RW	Timing Control 15
0x3713	SENSOR_RSTYZ_ GOLOW	0x20	RW	Timing Control 16
0x3714	SENSOR_EQ_GOLOW	0x08	RW	Timing Control 17
0x3715	SENSOR_REG15	0x04	RW	Timing Control 18
0x3716	SENSOR_STROBE_ CTRL	0x03	RW	Bit[7:3]: Not used Bit[2]: AEC frame reverse Bit[1]: Shadow canceling 1 line strobe mode enable Bit[0]: Shadow cancel auto mode enable
0x3717	SENSOR_STRBE_ WIDTH	0x01	RW	Strobe Width for Shadow Canceling
0x3718	SENSOR_STB_ST_ MAN	0x00	RW	Bit[7:0]: Shadow cancel manual strobe start line[15:8]
0x3719	SENSOR_STB_ST_ MAN	0x00	RW	Bit[7:0]: Shadow cancel manual strobe start line[7:0]
0x371A	SENSOR_STB_END_ MAN	0x01	RW	Bit[7:0]: Shadow cancel manual strobe end line[15:8]
0x371B	SENSOR_STB_END_ MAN	0x01	RW	Bit[7:0]: Shadow cancel manual strobe end line[7:0]
0x371C	SENSOR_BITSW_HI	0x00	RW	Bit[7:0]: Bitsw_gohi[15:8]
0x371D	SENSOR_BITSW_HI	0x00	RW	Bit[7:0]: Bitsw_gohi[7:0]
0x3740	SENSOR_STB_OK_ START[9:8]	–	R	Good Start Line of Shadow Canceling Strobe High Byte
0x3741	SENSOR_STB_OK_ START[7:0]	–	R	Good Start Line of Shadow Canceling Strobe Low Byte
0x3742	SENSOR_STB_OK_ END[9:8]	–	R	Good End Line of Shadow Canceling Strobe High Byte
0x3743	SENSOR_STB_OK_ END[7:0]	–	R	Good End Line of Shadow Canceling Strobe Low Byte
0x3744	SENSOR_STB_EXP_ WIDTH	–	R	Shadow Canceling Strobe Width For Each Line High Byte

table 7-3 sensor control (sheet 3 of 3)

address	register name	default value	R/W	description
0x3745	SENSOR_STB_EXP_ WIDTH	–	R	Shadow Canceling Strobe Width For Each Line Low Byte
0x3748~ 0x374F	SENSOR_CTRL48	–	R	Chip Debug Information

7.4 timing control [0x3800 - 0x3844]

table 7-4 timing control (sheet 1 of 3)

address	register name	default value	R/W	description
0x3800	TIMING_X_START_ADDR	0x00	RW	Horizontal Start Address of Array for Readout High Byte
0x3801	TIMING_X_START_ADDR	0x00	RW	Horizontal Start Address of Array for Readout Low Byte
0x3802	TIMING_Y_START_ADDR	0x00	RW	Vertical Start Address of Array for Readout High Byte
0x3803	TIMING_Y_START_ADDR	0x00	RW	Vertical Start Address of Array for Readout Low Byte
0x3804	TIMING_X_END_ADDR	0x05	RW	Horizontal End Address of Array for Readout High Byte
0x3805	TIMING_X_END_ADDR	0x0F	RW	Horizontal End Address of Array for Readout Low Byte
0x3806	TIMING_Y_END_ADDR	0x03	RW	Vertical End Address of Array for Readout High Byte
0x3807	TIMING_Y_END_ADDR	0x28	RW	Vertical End Address of Array for Readout Low Byte
0x3808	TIMING_X_OUTPUT_SIZE	0x05	RW	DVP Horizontal Output Size (pixel) High Byte
0x3809	TIMING_X_OUTPUT_SIZE	0x00	RW	DVP Horizontal Output Size (pixel) Low Byte
0x380A	TIMING_Y_OUTPUT_SIZE	0x03	RW	DVP Vertical Output Size (pixel) High Byte
0x380B	TIMING_Y_OUTPUT_SIZE	0x20	RW	DVP Vertical Output Size (pixel) Low Byte
0x380C	TIMING_HTS	0x07	RW	Horizontal Total Size High Byte
0x380D	TIMING_HTS	0x70	RW	Horizontal Total Size Low Byte
0x380E	TIMING_VTS	0x03	RW	Vertical Total Size High Byte

table 7-4 timing control (sheet 2 of 3)

address	register name	default value	R/W	description
0x380F	TIMING_VTS	0x48	RW	Vertical Total Size Low Byte
0x3810	TIMING_ISP_X_WIN	0x00	RW	ISP Horizontal Windowing Start Address High Byte
0x3811	TIMING_ISP_X_WIN	0x00	RW	ISP Horizontal Windowing Start Address Low Byte
0x3812	TIMING_ISP_Y_WIN	0x00	RW	ISP Vertical Windowing Start Address High Byte
0x3813	TIMING_ISP_Y_WIN	0x00	RW	ISP Vertical Windowing Start Address Low Byte
0x3815	TIMING_CTRL15	0x8C	RW	Bit[7]: Black line HREF enable Bit[6]: Reserved Bit[5]: Rip SOF enable Bit[4]: Horizontal crop manual enable Bit[3:0]: Black lines number
0x3817	TIMING_CTRL17	0x00	RW	Bit[7:4]: tc_sof Vertical start line number Bit[3:0]: Not used
0x3819	TIMING_CTRL19	0x00	RW	Bit[7:4]: SOF delay control Bit[3]: Debug control Bit[2]: Not used Bit[1:0]: Debug control
0x381C	TIMING_CTRL1C	0x00	RW	Bit[7]: Vflip to digital Bit[6]: Vflip in array Bit[5:2]: Chip debug Bit[1]: Vsub4 Bit[0]: Vsub2
0x381D	TIMING_CTRL1D	0x40	RW	Bit[7]: Vflip black line Bit[6]: wdr_en Bit[5:2]: Not used Bit[1]: Mirror to digital Bit[0]: Mirror to array
0x381E	CHIP DEBUG	0x00	RW	Vertical Start Offset High Byte
0x381F	CHIP DEBUG	0x0C	RW	Vertical Start Offset Low Byte
0x3820~ 0x3830	TIMING_GRP	–	RW	Chip Debug
0x3832	TIMING_TC_CS_RST	0x00	RW	Horizontal Counter Reset Value High Byte
0x3833	TIMING_TC_CS_RST	0x00	RW	Horizontal Counter Reset Value Low Byte
0x3834	TIMING_TC_R_RST	0x00	RW	Vertical Counter Reset Value (vts - tc_r_rst) High Byte
0x3835	TIMING_TC_R_RST	0x10	RW	Vertical Counter Reset Value (vts - tc_r_rst) Low Byte

table 7-4 timing control (sheet 3 of 3)

address	register name	default value	R/W	description
0x3844	TIMING_GRP_STS	–	W	Bit[7:4]: Not used Bit[3:0]: Chip debug

7.5 OTP control [0x3D00 - 0x3D1F]

table 7-5 OTP control (sheet 1 of 3)

address	register name	default value	R/W	description
0x3D00	OTP_DATA_0	0x00	RW	OTP Dump/load Data Buffer0
0x3D01	OTP_DATA_1	0x00	RW	OTP Dump/load Data Buffer1
0x3D02	OTP_DATA_2	0x00	RW	OTP Dump/load Data Buffer2
0x3D03	OTP_DATA_3	0x00	RW	OTP Dump/load Data Buffer3
0x3D04	OTP_DATA_4	0x00	RW	OTP Dump/load Data Buffer4
0x3D05	OTP_DATA_5	0x00	RW	OTP Dump/load Data Buffer5
0x3D06	OTP_DATA_6	0x00	RW	OTP Dump/load Data Buffer6
0x3D07	OTP_DATA_7	0x00	RW	OTP Dump/load Data Buffer7
0x3D08	OTP_DATA_8	0x00	RW	OTP Dump/load Data Buffer8
0x3D09	OTP_DATA_9	0x00	RW	OTP Dump/load Data Buffer9
0x3D0A	OTP_DATA_A	0x00	RW	OTP Dump/load Data Buffer10
0x3D0B	OTP_DATA_B	0x00	RW	OTP Dump/load Data Buffer11
0x3D0C	OTP_DATA_C	0x00	RW	OTP Dump/load Data Buffer12
0x3D0D	OTP_DATA_D	0x00	RW	OTP Dump/load Data Buffer13
0x3D0E	OTP_DATA_E	0x00	RW	OTP Dump/load Data Buffer14
0x3D0F	OTP_DATA_F	0x00	RW	OTP Dump/load Data Buffer15
0x3D30	OTP_DATA_10	0x00	RW	OTP Dump/load Data Buffer10
0x3D31	OTP_DATA_11	0x00	RW	OTP Dump/load Data Buffer11
0x3D32	OTP_DATA_12	0x00	RW	OTP Dump/load Data Buffer12
0x3D33	OTP_DATA_13	0x00	RW	OTP Dump/load Data Buffer13

table 7-5 OTP control (sheet 2 of 3)

address	register name	default value	R/W	description
0x3D34	OTP_DATA_14	0x00	RW	OTP Dump/load Data Buffer14
0x3D35	OTP_DATA_15	0x00	RW	OTP Dump/load Data Buffer15
0x3D36	OTP_DATA_16	0x00	RW	OTP Dump/load Data Buffer16
0x3D37	OTP_DATA_17	0x00	RW	OTP Dump/load Data Buffer17
0x3D38	OTP_DATA_18	0x00	RW	OTP Dump/load Data Buffer18
0x3D39	OTP_DATA_19	0x00	RW	OTP Dump/load Data Buffer19
0x3D3A	OTP_DATA_1A	0x00	RW	OTP Dump/load Data Buffer1A
0x3D3B	OTP_DATA_1B	0x00	RW	OTP Dump/load Data Buffer1B
0x3D3C	OTP_DATA_1C	0x00	RW	OTP Dump/load Data Buffer1C
0x3D3D	OTP_DATA_1D	0x00	RW	OTP Dump/load Data Buffer1D
0x3D3E	OTP_DATA_1E	0x00	RW	OTP Dump/load Data Buffer1E
0x3D3F	OTP_DATA_1F	0x00	RW	OTP Dump/load Data Buffer1F
0x3D40	OTP_DATA_20	0x00	RW	OTP Dump/load Data Buffer20
0x3D41	OTP_DATA_21	0x00	RW	OTP Dump/load Data Buffer21
0x3D42	OTP_DATA_22	0x00	RW	OTP Dump/load Data Buffer22
0x3D43	OTP_DATA_23	0x00	RW	OTP Dump/load Data Buffer23
0x3D44	OTP_DATA_24	0x00	RW	OTP Dump/load Data Buffer24
0x3D45	OTP_DATA_25	0x00	RW	OTP Dump/load Data Buffer25
0x3D46	OTP_DATA_26	0x00	RW	OTP Dump/load Data Buffer26
0x3D47	OTP_DATA_27	0x00	RW	OTP Dump/load Data Buffer27
0x3D48	OTP_DATA_28	0x00	RW	OTP Dump/load Data Buffer28
0x3D49	OTP_DATA_29	0x00	RW	OTP Dump/load Data Buffer29
0x3D4A	OTP_DATA_2A	0x00	RW	OTP Dump/load Data Buffer2A
0x3D4B	OTP_DATA_2B	0x00	RW	OTP Dump/load Data Buffer2B
0x3D4C	OTP_DATA_2C	0x00	RW	OTP Dump/load Data Buffer2C
0x3D4D	OTP_DATA_2D	0x00	RW	OTP Dump/load Data Buffer2D
0x3D4E	OTP_DATA_2E	0x00	RW	OTP Dump/load Data Buffer2E
0x3D4F	OTP_DATA_2F	0x00	RW	OTP Dump/load Data Buffer2F

table 7-5 OTP control (sheet 3 of 3)

address	register name	default value	R/W	description
0x3D50	OTP_DATA_30	0x00	RW	OTP Dump/load Data Buffer30
0x3D51	OTP_DATA_31	0x00	RW	OTP Dump/load Data Buffer31
0x3D52	OTP_DATA_32	0x00	RW	OTP Dump/load Data Buffer32
0x3D53	OTP_DATA_33	0x00	RW	OTP Dump/load Data Buffer33
0x3D54	OTP_DATA_34	0x00	RW	OTP Dump/load Data Buffer34
0x3D55	OTP_DATA_35	0x00	RW	OTP Dump/load Data Buffer35
0x3D56	OTP_DATA_36	0x00	RW	OTP Dump/load Data Buffer36
0x3D57	OTP_DATA_37	0x00	RW	OTP Dump/load Data Buffer37
0x3D58	OTP_DATA_38	0x00	RW	OTP Dump/load Data Buffer38
0x3D59	OTP_DATA_39	0x00	RW	OTP Dump/load Data Buffer39
0x3D5A	OTP_DATA_3A	0x00	RW	OTP Dump/load Data Buffer3A
0x3D5B	OTP_DATA_3B	0x00	RW	OTP Dump/load Data Buffer3B
0x3D5C	OTP_DATA_3C	0x00	RW	OTP Dump/load Data Buffer3C
0x3D5D	OTP_DATA_3D	0x00	RW	OTP Dump/load Data Buffer3D
0x3D5E	OTP_DATA_3E	0x00	RW	OTP Dump/load Data Buffer3E
0x3D5F	OTP_DATA_3F	0x00	RW	OTP Dump/load Data Buffer3F
0x3D10	OTP_MODE	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Bank select Bit[3:2]: Not used Bit[1:0]: opt_mode 00: OTP OFF 01: Load/dump OTP 10: Write/program OTP 11: OTP OFF
0x3D11	OTP_SPEED	0x46	RW	Bit[7]: Not used Bit[6:4]: write_speed Bit[3]: Not used Bit[2:0]: read_speed
0x3D1F	OTP_EF_STATUS	0x00	RW	Bit[7:1]: Not used Bit[0]: otp_busy

7.6 BLC functions [0x4000 - 0x5D30]

table 7-6 BLC control functions (sheet 1 of 9)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x01	RW	Bit[7:1]: Not used Bit[0]: BLC enable 0: Disable 1: Enable
0x4001	START LINE	0x04	RW	Bit[7:6]: Not used Bit[5:0]: start_line Start line for calculating normal offsets
0x4002	BLC CTRL02	0xC5	RW	Bit[7]: format_change_en 0: Change of format will not trigger BLC 1: Change of format will trigger BLC Bit[6]: offset_auto_en 0: Use the manual offsets 1: Use the calculated offsets Bit[5:0]: rest_frame_num Number indicates how many frames BLC will be updated continuously when the BLC is reset
0x4003	BLC CTRL03	0x08	RW	Bit[7]: trig_man BLC manual trigger signal, BLC will update manual_frame_num frames continuously from its rising edge Bit[6]: freeze_en When set, the BLC will freeze Bit[5:0]: manual_frame_num Number indicates how many frames BLC will be updated continuously when the trig_man is set
0x4004	LINE NUM	0x08	RW	Bit[7:6]: Not used Bit[5:0]: line_num Line number specifies the black lines used in offsets calculation

table 7-6 BLC control functions (sheet 2 of 9)

address	register name	default value	R/W	description
0x4005	BLC CTRL05	0x18	R/W	Bit[7:6]: Not used Bit[5]: one_line_mode When set, BLC offsets for B and Gr are the same. Gb and R offsets are the same Bit[4]: remove_black_line 0: Output image includes black lines 1: Output image does not include black lines Bit[3]: one_man_offset_mode When set and manual offsets enable is set, the manual offsets for B, Gb, Gr and R are same (the first manual offset) Bit[2]: bl_rblue_rvs When set, black lines' RBlue signal will be reversed Bit[1]: blc_always_do When set, BLC will always update Bit[0]: Not used
0x4006	NOT USED	–	–	Not Used
0x4007	BLC CTRL07	0x00	R/W	Bit[7:5]: Not used Bit[4:3]: hwin_sel 00: Horizontal size will be full size 01: Horizontal size will exclude the 16 left and 16 right pixels 10: Horizontal size will exclude the 1/16 left and 1/16 right window of full size 11: Horizontal size will exclude the 1/8 left and 1/8 right window of full size Bit[2]: sub128_en When set, output bypass data is subtracted by 128 Bit[1:0]: bypass_mode 00: Output limited input data 01: Output the 10 LSB input data 1x: Output the 10 MSB input data
0x4008	LONG BLC TARGET	0x10	R/W	Bit[7:0]: long_blc_target BLC target for long exposure data
0x4009	SHORT BLC TARGET	0x10	R/W	Bit[7:0]: short_blc_target BLC target for long exposure data
0x400A~ 0x400B	NOT USED	–	–	Not Used

table 7-6 BLC control functions (sheet 3 of 9)

address	register name	default value	R/W	description
0x400C	MANUAL OFFSET 00	0x00	R/W	Bit[7:1]: Not used Bit[0]: man_offset00[8] Manual offset for B channel of long exposure data
0x400D	MANUAL OFFSET 00	0x00	R/W	Bit[7:0]: man_offset00[7:0] Manual offset for B channel of long exposure data
0x400E	MANUAL OFFSET 01	0x00	R/W	Bit[7:1]: Not used Bit[0]: man_offset01[8] Manual offset for Gb channel of long exposure data
0x400F	MANUAL OFFSET 01	0x00	RW	Bit[7:0]: man_offset01[7:0] Manual offset for Gb channel of long exposure data
0x4010	MANUAL OFFSET 02	0x00	RW	Bit[7:1]: Not used Bit[0]: man_offset02[8] Manual offset for Gr channel of long exposure data
0x4011	MANUAL OFFSET 02	0x00	RW	Bit[7:0]: man_offset02[7:0] Manual offset for Gr channel of long exposure data
0x4012	MANUAL OFFSET 03	0x00	RW	Bit[7:1]: Not used Bit[0]: man_offset03[8] Manual offset for R channel of long exposure data
0x4013	MANUAL OFFSET 03	0x00	RW	Bit[7:0]: man_offset03[7:0] Manual offset for R channel of long exposure data
0x4014~ 0x4033	NOT USED	–	–	Not Used
0x4034	MANUAL OFFSET 10	0x00	RW	Bit[7:1]: Not used Bit[0]: man_offset10[8] Manual offset for B channel of short exposure data
0x4035	MANUAL OFFSET 10	0x00	RW	Bit[7:0]: man_offset10[7:0] Manual offset for B channel of short exposure data
0x4036	MANUAL OFFSET 11	0x00	RW	Bit[7:1]: Not used Bit[0]: man_offset11[8] Manual offset for Gb channel of short exposure data

table 7-6 BLC control functions (sheet 4 of 9)

address	register name	default value	R/W	description
0x4037	MANUAL OFFSET 11	0x00	RW	Bit[7:0]: man_offset11[7:0] Manual offset for Gb channel of short exposure data
0x4038	MANUAL OFFSET 12	0x00	RW	Bit[7:1]: Not used Bit[0]: man_offset12[8] Manual offset for Gr channel of short exposure data
0x4039	MANUAL OFFSET 12	0x00	RW	Bit[7:0]: man_offset12[7:0] Manual offset for Gr channel of short exposure data
0x403A	MANUAL OFFSET 13	0x00	RW	Bit[7:1]: Not used Bit[0]: man_offset13[8] Manual offset for R channel of short exposure data
0x403B	MANUAL OFFSET 13	0x00	RW	Bit[7:0]: man_offset13[7:0] Manual offset for R channel of short exposure data
0x403C~ 0x404B	NOT USED	–	–	Not Used
0x404C~ 0x404D	TOTAL BLACK LINE NUM	–	R	Debug Information for BLC Control Function
0x404E~ 0x404F	NOT USED	–	–	Not Used
0x4050	BLC AVG CTRL 1	0x20	RW	BLC Average Control 1
0x4051	BLC AVG CTRL 2	0x22	RW	BLC Average Control 2

table 7-6 BLC control functions (sheet 5 of 9)

address	register name	default value	R/W	description
0x4052	BLC CTRL52	0x00	RW	Bit[7:4]: BLC debug control Bit[3]: short_option 0: Short exposure channel will use BLC statistics of short exposure channel 1: Short exposure channel will use BLC statistics of long exposure channel Bit[2]: long_option 0: Long exposure channel will use BLC statistics of long exposure channel 1: Long exposure channel will use BLC statistics of short exposure channel Bit[1]: blc_mid_en 0: Keep the black line data 1: Median for black line data Bit[0]: one_channel When set, the used offsets will be average of calculated offsets for B,Gb,Gr and R channel
0x4053	BLC CTRL53	0x00	RW	Bit[7:0]: BLC debug control
0x4054	BLC CTRL54	0x00	RW	Bit[7:0]: BLC debug control
0x4055	BLC CTRL55	0xFF	RW	Bit[7]: BLC debug control Bit[6]: short_tmp_chg_en Short channel temperature changing enable signal Bit[5]: short_exp_chg_en Short channel exposure changing enable signal Bit[4]: short_gain_chg_en Short channel gain changing enable signal Bit[3]: long_ana_frz_en Long channel analog freeze enable signal Bit[2]: long_tmp_chg_en Long channel temperature changing enable signal Bit[1]: long_exp_chg_en long channel exposure changing enable signal Bit[0]: long_gain_chg_en Long channel gain changing enable signal

table 7-6 BLC control functions (sheet 6 of 9)

address	register name	default value	R/W	description
0x4056	OFFSET TOP LIMIT MSB	0x07	RW	BLC Control 1
0x4057	OFFSET TOP LIMIT LSB	0xFF	RW	BLC Control 2
0x4058	OFFSET BOT LIMIT MSB	0x01	RW	BLC Control 3
0x4059	OFFSET BOT LIMIT LSB	0xE0	RW	BLC Control 4
0x405A	BLC CTRL5A	0x70	RW	Bit[7]: Not used Bit[6:0]: BLC debug control
0x405B	BLC CTRL5B	0x00	RW	Bit[7:2]: Not used Bit[1:0]: BLC debug control
0xC4B7	AUTO_BLC_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: Auto black level cancelling 0: Disable 1: Enable
0xC4E0	BLC_TRIGGE_LIMIT	0x20	RW	BLC Adjustment Trigger Limitation
0xC4E1	BLC_STABLE_LIMIT	0x02	RW	BLC Adjustment Stable Limitation
0xC4E2	BLC_STEP	0x01	RW	Auto BLC Adjustment Relative Step
0xC4E3	BLC_PRE_SMOOTH_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Smooth offset statistics in first 16 frames 0: Disable 1: Enable
0xC4FA	BLC_HT_OPTION1_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: High temperature BLC option1 enable Increase stable and slow range Decrease adjustment step 0: Disable 1: Enable
0xC4FB	BLC_HT_OPTION2_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: High temperature BLC option2 enable Decrease maximum exposure lines 0: Disable 1: Enable

table 7-6 BLC control functions (sheet 7 of 9)

address	register name	default value	R/W	description
0xC4FC	BLC_HT_OPTION3_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: High temperature BLC option3 enable Switch analog gain to digital gain 0: Disable 1: Enable
0xC4FD	BLC_HT_TEMP_EXP_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: High temperature BLC temperature limits exposure when option2 is enabled 0: Disable 1: Enable
0xC4FE	BLC_HT_TEMP_MINEXP	0x04	RW	High Temperature BLC Min Exposure Lines Limited by temperature
0xC4FF	BLC_HT_EXPMAXSTEP	0x02	RW	High Temperature BLC Max Exposure Step
0xC500	BLC_HT_TEMP_TH_1L	0x50	RW	High Temperature BLC Temperature Threshold Long 1
0xC501	BLC_HT_TEMP_TH_1S	0x50	RW	High Temperature BLC Temperature Threshold Short 1
0xC502	BLC_HT_TEMP_TH_2L	0x64	RW	High Temperature BLC Temperature Threshold Long 2
0xC503	BLC_HT_TEMP_TH_2S	0x64	RW	High Temperature BLC Temperature Threshold Short 2
0xC504	BLC_HT_EXP_TH_11	0x01	RW	Bit[7:0]: High temperature BLC exposure threshold 1
0xC505	BLC_HT_EXP_TH_12	0xEC	RW	Bit[7:0]: High temperature BLC exposure threshold 1
0xC506	BLC_HT_EXP_TH_21	0x00	RW	Bit[7:0]: High temperature BLC Exposure Threshold 2
0xC507	BLC_HT_EXP_TH_22	0xC0	RW	Bit[7:0]: High temperature BLC Exposure Threshold 2
0xC508	BLC_HT_SA1_TH_11	0x01	RW	Bit[7:0]: High temperature BLC Threshold 1
0xC509	BLC_HT_SA1_TH_12	0xE0	RW	Bit[7:0]: High temperature BLC Threshold 1
0xC50A	BLC_HT_SA1_TH_21	0x01	RW	Bit[7:0]: High temperature BLC Threshold 2
0xC50B	BLC_HT_SA1_TH_22	0x2C	RW	Bit[7:0]: High temperature BLC Threshold 2
0xC50C	BLC_HT_SA1_TH_31	0x01	RW	Bit[7:0]: High temperature BLC Threshold 3
0xC50D	BLC_HT_SA1_TH_32	0x2C	RW	Bit[7:0]: High temperature BLC Threshold 3

table 7-6 BLC control functions (sheet 8 of 9)

address	register name	default value	R/W	description
0xC50E	BLC_HT_SA1_TH_41	0x00	RW	Bit[7:0]: High temperature BLC Threshold 4
0xC50F	BLC_HT_SA1_TH_42	0xC8	RW	Bit[7:0]: High temperature BLC Threshold 4
0x5B1C~ 0x5B49	BLC_R	–	R	Debug Information for BLC
0x5D1C	BLC_RW01	0x00	RW	Bit[7:3]: Not used Bit[2:0]: long_offset_00[10:8]
0x5D1D	BLC_RW02	0x00	RW	Bit[7:0]: long_offset_00[7:0]
0x5D1E	BLC_RW03	0x00	RW	Bit[7:3]: Not used Bit[2:0]: long_offset_01[10:8]
0x5D1F	BLC_RW04	0x00	RW	Bit[7:0]: long_offset_01[7:0]
0x5D20	BLC_RW05	0x00	RW	Bit[7:3]: Not used Bit[2:0]: long_offset_10[10:8]
0x5D21	BLC_RW06	0x00	RW	Bit[7:0]: long_offset_10[7:0]
0x5D22	BLC_RW07	0x00	RW	Bit[7:3]: Not used Bit[2:0]: long_offset_11[10:8]
0x5D23	BLC_RW08	0x00	RW	Bit[7:0]: long_offset_11[7:0]
0x5D24	BLC_RW09	0x00	RW	Bit[7:3]: Not used Bit[2:0]: short_offset_00[10:8]
0x5D25	BLC_RW10	0x00	RW	Bit[7:0]: short_offset_00[7:0]
0x5D26	BLC_RW11	0x00	RW	Bit[7:3]: Not used Bit[2:0]: short_offset_01[10:8]
0x5D27	BLC_RW12	0x00	RW	Bit[7:0]: short_offset_01[7:0]
0x5D28	BLC_RW13	0x00	RW	Bit[7:3]: Not used Bit[2:0]: short_offset_10[10:8]
0x5D29	BLC_RW14	0x00	RW	Bit[7:0]: short_offset_10[7:0]
0x5D2A	BLC_RW15	0x00	RW	Bit[7:3]: Not used Bit[2:0]: short_offset_11[10:8]
0x5D2B	BLC_RW16	0x00	RW	Bit[7:0]: short_offset_11[7:0]
0x5D2C	BLC_RW17	0x00	RW	Bit[7:4]: Not used Bit[3:0]: long_analog_offset_1
0x5D2D	BLC_RW18	0x00	RW	Bit[7:4]: Not used Bit[3:0]: short_analog_offset_1
0x5D2E	BLC_RW19	0x00	RW	Bit[7:2]: Not used Bit[1:0]: long_analog_offset_2

table 7-6 BLC control functions (sheet 9 of 9)

address	register name	default value	R/W	description
0x5D2F	BLC_RW20	0x00	RW	Bit[7:2]: Not used Bit[1:0]: short_analog_offset_2
0x5D30	BLC_RW21	0x00	RW	Bit[7]: short_ana_freeze Bit[6]: long_ana_freeze Bit[5]: short_tmp_chg Bit[4]: long_tmp_chg Bit[3]: short_exp_chg Bit[2]: long_exp_chg Bit[1]: short_gain_chg Bit[0]: long_gain_chg

7.7 AEC control [0x3503 - 0x5C17]

table 7-7 AEC control registers (sheet 1 of 20)

address	register name	default value	R/W	description
0x3503	AEC_PK_MANUAL	0x00	RW	Bit[7:6]: Not used Bit[5]: Gain delay option 0: One frame latch 1: Delay one frame latch Bit[4]: Choose delay option 0: Delay disable 1: Delay enable Bit[3:0]: Not used
0x3504	AEC_PK_MAN_DONE	0x00	RW	Bit[7:1]: Not used Bit[0]: AEC manual done
0x5600	AEC CTRL00	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Sampling 0x: 2 10: 4 11: 8
0x5601	AEC CTRL01	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Statwinleft[10:8] Horizontal start point for statistic image
0x5602	AEC CTRL02	0x00	RW	Bit[7:0]: Statwinleft[7:0] Horizontal start point for statistic image

table 7-7 AEC control registers (sheet 2 of 20)

address	register name	default value	R/W	description
0x5603	AEC CTRL03	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Statwintop[9:8] Vertical start point for statistic image
0x5604	AEC CTRL04	0x00	RW	Bit[7:0]: Statwintop[7:0] Vertical start point for statistic image
0x5605	AEC CTRL05	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Statwinright[10:8] Horizontal end point for statistic image
0x5606	AEC CTRL06	0x00	RW	Bit[7:0]: Statwinright[7:0] Horizontal end point for statistic image
0x5607	AEC CTRL07	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Statwinbottom[9:8] Vertical end point for statistic image
0x5608	AEC CTRL08	0x00	RW	Bit[7:0]: Statwinbottom[7:0] Vertical end point for statistic image
0x5609	AEC CTRL09	0x00	RW	Bit[7:3]: Not used Bit[2:0]: winleft_l[10:8] Horizontal start point to compute weight for long exposure sub-pixel
0x560A	AEC CTRL0A	0x64	RW	Bit[7:0]: winleft_l[7:0] Horizontal start point to calculate weight for long exposure sub-pixel
0x560B	AEC CTRL0B	0x00	RW	Bit[7:3]: Not used Bit[2:0]: winleft_s[10:8] Horizontal start point to calculate weight for short exposure sub-pixel
0x560C	AEC CTRL0C	0x64	RW	Bit[7:0]: winleft_s[7:0] Horizontal start point to calculate weight for short exposure sub-pixel

table 7-7 AEC control registers (sheet 3 of 20)

address	register name	default value	R/W	description
0x560D	AEC CTRL0D	0x00	RW	Bit[7:2]: Not used Bit[1:0]: wintop_l[9:8] Vertical start point to calculate weight for long exposure sub-pixel
0x560E	AEC CTRL0E	0x4B	RW	Bit[7:0]: wintop_l[7:0] Vertical start point to calculate weight for long exposure sub-pixel
0x560F	AEC CTRL0F	0x00	RW	Bit[7:2]: Not used Bit[1:0]: wintop_s[9:8] Vertical start point to calculate weight for short exposure sub-pixel
0x5610	AEC CTRL10	0x4B	RW	Bit[7:0]: wintop_s[7:0] Vertical start point to calculate weight for short exposure sub-pixel
0x5611	AEC CTRL11	0x00	RW	Bit[7:3]: Not used Bit[2:0]: winwidth_l[10:8] Horizontal width to calculate weight for long exposure sub-pixel
0x5612	AEC CTRL12	0xC8	RW	Bit[7:0]: winwidth_l[7:0] Horizontal width to calculate weight for long exposure sub-pixel
0x5613	AEC CTRL13	0x00	RW	Bit[7:3]: Not used Bit[2:0]: winwidth_s[10:8] Horizontal width to calculate weight for short exposure sub-pixel
0x5614	AEC CTRL14	0xC8	RW	Bit[7:0]: winwidth_s[7:0] Horizontal width to calculate weight for short exposure sub-pixel
0x5615	AEC CTRL15	0x00	RW	Bit[7:2]: Not used Bit[1:0]: winheight_l[9:8] Vertical width to calculate weight for long exposure sub-pixel
0x5616	AEC CTRL16	0x96	RW	Bit[7:0]: winheight_l[7:0] Vertical width to calculate weight for long exposure sub-pixel

table 7-7 AEC control registers (sheet 4 of 20)

address	register name	default value	R/W	description
0x5617	AEC CTRL17	0x00	RW	Bit[7:2]: Not used Bit[1:0]: winheight_s[9:8] Vertical width to calculate weight for long exposure sub-pixel
0x5618	AEC CTRL18	0x96	RW	Bit[7:0]: winheight_s[7:0] Vertical width to calculate weight for long exposure sub-pixel
0x5619	AEC CTRL19	0x00	RW	Bit[7:3]: Not used Bit[2:0]: roileft_l[10:8] Horizontal start point for ROI for long exposure sub-pixel
0x561A	AEC CTRL1A	0x00	RW	Bit[7:0]: roileft_l[7:0] Horizontal start point for ROI for long exposure sub-pixel
0x561B	AEC CTRL1B	0x00	RW	Bit[7:3]: Not used Bit[2:0]: roileft_s[10:8] Horizontal start point for ROI for short exposure sub-pixel
0x561C	AEC CTRL1C	0x00	RW	Bit[7:0]: roileft_s[7:0] Horizontal start point for ROI for short exposure sub-pixel
0x561D	AEC CTRL1D	0x00	RW	Bit[7:2]: Not used Bit[1:0]: roitop_l[9:8] Vertical start point for ROI for long exposure sub-pixel
0x561E	AEC CTRL1E	0x00	RW	Bit[7:0]: roitop_l[7:0] Vertical start point for ROI for long exposure sub-pixel
0x561F	AEC CTRL1F	0x00	RW	Bit[7:2]: Not used Bit[1:0]: roitop_s[9:8] Vertical start point for ROI for short exposure sub-pixel
0x5620	AEC CTRL20	0x00	RW	Bit[7:0]: roitop_s[7:0] Vertical start point for ROI for short exposure sub-pixel
0x5621	AEC CTRL21	0x00	RW	Bit[7:3]: Not used Bit[2:0]: roiright_l[10:8] Horizontal end point for ROI for long exposure sub-pixel
0x5622	AEC CTRL22	0x00	RW	Bit[7:0]: roiright_l[7:0] Horizontal end point for ROI for long exposure sub-pixel

table 7-7 AEC control registers (sheet 5 of 20)

address	register name	default value	R/W	description
0x5623	AEC CTRL23	0x00	RW	Bit[7:3]: Not used Bit[2:0]: roiright_s[10:8] Horizontal end point for ROI for short exposure sub-pixel
0x5624	AEC CTRL24	0x00	RW	Bit[7:0]: roiright_s[7:0] Horizontal end point for ROI for short exposure sub-pixel
0x5625	AEC CTRL25	0x00	RW	Bit[7:2]: Not used Bit[1:0]: roibottom_l[9:8] Vertical end point for ROI for long exposure sub-pixel
0x5626	AEC CTRL26	0x00	RW	Bit[7:0]: roibottom_l[7:0] Vertical end point for ROI for long exposure sub-pixel
0x5627	AEC CTRL27	0x00	RW	Bit[7:2]: Not used Bit[1:0]: roibottom_s[9:8] Vertical end point for ROI for short exposure sub-pixel
0x5628	AEC CTRL28	0x00	RW	Bit[7:0]: roibottom_s[7:0] Vertical end point for ROI for short exposure sub-pixel
0x5629	AEC CTRL29	0x00	RW	Bit[7:6]: Not used Bit[5:3]: r_roishift_l Bit[2:0]: r_roishift_s
0x562A	AEC CTRL2A	0x01	RW	ROIweightl0 for Long Exposure Sub-pixel
0x562B	AEC CTRL2B	0x01	RW	ROIweightl1 for Long Exposure Sub-pixel
0x562C	AEC CTRL2C	0x01	RW	ROIweights0 for Long Exposure Sub-pixel
0x562D	AEC CTRL2D	0x01	RW	ROIweights1 for Long Exposure Sub-pixel
0x562E	AEC CTRL2E	0x01	RW	Weightl0 for Long Exposure Sub-pixel
0x562F	AEC CTRL2F	0x01	RW	Weightl1 for Long Exposure Sub-pixel
0x5630	AEC CTRL30	0x01	RW	Weightl2 for Long Exposure Sub-pixel
0x5631	AEC CTRL31	0x01	RW	Weightl3 for Long Exposure Sub-pixel
0x5632	AEC CTRL32	0x01	RW	Weightl4 for Long Exposure Sub-pixel
0x5633	AEC CTRL33	0x01	RW	Weightl5 for Long Exposure Sub-pixel
0x5634	AEC CTRL34	0x01	RW	Weightl6 for Long Exposure Sub-pixel
0x5635	AEC CTRL35	0x01	RW	Weightl7 for Long Exposure Sub-pixel

table 7-7 AEC control registers (sheet 6 of 20)

address	register name	default value	R/W	description
0x5636	AEC CTRL36	0x01	RW	Weightl8 for Long Exposure Sub-pixel
0x5637	AEC CTRL37	0x01	RW	Weightl9 for Long Exposure Sub-pixel
0x5638	AEC CTRL38	0x01	RW	Weightla for Long Exposure Sub-pixel
0x5639	AEC CTRL39	0x01	RW	Weightlb for Long Exposure Sub-pixel
0x563A	AEC CTRL3A	0x01	RW	Weightlc for Long Exposure Sub-pixel
0x563B	AEC CTRL3B	0x01	RW	Weights0 for Short Exposure Sub-pixel
0x563C	AEC CTRL3C	0x01	RW	Weights1 for Short Exposure Sub-pixel
0x563D	AEC CTRL3D	0x01	RW	Weights2 for Short Exposure Sub-pixel
0x563E	AEC CTRL3E	0x01	RW	Weights3 for Short Exposure Sub-pixel
0x563F	AEC CTRL3F	0x01	RW	Weights4 for Short Exposure Sub-pixel
0x5640	AEC CTRL40	0x01	RW	Weights5 for Short Exposure Sub-pixel
0x5641	AEC CTRL41	0x01	RW	Weights6 for Short Exposure Sub-pixel
0x5642	AEC CTRL42	0x01	RW	Weights7 for Short Exposure Sub-pixel
0x5643	AEC CTRL43	0x01	RW	Weights8 for Short Exposure Sub-pixel
0x5644	AEC CTRL44	0x01	RW	Weights9 for Short Exposure Sub-pixel
0x5645	AEC CTRL45	0x01	RW	Weightsa for Short Exposure Sub-pixel
0x5646	AEC CTRL46	0x01	RW	Weightsb for Short Exposure Sub-pixel
0x5647	AEC CTRL47	0x01	RW	Weightsc for Short Exposure Sub-pixel
0x5648	AEC CTRL48	0x01	RW	Minwl for Long Exposure Sub-pixel
0x5649	AEC CTRL49	0x01	RW	Minws for Short Exposure Sub-pixel
0x564A	AEC CTRL4A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Maxwl[9:8] for long exposure sub-pixel
0x564B	AEC CTRL4B	0x20	RW	Bit[7:0]: Maxwl[7:0] for long exposure sub-pixel
0x564C	AEC CTRL4C	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Maxws[9:8] for short exposure sub-pixel
0x564D	AEC CTRL4D	0x00	RW	Bit[7:0]: Maxws[7:0] for short exposure sub-pixel
0x564E	AEC CTRL4E	0x00	RW	Poswshift

table 7-7 AEC control registers (sheet 7 of 20)

address	register name	default value	R/W	description
0x564F	AEC CTRL4F	0x04	RW	Lowlightthre
0x5650	AEC CTRL50	0xF0	RW	Highlightthre
0x5651	AEC CTRL51	0x01	RW	Bit[7]: Not used Bit[6:0]: Finalsaturatethre[14:8]
0x5652	AEC CTRL52	0x00	RW	Bit[7:0]: Finalsaturatethre[7:0]
0x5653	AEC CTRL53	0x04	RW	Bit[7:0]: r_blackthre1_l[15:8] for long exposure sub-pixel
0x5654	AEC CTRL54	0x00	RW	Bit[7:0]: r_blackthre1_l[7:0] for long exposure sub-pixel
0x5655	AEC CTRL55	0x10	RW	Bit[7:0]: r_blackthre1_s[15:8] for short exposure sub-pixel
0x5656	AEC CTRL56	0x00	RW	Bit[7:0]: r_blackthre1_s[7:0] for short exposure sub-pixel
0x5657	AEC CTRL57	0x20	RW	Bit[7:0]: r_blackthre2_l[15:8] for long exposure sub-pixel
0x5658	AEC CTRL58	0x00	RW	Bit[7:0]: r_blackthre2_l[7:0] for long exposure sub-pixel
0x5659	AEC CTRL59	0x40	RW	Bit[7:0]: r_blackthre2_s[15:8] for short exposure sub-pixel
0x565A	AEC CTRL5A	0x00	RW	Bit[7:0]: r_blackthre2_s[7:0] for short exposure sub-pixel
0x565B	AEC CTRL5B	0x10	RW	Bit[7]: Not used Bit[6:0]: r_blackweight1_l[6:0] for long exposure sub-pixel
0x565C	AEC CTRL5C	0x08	RW	Bit[7]: Not used Bit[6:0]: r_blackweight1_s[6:0] for short exposure sub-pixel
0x565D	AEC CTRL5D	0x14	RW	Bit[7]: Not used Bit[6:0]: r_blackweight2_l[6:0] for long exposure sub-pixel
0x565E	AEC CTRL5E	0x12	RW	Bit[7]: Not used Bit[6:0]: r_blackweight2_s[6:0] for short exposure sub-pixel
0x565F	AEC CTRL5F	0x08	RW	Bit[7:0]: r_saturatethre1_l[15:8] for long exposure sub-pixel
0x5660	AEC CTRL60	0x00	RW	Bit[7:0]: r_saturatethre1_l[7:0] for long exposure sub-pixel

table 7-7 AEC control registers (sheet 8 of 20)

address	register name	default value	R/W	description
0x5661	AEC CTRL61	0x04	RW	Bit[7:0]: r_saturatethre1_s[15:8] for short exposure sub-pixel
0x5662	AEC CTRL62	0x00	RW	Bit[7:0]: r_saturatethre1_s[7:0] for short exposure sub-pixel
0x5663	AEC CTRL63	0x10	RW	Bit[7:0]: r_saturatethre2_l[15:8] for long exposure sub-pixel
0x5664	AEC CTRL64	0x00	RW	Bit[7:0]: r_saturatethre2_l[7:0] for long exposure sub-pixel
0x5665	AEC CTRL65	0x20	RW	Bit[7:0]: r_saturatethre2_s[15:8] for short exposure sub-pixel
0x5666	AEC CTRL66	0x00	RW	Bit[7:0]: r_saturatethre2_s[7:0] for short exposure sub-pixel
0x5667	AEC CTRL67	0x10	RW	Bit[7]: Not used Bit[6:0]: r_saturateweight1_l[6:0] for long exposure sub-pixel
0x5668	AEC CTRL68	0x12	RW	Bit[7]: Not used Bit[6:0]: r_saturateweight1_s[6:0] for short exposure sub-pixel
0x5669	AEC CTRL69	0x12	RW	Bit[7]: Not used Bit[6:0]: r_saturateweight2_l[6:0] for long exposure sub-pixel
0x566A	AEC CTRL6A	0x14	RW	Bit[7]: Not used Bit[6:0]: r_saturateweight2_s[6:0] for short exposure sub-pixel
0x566B	AEC CTRL6B	0x00	RW	Bit[7]: fix_whole Bit[6]: fix_eof Bit[5:4]: fix_select 01: my_l 10: my_s 11: idat Bit[3:0]: fix_value
0x566C	AEC CTRL6C	0x00	RW	Bit[7:1]: Not used Bit[0]: r_his_en
0x566D	AEC CTRL6D	0x00	RW	r_his_addr
0x566E	AEC CTRL6E	–	R	Bit[7]: Not used Bit[6:0]: r_his_data[14:8]
0x566F	AEC CTRL6F	–	R	Bit[7:0]: r_his_data[7:0]
0x5680	AEC CTRL80	0x00	RW	Bit[7:1]: Not used Bit[0]: r_fixedratioenable

table 7-7 AEC control registers (sheet 9 of 20)

address	register name	default value	R/W	description
0x5681	AEC CTRL81	0x00	RW	Bit[7:3]: Not used Bit[2:0]: r_fixedratio[10:8]
0x5682	AEC CTRL82	0x07	RW	Bit[7:0]: r_fixedratio[7:0]
0x5683	AEC CTRL83	0x01	RW	Bit[7:0]: r_mintotalexp_l[15:8]
0x5684	AEC CTRL84	0x00	RW	Bit[7:0]: r_mintotalexp_l[7:0]
0x5685	AEC CTRL85	0x01	RW	Bit[7:0]: r_mintotalexp_s[15:8]
0x5686	AEC CTRL86	0x00	RW	Bit[7:0]: r_mintotalexp_s[7:0]
0x5687	AEC CTRL87	0x10	RW	Bit[7:0]: r_maxtotalexp_l[23:16]
0x5688	AEC CTRL88	0x20	RW	Bit[7:0]: r_maxtotalexp_l[15:8]
0x5689	AEC CTRL89	0x00	RW	Bit[7:0]: r_maxtotalexp_l[7:0]
0x568A	AEC CTRL8A	0x10	RW	Bit[7:0]: r_maxtotalexp_s[23:16]
0x568B	AEC CTRL8B	0x20	RW	Bit[7:0]: r_maxtotalexp_s[15:8]
0x568C	AEC CTRL8C	0x00	RW	Bit[7:0]: r_maxtotalexp_s[7:0]
0x568D	AEC CTRL8D	0x01	RW	Bit[7:1]: Not used Bit[0]: r_allowfractalexp
0x568E	AEC CTRL8E	0x04	RW	Bit[7:5]: Not used Bit[4:0]: r_minsaturatelevel
0x568F	AEC CTRL8F	0x04	RW	Bit[7:4]: Not used Bit[3:0]: r_wdrgainstep
0x5690	AEC CTRL90	0x88	RW	Bit[7:0]: r_logtargety[15:8]
0x5691	AEC CTRL91	0x00	RW	Bit[7:0]: r_logtargety[7:0]
0x5692	AEC CTRL92	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: r_gammastep
0x5693	AEC CTRL93	0x20	RW	Bit[7]: Not used Bit[6:0]: r_exprationstep
0x5694	AEC CTRL94	0x00	RW	Bit[7:3]: Not used Bit[2:0]: r_minration[10:8]
0x5695	AEC CTRL95	0x02	RW	Bit[7:0]: r_minration[7:0]
0x5696	AEC CTRL96	0x00	RW	Bit[7:3]: Not used Bit[2:0]: r_maxration[10:8]
0x5697	AEC CTRL97	0x80	RW	Bit[7:0]: r_maxration[7:0]
0x5698	AEC CTRL98	0x50	RW	Bit[7:0]: r_targety_l

table 7-7 AEC control registers (sheet 10 of 20)

address	register name	default value	R/W	description
0x5699	AEC CTRL99	0x60	RW	Bit[7:0]: r_targety_s
0x569A	AEC CTRL9A	0x20	RW	Bit[7]: Not used Bit[6:0]: r_weightthre1_l
0x569B	AEC CTRL9B	0x20	RW	Bit[7]: Not used Bit[6:0]: r_weightthre1_s
0x569C	AEC CTRL9C	0x60	RW	Bit[7]: Not used Bit[6:0]: r_weightthre2_l
0x569D	AEC CTRL9D	0x60	RW	Bit[7]: Not used Bit[6:0]: r_weightthre2_s
0x569E	AEC CTRL9E	0x20	RW	Bit[7]: Not used Bit[6:0]: r_slowrange_l
0x569F	AEC CTRL9F	0x20	RW	Bit[7]: Not used Bit[6:0]: r_slowrange_s
0x56A0	AEC CTRLA0	0x08	RW	Bit[7:6]: Not used Bit[5:0]: r_stablerange_l
0x56A1	AEC CTRLA1	0x08	RW	Bit[7:6]: Not used Bit[5:0]: r_stablerange_s
0x56A2	AEC CTRLA2	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: r_faststep_l
0x56A3	AEC CTRLA3	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: r_faststep_s
0x56A4	AEC CTRLA4	0x06	RW	Bit[7:5]: Not used Bit[4:0]: r_slowstep_l
0x56A5	AEC CTRLA5	0x06	RW	Bit[7:5]: Not used Bit[4:0]: r_slowstep_s
0x56A6	AEC CTRLA6	0x01	RW	Bit[7:2]: Not used Bit[1:0]: r_maxfastratio[9:8]
0x56A7	AEC CTRLA7	0x00	RW	Bit[7:0]: r_maxfastratio[7:0]
0x56A8	AEC CTRLA8	0x00	RW	Bit[7:2]: Not used Bit[1:0]: r_maxslowratio[9:8]
0x56A9	AEC CTRLA9	0x02	RW	Bit[7:0]: r_maxslowratio[7:0]
0x56AA	AEC CTRLAA	0x02	RW	Bit[7:4]: Not used Bit[3:0]: r_mingammalist0[11:8]
0x56AB	AEC CTRLAB	0x00	RW	Bit[7:0]: r_mingammalist0[7:0]
0x56AC	AEC CTRLAC	0x02	RW	Bit[7:4]: Not used Bit[3:0]: r_mingammalist1[11:8]

table 7-7 AEC control registers (sheet 11 of 20)

address	register name	default value	R/W	description
0x56AD	AEC CTRLAD	0x00	RW	Bit[7:0]: r_mingammalist1[7:0]
0x56AE	AEC CTRLAE	0x02	RW	Bit[7:4]: Not used Bit[3:0]: r_mingammalist2[11:8]
0x56AF	AEC CTRLAF	0x00	RW	Bit[7:0]: r_mingammalist2[7:0]
0x56B0	AEC CTRLB0	0x02	RW	Bit[7:4]: Not used Bit[3:0]: r_maxgammalist0[11:8]
0x56B1	AEC CTRLB1	0x60	RW	Bit[7:0]: r_maxgammalist0[7:0]
0x56B2	AEC CTRLB2	0x04	RW	Bit[7:4]: Not used Bit[3:0]: r_maxgammalist1[11:8]
0x56B3	AEC CTRLB3	0x00	RW	Bit[7:0]: r_maxgammalist1[7:0]
0x56B4	AEC CTRLB4	0x06	RW	Bit[7:4]: Not used Bit[3:0]: r_maxgammalist2[11:8]
0x56B5	AEC CTRLB5	0x00	RW	Bit[7:0]: r_maxgammalist2[7:0]
0x56B6	AEC CTRLB6	0x00	RW	Bit[7]: Not used Bit[6:0]: r_dynamicrangelist0[14:8]
0x56B7	AEC CTRLB7	0x10	RW	Bit[7:0]: r_dynamicrangelist0[7:0]
0x56B8	AEC CTRLB8	0x00	RW	Bit[7]: Not used Bit[6:0]: r_dynamicrangelist1[14:8]
0x56B9	AEC CTRLB9	0x80	RW	Bit[7:0]: r_dynamicrangelist1[7:0]
0x56BA	AEC CTRLBA	0x02	RW	Bit[7]: Not used Bit[6:0]: r_dynamicrangelist2[14:8]
0x56BB	AEC CTRLBB	0x00	RW	Bit[7:0]: r_dynamicrangelist2[7:0]
0x56BC	AEC CTRLBC	0x01	RW	Bit[7:1]: Not used Bit[0]: r_holdingbandenable
0x56BD	AEC CTRLBD	0x00	RW	Bit[7:2]: Not used Bit[1:0]: r_bandingfilterflag
0x56BE	AEC CTRLBE	0x01	RW	Bit[7:1]: Not used Bit[0]: r_bandingfilterenable
0x56BF	AEC CTRLBF	0x01	RW	Bit[7:1]: Not used Bit[0]: r_bandingfiltershortenable
0x56C0	AEC CTRLC0	0x01	RW	Bit[7:1]: Not used Bit[0]: r_lessthan1bandenable
0x56C1	AEC CTRLC1	0x00	RW	Bit[7:1]: Not used Bit[0]: r_lessthan1bandshortenable
0x56C2	AEC CTRLC2	0x03	RW	Bit[7:0]: r_hpixel[15:8]

table 7-7 AEC control registers (sheet 12 of 20)

address	register name	default value	R/W	description
0x56C3	AEC CTRLC3	0xC8	RW	Bit[7:0]: r_hpixel[7:0]
0x56C4	AEC CTRLC4	0x02	RW	Bit[7:0]: r_vpixel[15:8]
0x56C5	AEC CTRLC5	0x04	RW	Bit[7:0]: r_vpixel[7:0]
0x56C6	AEC CTRLC6	0x0F	RW	Bit[7:0]: r_targetlowfr
0x56C7	AEC CTRLC7	0x14	RW	Bit[7:0]: r_targethighfr
0x56D0	AEC CTRLD0	0x00	RW	Bit[7:3]: Not used Bit[2:0]: r_man_en
0x56D1	AEC CTRLD1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: r_cameragain_l_m[9:8]
0x56D2	AEC CTRLD2	0x10	RW	Bit[7:0]: r_cameragain_l_m[7:0]
0x56D3	AEC CTRLD3	0x00	RW	Bit[7:2]: Not used Bit[1:0]: r_cameragain_s_m[9:8]
0x56D4	AEC CTRLD4	0x10	RW	Bit[7:0]: r_cameragain_s_m[7:0]
0x56D5	AEC CTRLD5	0x00	RW	Bit[7:0]: r_exp_l_m[31:24]
0x56D6	AEC CTRLD6	0x00	RW	Bit[7:0]: r_exp_l_m[23:16]
0x56D7	AEC CTRLD7	0x00	RW	Bit[7:0]: r_exp_l_m[15:8]
0x56D8	AEC CTRLD8	0x00	RW	Bit[7:0]: r_exp_l_m[7:0]
0x56D9	AEC CTRLD9	0x00	RW	Bit[7:0]: r_exp_s_m[31:24]
0x56DA	AEC CTRLDA	0x00	RW	Bit[7:0]: r_exp_s_m[23:16]
0x56DB	AEC CTRLDB	0x00	RW	Bit[7:0]: r_exp_s_m[15:8]
0x56DC	AEC CTRLDC	0x00	RW	Bit[7:0]: r_exp_s_m[7:0]
0x56DF	AEC CTRLDF	0x02	RW	Bit[7:3]: Not used Bit[2:0]: r_digigain_l_m[10:8]
0x56E0	AEC CTRLE0	0x00	RW	Bit[7:0]: r_digigain_l_m[7:0]
0x56E1	AEC CTRLE1	0x02	RW	Bit[7:3]: Not used Bit[2:0]: r_digigain_s_m[10:8]
0x56E2	AEC CTRLE2	0x00	RW	Bit[7:0]: r_digigain_s_m[7:0]
0x56E3	AEC CTRLE3	0x00	RW	Bit[7:1]: Not used Bit[0]: r_exp_ctrl
0x56E4	AEC CTRLE4	0x00	RW	Bit[7:4]: Not used Bit[3:0]: r_exp_l_f[11:8]
0x56E5	AEC CTRLE5	0x00	RW	Bit[7:0]: r_exp_l_f[7:0]

table 7-7 AEC control registers (sheet 13 of 20)

address	register name	default value	R/W	description
0x56E6	AEC CTRLE6	0x00	RW	Bit[7:4]: Not used Bit[3:0]: r_exp_s_f[11:8]
0x56E7	AEC CTRLE7	0x00	RW	Bit[7:0]: r_exp_s_f[7:0]
0x56E8	AEC CTRLE8	0x00	RW	Bit[7:1]: Not used Bit[0]: r_snrgain_l_m[8]
0x56E9	AEC CTRLE9	0x00	RW	Bit[7:0]: r_snrgain_l_m[7:0]
0x56EA	AEC CTRLEA	0x00	RW	Bit[7:1]: Not used Bit[0]: r_snrgain_s_m[8]
0x56EB	AEC CTRLEB	0x00	RW	Bit[7:0]: r_snrgain_s_m[7:0]
0xC2F0	S_MANUAL_EXP11	0x34	RW	Bit[7:0]: manual_expo11[15:8]
0xC2F1	S_MANUAL_EXP11	0x00	RW	Bit[7:0]: manual_expo11[7:0]
0xC2F2	S_MANUAL_EXP12	0x06	RW	Bit[7:0]: manual_expo12[15:8]
0xC2F3	S_MANUAL_EXP12	0x80	RW	Bit[7:0]: manual_expo12[7:0]
0xC2F4	S_MANUAL_EXP21	0x34	RW	Bit[7:0]: manual_expo21[15:8]
0xC2F5	S_MANUAL_EXP21	0x00	RW	Bit[7:0]: manual_expo21[7:0]
0xC2F6	S_MANUAL_EXP22	0x06	RW	Bit[7:0]: manual_expo22[15:8]
0xC2F7	S_MANUAL_EXP22	0x80	RW	Bit[7:0]: manual_expo22[7:0]
0xC2F8	S_MANUAL_EXP31	0x34	RW	Bit[7:0]: manual_expo31[15:8]
0xC2F9	S_MANUAL_EXP31	0x00	RW	Bit[7:0]: manual_expo31[7:0]
0xC2FA	S_MANUAL_EXP32	0x06	RW	Bit[7:0]: manual_expo32[15:0]
0xC2FB	S_MANUAL_EXP22	0x80	RW	Bit[7:0]: manual_expo32[7:0]
0xC2FC	S_MANUAL_GAIN11	0x10	RW	Bit[7:0]: manual_gain11[15:8]
0xC2FD	S_MANUAL_GAIN11	0x18	RW	Bit[7:0]: manual_gain11[7:0]
0xC2FE	S_MANUAL_GAIN12	0x10	RW	Bit[7:0]: manual_gain12[15:8]
0xC2FF	S_MANUAL_GAIN12	0x18	RW	Bit[7:0]: manual_gain12[7:0]
0xC300	S_MANUAL_GAIN21	0x10	RW	Bit[7:0]: manual_gain21[15:8]
0xC301	S_MANUAL_GAIN21	0x18	RW	Bit[7:0]: manual_gain21[7:0]
0xC302	S_MANUAL_GAIN22	0x10	RW	Bit[7:0]: manual_gain22[15:8]
0xC303	S_MANUAL_GAIN22	0x18	RW	Bit[7:0]: manual_gain22[7:0]
0xC304	S_MANUAL_GAIN31	0x10	RW	Bit[7:0]: manual_gain31[15:8]

table 7-7 AEC control registers (sheet 14 of 20)

address	register name	default value	R/W	description
0xC305	S_MANUAL_GAIN31	0x18	RW	Bit[7:0]: manual_gain31[7:0]
0xC306	S_MANUAL_GAIN32	0x10	RW	Bit[7:0]: manual_gain32[15:8]
0xC307	S_MANUAL_GAIN32	0x18	RW	Bit[7:0]: manual_gain32[7:0]
0xC308	S_MANUAL_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: manual_en 0: Disable 1: Enable
0xC309	S_MANUAL_MODE	0x00	RW	Bit[7:3]: Not used Bit[2]: targetc_manual_en 0: Disable 1: Enable Bit[1]: targetb_manual_en 0: Disable 1: Enable Bit[0]: targeta_manual_en 0: Disable 1: Enable
0xC30A	S_MANUAL_DONE	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_done 00: Write protected 01: Write valid once 10: Write valid always
0xC450	TARGET_NUM	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Target number 01: AA mode 10: AB mode 11: ABC mode
0xC451	HW_STOP_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: HW stop frame enable (for AB/ABC mode, blanking time is not enough) 0: Duplicate setting for next frame 1: Stop next frame
0xC452	LS_SENS_RATIO_1	0x04	RW	Bit[7:0]: L/S sensitivity ratio[15:8]
0xC453	LS_SENS_RATIO_2	0x00	RW	Bit[7:0]: L/S sensitivity ratio[7:0]
0xC454	NONWDR_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Non-WDR mode 0: Disable 1: Enable

table 7-7 AEC control registers (sheet 15 of 20)

address	register name	default value	R/W	description
0xC455	SINGLE_EXP_MODE_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Non-WDR mode switch to combine long mode when being stabled 0: Disable 1: Enable
0xC456	FIXED_RATIO_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Fixed ratio mode 0: Disable 1: Enable
0xC457	GP_MODE_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Geometric proportion mode 0: Disable 1: Enable
0xC458	NIGHT_MODE_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Night mode 0: Disable 1: Enable
0xC459	NIGHT_MODE_CTRL	0x00	RW	Bit[7:1]: Not used Bit[0]: Only insert frame when in night mode 0: Disable 1: Enable
0xC45A	FRACTAL_EXP_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: Allow fractal exposure 0: Disable 1: Enable
0xC45B	NONLINEAR_GAIN_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: Non linear gain mode 0: Disable 1: Enable
0xC45C	MANU_GAMMA_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Manual gamma mode 0: Disable 1: Enable
0xC45D	HOLD_BAND_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Hold band mode 0: Disable 1: Enable

table 7-7 AEC control registers (sheet 16 of 20)

address	register name	default value	R/W	description
0xC45E	BAND_FILTER_FLAG	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Light source type 00: Frequency is zero or very high 01: 60Hz 10: 50Hz 11: Not valid
0xC45F	BAND_FILTER_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: Banding filter 0: Disable 1: Enable
0xC460	BAND_FILTER_SHORT	0x00	RW	Bit[7:1]: Not used Bit[0]: Short banding filter 0: Disable 1: Enable
0xC461	LESS_1BAND_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: Less than one band exposure mode 0: Disable 1: Enable
0xC462	LESS_1BAND_SHORT	0x01	RW	Bit[7:1]: Not used Bit[0]: Less than one band exposure for short 0: Disable 1: Enable
0xC463	WDR_GAIN_LIMIT_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: WDR gain limitation enable 0: Disable 1: Enable
0xC464	LOG_TARGET_11	0x88	RW	Bit[7:0]: Log target 1[15:8]
0xC465	LOG_TARGET_12	0x00	RW	Bit[7:0]: Log target 1[7:0]
0xC466	LOG_TARGET_21	0x8A	RW	Bit[7:0]: Log target 2[15:8]
0xC467	LOG_TARGET_22	0x00	RW	Bit[7:0]: Log target 2[7:0]
0xC468	LOG_TARGET_31	0x86	RW	Bit[7:0]: Log target 3[15:8]
0xC469	LOG_TARGET_32	0x00	RW	Bit[7:0]: Log target 3[7:0]
0xC46A	TARGET_LONG_1	0x40	RW	Target of Raw Data for Long 1
0xC46B	TARGET_LONG_2	0x50	RW	Target of Raw Data for Long 2
0xC46C	TARGET_LONG_3	0x30	RW	Target of Raw Data for Long 3
0xC46D	TARGET_SHORT_1	0x50	RW	Target of Raw Data for Short 1

table 7-7 AEC control registers (sheet 17 of 20)

address	register name	default value	R/W	description
0xC46E	TARGET_SHORT _2	0x60	RW	Target of Raw Data for Short 2
0xC46F	TARGET_SHORT _3	0x40	RW	Target of Raw Data for Short 3
0xC470	SLOW_RANGE_LONG	0x20	RW	Slow Range for Long Exposure
0xC471	SLOW_RANGE_SHORT	0x20	RW	Slow Range for Short Exposure
0xC472	STABLE_RANGE_IN	0x04	RW	Range Become Stable from Unstable
0xC473	STABLE_RANGE_OUT	0x08	RW	Range Become Unstable from Stable
0xC474	FAST_STEP_LONG	0x0A	RW	Fast AEC Adjustment Step for Long Exposure
0xC475	FAST_STEP_SHORT	0x0A	RW	Fast AEC Adjustment Step for Short Exposure
0xC476	SLOW_STEP_LONG	0x08	RW	Slow AEC Adjustment Step for Long Exposure
0xC477	SLOW_STEP_SHORT	0x08	RW	Slow AEC Adjustment Step for Short Exposure
0xC478	MAX_FAST_RATIO	0x40	RW	Max Fast Adjustment Ratio
0xC479	MAX_SLOW_RATIO	0x02	RW	Max Slow Adjustment Ratio
0xC47A	MAX_FRACTAL_EXP	0x0B	RW	Max Fractal Exposure (X/16)
0xC47B	MIN_FRACTAL_EXP	0x04	RW	Min Fractal Exposure (X/16)
0xC47C	MAX_SHORT_LE_1	0x34	RW	Bit[7:0]: Max short light exposure[31:24]
0xC47D	MAX_SHORT_LE_2	0x80	RW	Bit[7:0]: Max short light exposure[23:16]
0xC47E	MAX_SHORT_LE_3	0x00	RW	Bit[7:0]: Max short light exposure[15:8]
0xC47F	MAX_SHORT_LE_4	0x00	RW	Bit[7:0]: Max short light exposure[7:0]
0xC480	MAX _GAIN_LONG_1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Max gain for long[9:8]
0xC481	MAX _GAIN_LONG_2	0x80	RW	Bit[7:0]: Max gain for long[7:0]
0xC482	MAX_GAIN_SHORT_1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Max gain for short[9:8]
0xC483	MAX_GAIN_SHORT_1	0x80	RW	Bit[7:0]: Max gain for short[7:0]
0xC484	MIN_ GAIN_LONG_1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Min gain for long[9:8]
0xC485	MIN_ GAIN_LONG_2	0x10	RW	Bit[7:0]: Min gain for long[7:0]
0xC486	MIN_GAIN_SHORT_1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Min gain for short[9:8]
0xC487	MIN_GAIN_SHORT_2	0x10	RW	Bit[7:0]: Min gain for short[7:0]

table 7-7 AEC control registers (sheet 18 of 20)

address	register name	default value	R/W	description
0xC488	MAX_EXP_LONG_1	0x34	RW	Bit[7:0]: Max exposure for long[15:8]
0xC489	MAX_EXP_LONG_2	0x00	RW	Bit[7:0]: Max exposure for long[7:0]
0xC48A	MAX_EXP_SHORT_1	0x34	RW	Bit[7:0]: Max exposure for short[15:8]
0xC48B	MAX_EXP_SHORT_2	0x00	RW	Bit[7:0]: Max exposure for short[7:0]
0xC48C	MIN_EXP_LONG_1	0x00	RW	Bit[7:0]: Min exposure for long[15:8]
0xC48D	MIN_EXP_LONG_2	0x04	RW	Bit[7:0]: Min exposure for long[7:0]
0xC48E	MIN_EXP_SHORT_1	0x00	RW	Bit[7:0]: Min exposure for short[15:8]
0xC48F	MIN_EXP_ SHORT_2	0x04	RW	Bit[7:0]: Min exposure for short[7:0]
0xC490	FIXED_RATIO	0x01	RW	Fixed Ratio, Value+1
0xC491	NIGHT_MODE_STEP	0x0C	RW	AEC Adjustment Step in Night Mode
0xC492	GP_MODE_RATIO_B2A	0x20	RW	B/A Ratio in Gp Mode
0xC493	GP_MODE_RATIO_C2A	0x08	RW	C/A Ratio in Gp Mode
0xC494	WDR_GAIN_STEP	0x04	RW	WDR Gain Adjustment Step
0xC495	EXP_RATIO_STEP	0x20	RW	L/S Ratio Change Step
0xC496	GAMMA_STEP	0x04	RW	Gamma Adjustment Step
0xC497	MIN_SATU_LEVEL	0x08	RW	Min Saturate Level for Short
0xC498	MIN_GAMMA_LIST_11	0x02	RW	Bit[7:0]: Min gamma list 1[15:8]
0xC499	MIN_GAMMA_LIST_12	0x00	RW	Bit[7:0]: Min gamma list 1[7:0]
0xC49A	MIN_GAMMA_LIST_21	0x02	RW	Bit[7:0]: Min gamma list 2[15:8]
0xC49B	MIN_GAMMA_LIST_22	0x00	RW	Bit[7:0]: Min gamma list 2[7:0]
0xC49C	MIN_GAMMA_LIST_31	0x02	RW	Bit[7:0]: Min gamma list 3[15:8]
0xC49D	MIN_GAMMA_LIST_32	0x00	RW	Bit[7:0]: Min gamma list 3[7:0]
0xC49E	MAX_GAMMA_LIST_11	0x02	RW	Bit[7:0]: Max gamma list 1[15:8]
0xC49F	MAX_GAMMA_LIST_12	0x60	RW	Bit[7:0]: Max gamma list 1[7:0]
0xC4A0	MAX_GAMMA_LIST_21	0x04	RW	Bit[7:0]: Max gamma list 2[15:8]
0xC4A1	MAX_GAMMA_LIST_22	0x00	RW	Bit[7:0]: Max gamma list 2[7:0]
0xC4A2	MAX_GAMMA_LIST_31	0x05	RW	Bit[7:0]: Max gamma list 3[15:8]
0xC4A3	MAX_GAMMA_LIST_32	0x00	RW	Bit[7:0]: Max gamma list 3[7:0]

table 7-7 AEC control registers (sheet 19 of 20)

address	register name	default value	R/W	description
0xC4A4	DR_LIST_11	0x00	RW	Bit[7:0]: Dynamic range list 1[15:8]
0xC4A5	DR_LIST_12	0x10	RW	Bit[7:0]: Dynamic range list 1[7:0]
0xC4A6	DR_LIST_21	0x00	RW	Bit[7:0]: Dynamic range list 2[15:8]
0xC4A7	DR_LIST_22	0x80	RW	Bit[7:0]: Dynamic range list 2[7:0]
0xC4A8	DR_LIST_31	0x02	RW	Bit[7:0]: Dynamic range list 3[15:8]
0xC4A9	DR_LIST_32	0x00	RW	Bit[7:0]: Dynamic range list 3[7:0]
0xC4AA	BAND_VALUE_60HZ_1	0x0D	RW	Bit[7:0]: Band filter value for 60Hz[15:8]
0xC4AB	BAND_VALUE_60HZ_2	0x20	RW	Bit[7:0]: Band filter value for 60Hz[7:0]
0xC4AC	BAND_VALUE_50HZ_1	0x0F	RW	Bit[7:0]: Band filter value for 50Hz[15:8]
0xC4AD	BAND_VALUE_50HZ_2	0xC0	RW	Bit[7:0]: Band filter value for 50Hz[7:0]
0xC4AE	LINEAR_EXP_START_1	0x00	RW	Bit[7:0]: Linear exposure start point[15:8]
0xC4AF	LINEAR_EXP_START_2	0x80	RW	Bit[7:0]: Linear exposure start point[7:0]
0xC4B0	PRE_CHARGE_WIDTH	0x08	RW	Pixel Timing Control
0xC4B1	MIN_DR_RATIO	0x02	RW	Min Dynamic Ratio
0xC4B2	MAX_DR_RATIO_1	0x01	RW	Bit[7:0]: Max dynamic ratio[15:8]
0xC4B3	MAX_DR_RATIO_2	0x00	RW	Bit[7:0]: Max dynamic ratio[7:0]
0xC514	SENSOR_CLK_RATIO_1	0x04	RW	Bit[7:0]: Sensor clock ratio[15:8]
0xC515	SENSOR_CLK_RATIO_2	0x00	RW	Bit[7:0]: Sensor clock ratio[7:0]
0xC516	NON_WDR_STEP	0x08	RW	Non-WDR Ratio Adjustment Step
0xC518	VTS_ADDR_1	0x03	RW	Bit[7:0]: VTS[15:8]
0xC519	VTS_ADDR_2	0x48	RW	Bit[7:0]: VTS[7:0]
0xC51A	HTS_ADDR_1	0x07	RW	Bit[7:0]: HTS[15:8]
0xC51B	HTS_ADDR_2	0x70	RW	Bit[7:0]: HTS[7:0]
0x5A00~ 0x5A03	AEC_R	–	R	Debug Information for AEC control
0x5C00	AEC_RW00	0x00	RW	Bit[7:0]: Exposure long[31:24]
0x5C01	AEC_RW01	0x00	RW	Bit[7:0]: Exposure long[23:16]
0x5C02	AEC_RW02	0x00	RW	Bit[7:0]: Exposure long[15:8]
0x5C03	AEC_RW03	0x00	RW	Bit[7:0]: Exposure long[7:0]

table 7-7 AEC control registers (sheet 20 of 20)

address	register name	default value	R/W	description
0x5C04	AEC_RW04	0x00	RW	Bit[7:0]: Exposure short[31:24]
0x5C05	AEC_RW05	0x00	RW	Bit[7:0]: Exposure short[23:16]
0x5C06	AEC_RW06	0x00	RW	Bit[7:0]: Exposure short[15:8]
0x5C07	AEC_RW07	0x00	RW	Bit[7:0]: Exposure short[7:0]
0x5C08	AEC_RW08	0x00	RW	Bit[7:0]: add_vts[15:8]
0x5C09	AEC_RW09	0x00	RW	Bit[7:0]: add_vts[7:0]
0x5C0A	AEC_RW0A	0x00	RW	Bit[7:3]: Not used Bit[2]: evenframeflag Bit[1:0]: targettag[1:0]
0x5C0C	AEC_RW0C	0x00	RW	Bit[7:1]: Not used Bit[0]: Snrgain long[8]
0x5C0D	AEC_RW0D	0x00	RW	Bit[7:0]: Snrgain long[7:0]
0x5C0E	AEC_RW0E	0x00	RW	Bit[7:1]: Not used Bit[0]: Snrgain short[8]
0x5C0F	AEC_RW0F	0x00	RW	Bit[7:0]: Snrgain short[7:0]
0x5C10	AEC_RW10	0x00	RW	Bit[7:2]: Not used Bit[1:0]: PcameraGain long[9:8]
0x5C11	AEC_RW11	0x00	RW	Bit[7:0]: PcameraGain long[7:0]
0x5C12	AEC_RW12	0x00	RW	Bit[7:2]: Not used Bit[1:0]: PcameraGain short[9:8]
0x5C13	AEC_RW13	0x00	RW	Bit[7:0]: PcameraGain short[7:0]
0x5C14	AEC_RW14	0x00	RW	Bit[7:2]: Not used Bit[1:0]: PdigiGain long[9:8]
0x5C15	AEC_RW15	0x00	RW	Bit[7:0]: PdigiGain long[7:0]
0x5C16	AEC_RW16	0x00	RW	Bit[7:2]: Not used Bit[1:0]: PdigiGain short[9:8]
0x5C17	AEC_RW17	0x00	RW	Bit[7:0]: PdigiGain short[7:0]

7.8 ISP control [0x5000 - 0x5044]

table 7-8 ISP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP RW00	0xFF	RW	Bit[7]: Color matrix enable Bit[6]: Color interpolation enable Bit[5]: Denoise enable Bit[4]: White defect pixel correction enable Bit[3]: Black defect pixel correction enable Bit[2]: AWB statistic enable Bit[1]: AWB gain enable Bit[0]: Lens shading correction enable
0x5001	ISP RW01	0xBF	RW	Bit[7]: Data and its weight synchronization enable Bit[6]: Black/white mode enable Bit[5]: Dark level filter enable Bit[4]: Buffer control enable Bit[3]: AEC enable Bit[2]: Tone mapping enable Bit[1]: Normalize enable Bit[0]: Long-short combination enable
0x5002	ISP RW02	0x7E	RW	Bit[7]: OTP manual offset enable Bit[6]: OTP function enable Bit[5]: ALU function enable Bit[4]: CT AWB function enable Bit[3]: Digital gain enable Bit[2]: Window border cut enable Bit[1]: Dithering enable Bit[0]: Internal long/short sequence 0: LSLS 1: SLSL
0x5003	ISP RW03	0x04	RW	Bit[7:5]: Not used Bit[4]: YUV444to422_drop Bit[3]: Latch_sel 0: Pre_sof 1: VSYNC Bit[2:0]: EOF_sel 000: AEC_done 001: Simple_awb_done 010: Tone_mapping_done 011: Combine_done 100: AEC_done and simple_AWB_done and tone_mapping_done and combine_done

table 7-8 ISP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5004	ISP RW04	0x14	RW	Bit[7:5]: Not used Bit[4]: Auto window enable 0: Manually set image window for DSP blocks 1: Automatically handle image window Bit[3:0]: Dummy line number for ISP
0x5005	ISP RW05	0x08	RW	Bit[7]: vap_v_sel Bit[6]: lenc_offset_man_en Bit[5]: vap_second_line Bit[4]: vap_second_pix Bit[3]: vap_mean Bit[2:1]: vap_drop Bit[0]: vap_en
0x5006	ISP RW06	0x00	RW	Bit[7:6]: raw_mode_man Bit[5:4]: yuv_mode_man Bit[3]: raw_mode_man_en Bit[2]: yuv_mode_man_en Bit[1:0]: Reserved
0x5007	ISP RW07	0x00	RW	Bit[7:3]: Not used Bit[2:0]: isp_x_offset[10:8]
0x5008	ISP RW08	0x00	RW	Bit[7:0]: isp_x_offset[7:0]
0x5009	ISP RW09	0x00	RW	Bit[7:2]: Not used Bit[1:0]: isp_y_offset[9:8]
0x500A	ISP RW10	0x00	RW	Bit[7:0]: isp_y_offset[7:0]
0x500B	ISP RW11	0x00	RW	Bit[7:3]: Not used Bit[2:0]: otp_x_offset[10:8]
0x500C	ISP RW12	0x00	RW	Bit[7:0]: otp_x_offset[7:0]
0x500D	ISP RW13	0x00	RW	Bit[7:2]: Not used Bit[1:0]: otp_y_offset[9:8]
0x500E	ISP RW14	0x00	RW	Bit[7:0]: otp_y_offset[7:0]
0x503B	ISP RW59	0x00	RW	Bit[7:2]: Not used Bit[1:0]: line_int_vsize[9:8]
0x503C	ISP RW60	0x02	RW	Bit[7:0]: line_int_vsize[7:0]
0x503D	ISP RW61	0x00	RW	Bit[7]: pre_isp_test_en_i Bit[6]: Not used Bit[5:4]: pre_isp_bar_style_i Bit[3]: Not used Bit[2]: pre_isp_rolling_i Bit[1]: pre_isp_isp_test_i Bit[0]: pre_isp_rnd_same_i

table 7-8 ISP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x503E	ISP RW62	0x00	RW	Bit[7:4]: pre_isp_seed_i Bit[3]: pre_isp_squ_bw_i Bit[2]: pre_isp_trans_i Bit[1:0]: pre_isp_test_sel_i
0x5040~ 0x5043	ISP RO	–	R	Debug Information for ISP TOP Control
0x5044	ISP RW68	0x00	RW	Bit[7:0]: isp_risc_debug[7:0]

7.9 LENC control [0x5080 - 0x50B8]

table 7-9 LENC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5080	LENC CTRL0	0x10	RW	Bit[7]: Not used Bit[6]: Gain manual mode enable 0: Use auto gain 1: Use manual gain set by user Bit[5]: Auto LENC switch enable 0: LENC gain adjust according to sensor gain 1: LENC gain fix to 'd16 Bit[4:0]: Manual gain input
0x5081	LENC CTRL1	0x00	RW	Bit[7:3]: Not used Bit[2:0]: long_red_x0[10:8]
0x5082	LENC CTRL2	0x00	RW	Bit[7:0]: long_red_x0[7:0]
0x5083	LENC CTRL3	0x00	RW	Bit[7:2]: Not used Bit[1:0]: long_red_y0[9:8]
0x5084	LENC CTRL4	0x00	RW	Bit[7:0]: long_red_y0[7:0]
0x5085	LENC CTRL5	0x00	RW	Bit[7]: Not used Bit[6:0]: long_red_a1
0x5086	LENC CTRL6	0x01	RW	Bit[7:4]: Not used Bit[3:0]: long_red_a2
0x5087	LENC CTRL7	0x00	RW	Bit[7]: long_red_sign Bit[6:0]: long_red_b1
0x5088	LENC CTRL8	0x01	RW	Bit[7:4]: Not used Bit[3:0]: long_red_b2
0x5089	LENC CTRL9	0x00	RW	Bit[7:3]: Not used Bit[2:0]: long_grn_x0[10:8]

table 7-9 LENC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x508A	LENC CTRL10	0x00	RW	Bit[7:0]: long_grn_x0[7:0]
0x508B	LENC CTRL11	0x00	RW	Bit[7:2]: Not used Bit[1:0]: long_grn_y0[9:8]
0x508C	LENC CTRL12	0x00	RW	Bit[7:0]: long_grn_y0[7:0]
0x508D	LENC CTRL13	0x00	RW	Bit[7]: Not used Bit[6:0]: long_grn_a1
0x508E	LENC CTRL14	0x01	RW	Bit[7:4]: Not used Bit[3:0]: long_grn_a2
0x508F	LENC CTRL15	0x00	RW	Bit[7]: long_grn_sign Bit[6:0]: long_grn_b1
0x5090	LENC CTRL16	0x01	RW	Bit[7:4]: Not used Bit[3:0]: long_grn_b2
0x5091	LENC CTRL17	0x00	RW	Bit[7:3]: Not used Bit[2:0]: long_blu_x0[10:8]
0x5092	LENC CTRL18	0x00	RW	Bit[7:0]: long_blu_x0[7:0]
0x5093	LENC CTRL19	0x00	RW	Bit[7:2]: Not used Bit[1:0]: long_blu_y0[9:8]
0x5094	LENC CTRL20	0x00	RW	Bit[7:0]: long_blu_y0[7:0]
0x5095	LENC CTRL21	0x00	RW	Bit[7]: Not used Bit[6:0]: long_blu_a1
0x5096	LENC CTRL22	0x01	RW	Bit[7:4]: Not used Bit[3:0]: long_blu_a2
0x5097	LENC CTRL23	0x0	RW	Bit[7]: long_blu_sign Bit[6:0]: long_blu_b1
0x5098	LENC CTRL24	0x01	RW	Bit[7:4]: Not used Bit[3:0]: long_blu_b2
0x509C	LENC CTRL28	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Min LENC gain
0x509D	LENC CTRL29	0x00	RW	Bit[7:1]: Not used Bit[0]: Sensor gain1[8] (must be less than 0x200)
0x509E	LENC CTRL30	0x00	RW	Bit[7:0]: Sensor gain1[7:0]
0x509F	LENC CTRL31	0x00	RW	Bit[7:1]: Not used Bit[0]: Sensor gain2[8] (must be less than 0x200)
0x50A0	LENC CTRL32	0x00	RW	Bit[7:0]: Sensor gain2[7:0]

table 7-9 LENC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x50A1	LENC CTRL33	0x00	RW	Bit[7:3]: Not used Bit[2:0]: short_red_x0[10:8]
0x50A2	LENC CTRL34	0x00	RW	Bit[7:0]: short_red_x0[7:0]
0x50A3	LENC CTRL35	0x00	RW	Bit[7:2]: Not used Bit[1:0]: short_red_y0[9:8]
0x50A4	LENC CTRL36	0x00	RW	Bit[7:0]: short_red_y0[7:0]
0x50A5	LENC CTRL37	0x00	RW	Bit[7]: Not used Bit[6:0]: short_red_a1
0x50A6	LENC CTRL38	0x01	RW	Bit[7:4]: Not used Bit[3:0]: short_red_a2
0x50A7	LENC CTRL39	0x00	RW	Bit[7]: short_red_sign Bit[6:0]: short_red_b1
0x50A8	LENC CTRL40	0x01	RW	Bit[7:4]: Not used Bit[3:0]: short_red_b2
0x50A9	LENC CTRL41	0x00	RW	Bit[7:3]: Not used Bit[2:0]: short_grn_x0[10:8]
0x50AA	LENC CTRL42	0x00	RW	Bit[7:0]: short_grn_x0[7:0]
0x50AB	LENC CTRL43	0x00	RW	Bit[7:2]: Not used Bit[1:0]: short_grn_y0[9:8]
0x50AC	LENC CTRL44	0x00	RW	Bit[7:0]: short_grn_y0[7:0]
0x50AD	LENC CTRL45	0x00	RW	Bit[7]: Not used Bit[6:0]: short_grn_a1
0x50AE	LENC CTRL46	0x01	RW	Bit[7:4]: Not used Bit[3:0]: short_grn_a2
0x50AF	LENC CTRL47	0x00	RW	Bit[7]: short_grn_sign Bit[6:0]: short_grn_b1
0x50B0	LENC CTRL48	0x01	RW	Bit[7:4]: Not used Bit[3:0]: short_grn_b2
0x50B1	LENC CTRL49	0x00	RW	Bit[7:3]: Not used Bit[2:0]: short_blu_x0[10:8]
0x50B2	LENC CTRL50	0x00	RW	Bit[7:0]: short_blu_x0[7:0]
0x50B3	LENC CTRL51	0x00	RW	Bit[7:2]: Not used Bit[1:0]: short_blu_y0[9:8]
0x50B4	LENC CTRL52	0x00	RW	Bit[7:0]: short_blu_y0[7:0]
0x50B5	LENC CTRL53	0x00	RW	Bit[7]: Not used Bit[6:0]: short_blu_a1

table 7-9 LENC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x50B6	LENC CTRL54	0x01	RW	Bit[7:4]: Not used Bit[3:0]: short_blu_a2
0x50B7	LENC CTRL55	0x00	RW	Bit[7]: short_blu_sign Bit[6:0]: short_blu_b1
0x50B8	LENC CTRL56	0x01	RW	Bit[7:4]: Not used Bit[3:0]: short_blu_b2

7.10 white/black pixel cancellation [0x5180 - 0x51A3]

table 7-10 white/black pixel cancellation registers

address	register name	default value	R/W	description
0x5180	WBC CTRL00	0x1C	RW	Bit[7:0]: Debug mode for long exposure sub-pixel
0x5181	WBC CTRL01	0x13	RW	Bit[7:5]: Not used Bit[4]: Debug mode Bit[3:2]: Not used Bit[1:0]: Option for padding the boundary pixel for long exposure sub-pixel
0x5182~ 0x5191	DEBUG CONTROL	–	RW	WBC Debug Control for Long Exposure Sub-pixel
0x5192	WBC CTRL12	0x1C	RW	Bit[7:0]: Debug mode for short exposure sub-pixel
0x5193	WBC CTRL13	0x13	RW	Bit[7:5]: Not used Bit[4]: Debug mode Bit[3:2]: Not used Bit[1:0]: Option for padding the boundary pixel for short exposure sub-pixel
0x5194~ 0x51A3	DEBUG CONTROL	–	RW	WBC Debug Control for Short Exposure Sub-pixel

7.11 VAP control [0x5900 - 0x5910]

table 7-11 VAP control registers

address	register name	default value	R/W	description
0x5900	VAP CTRL00	0x01	RW	Bit[7]: debug_en 0: Disable debug mode 1: Enable debug mode Bit[6]: single_channel 0: Disable signal channel function 1: Enable signal channel function Bit[5]: sum_en for even-line and even-column pixels 0: Drop mode 1: Sum mode Bit[4]: sum_en for even-line and odd-column pixels 0: Drop mode 1: Sum mode Bit[3]: sum_en for odd-line and even-column pixels 0: Drop mode 1: Sum mode Bit[2]: sum_en for odd-line and odd-column pixels 0: Drop mode 1: Sum mode Bit[1]: hsub4_drop_mode 0: Output first pixel of first group and second pixel of third group This option only operates in 1:4 horizontal sub-sample drop mode 1: Output the first group Bit[0]: avg_en 0: Limitation mode 1: Average mode
0x5901	VAP CTRL01	0x00	RW	Bit[7:4]: Not used Bit[3:2]: hsub_coef Horizontal sub-sample coefficient 00: Sub-sample 1 01: Sub-sample 2 1x: Sub-sample 4 Bit[1:0]: vsub_coef Vertical sub-sample coefficient 00: Sub-sample 1 01: Sub-sample 2 1x: Sub-sample 4

7.12 AWB control [0x5100 - 0x5D1B]

table 7-12 AWB control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x5100	GAIN AWB CTRL0	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_gain_b_long[9:8]
0x5101	GAIN AWB CTRL1	0x80	RW	Bit[7:0]: manual_gain_b_long[7:0]
0x5102	GAIN AWB CTRL2	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_gain_gb_long[9:8]
0x5103	GAIN AWB CTRL3	0x80	RW	Bit[7:0]: manual_gain_gb_long[7:0]
0x5104	GAIN AWB CTRL4	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_gain_gr_long[9:8]
0x5105	GAIN AWB CTRL5	0x80	RW	Bit[7:0]: manual_gain_gr_long[7:0]
0x5106	GAIN AWB CTRL6	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_gain_r_long[9:8]
0x5107	GAIN AWB CTRL7	0x80	RW	Bit[7:0]: manual_gain_r_long[7:0]
0x5108	GAIN AWB CTRL8	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_offset_b_long[9:8]
0x5109	GAIN AWB CTRL9	0x00	RW	Bit[7:0]: manual_offset_b_long[7:0]
0x510A	GAIN AWB CTRL10	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_offset_gb_long[9:8]
0x510B	GAIN AWB CTRL11	0x00	RW	Bit[7:0]: manual_offset_gb_long[7:0]
0x510C	GAIN AWB CTRL12	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_offset_gr_long[9:8]
0x510D	GAIN AWB CTRL13	0x00	RW	Bit[7:0]: manual_offset_gr_long[7:0]
0x510E	GAIN AWB CTRL14	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_offset_r_long[9:8]
0x510F	GAIN AWB CTRL15	0x00	RW	Bit[7:0]: manual_offset_r_long[7:0]
0x5110	GAIN AWB CTRL16	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_gain_b_short[9:8]
0x5111	GAIN AWB CTRL17	0x80	RW	Bit[7:0]: manual_gain_b_short[7:0]
0x5112	GAIN AWB CTRL18	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_gain_gb_short[9:8]
0x5113	GAIN AWB CTRL19	0x80	RW	Bit[7:0]: manual_gain_gb_short[7:0]
0x5114	GAIN AWB CTRL20	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_gain_gr_short[9:8]

table 7-12 AWB control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x5115	GAIN AWB CTRL21	0x80	RW	Bit[7:0]: manual_gain_gr_short[7:0]
0x5116	GAIN AWB CTRL22	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_gain_r_short[9:8]
0x5117	GAIN AWB CTRL23	0x80	RW	Bit[7:0]: manual_gain_r_short[7:0]
0x5118	GAIN AWB CTRL24	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_offset_b_short[9:8]
0x5119	GAIN AWB CTRL25	0x00	RW	Bit[7:0]: manual_offset_b_short[7:0]
0x511A	GAIN AWB CTRL26	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_offset_gb_short[9:8]
0x511B	GAIN AWB CTRL27	0x00	RW	Bit[7:0]: manual_offset_gb_short[7:0]
0x511C	GAIN AWB CTRL28	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_offset_gr_short[9:8]
0x511D	GAIN AWB CTRL29	0x00	RW	Bit[7:0]: manual_offset_gr_short[7:0]
0x511E	GAIN AWB CTRL30	0x00	RW	Bit[7:2]: Not used Bit[1:0]: manual_offset_r_short[9:8]
0x511F	GAIN AWB CTRL31	0x00	RW	Bit[7:0]: manual_offset_r_short[7:0]
0x5120	GAIN AWB CTRL32	0x00	RW	Bit[7:1]: Not used Bit[0]: awb_gain_manual_en 0: Reserved 1: AWB gain adjusted by user
0x5580	AWB CT CTRL0	0xFF	RW	Bit[7:0]: awb_b_block_l
0x5581	AWB CT CTRL1	0x5B	RW	Bit[7:6]: step_local Bit[5:4]: step_fast Bit[3]: slop_8x_l Bit[2]: slop_4x_l Bit[1]: one_zone Bit[0]: avg_all
0x5582	AWB CT CTRL2	0x11	RW	Bit[7:4]: max_local_cnt Bit[3:0]: max_fast_cnt
0x5583	AWB CT CTRL3	0x10	RW	Bit[7]: slop_8x_s Bit[6]: slop_4x_s Bit[5]: Not used Bit[4]: awb_simf Bit[3:2]: awb_win Bit[1:0]: Not used

table 7-12 AWB control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x5584	AWB CT CTRL4	0x25	RW	Bit[7:6]: count_area_sel Bit[5]: g_en Bit[4:2]: count_limit_ctrl Bit[1:0]: cnt_th
0x5585	AWB CT CTRL5	0x24	RW	Bit[7:4]: stable_range_us Unstable stable range Bit[3:0]: stable_range_s Stable range
0x5586~ 0x5590	AWB CT CTRL	–	RW	CT AWB Control for Long Exposure Sub-pixel
0x5591	AWB CT CTRL17	0xFF	RW	Bit[7:0]: awb_top_limit_l
0x5592	AWB CT CTRL18	0x00	RW	Bit[7:0]: awb_bot_limit_l
0x5596	AWB CT CTRL22	0x03	RW	Bit[7]: awb_gain_m Bit[6]: Not used Bit[5]: awb_freeze Bit[4]: Not used Bit[3:2]: awb_sim_sel 00: awb_simple from after awb_gain 01: awb_simple from after raw_gma 10: awb_simple from after WDR 11: awb_simple from after awb_gain Bit[1]: fast_enable Bit[0]: awb_bias_stat
0x5597~ 0x55AB	AWB CT CTRL	–	RW	Advanced AWB Control Registers for Short Exposure Channel
0x55AF	AWB CT CTRL41	0x00	RW	Bit[7]: bsum_l_fix Bit[6]: gsum_l_fix Bit[5]: rsum_l_fix Bit[4]: bsum_s_fix Bit[3]: gsum_s_fix Bit[2]: rsum_s_fix Bit[1]: allcnt_l_fix Bit[0]: allcnt_s_fix
0x55B0	AWB CT CTRL42	0x00	RW	Bit[7:6]: Not used Bit[5]: fix_whole Bit[4]: fix_eof Bit[3:0]: fix_value
0x5700	AWB CTRL0	0x00	RW	Bit[7:2]: Not used Bit[1:0]: midtone_ythre_l1[9:8]
0x5701	AWB CTRL1	0x10	RW	Bit[7:0]: midtone_ythre_l1[7:0] (midtone_ythre_l1+midtone_ythre_l2 ≤ 0x3FF)

table 7-12 AWB control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x5702	AWB CTRL2	0x01	RW	Bit[7:2]: Not used Bit[1:0]: midtone_ythre_l2[9:8]
0x5703	AWB CTRL3	0x00	RW	Bit[7:0]: midtone_ythre_l2[7:0] (midtone_ythre_l1+midtone_ythre_l2 ≤ 0x3FF)
0x5704	AWB CTRL4	0x03	RW	Bit[7:2]: Not used Bit[1:0]: midtone_ythre_h1[9:8]
0x5705	AWB CTRL5	0x68	RW	Bit[7:0]: midtone_ythre_h1[7:0] (midtone_ythre_h1+midtone_ythre_h2 ≤ 0x3FF)
0x5706	AWB CTRL6	0x00	RW	Bit[7:2]: Not used Bit[1:0]: midtone_ythre_h2[9:8]
0x5707	AWB CTRL7	0x80	RW	Bit[7:0]: midtone_ythre_h2[7:0] (midtone_ythre_h1+midtone_ythre_h2 ≤ 0x3FF)
0x5708	AWB CTRL8	0x00	RW	Bit[7:2]: Not used Bit[1:0]: gamma_ythre_l[9:8]
0x5709	AWB CTRL9	0x20	RW	Bit[7:0]: gamma_ythre_l[7:0]
0x570A	AWB CTRL10	0x00	RW	Bit[7:2]: Not used Bit[1:0]: gamma_ythre_h[9:8]
0x570B	AWB CTRL11	0x10	RW	Bit[7:0]: gamma_ythre_h[7:0]
0x570C	AWB CTRL12	0x00	RW	Bit[7:2]: Not used Bit[1:0]: gamma_uvthre1[9:8]
0x570D	AWB CTRL13	0x40	RW	Bit[7:0]: gamma_uvthre1[7:0]
0x570E	AWB CTRL14	0x00	RW	Bit[7:2]: Not used Bit[1:0]: gamma_uvthre2[9:8]
0x570F	AWB CTRL15	0x40	RW	Bit[7:0]: gamma_uvthre2[7:0]
0x5710	AWB CTRL16	0x00	RW	Bit[7:2]: Not used Bit[1:0]: shadow_ythre1[9:8]
0x5711	AWB CTRL17	0x40	RW	Bit[7:0]: shadow_ythre1[7:0] (shadow_ythre1 + shadow_ythre2 ≤ 0x3FF)
0x5712	AWB CTRL18	0x00	RW	Bit[7:2]: Not used Bit[1:0]: shadow_ythre2[9:8]
0x5713	AWB CTRL19	0x80	RW	Bit[7:0]: shadow_ythre2[7:0] (shadow_ythre1 + shadow_ythre2 ≤ 0x3FF)
0x5714	AWB CTRL20	0x00	RW	Bit[7:2]: Not used Bit[1:0]: shadow_uv_thre1[9:8]

table 7-12 AWB control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x5715	AWB CTRL21	0x10	RW	Bit[7:0]: shadow_uv_thre1[7:0] (shadow_uv_thre1 + shadow_uv_thre2 ≤ 0x3FF)
0x5716	AWB CTRL22	0x00	RW	Bit[7:2]: Not used Bit[1:0]: shadow_uv_thre2[9:8]
0x5717	AWB CTRL23	0x10	RW	Bit[7:0]: shadow_uv_thre2[7:0] (shadow_uv_thre1 + shadow_uv_thre2 ≤ 0x3FF)
0x5718	AWB CTRL24	0x3C	RW	Bit[7:6]: Not used Bit[5:2]: Debug mode Bit[1]: Debug mode 2 (EOF to VSYNC fix value, other than zero) Bit[0]: Debug mode 1 (always fix value)
0xC4B8	CT_AWB_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: Color temperature based AWB 0: Disable 1: Enable
0xC4B9	AWB_WORK_MODE	0x01	RW	Bit[7:2]: Not used Bit[1:0]: AWB work mode 00 Separate mode 01: Long 10: Short 11: Combine
0xC4BA	AWB_FEEDBACK_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: Feedback for simple AWB 0: Disable 1: Enable
0xC4BB	AWB_SHADOW_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: Shadow correction for simple AWB 0: Disable 1: Enable
0xC4CC	SIMPLE_MIN_NUM_1	0x10	RW	Bit[7:0]: Min statistic num for simple AWB[15:8]
0xC4CD	SIMPLE_MIN_NUM_2	0x00	RW	Bit[7:0]: Min statistic num for simple AWB[7:0]
0xC4CE	CT_MIN_NUM_1	0x32	RW	Bit[7:0]: Min statistic num for CT AWB[15:8]
0xC4CF	CT_MIN_NUM_2	0x00	RW	Bit[7:0]: Min statistic num for CT AWB[7:0]
0xC4D0	AWB_STEP_1	0x04	RW	Relative AWB Adjustment Step
0xC4D1	AWB_STEP_2	0x80	RW	Absolute AWB Adjustment Step
0xC4D2	AWB_COMB_ALPHA	0x0C	RW	AWB Combination Alpha
0xC4D3	AWB_SLOW_STEP	0x10	RW	AWB Gamma Offset Adjustment Step

table 7-12 AWB control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0xC4D4	GAMMA_OFFSET_MIN_1	0x03	RW	Bit[7:0]: Min gamma offset[15:8]
0xC4D5	GAMMA_OFFSET_MIN_2	0x99	RW	Bit[7:0]: Min gamma offset[7:0]
0xC4D6	GAMMAOFFSET_MAX_1	0x04	RW	Bit[7:0]: Max gamma offset[15:8]
0xC4D7	GAMMAOFFSET_MAX_2	0x66	RW	Bit[7:0]: Max gamma offset[7:0]
0xC4D8	UV_MATRIX_11	0x22	RW	UV Matrix 11
0xC4D9	UV_MATRIX_12	0x0B	RW	UV Matrix 12
0xC4DA	UV_MATRIX_21	0x06	RW	UV Matrix 21
0xC4DB	UV_MATRIX_22	0x22	RW	UV Matrix 22
0xC4DC	AWB_STABLE_RG_1	0x20	RW	Simple AWB Stable Range 1
0xC4DD	AWB_STABLE_RG_2	0x40	RW	Simple AWB Stable Range 2
0xC4DE	SHADOW_OFFSET_STEP	0x10	RW	Shadow Offset Step
0xC4DF	SHADOW_STABLE_RG	0x04	RW	Shadow Offset Stable Range
0x5AB0~ 0x5B1B	AWB_R	–	R	Debug information for AWB gain control
0x5CFC	WBG_RW01	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Long_AWB_gain_B[9:8]
0x5CFD	WBG_RW02	0x80	RW	Bit[7:0]: Long_AWB_gain_B[7:0]
0x5CFE	WBG_RW03	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Long_AWB_gain_Gb[9:8]
0x5CFF	WBG_RW04	0x80	RW	Bit[7:0]: Long_AWB_gain_Gb[7:0]
0x5D00	WBG_RW05	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Long_AWB_gain_Gr[9:8]
0x5D01	WBG_RW06	0x80	RW	Bit[7:0]: Long_AWB_gain_Gr[7:0]
0x5D02	WBG_RW07	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Long_AWB_gain_R[9:8]
0x5D03	WBG_RW08	0x80	RW	Bit[7:0]: Long_AWB_gain_R[7:0]
0x5D04	WBG_RW09	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Short_AWB_gain_B[9:8]

table 7-12 AWB control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x5D05	WBG_RW10	0x80	RW	Bit[7:0]: Short_AWB_gain_B[7:0]
0x5D06	WBG_RW11	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Short_AWB_gain_Gb[9:8]
0x5D07	WBG_RW12	0x80	RW	Bit[7:0]: Short_AWB_gain_Gb[7:0]
0x5D08	WBG_RW13	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Short_AWB_gain_Gr[9:8]
0x5D09	WBG_RW14	0x80	RW	Bit[7:0]: Short_AWB_gain_Gr[7:0]
0x5D0A	WBG_RW15	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Short_AWB_gain_R[9:8]
0x5D0B	WBG_RW16	0x80	RW	Bit[7:0]: Short_AWB_gain_R[7:0]
0x5D0C	WBG_RW17	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Long_AWBOFFSET_B[9:8] Complementary code
0x5D0D	WBG_RW18	0x00	RW	Bit[7:0]: Long_AWBOFFSET_B[7:0] Complementary code
0x5D0E	WBG_RW19	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Long_AWBOFFSET_GB[9:8] Complementary code
0x5D0F	WBG_RW20	0x00	RW	Bit[7:0]: Long_AWBOFFSET_GB[7:0] Complementary code
0x5D10	WBG_RW21	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Long_AWBOFFSET_GR[9:8] Complementary code
0x5D11	WBG_RW22	0x00	RW	Bit[7:0]: Long_AWBOFFSET_GR[7:0] Complementary code
0x5D12	WBG_RW23	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Long_AWBOFFSET_R[9:8] Complementary code
0x5D13	WBG_RW24	0x00	RW	Bit[7:0]: Long_AWBOFFSET_R[7:0] Complementary code
0x5D14	WBG_RW25	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Short_AWBOFFSET_B[9:8] Complementary code
0x5D15	WBG_RW26	0x00	RW	Bit[7:0]: Short_AWBOFFSET_B[7:0] Complementary code
0x5D16	WBG_RW27	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Short_AWBOFFSET_Gb[9:8] Complementary code

table 7-12 AWB control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x5D17	WBG_RW28	0x00	RW	Bit[7:0]: Short_AWBOFFSET_Gb[7:0] Complementary code
0x5D18	WBG_RW29	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Short_AWBOFFSET_Gr[9:8] Complementary code
0x5D19	WBG_RW30	0x00	RW	Bit[7:0]: Short_AWBOFFSET_Gr[7:0] Complementary code
0x5D1A	WBG_RW31	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Short_AWBOFFSET_R[9:8] Complementary code
0x5D1B	WBG_RW32	0x00	RW	Bit[7:0]: Short_AWBOFFSET_R[7:0] Complementary code

7.13 DNS control [0x5210 - 0x5256]

table 7-13 DNS control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5210	DNS CTRL10	0x04	RW	Bit[7:4]: Not used Bit[3:0]: noise_y_a for long exposure sub-pixel
0x5211	DNS CTRL11	0x08	RW	Bit[7:5]: Not used Bit[4:0]: noise_uv_a for long exposure sub-pixel
0x5212	DNS CTRL12	0x00	RW	Bit[7:1]: Not used Bit[0]: dns_manual for long exposure sub-pixel
0x5213	DNS CTRL13	0x02	RW	noise_y for Long Exposure Sub-pixel
0x5214	DNS CTRL14	00x0	RW	Bit[7:1]: Not used Bit[0]: noise_u[8] for long exposure sub-pixel
0x5215	DNS CTRL15	0x02	RW	Bit[7:0]: noise_u[7:0] for long exposure sub-pixel
0x5216	DNS CTRL16	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_v[8] for long exposure sub-pixel
0x5217	DNS CTRL17	0x02	RW	Bit[7:0]: noise_v[7:0] for long exposure sub-pixel
0x5218	DNS CTRL18	0x06	RW	dns_edgethre for Long Exposure Sub-pixel
0x5219	DNS CTRL19	0x04	RW	Bit[7:4]: Not used Bit[3:0]: dns_gbgr_extra[3:0] for long exposure sub-pixel

table 7-13 DNS control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x521A	DNS CTRL20	0x02	RW	noise_y_list_0 for Long Exposure Sub-pixel
0x521B	DNS CTRL21	0x04	RW	noise_y_list_1 for Long Exposure Sub-pixel
0x521C	DNS CTRL22	0x08	RW	noise_y_list_2 for Long Exposure Sub-pixel
0x521D	DNS CTRL23	0x14	RW	noise_y_list_3 for Long Exposure Sub-pixel
0x521E	DNS CTRL24	0x1E	RW	noise_y_list_4 for Long Exposure Sub-pixel
0x521F	DNS CTRL25	0x28	RW	noise_y_list_5 for Long Exposure Sub-pixel
0x5220	DNS CTRL26	0x32	RW	noise_y_list_6_l for Long Exposure Sub-pixel
0x5221	DNS CTRL27	0x00	RW	Bit[7:1]: Not used Bit[0]: dns_dummy[0] for long exposure sub-pixel
0x5222	DNS CTRL28	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_0[8] for long exposure sub-pixel
0x5223	DNS CTRL29	0x02	RW	Bit[7:0]: noise_uv_list_0[7:0] for long exposure sub-pixel
0x5224	DNS CTRL30	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_1[8] for long exposure sub-pixel
0x5225	DNS CTRL31	0x04	RW	Bit[7:0]: noise_uv_list_1[7:0] for long exposure sub-pixel
0x5226	DNS CTRL32	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_2[8] for long exposure sub-pixel
0x5227	DNS CTRL33	0x0C	RW	Bit[7:0]: noise_uv_list_2[7:0] for long exposure sub-pixel
0x5228	DNS CTRL34	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_3[8] for long exposure sub-pixel
0x5229	DNS CTRL35	0x28	RW	Bit[7:0]: noise_uv_list_3[7:0] for long exposure sub-pixel
0x522A	DNS CTRL36	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_4[8] for long exposure sub-pixel
0x522B	DNS CTRL37	0x32	RW	Bit[7:0]: noise_uv_list_4[7:0] for long exposure sub-pixel
0x522C	DNS CTRL38	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_5[8] for long exposure sub-pixel
0x522D	DNS CTRL39	0x3C	RW	Bit[7:0]: noise_uv_list_5[7:0] for long exposure sub-pixel
0x522E	DNS CTRL40	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_6[8] for long exposure sub-pixel
0x522F	DNS CTRL41	0x4C	RW	Bit[7:0]: noise_uv_list_6[7:0] for long exposure sub-pixel
0x5238	DNS CTRL50	0x04	RW	Bit[7:4]: Not used Bit[3:0]: noise_y_a for short exposure sub-pixel

table 7-13 DNS control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5239	DNS CTRL51	0x08	RW	Bit[7:5]: Not used Bit[4:0]: noise_uv_a for short exposure sub-pixel
0x523A	DNS CTRL52	0x00	RW	Bit[7:1]: Not used Bit[0]: dns_manual for short exposure sub-pixel
0x523B	DNS CTRL53	0x02	RW	noise_y for Short Exposure Sub-pixel
0x523C	DNS CTRL54	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_u[8] for short exposure sub-pixel
0x523D	DNS CTRL55	0x02	RW	Bit[7:0]: noise_u[7:0] for short exposure sub-pixel
0x523E	DNS CTRL56	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_v[8] for short exposure sub-pixel
0x523F	DNS CTRL57	0x02	RW	Bit[7:0]: noise_v[7:0] for short exposure sub-pixel
0x5240	DNS CTRL58	0x06	RW	dns_edgethre for Short Exposure Sub-pixel
0x5241	DNS CTRL59	0x04	RW	Bit[7:4]: Not used Bit[3:0]: dns_gbgr_extra[3:0] for short exposure sub-pixel
0x5242	DNS CTRL60	0x02	RW	noise_y_list_0 for Short Exposure Sub-pixel
0x5243	DNS CTRL61	0x04	RW	noise_y_list_1 for Short Exposure Sub-pixel
0x5244	DNS CTRL62	0x08	RW	noise_y_list_2 for Short Exposure Sub-pixel
0x5245	DNS CTRL63	0x14	RW	noise_y_list_3 for Short Exposure Sub-pixel
0x5246	DNS CTRL64	0x1E	RW	noise_y_list_4 for Short Exposure Sub-pixel
0x5247	DNS CTRL65	0x28	RW	noise_y_list_5 for Short Exposure Sub-pixel
0x5248	DNS CTRL66	0x32	RW	noise_y_list_6 for Short Exposure Sub-pixel
0x5249	DNS CTRL67	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_0[8] for short exposure sub-pixel
0x524A	DNS CTRL68	0x02	RW	Bit[7:0]: noise_uv_list_0[7:0] for short exposure sub-pixel
0x524B	DNS CTRL69	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_1[8] for short exposure sub-pixel
0x524C	DNS CTRL70	0x04	RW	Bit[7:0]: noise_uv_list_1[7:0] for short exposure sub-pixel
0x524D	DNS CTRL71	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_2[8] for short exposure sub-pixel
0x524E	DNS CTRL72	0x0C	RW	Bit[7:0]: noise_uv_list_2[7:0] for short exposure sub-pixel

table 7-13 DNS control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x524F	DNS CTRL73	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_3[8] for short exposure sub-pixel
0x5250	DNS CTRL74	0x28	RW	Bit[7:0]: noise_uv_list_3[7:0] for short exposure sub-pixel
0x5251	DNS CTRL75	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_4[8] for short exposure sub-pixel
0x5252	DNS CTRL76	0x32	RW	Bit[7:0]: noise_uv_list_4[7:0] for short exposure sub-pixel
0x5253	DNS CTRL77	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_5[8] for short exposure sub-pixel
0x5254	DNS CTRL78	0x3C	RW	Bit[7:0]: noise_uv_list_5[7:0] for short exposure sub-pixel
0x5255	DNS CTRLL79	0x00	RW	Bit[7:1]: Not used Bit[0]: noise_uv_list_6[8] for short exposure sub-pixel
0x5256	DNS CTRLL80	0x4C	RW	Bit[7:0]: noise_uv_list_6[7:0] for short exposure sub-pixel

7.14 CIP control [0x5280 - 0x52E1]

table 7-14 CIP control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x5280	CIP CTRL00	0x00	RW	Bit[7:2]: Not used Bit[1:0]: min_gain[9:8] for long exposure sub-pixel Min_gain is used in CIP_start module to judge in which range the current sensor is in
0x5281	CIP CTRL01	0x10	RW	Bit[7:0]: min_gain[7:0] for long exposure sub-pixel Min_gain is used in CIP_start module to judge in which range the current sensor is in

table 7-14 CIP control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x5282	CIP CTRL02	0x00	RW	Bit[7:2]: Not used Bit[1:0]: max_gain[9:8] for long exposure sub-pixel Max_gain is used in CIP_start module to judge in which range the current sensor is in
0x5283	CIP CTRL03	0x80	RW	Bit[7:0]: max_gain[7:0] for long exposure sub-pixel Max_gain is used in CIP_start module to judge in which range the current sensor is in
0x5284	CIP CTRL04	0x00	RW	Bit[7:1]: Not used Bit[0]: min_noise[8] for long exposure sub-pixel min_noise is used for calculating int_noise in auto mode
0x5285	CIP CTRL05	0x10	RW	Bit[7:0]: min_noise[7:0] for long exposure sub-pixel min_noise is used for calculating int_noise in auto mode
0x5286	CIP CTRL06	0x01	RW	Bit[7:2]: Not used Bit[1:0]: noise_slope[9:8] for long exposure sub-pixel Slope value used for calculating int_noise in auto mode
0x5287	CIP CTRL07	0x00	RW	Bit[7:0]: noise_slope[7:0] for long exposure sub-pixel Slope value used for calculating int_noise in auto mode
0x5288	CIP CTRL08	0x10	RW	Bit[7:0]: unsharpen_mask0 for long exposure sub-pixel UnSharpenMask0 used in some filters as multipliers
0x5289	CIP CTRL09	0x30	RW	Bit[7:0]: unsharpen_mask1 for long exposure sub-pixel UnSharpenMask0 used in some filters as multipliers
0x528A	CIP CTRL0A	0x01	RW	Bit[7:2]: Not used Bit[1]: man_en Enable manual mode for long exposure sub-pixel Bit[0]: anti_aliasing Enable anti-aliasing for long exposure sub-pixel

table 7-14 CIP control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x528B	CIP CTRL0B	0x02	RW	Bit[7:4]: Not used Bit[3:0]: combine_alpha[3:0] for long exposure sub-pixel Combine coefficients for U, V and H components
0x528C	CIP CTRL0C	0x00	RW	Bit[7:5]: Not used Bit[4:0]: min_sharpen[4:0] for long exposure sub-pixel Min_sharpen is used for sharpen_p calculation in auto mode
0x528D	CIP CTRL0D	0x10	RW	Bit[7:6]: Not used Bit[5:0]: max_sharpen[5:0] for long exposure sub-pixel Max_sharpen is used for sharpen_p calculation in auto mode
0x528E	CIP CTRL0E	0x10	RW	Bit[7:6]: Not used Bit[5:0]: min_sharpen_tp[5:0] for long exposure sub-pixel Min_sharpen_tp is used for sharpen_tp computation in auto mode
0x528F	CIP CTRL0F	0x60	RW	Bit[7:0]: max_sharpen_tp[7:0] for long exposure sub-pixel Max_sharpen_tp is used for sharpen_tp computation in auto mode
0x5290	CIP CTRL10	0x20	RW	Bit[7:6]: Not used Bit[5:0]: min_sharpen_tm[5:0] for long exposure sub-pixel Min_sharpen_tm is used for sharpen_tm computation in auto mode
0x5291	CIP CTRL11	0x60	RW	Bit[7:0]: max_sharpen_tm[7:0] for long exposure sub-pixel Max_sharpen_tm is used for sharpen_tm computation in auto mode
0x5292	CIP CTRL12	0x40	RW	Bit[7:0]: sharpen_tya[7:0] for long exposure sub-pixel Threshold used for the function of adaptive sharpen
0x5293	CIP CTRL13	0x10	RW	Bit[7:5]: Not used Bit[4:0]: sharpen_alpha[4:0] for long exposure sub-pixel Sharpen_alpha is used for calculating sharpen_m after sharpen_p is obtained

table 7-14 CIP control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x5294	CIP CTRL14	0x06	RW	Bit[7:6]: Not used Bit[5:0]: mthre[5:0] for long exposure sub-pixel Threshold for medium frequency signals
0x5295	CIP CTRL15	0x08	RW	Bit[7:6]: Not used Bit[5:0]: hthre[5:0] for long exposure sub-pixel Threshold for high frequency signals
0x5297	CIP CTRL17	0x06	RW	Bit[7:4]: Not used Bit[3:0]: hfreq_coef[3:0] for long exposure sub-pixel Coefficients for high frequency signals
0x5298	CIP CTRL18	0x00	RW	Bit[7:2]: Not used Bit[1:0]: efreq_coef[1:0] for long exposure sub-pixel Coefficients for E frequency signals
0x5299	CIP CTRL19	0x08	RW	Bit[7:6]: Not used Bit[5:0]: lthre[5:0] for long exposure sub-pixel Threshold for low frequency signals
0x529A	CIP CTRL1A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_int_noise[9:8] for long exposure sub-pixel int_noise is input only in manual mode and is used as threshold in some filters
0x529B	CIP CTRL1B	0x30	RW	Bit[7:0]: man_int_noise[7:0] for long exposure sub-pixel int_noise is input only in manual mode and is used as threshold in some filters
0x529C	CIP CTRL1C	0x00	RW	Bit[7:1]: Not used Bit[0]: man_inv_noise[8] for long exposure sub-pixel inv_noise is input only in manual mode and is used as threshold in some filters
0x529D	CIP CTRL1D	0x55	RW	Bit[7:0]: man_inv_noise[7:0] for long exposure sub-pixel inv_noise is input only in manual mode and is used as threshold in some filters
0x529E	CIP CTRL1E	0x08	RW	Bit[7:6]: Not used Bit[5:0]: man_sharpen_p[5:0] for long exposure sub-pixel sharpen_p is input only in manual mode and is used for the function of adaptive sharpen

table 7-14 CIP control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x529F	CIP CTRL1F	0x08	RW	Bit[7]: Not used Bit[6:0]: man_sharpen_m[6:0] for long exposure sub-pixel sharpen_m is input only in manual mode and is used for the function of adaptive sharpen
0x52A0	CIP CTRL20	0x06	RW	Bit[7:0]: man_sharpen_tp[7:0] for long exposure sub-pixel sharpen_tp is input only in manual mode and is used for the function of adaptive sharpen
0x52A1	CIP CTRL21	0x08	RW	Bit[7:0]: man_sharpen_tm[7:0] for long exposure sub-pixel sharpen_tm is input only in manual mode and is used for the function of adaptive sharpen
0x52C0	CIP CTRL40	0x00	RW	Bit[7:2]: Not used Bit[1:0]: min_gain[9:8] for short exposure sub-pixel Min_gain is used in CIP_start module to judge in which range the current sensor is in
0x52C1	CIP CTRL41	0x10	RW	Bit[7:0]: min_gain[7:0] for short exposure sub-pixel Min_gain is used in CIP_start module to judge in which range the current sensor is in
0x52C2	CIP CTRL42	0x00	RW	Bit[7:2]: Not used Bit[1:0]: max_gain[9:8] for short exposure sub-pixel Max_gain is used in CIP_start module to judge in which range the current sensor is in
0x52C3	CIP CTRL43	0x80	RW	Bit[7:0]: max_gain[7:0] for short exposure sub-pixel Max_gain is used in CIP_start module to judge in which range the current sensor is in
0x52C4	CIP CTRL44	0x00	RW	Bit[7:1]: Not used Bit[0]: min_noise[8] for short exposure sub-pixel min_noise is used for calculating int_noise in auto mode

table 7-14 CIP control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x52C5	CIP CTRL45	0x10	RW	Bit[7:0]: min_noise[7:0] for short exposure sub-pixel min_noise is used for calculating int_noise in auto mode
0x52C6	CIP CTRL46	0x01	RW	Bit[7:2]: Not used Bit[1:0]: noise_slope[9:8] for short exposure sub-pixel Slope value used for calculating int_noise in auto mode
0x52C7	CIP CTRL47	0x00	RW	Bit[7:0]: noise_slope[7:0] for short exposure sub-pixel Slope value used for calculating int_noise in auto mode
0x52C8	CIP CTRL48	0x10	RW	Bit[7:0]: unsharpen_mask0 for short exposure sub-pixel UnSharpenMask0 used in some filters as multipliers
0x52C9	CIP CTRL49	0x30	RW	Bit[7:0]: unsharpen_mask1 for short exposure sub-pixel UnSharpenMask0 used in some filters as multipliers
0x52CA	CIP CTRL4A	0x01	RW	Bit[7:2]: Not used Bit[1]: man_en Enable manual mode for short exposure sub-pixel Bit[0]: anti_aliasing for short exposure sub-pixel Enable anti-aliasing
0x52CB	CIP CTRL4B	0x02	RW	Bit[7:4]: Not used Bit[3:0]: combine_alpha[3:0] for short exposure sub-pixel Combine coefficients for U, V and H components
0x52CC	CIP CTRL4C	0x00	RW	Bit[7:5]: Not used Bit[4:0]: min_sharpen[4:0] for short exposure sub-pixel Min_sharpen is used for sharpen_p calculation in auto mode
0x52CD	CIP CTRL4D	0x00	RW	Bit[7:6]: Not used Bit[5:0]: max_sharpen[5:0] for short exposure sub-pixel Max_sharpen is used for sharpen_p calculation in auto mode

table 7-14 CIP control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x52CE	CIP CTRL4E	0x10	RW	Bit[7:6]: Not used Bit[5:0]: min_sharpen_tp[5:0] for short exposure sub-pixel Min_sharpen_tp is used for sharpen_tp computation in auto mode
0x52CF	CIP CTRL4F	0x60	RW	Bit[7:0]: max_sharpen_tp[7:0] for short exposure sub-pixel Max_sharpen_tp is used for sharpen_tp computation in auto mode
0x52D0	CIP CTRL50	0x20	RW	Bit[7:6]: Not used Bit[5:0]: min_sharpen_tm[5:0] for short exposure sub-pixel Min_sharpen_tm is used for sharpen_tm computation in auto mode
0x52D1	CIP CTRL51	0x60	RW	Bit[7:0]: max_sharpen_tm[7:0] for short exposure sub-pixel Max_sharpen_tm is used for sharpen_tm computation in auto mode
0x52D2	CIP CTRL52	0x40	RW	Bit[7:0]: sharpen_tya[7:0] for short exposure sub-pixel Threshold used for the function of adaptive sharpen
0x52D3	CIP CTRL53	0x10	RW	Bit[7:5]: Not used Bit[4:0]: sharpen_alpha[4:0] for short exposure sub-pixel Sharpen_alpha is used for calculating sharpen_m after sharpen_p is obtained
0x52D4	CIP CTRL54	0x06	RW	Bit[7:6]: Not used Bit[5:0]: mthre[5:0] for short exposure sub-pixel Threshold for medium frequency signals
0x52D5	CIP CTRL55	0x08	RW	Bit[7:6]: Not used Bit[5:0]: hthre[5:0] for short exposure sub-pixel Threshold for high frequency signals
0x52D7	CIP CTRL57	0x06	RW	Bit[7:4]: Not used Bit[3:0]: hfreq_coef[3:0] for short exposure sub-pixel Coefficients for high frequency signals
0x52D8	CIP CTRL58	0x00	RW	Bit[7:2]: Not used Bit[1:0]: efreq_coef[1:0] for short exposure sub-pixel Coefficients for E frequency signals

table 7-14 CIP control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x52D9	CIP CTRL59	0x08	RW	Bit[7:6]: Not used Bit[5:0]: Ithre[5:0] for short exposure sub-pixel: Threshold for low frequency signals
0x52DA	CIP CTRL5A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_int_noise[9:8] for short exposure sub-pixel int_noise is input only in manual mode and is used as threshold in some filters
0x52DB	CIP CTRL5B	0x30	RW	Bit[7:0]: man_int_noise[7:0] for short exposure sub-pixel int_noise is input only in manual mode and is used as threshold in some filters
0x52DC	CIP CTRL5C	0x00	RW	Bit[7:1]: Not used Bit[0]: man_inv_noise[8] for short exposure sub-pixel in_noise is input only in manual mode and is used as threshold in some filters
0x52DD	CIP CTRL5D	0x55	RW	Bit[7:0]: man_inv_noise[7:0] for short exposure sub-pixel in_noise is input only in manual mode and is used as threshold in some filters
0x52DE	CIP CTRL5E	0x08	RW	Bit[7:6]: Not used Bit[5:0]: man_sharpen_p[5:0] for short exposure sub-pixel sharpen_p is input only in manual mode and is used for the function of adaptive sharpen
0x52DF	CIP CTRL5F	0x08	RW	Bit[6:0]: man_sharpen_m[6:0] for short exposure sub-pixel sharpen_m is input only in manual mode and is used for the function of adaptive sharpen
0x52E0	CIP CTRL60	0x06	RW	Bit[7:0]: man_sharpen_tp[7:0] for short exposure sub-pixel sharpen_tp is input only in manual mode and is used for the function of adaptive sharpen
0x52E1	CIP CTRL61	0x08	RW	Bit[7:0]: man_sharpen_tm[7:0] for short exposure sub-pixel: sharpen_tm is input only in manual mode and is used for the function of adaptive sharpen

7.15 CMX control [0xC318 - 0xC347]

table 7-15 CMX control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0xC318	COLOR_MATRIX_L_1_1	0x00	RW	Long Color Matrix 1[15:8]
0xC319	COLOR_MATRIX_L_1_2	0x3C	RW	Long Color Matrix 1[7:0]
0xC31A	COLOR_MATRIX_L_2_1	0x00	RW	Long Color Matrix 2[15:8]
0xC31B	COLOR_MATRIX_L_2_2	0xA9	RW	Long Color Matrix 2[7:0]
0xC31C	COLOR_MATRIX_L_3_1	0x00	RW	Long Color Matrix 3[15:8]
0xC31D	COLOR_MATRIX_L_3_2	0x1B	RW	Long Color Matrix 3[7:0]
0xC31E	COLOR_MATRIX_L_4_1	0x00	RW	Long Color Matrix 4[15:8]
0xC31F	COLOR_MATRIX_L_4_2	0xD6	RW	Long Color Matrix 4[7:0]
0xC320	COLOR_MATRIX_L_5_1	0xFF	RW	Long Color Matrix 5[15:8]
0xC321	COLOR_MATRIX_L_5_2	0x3C	RW	Long Color Matrix 5[7:0]
0xC322	COLOR_MATRIX_L_6_1	0xFF	RW	Long Color Matrix 6[15:8]
0xC323	COLOR_MATRIX_L_6_2	0xEE	RW	Long Color Matrix 6[7:0]
0xC324	COLOR_MATRIX_L_7_1	0xFF	RW	Long Color Matrix 7[15:8]
0xC325	COLOR_MATRIX_L_7_2	0xE9	RW	Long Color Matrix 7[7:0]
0xC326	COLOR_MATRIX_L_8_1	0x00	RW	Long Color Matrix 8[15:8]
0xC327	COLOR_MATRIX_L_8_2	0x4C	RW	Long Color Matrix 8[7:0]
0xC328	COLOR_MATRIX_L_9_1	0xFF	RW	Long Color Matrix 9[15:8]
0xC329	COLOR_MATRIX_L_9_2	0xCB	RW	Long Color Matrix 9[7:0]
0xC32A	COLOR_MATRIX_L_10_1	0xFF	RW	Long Color Matrix 10[15:8]
0xC32B	COLOR_MATRIX_L_10_2	0xDD	RW	Long Color Matrix 10[7:0]
0xC32C	COLOR_MATRIX_L_11_1	0xFF	RW	Long Color Matrix 11[15:8]
0xC32D	COLOR_MATRIX_L_11_2	0xB5	RW	Long Color Matrix 11[7:0]
0xC32E	COLOR_MATRIX_L_12_1	0x00	RW	Long Color Matrix 12[15:8]
0xC32F	COLOR_MATRIX_L_12_2	0x6E	RW	Long Color Matrix 12[7:0]
0xC330	COLOR_MATRIX_S_1_1	0x00	RW	Short Color Matrix 1[15:8]
0xC331	COLOR_MATRIX_S_1_2	0x29	RW	Short Color Matrix 1[7:0]

table 7-15 CMX control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0xC332	COLOR_MATRIX_S_2_1	0x00	RW	Short Color Matrix 2[15:8]
0xC333	COLOR_MATRIX_S_2_2	0xB1	RW	Short Color Matrix 2[7:0]
0xC334	COLOR_MATRIX_S_3_1	0x00	RW	Short Color Matrix 3[15:8]
0xC335	COLOR_MATRIX_S_3_2	0x26	RW	Short Color Matrix 3[7:0]
0xC336	COLOR_MATRIX_S_4_1	0x00	RW	Short Color Matrix 4[15:8]
0xC337	COLOR_MATRIX_S_4_2	0xC2	RW	Short Color Matrix 4[7:0]
0xC338	COLOR_MATRIX_S_5_1	0xFF	RW	Short Color Matrix 5[15:8]
0xC339	COLOR_MATRIX_S_5_2	0x54	RW	Short Color Matrix 5[7:0]
0xC33A	COLOR_MATRIX_S_6_1	0xFF	RW	Short Color Matrix 6[15:8]
0xC33B	COLOR_MATRIX_S_6_2	0xEA	RW	Short Color Matrix 6[7:0]
0xC33C	COLOR_MATRIX_S_7_1	0xFF	RW	Short Color Matrix 7[15:8]
0xC33D	COLOR_MATRIX_S_7_2	0xE8	RW	Short Color Matrix 7[7:0]
0xC33E	COLOR_MATRIX_S_8_1	0x00	RW	Short Color Matrix 8[15:8]
0xC33F	COLOR_MATRIX_S_8_2	0x4E	RW	Short Color Matrix 8[7:0]
0xC340	COLOR_MATRIX_S_9_1	0xFF	RW	Short Color Matrix 9[15:8]
0xC341	COLOR_MATRIX_S_9_2	0xCA	RW	Short Color Matrix 9[7:0]
0xC342	COLOR_MATRIX_S_10_1	0xFF	RW	Short Color Matrix 10[15:8]
0xC343	COLOR_MATRIX_S_10_2	0xE5	RW	Short Color Matrix 10[7:0]
0xC344	COLOR_MATRIX_S_11_1	0xFF	RW	Short Color Matrix 11[15:8]
0xC345	COLOR_MATRIX_S_11_2	0xA8	RW	Short Color Matrix 11[7:0]
0xC346	COLOR_MATRIX_S_12_1	0x00	RW	Short Color Matrix 12[15:8]
0xC347	COLOR_MATRIX_S_12_2	0x73	RW	Short Color Matrix 12[7:0]

7.16 LLF control [0x5380 - 0x538A]

table 7-16 LLF control registers

address	register name	default value	R/W	description
0x5380	LLF RW00	0x10	RW	Bit[7:5]: Not used Bit[4:0]: Step
0x5381	LLF RW01	0x02	RW	Bit[7:2]: Not used Bit[1:0]: max_low_level[9:8]
0x5382	LLF RW02	0x00	RW	Bit[7:0]: max_low_level[7:0]
0x5383	LLF RW03	0x04	RW	Bit[7:6]: Not used Bit[5:0]: ps_thres[13:8]
0x5384	LLF RO04	–	R	Bit[7:0]: ps_thres[7:0]
0x5385	LLF RO05	–	R	Bit[7:5]: Not used Bit[4:0]: low_pre_sum[20:16]
0x5386	LLF RO06	–	R	Bit[7:0]: low_pre_sum[15:8]
0x5387	LLF RO07	–	R	Bit[7:0]: low_pre_sum[7:0]
0x5388	LLF RO08	–	R	Bit[7:5]: Not used Bit[4:0]: low_next_sum[20:16]
0x5389	LLF RO09	–	R	Bit[7:0]: low_next_sum[15:8]
0x538A	LLF RO10	–	R	Bit[7:0]: low_next_sum[7:0]

7.17 combine control [0x5400 - 0x5C6F]

table 7-17 combine control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x5400	COMB CTRL0	0x0F	RW	Bit[7:4]: Not used Bit[3]: Dark boost enable 0: Dark boost disable 1: Dark boost enable Bit[2]: combine_uv_weight enable 0: Combine without UV weight 1: Combine with UV weight Bit[1]: color_diff_compensate enable 0: Compensate disable 1: Compensate enable Bit[0]: Compensate error enable 0: Compensate error disable 1: Compensate error enable
0x5401	COMB CTRL1	0x05	RW	Bit[7:4]: Not used Bit[3:0]: comb_thre_s0 Threshold1 of short channel
0x5402	COMB CTRL2	0x08	RW	Bit[7:4]: Not used Bit[3:0]: comb_thre_s1 Threshold2 of short channel
0x5403	COMB CTRL3	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: comb_thre_s2 Threshold3 of short channel
0x5404	COMB CTRL4	0x09	RW	Bit[7:4]: Not used Bit[3:0]: comb_thre_l0 Threshold1 of long channel
0x5405	COMB CTRL5	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: comb_thre_l1 Threshold2 of long channel
0x5406	COMB CTRL6	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: comb_thre_l2 Threshold3 of long channel
0x5407	COMB CTRL7	0x05	RW	Bit[7:4]: Not used Bit[3:0]: comb_uv_thre_s0 UV threshold1 of short channel
0x5408	COMB CTRL8	0x08	RW	Bit[7:4]: Not used Bit[3:0]: comb_uv_thre_s1 UV threshold2 of short channel
0x5409	COMB CTRL9	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: comb_uv_thre_s2 UV threshold3 of short channel

table 7-17 combine control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x540A	COMB CTRL10	0x09	RW	Bit[7:4]: Not used Bit[3:0]: comb_uv_thre_l0 UV threshold1 of long channel
0x540B	COMB CTRL11	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: comb_uv_thre_l1 UV threshold2 of long channel
0x540C	COMB CTRL12	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: comb_uv_thre_l2 UV threshold3 of long channel
0x540D	COMB CTRL13	0x80	RW	comb_weight00
0x540E	COMB CTRL14	0x80	RW	comb_weight01
0x540F	COMB CTRL15	0x60	RW	comb_weight02
0x5410	COMB CTRL16	0x40	RW	comb_weight03
0x5411	COMB CTRL17	0x80	RW	comb_weight10
0x5412	COMB CTRL18	0x80	RW	comb_weight11
0x5413	COMB CTRL19	0x20	RW	comb_weight12
0x5414	COMB CTRL20	0x10	RW	comb_weight13
0x5415	COMB CTRL21	0x80	RW	comb_weight20
0x5416	COMB CTRL22	0x80	RW	comb_weight21
0x5417	COMB CTRL23	0x00	RW	comb_weight22
0x5418	COMB CTRL24	0x00	RW	comb_weight23
0x5419	COMB CTRL25	0x80	RW	comb_weight30
0x541A	COMB CTRL26	0x80	RW	comb_weight31
0x541B	COMB CTRL27	0x00	RW	comb_weight32
0x541C	COMB CTRL28	0x00	RW	comb_weight33
0x541D	COMB CTRL29	0x80	RW	comb_uv_weight00
0x541E	COMB CTRL30	0x80	RW	comb_uv_weight01
0x541F	COMB CTRL31	0x80	RW	comb_uv_weight02
0x5420	COMB CTRL32	0x80	RW	comb_uv_weight03
0x5421	COMB CTRL33	0x80	RW	comb_uv_weight10
0x5422	COMB CTRL34	0x80	RW	comb_uv_weight11

table 7-17 combine control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x5423	COMB CTRL35	0x60	RW	comb_uv_weight12
0x5424	COMB CTRL36	0x40	RW	comb_uv_weight13
0x5425	COMB CTRL37	0x80	RW	comb_uv_weight20
0x5426	COMB CTRL38	0x80	RW	comb_uv_weight21
0x5427	COMB CTRL39	0x00	RW	comb_uv_weight22
0x5428	COMB CTRL40	0x00	RW	comb_uv_weight23
0x5429	COMB CTRL41	0x80	RW	comb_uv_weight30
0x542A	COMB CTRL42	0x80	RW	comb_uv_weight31
0x542B	COMB CTRL43	0x00	RW	comb_uv_weight32
0x542C	COMB CTRL44	0x00	RW	comb_uv_weight33
0x542D	COMB CTRL45	0x3C	RW	Debug Mode for Combine Bit[7:6]: Not used Bit[5:2]: Fixed value for RO register Bit[1]: Debug mode 2 (EOF to VSYNC fixed value, other than zero) Bit[0]: Debug mode 1 (always fixed value)
0xC30C	COMB_CTRL_PT1	0x00	RW	Bit[7:0]: Combine control point number 1
0xC30D	COMB_CTRL_PT2	0x01	RW	Bit[7:0]: Combine control point number 2
0xC30E	COMB_CTRL_PT3	0x02	RW	Bit[7:0]: Combine control point number 3
0xC30F	COMB_CTRL_PT4	0x03	RW	Bit[7:0]: Combine control point number 4
0xC4B4	CUT_BL_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: Cut black level 0: Disable 1: Enable
0xC4B5	DARKBOOST_AUTO_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: Dark boost auto switch 0: Disable 1: Enable
0xC4B6	AUTO_LOW_LEVEL_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: Auto low level 0: Disable 1: Enable
0xC4BC	MAX_CURVE_GAIN_1	0x00	RW	Bit[7:0]: Max curve gain[15:8]
0xC4BD	MAX_CURVE_GAIN_2	0x90	RW	Bit[7:0]: Max curve gain[7:0]

table 7-17 combine control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0xC4BE	MANUAL_GAMMA_1	0x02	RW	Bit[7:0]: Manual gamma[15:8]
0xC4BF	MANUAL_GAMMA_2	0x00	RW	Bit[7:0]: Manual gamma[7:0]
0xC4C0	DB_GAIN_THRE_11	0x00	RW	Bit[7:0]: Dark boost gain threshold 1[15:8]
0xC4C1	DB_GAIN_THRE_12	0x20	RW	Bit[7:0]: Dark boost gain threshold 1[7:0]
0xC4C2	DB_GAIN_THRE_21	0x00	RW	Bit[7:0]: Dark boost gain threshold 2[15:8]
0xC4C3	DB_GAIN_THRE_22	0x80	RW	Bit[7:0]: Dark boost gain threshold 2[7:0]
0xC4C4	DB_AMT	0x10	RW	Dark Boost Amount
0xC4C5	DB_AMT_MIN	0x00	RW	Min Dark Boost Amount
0xC4C6	DB_AMT_MAX	0x10	RW	Max Dark Boost Amount
0xC4C7	ERROR_STEP	0x04	RW	Combine Error Compensation Step
0xC4C8	DB_MAX_GAMMA_1	0x03	RW	Bit[7:0]: Max dark boost gamma[15:8]
0xC4C9	DB_MAX_GAMMA_2	0xA0	RW	Bit[7:0]: Max dark boost gamma[7:0]
0xC4CA	DARK_TONE_WIDTH_1	0x10	RW	Bit[7:0]: Dark boost tone width[15:8]
0xC4CB	DARK_TONE_WIDTH_2	0x00	RW	Bit[7:0]: Dark boost tone width[7:0]
0x5A08~ 0x5A97	COMB_R	–	R	Debug Information for Combine Control Registers
0x5C18	COMB_RW01	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf0[10:8]
0x5C19	COMB_RW02	0x00	RW	Bit[7:0]: pLocalGainBuf0[7:0]
0x5C1A	COMB_RW03	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf1[10:8]
0x5C1B	COMB_RW04	0x00	RW	Bit[7:0]: pLocalGainBuf1[7:0]
0x5C1C	COMB_RW05	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf2[10:8]
0x5C1D	COMB_RW06	0x00	RW	Bit[7:0]: pLocalGainBuf2[7:0]
0x5C1E	COMB_RW07	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf3[10:8]
0x5C1F	COMB_RW08	0x00	RW	Bit[7:0]: pLocalGainBuf3[7:0]
0x5C20	COMB_RW09	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf4[10:8]
0x5C21	COMB_RW10	0x00	RW	Bit[7:0]: pLocalGainBuf4[7:0]

table 7-17 combine control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x5C22	COMB_RW11	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf5[10:8]
0x5C23	COMB_RW12	0x00	RW	Bit[7:0]: pLocalGainBuf5[7:0]
0x5C24	COMB_RW13	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf6[10:8]
0x5C25	COMB_RW14	0x00	RW	Bit[7:0]: pLocalGainBuf6[7:0]
0x5C26	COMB_RW15	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf7[10:8]
0x5C27	COMB_RW16	0x00	RW	Bit[7:0]: pLocalGainBuf7[7:0]
0x5C28	COMB_RW17	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf8[10:8]
0x5C29	COMB_RW18	0x00	RW	Bit[7:0]: pLocalGainBuf8[7:0]
0x5C2A	COMB_RW19	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf9[10:8]
0x5C2B	COMB_RW20	0x00	RW	Bit[7:0]: pLocalGainBuf9[7:0]
0x5C2C	COMB_RW21	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf10[10:8]
0x5C2D	COMB_RW22	0x00	RW	Bit[7:0]: pLocalGainBuf10[7:0]
0x5C2E	COMB_RW23	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf11[10:8]
0x5C2F	COMB_RW24	0x00	RW	Bit[7:0]: pLocalGainBuf11[7:0]
0x5C30	COMB_RW25	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf12[10:8]
0x5C31	COMB_RW26	0x00	RW	Bit[7:0]: pLocalGainBuf12[7:0]
0x5C32	COMB_RW27	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf13[10:8]
0x5C33	COMB_RW28	0x00	RW	Bit[7:0]: pLocalGainBuf13[7:0]
0x5C34	COMB_RW29	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf14[10:8]
0x5C35	COMB_RW30	0x00	RW	Bit[7:0]: pLocalGainBuf14[7:0]
0x5C36	COMB_RW31	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf15[10:8]
0x5C37	COMB_RW32	0x00	RW	Bit[7:0]: pLocalGainBuf15[7:0]

table 7-17 combine control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x5C38	COMB_RW33	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf16[10:8]
0x5C39	COMB_RW34	0x00	RW	Bit[7:0]: pLocalGainBuf16[7:0]
0x5C3A	COMB_RW35	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf17[10:8]
0x5C3B	COMB_RW36	0x00	RW	Bit[7:0]: pLocalGainBuf17[7:0]
0x5C3C	COMB_RW37	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf18[10:8]
0x5C3D	COMB_RW38	0x00	RW	Bit[7:0]: pLocalGainBuf18[7:0]
0x5C3E	COMB_RW39	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf19[10:8]
0x5C3F	COMB_RW40	0x00	RW	Bit[7:0]: pLocalGainBuf19[7:0]
0x5C40	COMB_RW41	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf20[10:8]
0x5C41	COMB_RW42	0x00	RW	Bit[7:0]: pLocalGainBuf20[7:0]
0x5C42	COMB_RW43	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf21[10:8]
0x5C43	COMB_RW44	0x00	RW	Bit[7:0]: pLocalGainBuf21[7:0]
0x5C44	COMB_RW45	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf22[10:8]
0x5C45	COMB_RW46	0x00	RW	Bit[7:0]: pLocalGainBuf22[7:0]
0x5C46	COMB_RW47	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf23[10:8]
0x5C47	COMB_RW48	0x00	RW	Bit[7:0]: pLocalGainBuf23[7:0]
0x5C48	COMB_RW49	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pLocalGainBuf24[10:8]
0x5C49	COMB_RW50	0x00	RW	Bit[7:0]: pLocalGainBuf24[7:0]
0x5C4A	COMB_RW51	0x00	RW	Bit[7:6]: Not used Bit[5:0]: AWBLogRatio_R[13:8] Two's complement
0x5C4B	COMB_RW52	0x00	RW	Bit[7:0]: AWBLogRatio_R[7:0] Two's complement
0x5C4C	COMB_RW53	0x00	RW	Bit[7:6]: Not used Bit[5:0]: AWBLogRatio_G[13:8] Two's complement

table 7-17 combine control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x5C4D	COMB_RW54	0x00	RW	Bit[7:0]: AWBLogRatio_G[7:0] Two's complement
0x5C4E	COMB_RW55	0x00	RW	Bit[7:6]: Not used Bit[5:0]: AWBLogRatio_B[13:8] Two's complement
0x5C4F	COMB_RW56	0x00	RW	Bit[7:0]: AWBLogRatio_B[7:0] Two's complement
0x5C50	NOT USED	–	–	Not Used
0x5C51	COMB_RW58	0x00	RW	Bit[7:1]: Not used Bit[0]: LogBlackX[16] Two's complement
0x5C52	COMB_RW59	0x1F	RW	Bit[7:0]: LogBlackX[15:8] Two's complement
0x5C53	COMB_RW60	0x37	RW	Bit[7:0]: LogBlackX[7:0] Two's complement
0x5C54	NOT USED	–	–	Not Used
0x5C55	COMB_RW62	0x00	RW	Bit[7:1]: Not used Bit[0]: LogBlackY[16] Two's complement
0x5C56	COMB_RW63	0x45	RW	Bit[7:0]: LogBlackY[15:8] Two's complement
0x5C57	COMB_RW64	0x97	RW	Bit[7:0]: LogBlackY[7:0] Two's complement
0x5C58	COMB_RW65	0x65	RW	Bit[7:0]: LogYMax[15:8]
0x5C59	COMB_RW66	0x97	RW	Bit[7:0]: LogYMax[7:0]
0x5C5A	COMB_RW67	0x65	RW	Bit[7:0]: LogXMax[15:8]
0x5C5B	COMB_RW68	0x97	RW	Bit[7:0]: LogXMax[7:0]
0x5C5C	COMB_RW69	0x15	RW	Bit[7]: Not used Bit[6:0]: GlobalLogRatio[14:8]
0x5C5D	COMB_RW70	0x97	RW	Bit[7:0]: GlobalLogRatio[7:0]
0x5C5E	COMB_RW71	0x00	RW	Bit[7]: Not used Bit[6:0]: GlobalLogWDRGain[14:8]
0x5C5F	COMB_RW72	0x00	RW	Bit[7:0]: GlobalLogWDRGain[7:0]
0x5C60	COMB_RW73	0x01	RW	Bit[7:2]: Not used Bit[1:0]: GlobalLogWDRGamma[9:8]

table 7-17 combine control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x5C61	COMB_RW74	0xD1	RW	Bit[7:0]: GlobalLogWDRGamma[7:0]
0x5C62	COMB_RW75	0x01	RW	Bit[7:2]: Not used Bit[1:0]: nCutBlackLevel[9:8]
0x5C63	COMB_RW76	0x00	RW	Bit[7:0]: nCutBlackLevel[7:0]
0x5C64	COMB_RW77	0x55	RW	Bit[7:0]: nDarkBoostYThre1[15:8]
0x5C65	COMB_RW78	0x97	RW	Bit[7:0]: nDarkBoostYThre1[7:0]
0x5C66	COMB_RW79	0x5D	RW	Bit[7:0]: nDarkBoostYThre2[15:8]
0x5C67	COMB_RW80	0x97	RW	Bit[7:0]: nDarkBoostYThre2[7:0]
0x5C68~ 0x5C69	NOT USED	–	–	Not Used
0x5C6A	COMB_RW83	0x00	RW	Bit[7:0]: nLogE[15:8] Two's complement
0x5C6B	COMB_RW84	0x00	RW	Bit[7:0]: nLogE[7:0] Two's complement
0x5C6C	COMB_RW85	0x00	RW	Not Used
0x5C6D	COMB_RW86	0x00	RW	Bit[7:2]: Not used Bit[1:0]: OutputRange[17:16]
0x5C6E	COMB_RW87	0x19	RW	Bit[7:0]: OutputRange[15:8]
0x5C6F	COMB_RW88	0xF9	RW	Bit[7:0]: OutputRange[7:0]

7.18 NMLZ control [0x5480 - 0x5C78]

table 7-18 NMLZ control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5480	NORM RW00	0x21	RW	Bit[7:5]: Not used Bit[4:0]: step
0x5481	NORM RW01	0x10	RW	Bit[7]: Not used Bit[6:0]: max_low_level 16 ~ 127
0x5482	NORM RW02	0xF8	RW	Bit[7:0]: min_low_level -128 to -16, complementary code

table 7-18 NMLZ control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5483	NORM RW03	0x04	RW	Bit[7]: Not used Bit[6:0]: ps_thres[14:8]
0x5484	NORM RW04	0x00	RW	Bit[7:0]: ps_thres[7:0]
0x5485~ 0x5A98	NORM RO	–	R	Debug Information for NMLZ Control
0x5C71	NML_RW02	0x00	RW	Bit[7:6]: Not used Bit[5:0]: nNormalizeGain[21:16]
0x5C72	NML_RW03	0x2A	RW	Bit[7:0]: nNormalizeGain[15:8]
0x5C73	NML_RW04	0x28	RW	Bit[7:0]: nNormalizeGain[7:0]
0x5C74	NOT USED	–	–	Not Used
0x5C75	NML_RW06	0x00	RW	Bit[7:2]: Not used Bit[1:0]: nWDROffset[17:16]
0x5C76	NML_RW07	0x01	RW	Bit[7:0]: nWDROffset[15:8]
0x5C77	NML_RW08	0xAF	RW	Bit[7:0]: nWDROffset[7:0]
0x5C78	NML_RW09	0x00	RW	Bit[7:0]: RW_CurLowLevel[7:0] Signed complementary code

7.19 TMAP control [0x5500 - 0x5CFB]

table 7-19 TMAP control registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x5500	TOMP RW00	0x03	RW	Bit[7:3]: Not used Bit[2:0]: edge_thre 000: 16 001: 32 010: 64 011: 128 100: 256 101: 512

table 7-19 TMAP control registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x5501	TOMP RW01	0x3A	RW	Bit[7:6]: Not used Bit[5]: h_dark_en Bit[4]: uv_dark_en Bit[3:2]: h_dark_thre 00: 16 01: 32 10: 48 11: 64 Bit[1:0]: uv_dark_thre 00: 16 01: 32 10: 48 11: 64
0x5502	TOMP RW02	0x00	RW	Bit[7:1]: Not used Bit[0]: curve_step[8]
0x5503	TOMP RW03	0x40	RW	Bit[7:0]: curve_step[7:0]
0x5504	TOMP RW04	0xC6	RW	Bit[7:4]: max_alpha Bit[3:0]: min_alpha
0x5505	TOMP RW05	0x00	RW	Bit[7:4]: Not used Bit[3:0]: alpha
0x5506	TOMP RW06	0x00	RW	Bit[7]: Not used Bit[6:0]: min_dynamic_range[14:8]
0x5507	TOMP RW07	0x40	RW	Bit[7:0]: min_dynamic_range[7:0]
0x5508	TOMP RW08	0x04	RW	Bit[7]: Not used Bit[6:0]: max_dynamic_range[14:8]
0x5509	TOMP RW09	0x00	RW	Bit[7:0]: max_dynamic_range[7:0]
0x550A	TOMP RW10	0x00	RW	Bit[7:0]: dbg_ctrl_0
0x550B	TOMP RW11	0x00	RW	Bit[7:0]: dbg_ctrl_1
0x550C	TOMP RW12	0x00	RW	Bit[7:0]: dbg_ctrl_2
0x550D	TOMP RW13	0x00	RW	Bit[7:1]: Not used Bit[0]: dbg_sram_freeze
0x550E	TOMP RW14	0x00	RW	Bit[7:0]: dbg_addr
0x550F~ 0x5511	TOMP RO	–	R	Debug Information for TMAP Control
0xC4E4	CONTRAST_CURVE_1	0x10	RW	Contrast Curve 1
0xC4E5	CONTRAST_CURVE_2	0x20	RW	Contrast Curve 2
0xC4E6	CONTRAST_CURVE_3	0x30	RW	Contrast Curve 3

table 7-19 TMAP control registers (sheet 3 of 9)

address	register name	default value	R/W	description
0xC4E7	CONTRAST_CURVE_4	0x40	RW	Contrast Curve 4
0xC4E8	CONTRAST_CURVE_5	0x50	RW	Contrast Curve 5
0xC4E9	CONTRAST_CURVE_6	0x60	RW	Contrast Curve 6
0xC4EA	CONTRAST_CURVE_7	0x70	RW	Contrast Curve 7
0xC4EB	CONTRAST_CURVE_8	0x80	RW	Contrast Curve 8
0xC4EC	CONTRAST_CURVE_9	0x90	RW	Contrast Curve 9
0xC4ED	CONTRAST_CURVE_10	0xA0	RW	Contrast Curve 10
0xC4EE	CONTRAST_CURVE_11	0xB0	RW	Contrast Curve 11
0xC4EF	CONTRAST_CURVE_12	0xC0	RW	Contrast Curve 12
0xC4F0	CONTRAST_CURVE_13	0xD0	RW	Contrast Curve 13
0xC4F1	CONTRAST_CURVE_14	0xE0	RW	Contrast Curve 14
0xC4F2	CONTRAST_CURVE_15	0xF0	RW	Contrast Curve 15
0xC4F3	CURVE_STEP	0x80	RW	Curve Adjustment Step
0xC4F4	CURVE_MIN_DR_1	0x00	RW	Bit[7:0]: Curve min dynamic range[15:8]
0xC4F5	CURVE_MIN_DR_2	0x20	RW	Bit[7:0]: Curve min dynamic range[7:0]
0xC4F6	CURVE_MAX_DR_1	0x02	RW	Bit[7:0]: Curve max dynamic range[15:8]
0xC4F7	CURVE_MAX_DR_2	0x00	RW	Bit[7:0]: Curve max dynamic range[7:0]
0xC4F8	CURVE_MIN_ALPHA	0x00	RW	Min Curve Alpha
0xC4F9	CURVE_MAX_ALPHA	0x0A	RW	Max Curve Alpha
0x5A9C~ 0x5AAD	TMP_R	–	R	Debug Information for TMAP Control
0x5C7D	TMP_RW02	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList0[17:16]
0x5C7E	TMP_RW03	0x40	RW	Bit[7:0]: pCurveList0[15:8]
0x5C7F	TMP_RW04	0x00	RW	Bit[7:0]: pCurveList0[7:0]
0x5C80	NOT USED	–	–	Not Used
0x5C81	TMP_RW06	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList1[17:16]
0x5C82	TMP_RW07	0x80	RW	Bit[7:0]: pCurveList1[15:8]
0x5C83	TMP_RW08	0x00	RW	Bit[7:0]: pCurveList1[7:0]

table 7-19 TMAP control registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x5C84	NOT USED	–	–	Not Used
0x5C85	TMP_RW10	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList2[17:16]
0x5C86	TMP_RW11	0xC0	RW	Bit[7:0]: pCurveList2[15:8]
0x5C87	TMP_RW12	0x00	RW	Bit[7:0]: pCurveList2[7:0]
0x5C88	NOT USED	–	–	Not Used
0x5C89	TMP_RW14	0x10	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList3[17:16]
0x5C8A	TMP_RW15	0x00	RW	Bit[7:0]: pCurveList3[15:8]
0x5C8B	TMP_RW16	0x00	RW	Bit[7:0]: pCurveList3[7:0]
0x5C8C	NOT USED	–	–	Not Used
0x5C8D	TMP_RW18	0x10	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList4[17:16]
0x5C8E	TMP_RW19	0x40	RW	Bit[7:0]: pCurveList4[15:8]
0x5C8F	TMP_RW20	0x00	RW	Bit[7:0]: pCurveList4[7:0]
0x5C90	NOT USED	–	–	Not Used
0x5C91	TMP_RW22	0x10	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList5[17:16]
0x5C92	TMP_RW23	0x80	RW	Bit[7:0]: pCurveList5[15:8]
0x5C93	TMP_RW24	0x00	RW	Bit[7:0]: pCurveList5[7:0]
0x5C94	NOT USED	–	–	Not Used
0x5C95	TMP_RW26	0x10	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList6[17:16]
0x5C96	TMP_RW27	0xC0	RW	Bit[7:0]: pCurveList6[15:8]
0x5C97	TMP_RW28	0x00	RW	Bit[7:0]: pCurveList6[7:0]
0x5C98	NOT USED	–	–	Not Used
0x5C99	TMP_RW30	0x20	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList7[17:16]
0x5C9A	TMP_RW31	0x00	RW	Bit[7:0]: pCurveList7[15:8]
0x5C9B	TMP_RW32	0x00	RW	Bit[7:0]: pCurveList7[7:0]
0x5C9C	NOT USED	–	–	Not Used

table 7-19 TMAP control registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x5C9D	TMP_RW34	0x20	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList8[17:16]
0x5C9E	TMP_RW35	0x40	RW	Bit[7:0]: pCurveList8[15:8]
0x5C9F	TMP_RW36	0x00	RW	Bit[7:0]: pCurveList8[7:0]
0x5CA0	NOT USED	–	–	Not Used
0x5CA1	TMP_RW38	0x20	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList9[17:16]
0x5CA2	TMP_RW39	0x80	RW	Bit[7:0]: pCurveList9[15:8]
0x5CA3	TMP_RW40	0x00	RW	Bit[7:0]: pCurveList9[7:0]
0x5CA4	NOT USED	–	–	Not Used
0x5CA5	TMP_RW42	0x20	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList10[17:16]
0x5CA6	TMP_RW43	0xC0	RW	Bit[7:0]: pCurveList10[15:8]
0x5CA7	TMP_RW44	0x00	RW	Bit[7:0]: pCurveList10[7:0]
0x5CA8	NOT USED	–	–	Not Used
0x5CA9	TMP_RW46	0x30	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList11[17:16]
0x5CAA	TMP_RW47	0x00	RW	Bit[7:0]: pCurveList11[15:8]
0x5CAB	TMP_RW48	0x00	RW	Bit[7:0]: pCurveList11[7:0]
0x5CAC	NOT USED	–	–	Not Used
0x5CAD	TMP_RW50	0x30	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList12[17:16]
0x5CAE	TMP_RW51	0x40	RW	Bit[7:0]: pCurveList12[15:8]
0x5CAF	TMP_RW52	0x00	RW	Bit[7:0]: pCurveList12[7:0]
0x5CB0	NOT USED	–	–	Not Used
0x5CB1	TMP_RW54	0x30	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList13[17:16]
0x5CB2	TMP_RW55	0x80	RW	Bit[7:0]: pCurveList13[15:8]
0x5CB3	TMP_RW56	0x00	RW	Bit[7:0]: pCurveList13[7:0]
0x5CB4	NOT USED	–	–	Not Used
0x5CB5	TMP_RW58	0x30	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList14[17:16]

table 7-19 TMAP control registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x5CB6	TMP_RW59	0xC0	RW	Bit[7:0]: pCurveList14[15:8]
0x5CB7	TMP_RW60	0x00	RW	Bit[7:0]: pCurveList14[7:0]
0x5CB8	NOT USED	–	–	Not Used
0x5CB9	TMP_RW62	0x30	RW	Bit[7:2]: Not used Bit[1:0]: pCurveList15[17:16]
0x5CBA	TMP_RW63	0xFF	RW	Bit[7:0]: pCurveList15[15:8]
0x5CBB	TMP_RW64	0xFF	RW	Bit[7:0]: pCurveList15[7:0]
0x5CBC	TMP_RW65	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList0[9:8]
0x5CBD	TMP_RW66	0x00	RW	Bit[7:0]: pCurveGainList0[7:0]
0x5CBE	TMP_RW67	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList1[9:8]
0x5CBF	TMP_RW68	0x00	RW	Bit[7:0]: pCurveGainList1[7:0]
0x5CC0	TMP_RW69	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList2[9:8]
0x5CC1	TMP_RW70	0x00	RW	Bit[7:0]: pCurveGainList2[7:0]
0x5CC2	TMP_RW71	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList3[9:8]
0x5CC3	TMP_RW72	0x00	RW	Bit[7:0]: pCurveGainList3[7:0]
0x5CC4	TMP_RW73	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList4[9:8]
0x5CC5	TMP_RW74	0x00	RW	Bit[7:0]: pCurveGainList4[7:0]
0x5CC6	TMP_RW75	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList5[9:8]
0x5CC7	TMP_RW76	0x00	RW	Bit[7:0]: pCurveGainList5[7:0]
0x5CC8	TMP_RW77	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList6[9:8]
0x5CC9	TMP_RW78	0x00	RW	Bit[7:0]: pCurveGainList6[7:0]
0x5CCA	TMP_RW79	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList7[9:8]
0x5CCB	TMP_RW80	0x00	RW	Bit[7:0]: pCurveGainList7[7:0]
0x5CCC	TMP_RW81	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList8[9:8]

table 7-19 TMAP control registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x5CCD	TMP_RW82	0x00	RW	Bit[7:0]: pCurveGainList8[7:0]
0x5CCE	TMP_RW83	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList9[9:8]
0x5CCF	TMP_RW84	0x00	RW	Bit[7:0]: pCurveGainList9[7:0]
0x5CD0	TMP_RW85	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList10[9:8]
0x5CD1	TMP_RW86	0x00	RW	Bit[7:0]: pCurveGainList10[7:0]
0x5CD2	TMP_RW87	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList11[9:8]
0x5CD3	TMP_RW88	0x00	RW	Bit[7:0]: pCurveGainList11[7:0]
0x5CD4	TMP_RW89	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList12[9:8]
0x5CD5	TMP_RW90	0x00	RW	Bit[7:0]: pCurveGainList12[7:0]
0x5CD6	TMP_RW91	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList13[9:8]
0x5CD7	TMP_RW92	0x00	RW	Bit[7:0]: pCurveGainList13[7:0]
0x5CD8	TMP_RW93	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList14[9:8]
0x5CD9	TMP_RW94	0x00	RW	Bit[7:0]: pCurveGainList14[7:0]
0x5CDA	TMP_RW95	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pCurveGainList15[9:8]
0x5CDB	TMP_RW96	0x00	RW	Bit[7:0]: pCurveGainList15[7:0]
0x5CDC	TMP_RW97	0x01	RW	Bit[7:0]: pCurveSegAList0[7:0]
0x5CDD	TMP_RW98	0x01	RW	Bit[7:0]: pCurveSegAList1[7:0]
0x5CDE	TMP_RW99	0x01	RW	Bit[7:0]: pCurveSegAList2[7:0]
0x5CDF	TMP_RW100	0x01	RW	Bit[7:0]: pCurveSegAList3[7:0]
0x5CE0	TMP_RW101	0x01	RW	Bit[7:0]: pCurveSegAList4[7:0]
0x5CE1	TMP_RW102	0x01	RW	Bit[7:0]: pCurveSegAList5[7:0]
0x5CE2	TMP_RW103	0x01	RW	Bit[7:0]: pCurveSegAList6[7:0]
0x5CE3	TMP_RW104	0x01	RW	Bit[7:0]: pCurveSegAList7[7:0]
0x5CE4	TMP_RW105	0x01	RW	Bit[7:0]: pCurveSegAList8[7:0]
0x5CE5	TMP_RW106	0x01	RW	Bit[7:0]: pCurveSegAList9[7:0]

table 7-19 TMAP control registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x5CE6	TMP_RW107	0x01	RW	Bit[7:0]: pCurveSegAList10[7:0]
0x5CE7	TMP_RW108	0x01	RW	Bit[7:0]: pCurveSegAList11[7:0]
0x5CE8	TMP_RW109	0x01	RW	Bit[7:0]: pCurveSegAList12[7:0]
0x5CE9	TMP_RW110	0x01	RW	Bit[7:0]: pCurveSegAList13[7:0]
0x5CEA	TMP_RW111	0x01	RW	Bit[7:0]: pCurveSegAList14[7:0]
0x5CEB	TMP_RW112	0x80	RW	Bit[7:0]: pCurveSegAList15[7:0]
0x5CEC	TMP_RW113	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList0[4:0]
0x5CED	TMP_RW114	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList1[4:0]
0x5CEE	TMP_RW115	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList2[4:0]
0x5CEF	TMP_RW116	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList3[4:0]
0x5CF0	TMP_RW117	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList4[4:0]
0x5CF1	TMP_RW118	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList5[4:0]
0x5CF2	TMP_RW119	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList6[4:0]
0x5CF3	TMP_RW120	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList7[4:0]
0x5CF4	TMP_RW121	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList8[4:0]
0x5CF5	TMP_RW122	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList9[4:0]
0x5CF6	TMP_RW123	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList10[4:0]
0x5CF7	TMP_RW124	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList11[4:0]
0x5CF8	TMP_RW125	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList12[4:0]
0x5CF9	TMP_RW126	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList13[4:0]
0x5CFA	TMP_RW127	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList14[4:0]

table 7-19 TMAP control registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x5CFB	TMP_RW128	0x15	RW	Bit[7:5]: Not used Bit[4:0]: pCurveSegBList15[4:0]

7.20 FC control [0x4200 - 0x4203]

table 7-20 FC control

address	register name	default value	R/W	description
0x4200	FC_R0	0x00	RW	Bit[7:3]: Not used Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fcnt_reset
0x4201	FC_R1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_on_number
0x4202	FC_R2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_off_number
0x4203	FC_R3	0x00	RW	Bit[7]: Not used Bit[6]: rblue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

7.21 format control [0x4300 - 0x4309]

table 7-21 format control (sheet 1 of 2)

address	register name	default value	R/W	description
0x4300	FORMAT_CTRL00	0xF8	RW	Bit[7:4]: Output format select 0x3: YUV mode 0xF: RAW mode Others: Not allowed Bit[3:0]: pix_order_ctrl
0x4302	FORMAT_YMAX	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Ymax[9:8]

table 7-21 format control (sheet 2 of 2)

address	register name	default value	R/W	description
0x4303	FORMAT_YMAX	0xFF	RW	Bit[7:0]: Ymax[7:0]
0x4304	FORMAT_YMIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Ymin[9:8]
0x4305	FORMAT_YMIN	0x00	RW	Bit[7:0]: Ymin[7:0]
0x4306	FORMAT_UMAX	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Umax[9:8]
0x4307	FORMAT_UMAX	0xFF	RW	Bit[7:0]: Umax[7:0]
0x4308	FORMAT_UMIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Umin[9:8]
0x4309	FORMAT_UMIN	0x00	RW	Bit[7:0]: Umin[7:0]

7.22 VFIFO control [0x4600 - 0x4639]

table 7-22 VFIFO control (sheet 1 of 4)

address	register name	default value	R/W	description
0x4600	VFIFO_AFIFO_SRAM_CTRL	0x04	RW	Bit[7:4]: Not used Bit[3]: r_fi_pt AFIFO bypass Bit[2]: r_16bitin 16-bit data into AFIFO Bit[1]: r_sram_pt Bit[0]: r_sram_nofrst
0x4601	VFIFO_READ_CTRL	0x14	RW	Bit[7:4]: Ipcnt control Bit[3]: Ipcnt free Bit[2:0]: read sel 00: Rstartp sel 01: Read SRAM signal sel/href_o start, end point control 10: Read start point sel 11: Not valid
0x4602	VFIFO_FIRST1_POSITION	0x00	RW	Bit[7:0]: r_first_pos_high
0x4603	VFIFO_FIRST1_POSITION	0x00	RW	Bit[7:0]: r_first_pos_low

table 7-22 VFIFO control (sheet 2 of 4)

address	register name	default value	R/W	description
0x4605	VFIFO_LLEN_FIRS1_SEL	0x08	RW	Bit[7:4]: Not used Bit[3]: r_8b_yuv422 0: 10-bit YUV422 mode 1: 8-bit YUV422 mode Bit[2]: Line length select 0: Auto cal 1: From register Bit[1:0]: r_first_sel in readout module
0x4606	VFIFO_LINE_LENGTH_MAN	0x00	RW	Bit[7:0]: Manual set line length[15:8]
0x4607	VFIFO_LINE_LENGTH_MAN	0x00	RW	Bit[7:0]: Manual set line length[7:0]
0x4608	VFIFO_READ_START	0x00	RW	Bit[7:0]: Read start[15:8]
0x4609	VFIFO_READ_START	0x08	RW	Bit[7:0]: Read start[7:0]
0x460A	VFIFO_HSYNC_START_POSITION	0x00	RW	Bit[7:0]: r_hsync_st[15:8]
0x460B	VFIFO_HSYNC_START_POSITION	0xBF	RW	Bit[7:0]: r_hsync_st[7:0]
0x460C	VFIFO_HSYNC_CTRL	0x00	RW	Bit[7:4]: HSYNC header width Bit[3:0]: HSYNC trail width
0x460D	VFIFO_SRAM_TST_CTRL	0x0F	RW	Bit[7:5]: Not used Bit[4]: VFIFO TEST1 Bit[3:0]: VFIFO RM
0x460E	VFIFO_EMBD_LINE_CTRL	0x08	RW	Bit[7:4]: Not used Bit[3]: r_sof_clr_ram default 1 Bit[2]: r_st_mod 0: PCLK cycles trigger (default) 1: Byte size trigger Bit[1]: r_embd_rom Test ROM via embedded line enable Bit[0]: r_embd_en Embedded line mode enable
0x460F	VFIFO_EMBD_LINE_NUM	0x01	RW	Bit[7:0]: Embedded line amount

table 7-22 VFIFO control (sheet 3 of 4)

address	register name	default value	R/W	description
0x4620	ROI_CTRL0	0x0E	RW	Bit[7]: r_roi_sync_byp = r_roi0[7]: // 1'b0 Bit[6]: r_fr_comp ROI output 8-bit data Front comp 2-bit 0 or back Bit[5]: r_full_dat_mod = r_roi0[5]: //1'b0 Bit[4]: Not used Bit[3]: r_roi_en_3 = r_roi0[3] Bit[2]: r_roi_en_2 = r_roi0[2] Bit[1]: r_roi_en_1 = r_roi0[1] Bit[0]: r_roi_func_e = r_roi0[0]
0x4621	ROI_CTRL1	0x31	RW	Bit[7]: Not used Bit[6:4]: r_sc_fsz_delay Delay default 3 Bit[3:0]: roi_sync_cod_stv Sync code start value default 1 manual setting 8 at maximum
0x4622	ROI_XOFFS_1	0x00	RW	Window 1 Xoffset High Byte
0x4623	ROI_XOFFS_1	0x00	RW	Window 1 Xoffset Low Byte
0x4624	ROI_YOFFS_1	0x00	RW	Window 1 Yoffset High Byte
0x4625	ROI_YOFFS_1	0x00	RW	Window 1 Yoffset Low Byte
0x4626	ROI_XOFFS_2	0x02	RW	Window 2 Xoffset High Byte
0x4627	ROI_XOFFS_2	0x4E	RW	Window 2 Xoffset Low Byte
0x4628	ROI_YOFFS_2	0x01	RW	Window 2 Yoffset High Byte
0x4629	ROI_YOFFS_2	0x5E	RW	Window 2 Yoffset Low Byte
0x462A	ROI_XOFFS_3	0x04	RW	Window 3 Xoffset High Byte
0x462B	ROI_XOFFS_3	0x9C	RW	Window 3 Xoffset Low Byte
0x462C	ROI_YOFFS_3	0x02	RW	Window 3 Yoffset High Byte
0x462D	ROI_YOFFS_3	0xBC	RW	Window 3 Yoffset Low Byte
0x462E	ROI_HSIZE1_H	0x00	RW	Bit[7:1]: Not used Bit[0]: Window 1 hsize[8]
0x462F	ROI_HSIZE1_L	0x64	RW	Bit[7:0]: Window 1 hsize[7:0]
0x4630	ROI_VSIZE1_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: roi_vsize1[9:8]
0x4631	ROI_VSIZE1_L	0x64	RW	Bit[7:0]: roi_vsize1[7:0]
0x4632	ROI_HSIZE2_H	0x00	RW	Bit[7:1]: Not used Bit[0]: roi_hsize2[8]

table 7-22 VFIFO control (sheet 4 of 4)

address	register name	default value	R/W	description
0x4633	ROI_HSIZE2_L	0x64	RW	Bit[7:0]: roi_hsize2[7:0]
0x4634	ROI_VSIZE2_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: r_roi_vsize2[9:8]
0x4635	ROI_VSIZE2_L	0x64	RW	Bit[7:0]: r_roi_vsize2[7:0]
0x4636	ROI_HSIZE3_H	0x00	RW	Bit[7:1]: Not used Bit[0]: r_roi_hsize3[8]
0x4637	ROI_HSIZE3_L	0x64	RW	Bit[7:0]: r_roi_hsize3[7:0]
0x4638	ROI_VSIZE3_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: r_roi_vsize3[9:8]
0x4639	ROI_VSIZE3_L	0x64	RW	Bit[7:0]: r_roi_vsize3[7:0]

7.23 DVP control [0x4700 - 0x470D]

table 7-23 DVP control (sheet 1 of 2)

address	register name	default value	R/W	description
0x4700	DVP_MOD_SEL	0x04	RW	Bit[7:4]: Not used Bit[3]: CCIR v select Bit[2]: CCIR f value Bit[1]: CCIR656 mode enable Bit[0]: HSYNC mode enable
0x4701	DVP_VSYNC_WIDTH	0x01	RW	VSYNC Length, Line Count
0x4702	DVP_HSYVSY_NEG_WIDTH	0x00	RW	VSYNC Length, Pixel Count High Byte
0x4703	DVP_HSYVSY_NEG_WIDTH	0x01	RW	VSYNC Length, Pixel Count Low Byte
0x4704	DVP_VSYNC_MODE	0x00	RW	Bit[7:4]: Not used Bit[3:2]: r_vsyncout_sel Bit[1]: r_vsync3_mod Bit[0]: r_vsync2_mod
0x4705	DVP_EOF_VSYNC_DELAY	0x00	RW	SOF/EOF Negative Edge to VSYNC Positive Edge High Byte
0x4706	DVP_EOF_VSYNC_DELAY	0x00	RW	SOF/EOF Negative Edge to VSYNC Positive Edge Middle Byte
0x4707	DVP_EOF_VSYNC_DELAY	0x00	RW	SOF/EOF Negative Edge to VSYNC Positive Edge Low Byte

table 7-23 DVP control (sheet 2 of 2)

address	register name	default value	R/W	description
0x4708	DVP_POL_CTRL	0x01	RW	Bit[7]: CLK DDR mode enable Bit[6]: Not used Bit[5]: VSYNC gate clock enable Bit[4]: HREF gate clock enable Bit[3]: No first for FIFO Bit[2]: HREF polarity Bit[1]: VSYNC polarity Bit[0]: PCLK polarity / PCLK gate low enable
0x4709	DVP_MOTO_ORDER	0x00	RW	Bit[7]: fifo_bypass mode Bit[6:4]: Data bit swap Bit[3]: Bit test mode Bit[2]: Bit test 10-bit Bit[1]: Bit test 8-bit Bit[0]: Bit test enable
0x470A	DVP_BYP_SEL	0x00	RW	Bypass Enable High Byte
0x470B	DVP_BYP_SEL	0x00	RW	Bypass Enable Low Byte
0x470C	DVP_ BYPASS	0x00	RW	Bit[7:5]: Not used Bit[4]: href_sel Bit[3:0]: bypass_sel
0x470D	DVP_ROI_HREF_SEL	0x00	RW	Bit[7:3]: Not used Bit[2:0]: ROI HREF output select 000: Combine HREF out via dvp_href_o 001: 1/2 sc HREF out via dvp_href_o 010: ROI window 1 out via dvp_href_o 011: ROI window 2 out via dvp_href_o 100: ROI window 3 out via dvp_href_o

7.24 temperature sensor control [0x6706 - 0x6721]

table 7-24 temperature sensor control (TPM) (sheet 1 of 2)

address	register name	default value	R/W	description
0x6706	TPM_CTRL0	0x71	RW	Bit[7:4]: Reserved Bit[3:0]: Module clock divider

table 7-24 temperature sensor control (TPM) (sheet 2 of 2)

address	register name	default value	R/W	description
0x6707	TPM_STALL	0x00	RW	Bit[0]: tpm_stall
0x6710~ 0x6714	TPM_DB_NUM	–	R	Debug Information for TPM Control
0x6715	TPM_01	–	R	Bit[7]: Sign Bit[6:0]: TPM o1[14:8] Temperature high byte
0x6716	TPM_DB_NUM	–	R	Debug Information for TPM Control
0x6717	TPM_01	–	R	Bit[7:0]: TPM o1[7:0] Temperature low byte
0x6718	TPM_DB_NUM	–	R	Debug Information for TPM Control
0x6719	TPM_02	–	R	If 0x6719 < 192, temperature = 0x6719 If 0x6719 ≥ 192, temperature = -(256-0x6719)
0x6720~ 0x6721	TPM_DB_NUM	–	R	Debug Information for TPM Control

7.25 embedded line control [0x6800 - 0x6807]

table 7-25 embedded line control registers (EMB)

address	register name	default value	R/W	description
0x6800	EMB_LINE_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: emb_line enable
0x6801	EMB_LINE_TAG	0xDA	RW	Bit[7:0]: emb_line tag[9:2]
0x6802	EMB_LINE_TAG	0x01	RW	Bit[7:2]: Not used Bit[1:0]: emb_line tag[1:0]
0x6803	EMB_LINE_SOF_CTRL	0x11	RW	Bit[7:4]: s2h_width Bit[3:0]: sof_width
0x6804	EMB_SIZE_MANU_EN	0x00	RW	Bit[7:1]: Not used Bit[0]: emb_size manual enable
0x6805	EMB_SIZE_MANU	0x04	RW	Bit[7:0]: emb_size[15:8]
0x6806	EMB_SIZE_MANU	0x00	RW	Bit[7:0]: emb_size[7:0]
0x6807	EMB_MASK_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: emb_line mask enable

7.26 group writer [0x6F00 - 0x6F1F]

table 7-26 group writer registers

address	register name	default value	R/W	description
0x6F00	GROUP WRITER COMMAND	0x00	RW	Bit[7:6]: Operation code Bit[5:4]: Group ID Bit[3:2]: Chip debug Bit[1:0]: Group write function enable, must be 2'b11
0x6F04	PARI_ADDR_MIN	0x00	RW	Debug Control
0x6F05	PARI_ADDR_MIN	0x06	RW	Debug Control
0x6F06	PARI_ADDR_MIN	0x00	RW	Group Write Command Register Address, Must Be 0x6F
0x6F07	PARI_ADDR_MIN	0x00	RW	Group Write Command Register Address, Must Be 0x00
0x6F08	PARI_ADDR_MAX	0x00	RW	Debug Control
0x6F09	PARI_ADDR_MAX	0x06	RW	Debug Control
0x6F0A	PARI_ADDR_MAX	0x6D	RW	Group Write Command Register Address, Must Be 0x6F
0x6F0B	PARI_ADDR_MAX	0xFF	RW	Group Write Command Register Address, Must Be 0x00
0x6F0C~ 0x6F1F	PARI_MASTER_SEL	–	RW	Debug Control

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-20°C to +70°C junction temperature
stable image temperature[b]	0°C to +50°C junction temperature

a. sensor functions in the operating range; however, some image quality changes may be noticable at temperature extremes

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-20°C < T_J < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	3.14	3.3	3.47	V
V_{DD-D}	supply voltage (digital)	1.6	1.65	1.7	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.47	V
I_{DD-A}	active (operating) current		60	85	mA
I_{DD-D}			170	240	mA
I_{DD-IO}			30[a]		mA
$I_{DDS-PWDN-A}$	standby current[b]		5		µA
$I_{DDS-PWDN-D}$			270		µA
$I_{DDS-PWDN-IO}$			10		µA
digital inputs (typical conditions: AVDD = 3.3V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[c]	SCL and SDA	-0.5	0.0	0.54	V
V_{IH}[c]	SCL and SDA	1.26	1.8	2.3	V

a. varies with loading

b. standby current based on room temperature

c. based on DOVDD = 1.8V.

8.4 AC characteristics

table 8-4 AC characteristics (T_A = 25°C, V_{DD-A} = 3.3V, V_{DD-IO} = 1.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		48		MHz
DLE	DC differential linearity error		<0.5		LSB
ILE	DC integral linearity error		<0.5		LSB
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-5 timing characteristics

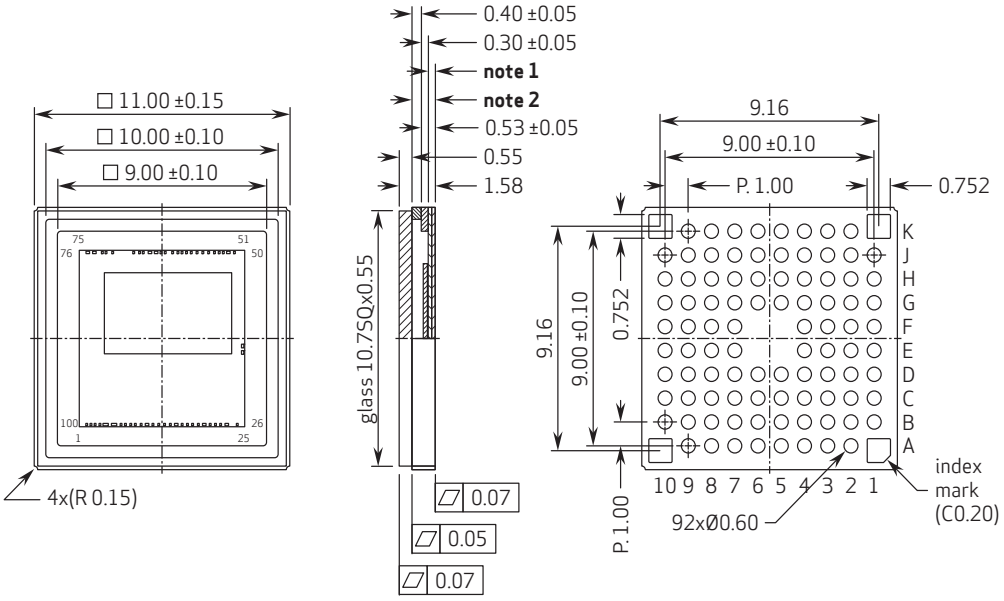
symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)		24		MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using the internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications



note 1 0.30 ±0.05 (0.15x2) (including alumina coat)

note 2 1.00 ±0.10 (including alumina coat)

10633_CLGA_DS_9_1

9.2 IR reflow specifications

note
The OV10633/OV10133 uses a lead free package.

figure 9-2 IR reflow ramp rate requirements

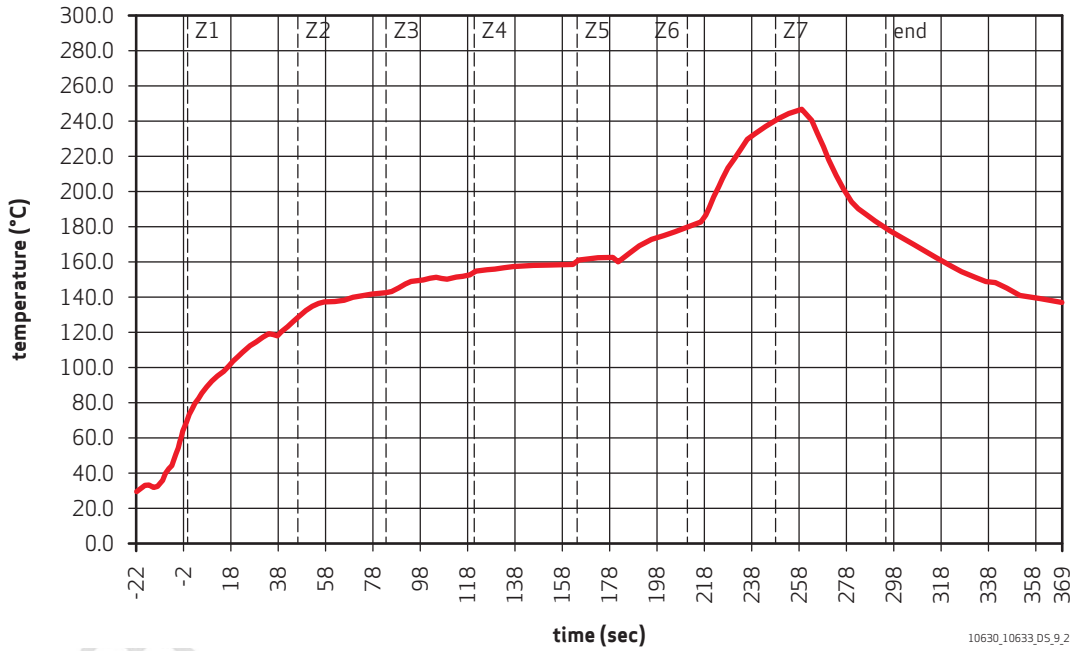


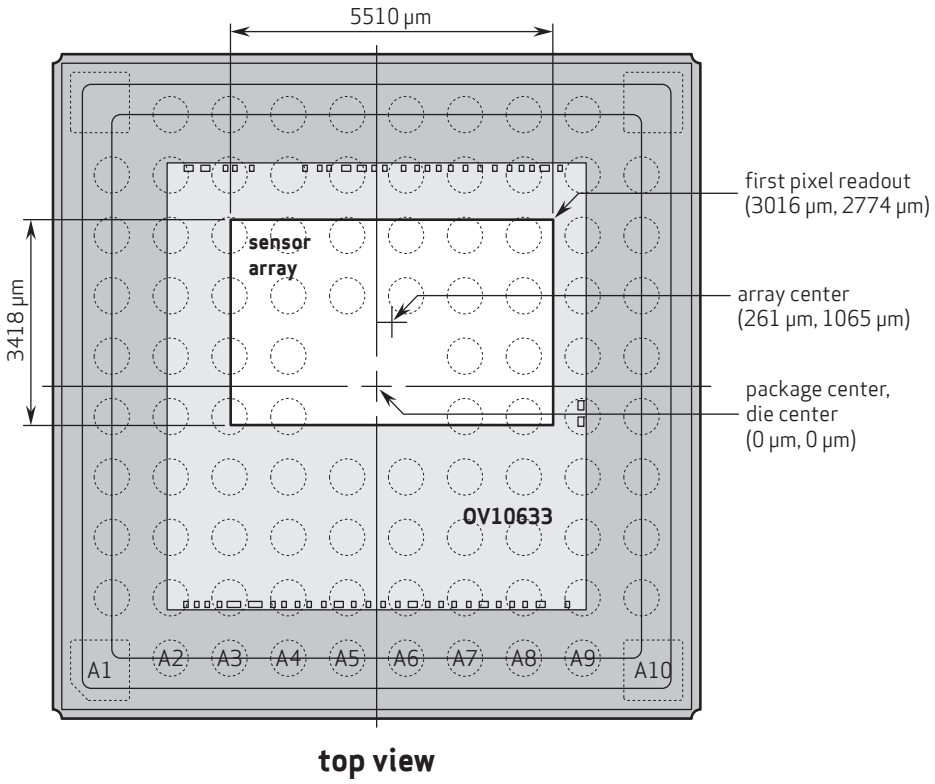
table 9-1 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A10 oriented up on the PCB.

10633_CLGA_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

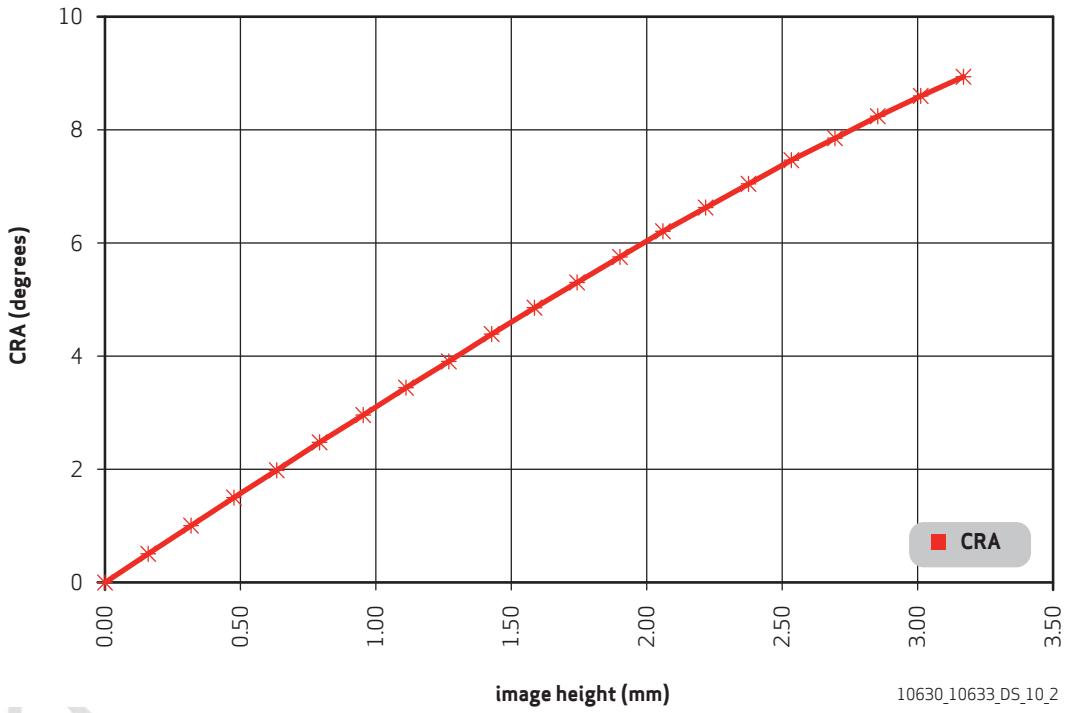


table 10-1 CRA versus image height plot (sheet 1 of 2)

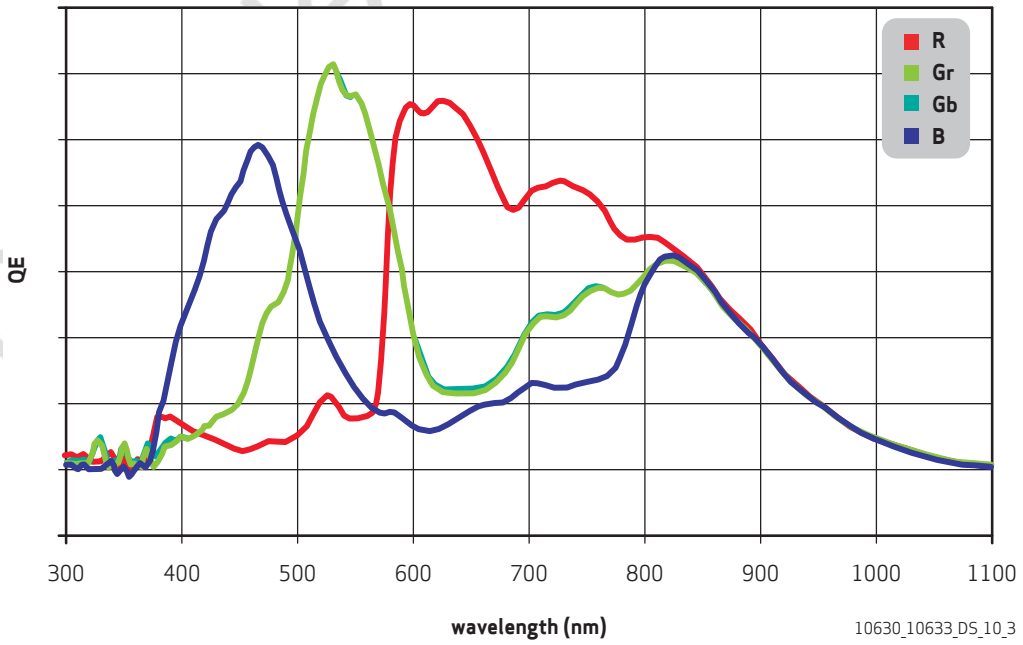
field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.0
0.05	0.158	0.5
0.10	0.317	1.0
0.15	0.475	1.5
0.20	0.634	2.0
0.25	0.792	2.5
0.30	0.951	3.0
0.35	1.109	3.4
0.40	1.268	3.9
0.45	1.426	4.4

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.50	1.585	4.9
0.55	1.743	5.3
0.60	1.902	5.8
0.65	2.060	6.2
0.70	2.219	6.6
0.75	2.377	7.1
0.80	2.536	7.5
0.85	2.694	7.9
0.90	2.853	8.2
0.95	3.011	8.6
1.00	3.170	9.0

10.3 spectrum response curve

figure 10-3 spectrum response curve diagram



revision history

version 1.5 04.15.2011

- created CLGA version by modifying the CSP4 version 1.5

version 1.51 04.22.2011

- in table 1-1, added pin number G10
- in section 10, updated figure 10-1

version 1.6 06.22.2011

- removed references to 1280x800 throughout datasheet
- in section 2, updated figure 2-2
- in sub-section 2.6.2, updated 7-bit address information
- in table 4-4, removed "Low Byte of" in description for register 0x380D and changed "Horizontal" to "Vertical" in description for register 0x3812
- in section 4, updated registers used in AEC/AGC functions
- in table 4-5, changed register description for 0x5605 from "9:8" to "10:8"
- in table 5-3, updated register description for 0x5593 to "red_limit_l", 0x5594 to "green_limit_l"
- in table 5-5, updated register description for 0x5192~0x51A3 by changing "long" to "short"
- in section 6, updated figure 6-1
- in table 5-7, removed registers 0x5300~0x5327
- in table 6-3, changed long and short RAW value from "491651" to "49165"
- in table 7-1, changed register description for 0x3033 from "PLL pclk" to "system clock" and Bit[1:0] to "Reserved"
- in table 7-8, changed register description for 0x5605 from "9:8" to "10:8"
- in table 7-11, updated register description for 0x5192~0x51A3 by changing "long" to "short"
- in table 7-13, removed registers 0x5593~0x5595 and 0x55AC~0x55AE
- in table 7-9, changed register description for 0x5006[1:0] to "Reserved"
- in table 7-16, removed registers 0x5300~0x5327
- in section 9, updated figure 9-1

version 1.61 06.29.2011

- in section 2, updated figure 2-2

version 1.62 07.26.2011

- on page i, under key specification, added note to core power supply

- in table 1-1, removed pins E5, E6, F5, and F6
- in table 2-3, updated note b
- in section 6, updated figure 6-1
- in section 9, updated figure 9-1

version 1.7 10.05.2011

- on page i, under ordering information, removed "Z" from part number
- on page i, under key specifications, replaced all TBDs, changed core power supply from "1.425~1.575V..." to "1.6~1.7V", changed power requirements for active from "524..." to "532 mW..." changed power requirements for standby from "50 µA..." to "480 µW..."
- in table 8-3, updated typical active current from "65" to "60", added maximum values for I_{DD-A} and I_{DD-D}, changed typical standby current from "50" to "300", added I_{DD-A}, I_{DD-D}, I_{DD-IO} information for standby current and removed TBDs

version 1.71 10.13.2011

- in table 8-3, removed $I_{DDS-PWDN}$, updated supply symbols for standby current and changed unit to "µA"

version 1.8 11.02.2011

- in section 4, updated figure 4-7, added figures 4-8, 4-9, removed section 4.4.2, split table 4-5 into three tables, "position window control", "AEC position weight registers" and "AEC/AGC target/range control registers", removed registers 0x564E~0x566B, 0x5680~0x56C7, and 0x5C00~0x5C17
- in section 5, updated section descriptions for sections 5.1, 5.2, 5.3, 5.4, 5.6, 5.8, 5.11
- in section 5, added "level control" to section 5.1 title, removed registers 0x5108~0xC4DF, added new sub-sections, 5.3.1, 5.3.2, 5.3.3, 5.3.5 added tables 5-4, 5-5, 5-6, 5-7, updated section 5.4 title, added new figures 5-2, 5-3, removed sections 5.9, 5.13 and added sections 5.12, and 5.13
- in table 6-1, updated default value from "0x71" to "0x78"
- in section 7, extensive updates to registers tables

version 2.0 11.28.2011

- changed datasheet from preliminary specification to product specification
- in table 1-1, changed description for DVDD pins from "1.5V..." to "1.65V..."
- in table 6-4, replaced TBDs, updated values and footnotes
- in table 8-3, added row for V_{DD-D}

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