KEYSIGHT TECHNOLOGIES

PCI Express Test Report

Overall Result: FAIL

Test Configuration Details	
Device Description	
SigTest Version	3.2.0
Device ID	Device 1
Preset Type	None
Test Session Details	
Infiniium SW Version	05.52.0011
Infiniium Model Number	DSO91304A
Infiniium Serial Number	MY53240105
Application SW Version	3.44
Debug Mode Used	No
Probe (Channel 1)	Model: 1169A Serial: US55012644 Head: N5380A/B Atten: Calibrated (20 MAR 2017 11:01:28), Using Cal Atten (2.1116E+000) Skew: Calibrated (20 MAR 2017 11:01:37), Using Cal Skew
Probe (Channel 3)	Model: 1169A Serial: US44005844 Head: N5380A/B Atten: Calibrated (20 MAR 2017 11:03:54), Using Cal Atten (2.0013E+000) Skew: Calibrated (20 MAR 2017 11:04:09), Using Cal Skew
Last Test Date	2017-03-20 11:40:30 UTC +08:00

Summary of Results

Test Statistics	
Failed	3
Passed	5
Total	8

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	System Board Tx, Unit Interval (PCIE 2.0, 5.0 GT/s)	200.0010 ps	49.2 %	199.9400 ps <= VALUE <= 200.0600 ps
✓	0	1	System Board Tx, Template Tests (PCIE 2.0, 5.0 GT/s)	Pass	100.0 %	Pass/Fail
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 2.0, 5.0 GT/s)	492.0 mV	25.5 %	250.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Peak Differential Output Voltage (Non Transition)(PCIE 2.0, 5.0 GT/s)	544.5 mV	31.0 %	250.0 mV <= VALUE <= 1.2000 V
✗	1	1	System Board Tx, Eye-Width without crosstalk (PCIE 2.0, 5.0 GT/s)	38.04 ps	**-64.8 %**	VALUE >= 108.00 ps
✗	1	1	System Board Tx, RMS Random Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)	9.979 ps	**-52.6 %**	VALUE <= 6.540 ps
✓	0	1	System Board Tx, Maximum Deterministic Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)	21.557 ps	51.0 %	VALUE <= 44.000 ps
✗	1	1	System Board Tx, Total Jitter at BER-12 without crosstalk (PCIE 2.0, 5.0 GT/s)	161.956 ps	**-76.0 %**	VALUE <= 92.000 ps

Report Detail

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✓System Board Tx, Unit Interval (PCIE 2.0, 5.0 GT/s)

Reference: This test is not required. It is informative only.

Test Summary: Pass Test Description: A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.

Pass Limits: [199.9400 ps to 200.0600 ps] **Mean UI (ps)** 200.0010 ps

Result Details

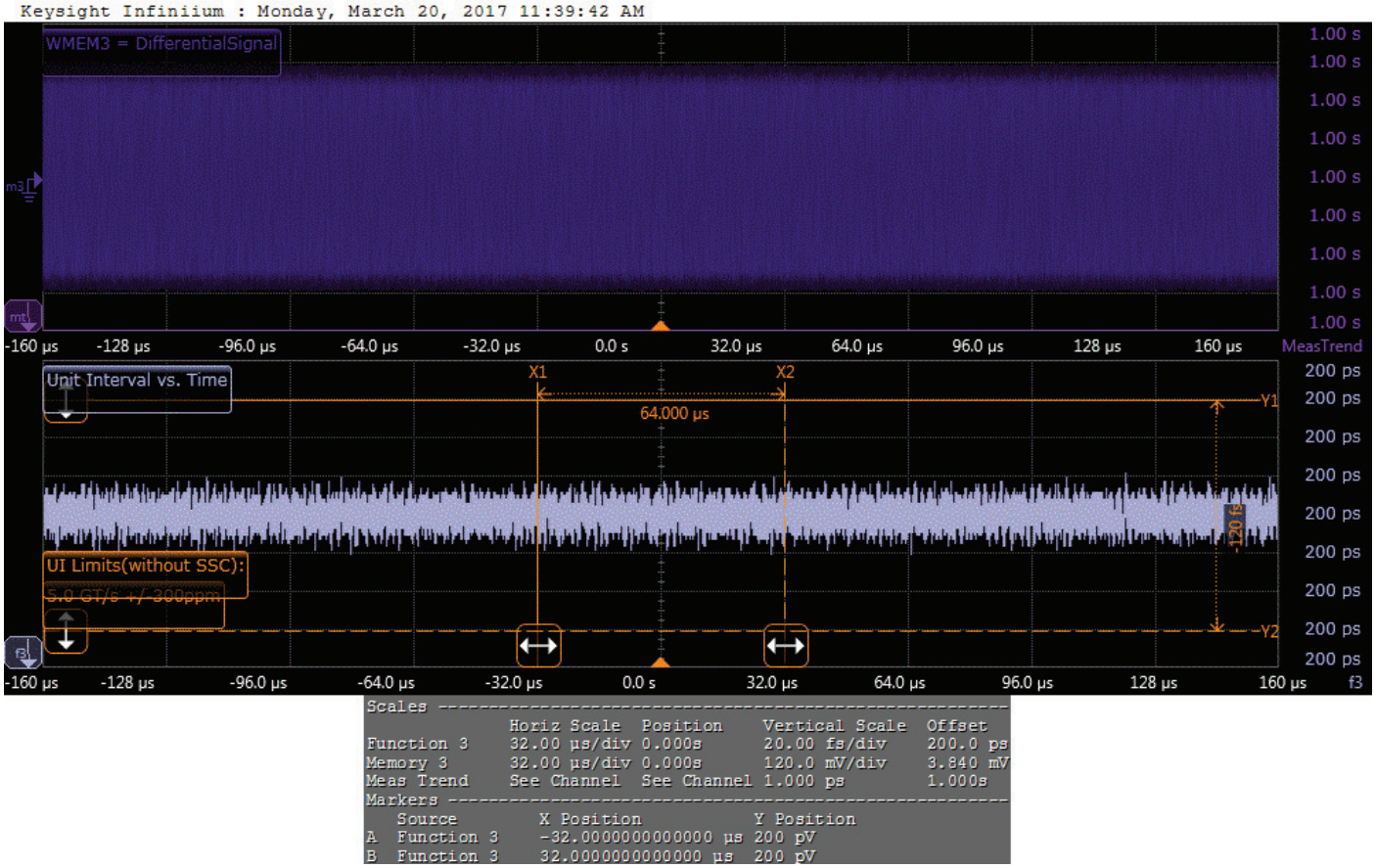
Data Lane Lane0 **Note:** Non-SSC Limits Used: 5.0 GT/s +/-300ppm **#3500 UI Blocks Measured** 1.596512 M

Min UI 199.9800 ps **Max UI** 200.0220 ps **Mean UI** 200.0010 ps **Worst Case Data Rate** 4.999450060493 Gbits/sec

Mean Data Rate 4.999975000125 Gbits/sec **Connection Type** Chan 1(Data), 3(Clock) - 2 Differential Probes

Trial 1

Trial 1: Mean Data Rate



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✓System Board Tx, Template Tests (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Figure 4-12

Test Summary: Pass

Test Description: System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-15 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.

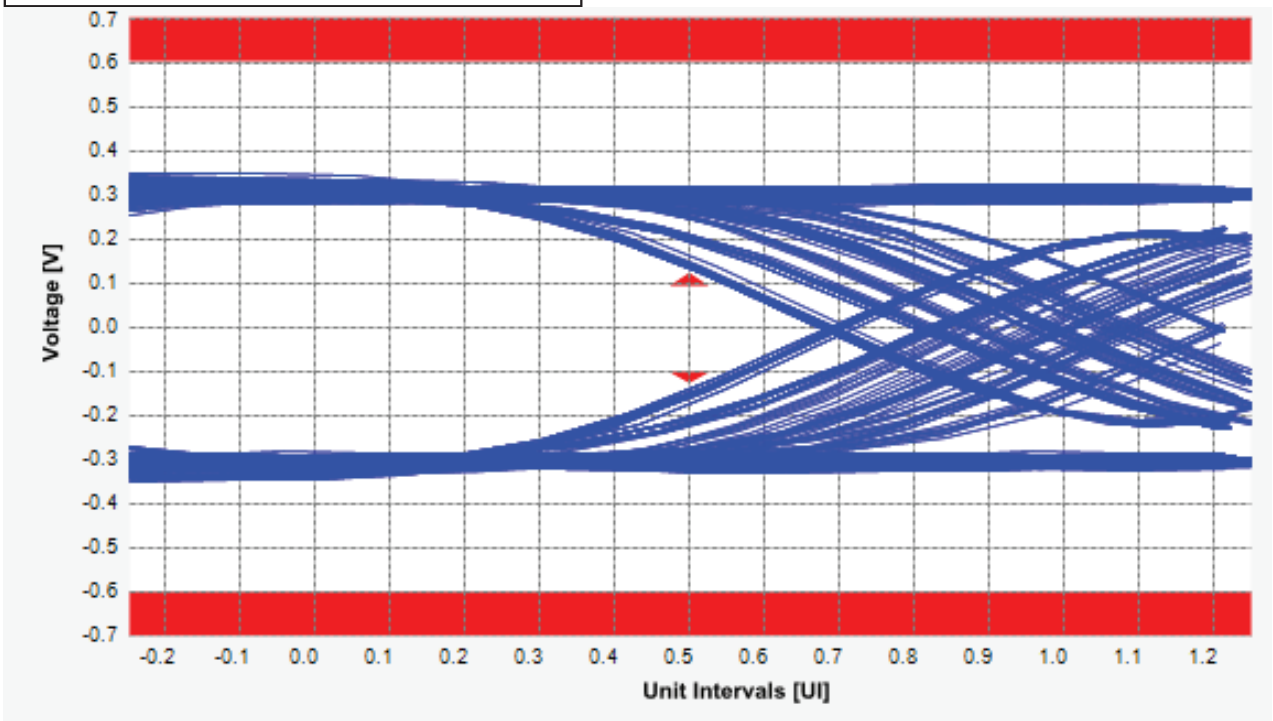
Pass Limits: Pass/Fail **Total # Failures** Pass

Result Details

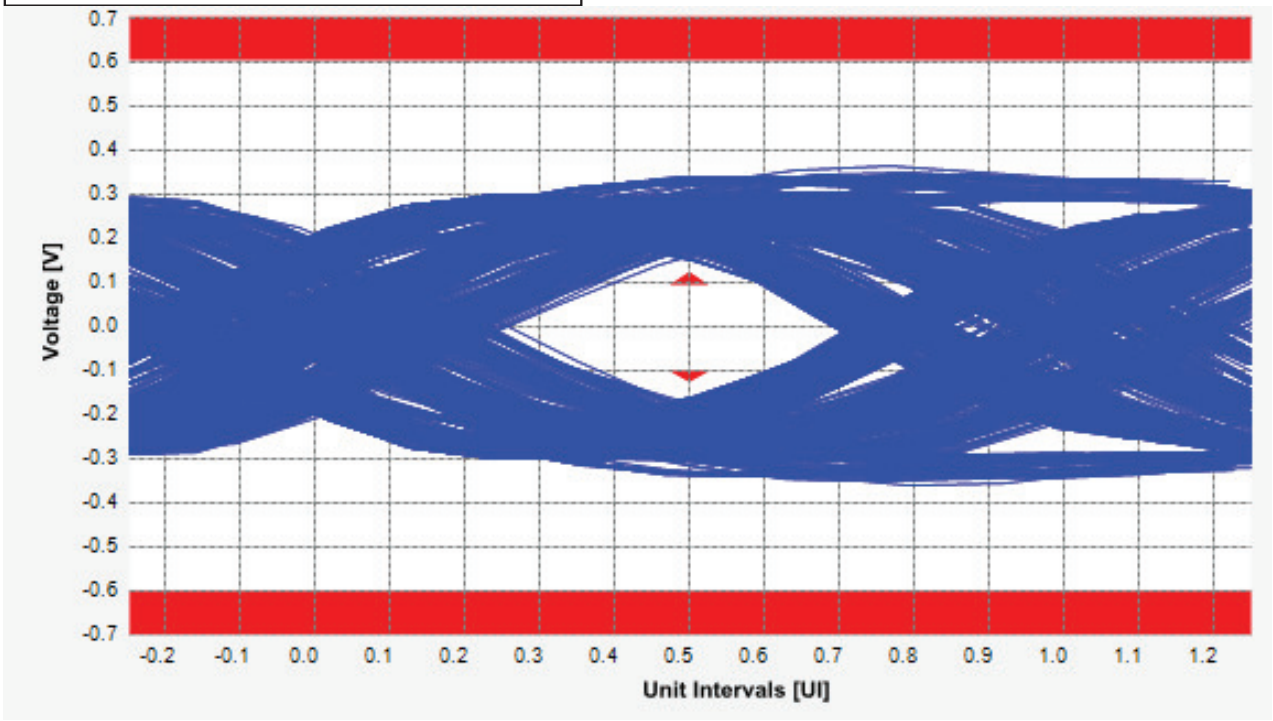
Total #UI Measured 1.600000000 M	**Non-Transition Failures** 0.000	**Transition Failures** 0.000
Non-Transition Eye Diagram (See image)	**Transition Eye Diagram** (See image)	**Data Lane** Lane0
Reference Clock Clean	**Transition Min Voltage** -357.1 mV	**Transition Max Voltage** 364.8 mV
Transition Eye Top Margin 39.20 %	**Transition Eye Bottom Margin** 40.48 %	
Non Transition Min Voltage -342.7 mV	**Non Transition Max Voltage** 346.6 mV	
Non Transition Eye Top Margin 42.23 %	**Non Transition Eye Bottom Margin** 42.89 %	
Transition Minimum Eye Height 310.3 mV	**Non Transition Minimum Eye Height** 270.1 mV	
Transition Eye Height Margin 24.12 %	**Non Transition Eye Height Margin** 8.02 %	**Sample Rate (GSa/s)** 40.0

Trial 1

Trial 1: Non-Transition Eye Diagram



Trial 1: Transition Eye Diagram



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✓System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-15

Test Summary: Pass Test Description: This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.

Pass Limits: [250.0 mV to 1.2000 V] **PeakVoltage Mean** 492.0 mV

Result Details

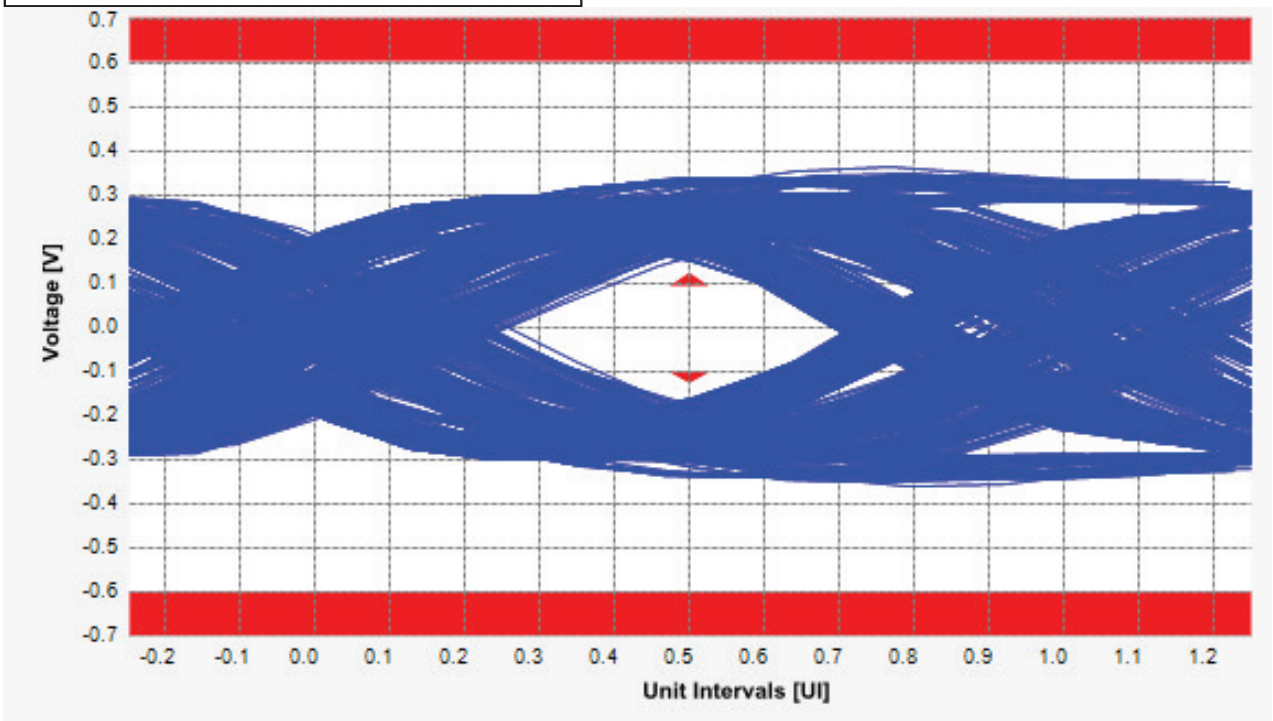
Total #UI Measured 1.600000000 M **Largest Transition Amplitude (Outer eye)** 721.9 mV

Smallest Transition Amplitude (Inner eye) 291.1 mV **Data Lane** Lane0 **Transition Eye Diagram** (See image)

Connection Type Chan 1(Data), 3(Clock) - 2 Differential Probes

Trial 1

Trial 1: Transition Eye Diagram



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✓System Board Tx, Peak Differential Output Voltage (Non Transition)(PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-15

Test Summary: Pass | Test Description: This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.

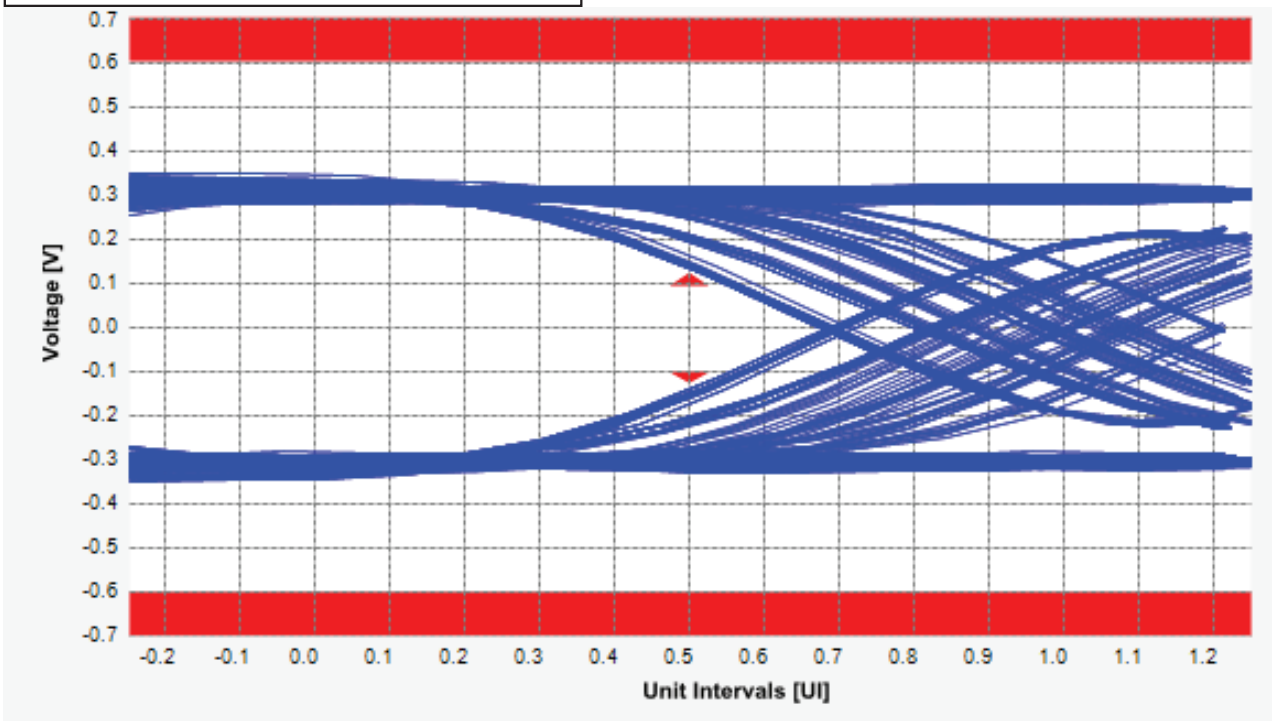
Pass Limits: [250.0 mV to 1.2000 V] | **PeakVoltage Mean** 544.5 mV

Result Details

Total #UI Measured 1.600000000 M	**Largest Non Transition Amplitude (Outer eye)** 689.3 mV
Smallest Non Transition Amplitude (Inner eye) 228.4 mV	**Data Lane** Lane0
Transition Eye Diagram (See image)	**Connection Type** Chan 1(Data), 3(Clock) - 2 Differential Probes

Trial 1

Trial 1: Transition Eye Diagram



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✗System Board Tx, Eye-Width without crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-15

Test Summary: **FAIL** Test Description: This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].

Pass Limits: >= 108.00 ps | **Eye-Width** 38.04 ps

Result Details

Total #UI Measured 1.600000000 M | **TJ at BER-12** 161.956 ps

Worst Filter Info PLL Damping Factor = 1.16, PLL Frequency = 5000000Hz | **Worst Transport Delay** 858.9935000 ms

Data Lane Lane0 | **Connection Type** Chan 1(Data), 3(Clock) - 2 Differential Probes

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✗System Board Tx, RMS Random Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: This test is not required. It is informative only.

Test Summary: **FAIL** Test Description: The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.

Pass Limits: <= 6.540 ps | **Rj_rms** 9.979 ps

Result Details

Total #UI Measured 1.600000000 M | **Worst Filter Info** PLL Damping Factor = 1.16, PLL Frequency = 5000000Hz

Worst Transport Delay 858.9935000 ms | **Data Lane** Lane0 | **Sample Rate (GSa/s)** 40.0

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✓System Board Tx, Maximum Deterministic Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-16

Test Summary: Pass Test Description: System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.

Pass Limits: <= 44.000 ps | **Dj_dd** 21.557 ps

Result Details

Total #UI Measured 1.600000000 M | **Worst Filter Info** PLL Damping Factor = 1.16, PLL Frequency = 5000000Hz

Worst Transport Delay 858.9935000 ms | **Data Lane** Lane0 | **Sample Rate (GSa/s)** 40.0

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✗System Board Tx, Total Jitter at BER-12 without crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.2, Table 4-16

Test Summary: **FAIL** Test Description: System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.

Pass Limits: <= 92.000 ps | **Tj at BER 10-12** 161.956 ps

Result Details

Total #UI Measured 1.600000000 M | **Worst Filter Info** PLL Damping Factor = 1.16, PLL Frequency = 5000000Hz

Worst Transport Delay 858.9935000 ms | **Data Lane** Lane0 | **Sample Rate (GSa/s)** 40.0

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