

# AM64xx STARTER KIT EVM BOARD

## SK-AM64

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<b>REV</b>	E3
<b>VER</b>	3.1

Note: Raspberry Pi is the trademark / wordmark of Raspberry Pi Foundation

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## REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
2.0	01st JULY 2021	Drafted from "PROC100E2_SCH" Document	Mistral Design Team	Krishna Prasad	Krishna Prasad
3.0	01st JULY 2021	FL23 Part changed to NFM21PC105B1A3D Schematics Baselined	Mistral Design Team	Krishna Prasad	Krishna Prasad
3.1	18th AUG 2021	R6 made DNI	Mistral Design Team	Krishna Prasad	Krishna Prasad

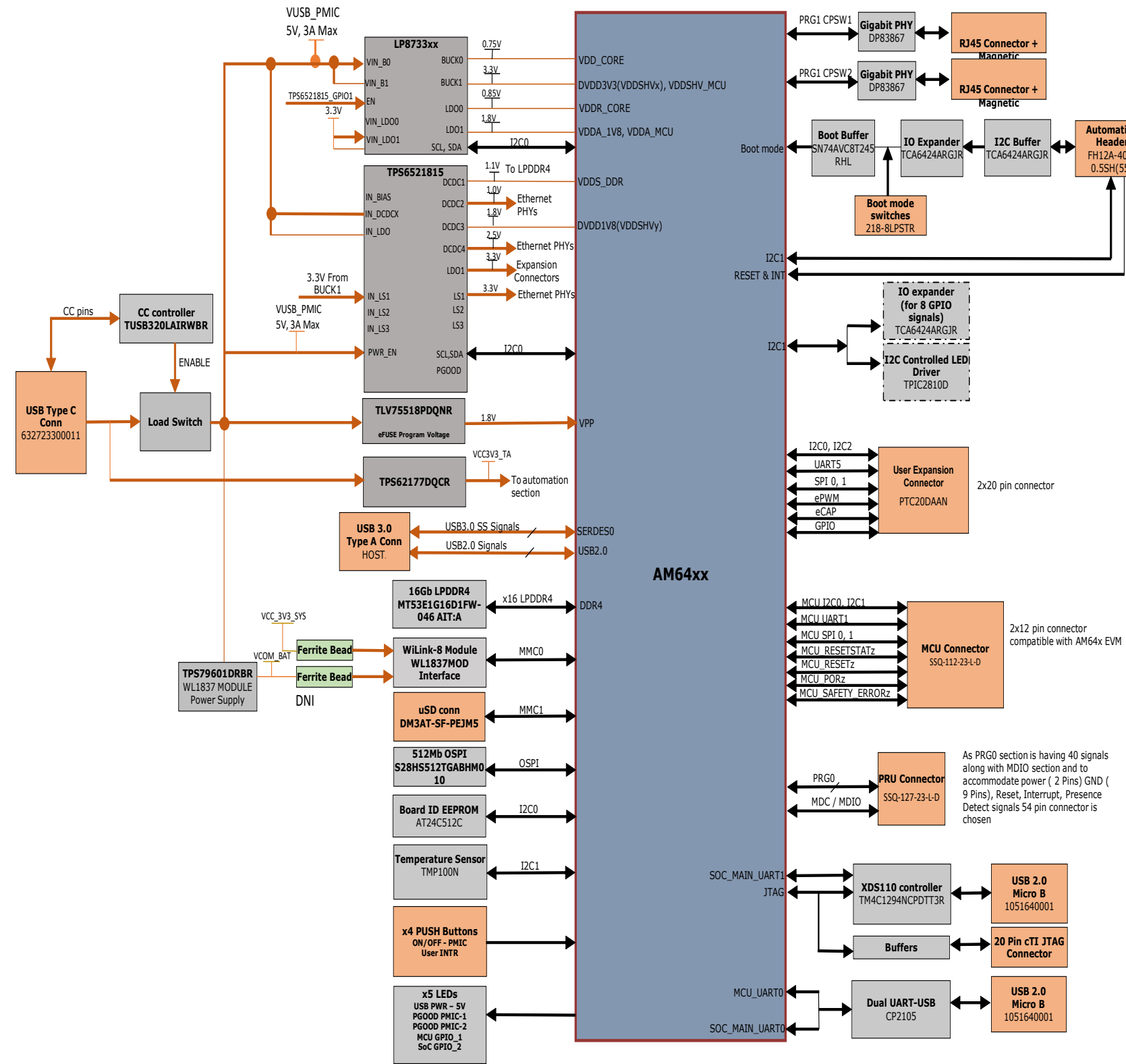
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Title REVISION HISTORY

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Date:	Monday, September 27, 2021	Sheet 2 of 45

# BLOCK DIAGRAM\_AM64x\_SKEVM



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Title BLOCK DIAGRAM

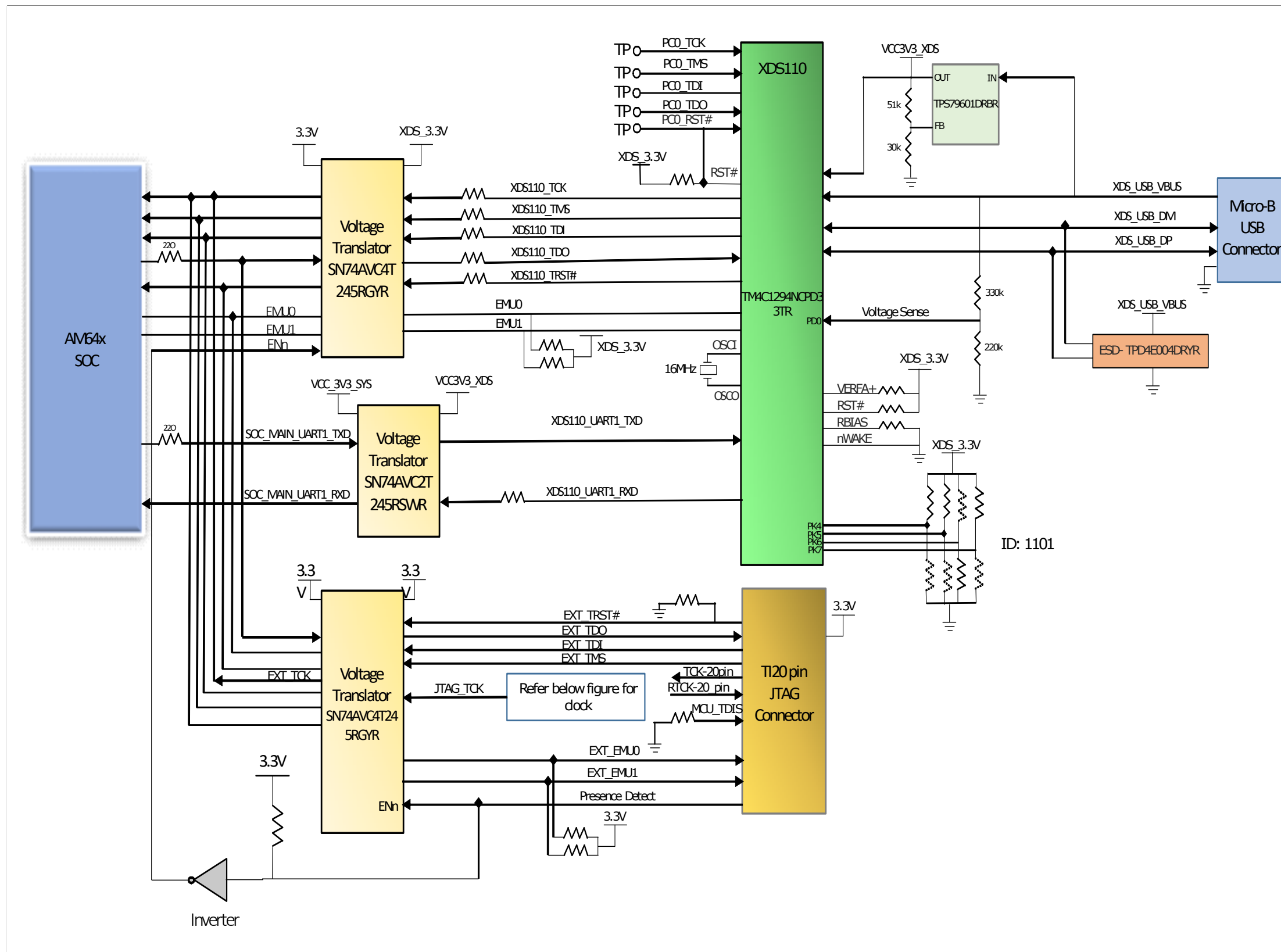
Size PROC100 001 SKAM64

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# BLOCK DIAGRAM\_XDS110



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Title BLOCK DIAGRAM\_XDS110

Size PROC100 001 SKAM64

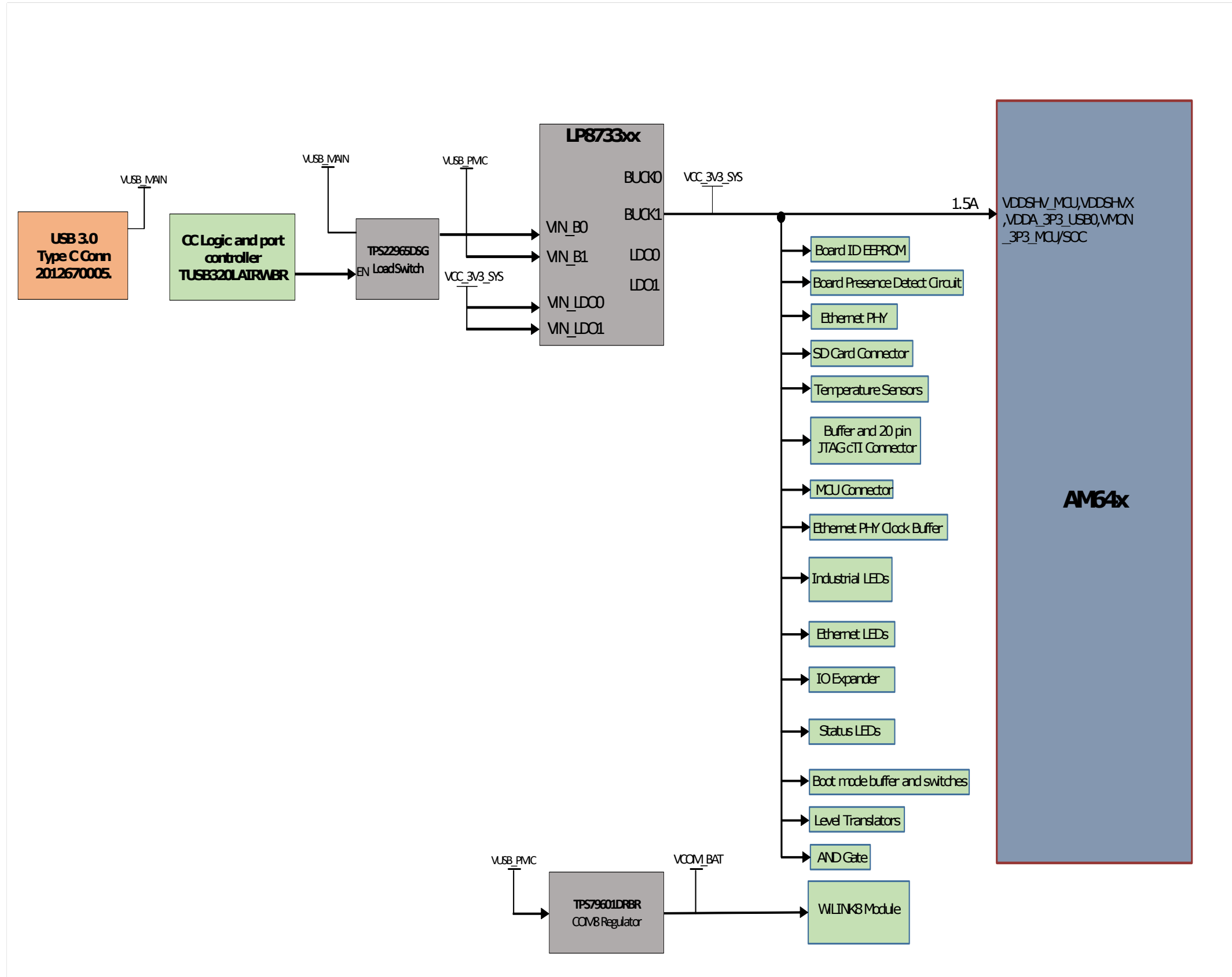
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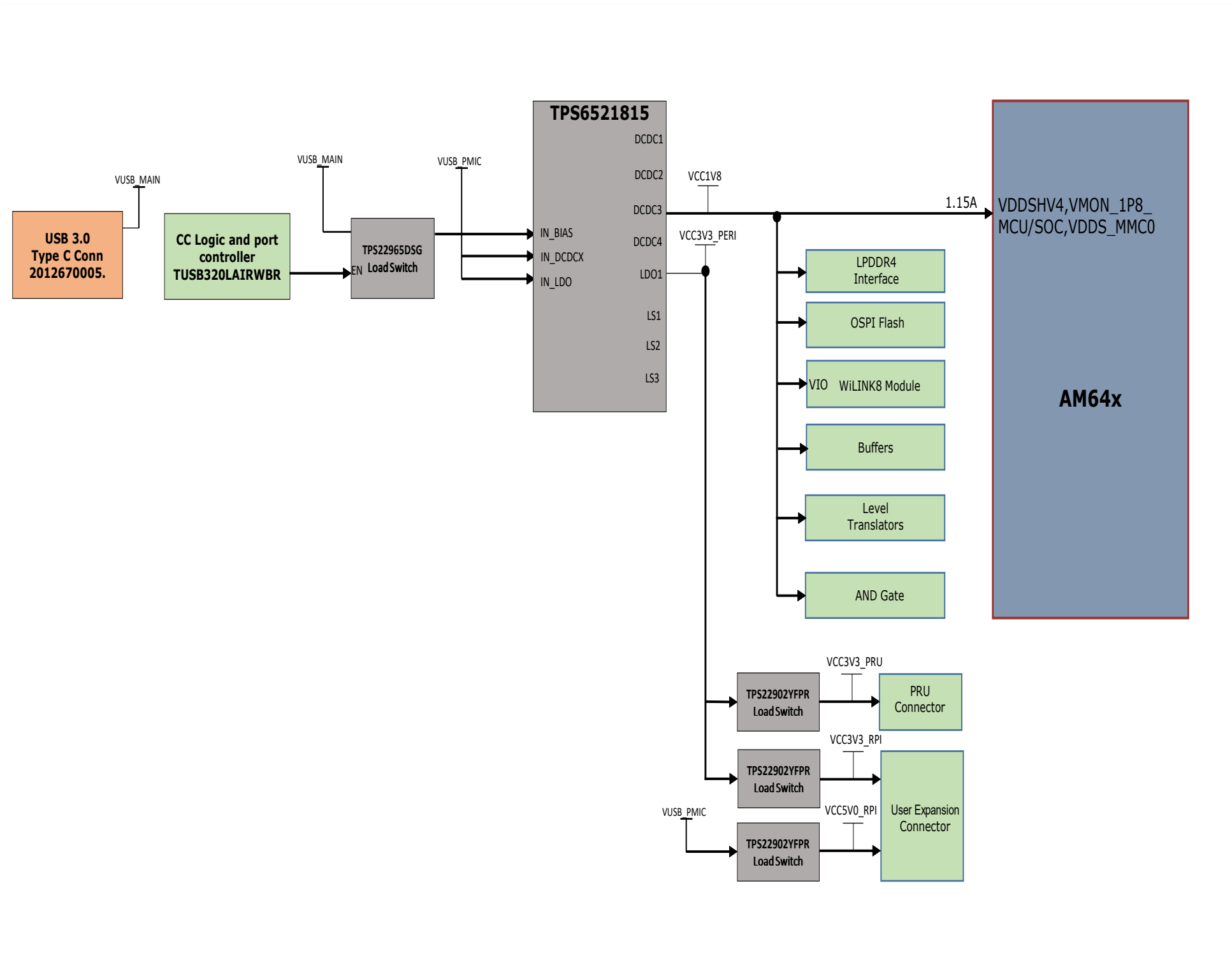
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# 3V3 SUPPLY POWER FLOW



# 1V8 SUPPLY POWER FLOW



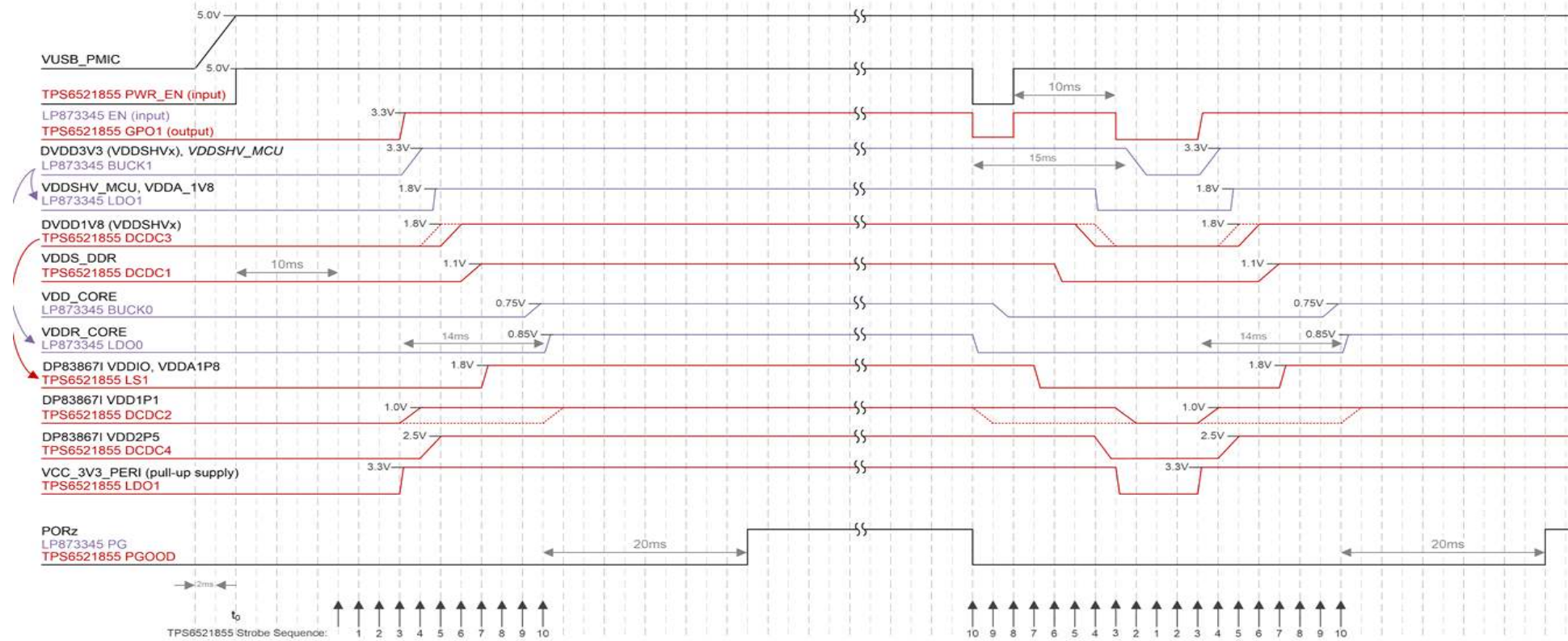
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Title 1V8 SUPPLY POWER FLOW

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# POWER SEQUENCE



## LP873345 OTP Configuration

STARTUP\_DELAY\_SEL=1  
 BUCK1\_STARTUP\_DELAY[3:0] = 0x0 = 0ms  
 LDO1\_STARTUP\_DELAY[3:0] = 0x3 = 3ms  
 BUCK0\_STARTUP\_DELAY[3:0] = 0xC = 12ms  
 LDO0\_STARTUP\_DELAY[3:0] = 0xE = 14ms  
  
 BUCK1\_SHUTDOWN\_DELAY[3:0] = 0xF = 15ms  
 LDO1\_SHUTDOWN\_DELAY[3:0] = 0xC = 12ms  
 BUCK0\_SHUTDOWN\_DELAY[3:0] = 0x2 = 2ms  
 LDO0\_SHUTDOWN\_DELAY[3:0] = 0x0 = 0ms  
 \*Max delay time = 0xF = 15ms  
  
 LP873345 GPOx (outputs) = un-used  
 BUCK0\_RDIS\_EN = 1b, BUCK1\_RDIS\_EN = 1b  
 LDO0\_RDIS\_EN = 1b, LDO1\_RDIS\_EN = 1b  
  
 PGOOD = Push-pull, active high  
 (VOL = VANA = 5V, VI of SN74LVC1G11 rated up to 5.5V, independent of VCC supply)

## TPS6521855 EEPROM Configuration

SEQ1-2 = 0x00  
 (DLY1-9 = 0b = 2ms, DLYFACTR = 0b = 1x)  
 SEQ3[3:0] = DC1\_SEQ = 0x5 = Strobe 5  
 SEQ3[7:4] = DC2\_SEQ = 0x6 = Strobe 6  
 SEQ4[3:0] = DC3\_SEQ = 0x5 = Strobe 5  
 SEQ4[7:4] = DC4\_SEQ = 0x4 = Strobe 4  
 SEQ6[3:0] = LDO1\_SEQ = 0x3 = Strobe 3  
 SEQ6[7:4] = LS1\_SEQ = 0x7 = Strobe 7  
 SEQ7[3:0] = GPO1\_SEQ = 0x3 = Strobe 3  
 SEQ7[7:4] = GPO3\_SEQ = 0x0 = Disconnected from sequencer  
  
 SEQ5 = 0x00 = DCDC5/6 disconnected from sequencer  
 \*PWR\_EN deglitch + 9\*2ms = 10ms + 18ms = 28ms  
 CONFIG1 = 0x08  
 (GPO2\_BUF = 0b, PGDLY = 01b = 20ms, STRICT = 0b)  
 CONFIG1 = 0x40  
 (DC12\_RST = 0b, UVLOHYS = 1b = 400mV)

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Title POWER SEQUENCE

Size PROC100 001 SKAM64

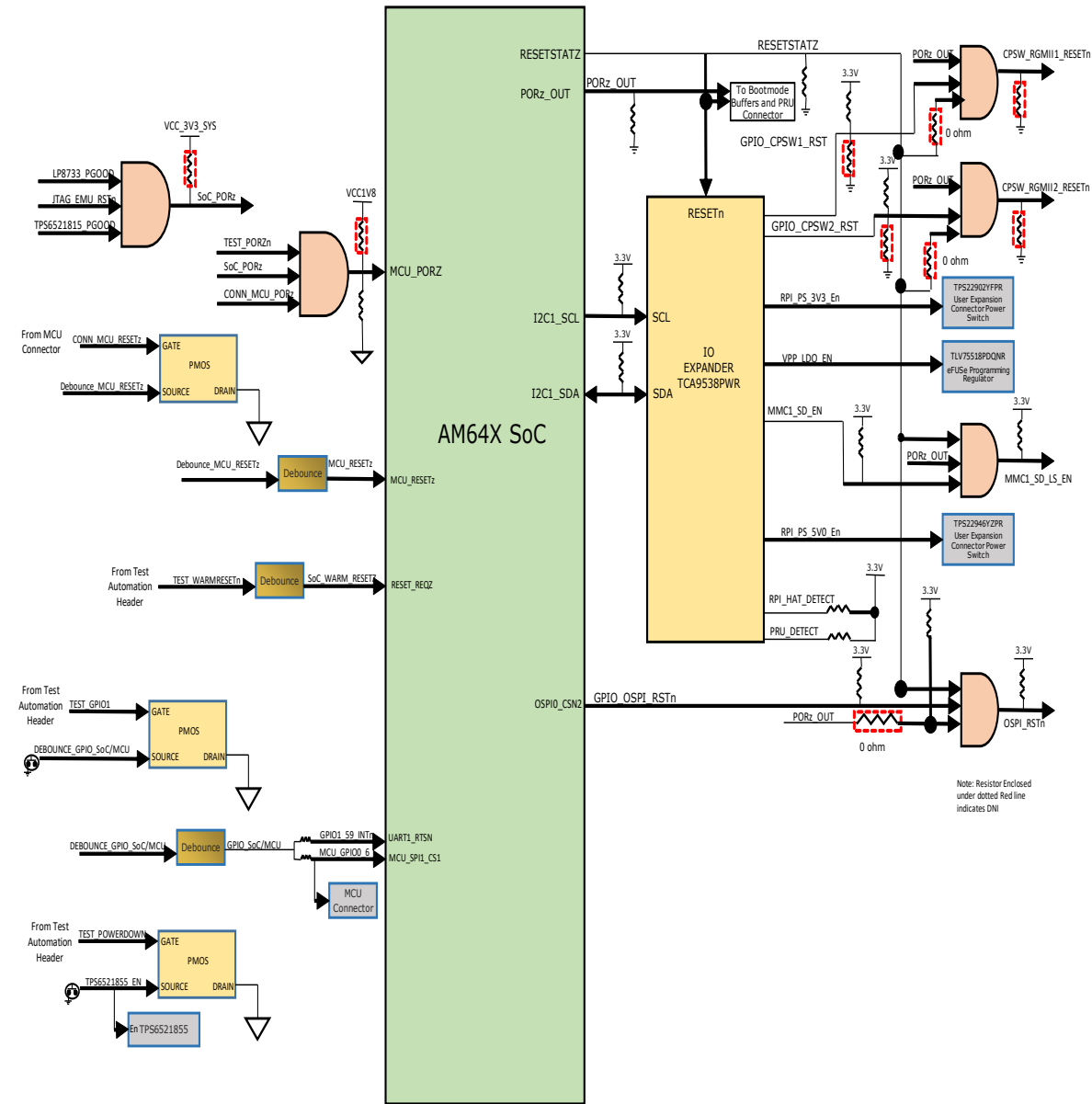
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# RESET ARCHITECTURE



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Title RESET ARCHITECTURE

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# GPIO MAPPING TABLE

AM64xx GPIO MAPPING TABLE										
SI.NO	GPIO Description	GPIO Netname	Functionality	GPIO Used	SoC Muxed Signal Name	Direction with respect to SoC	Default State	Active State	Voltage Domain On Processor Side	Voltage Connected on SKEVM
1	IO Expander Interrupt	IO_EXP_INTn_SDIO	Interrupt	GPIO1_78	MMC1_SDWP	Input	High	Low	VDDSHV0	SoC_DVDD3V3
2	Enable for COM8 Level Translator	COM8_LS_EN	Enable	GPIO0_62	PRG1_PRU0_GPO17	Output	High	Low	VDDSHV2	SoC_DVDD3V3
3	Enable for WLAN Interface in COM8 Connector	WLAN_EN_SoC_LS	Enable	GPIO0_48	PRG1_PRU0_GPO3	Output	Low	High	VDDSHV2	SoC_DVDD3V3
4	Enable for BT Interface in COM8 Connector	BT_EN_SOC_LS	Enable	GPIO0_49	PRG1_PRU0_GPO4	Output	Low	High	VDDSHV2	SoC_DVDD3V3
5	WLAN SDIO out-of band interrupt line	WLAN_IRQ_LS	Interrupt	GPIO0_46	PRG1_PRU0_GPO1	Input	High	Low	VDDSHV2	SoC_DVDD3V3
6	OSPI Interrupt	OSPI_INTn	Interrupt	GPIO0_14	OSPIO_CSN3	Input	High	Low	VDDSHV4	SoC_DVDD1V8
7	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	Reset	GPIO0_13	OSPIO_CSN2	Output	High	Low	VDDSHV4	SoC_DVDD1V8
8	User LED	TEST_LED1	Test	GPIO0_60	PRG1_PRU0_GPO15	Output	Low	High	VDDSHV2	SoC_DVDD3V3
9	User LED	TEST_LED2	Test	MCU_GPIO0_5	MCU_SPI1_CS0	Output	Low	High	VDDSHV_MCU	SoC_DVDD3V3
10	SD card load switch enable control	MMC1_SD_EN	Enable	IO Expander-P3		Output	High	High	VDDSHV0	SoC_DVDD3V3
11	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn								
12	PRU Connector Interrupt	PRU_INTn	Interrupt	GPIO1_70	EXTINTn	Input	High	Low	VDDSHV0	SoC_DVDD3V3
13	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	Reset	IO Expander-P1		Output	High	Low	VDDSHV0	SoC_DVDD3V3
14	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	Reset	IO Expander-P0		Output	High	Low	VDDSHV0	SoC_DVDD3V3
15	TEST GPIO1 from Test Automation Connector	TEST_GPIO1	GPIO for communication with AM64x	GPIO1_59	UART1_RTSN	Input	High	Low	VDDSHV0	SoC_DVDD3V3
				MCU_GPIO0_6	MCU_SPI1_CS1	Input	High	Low	VDDSHV_MCU	SoC_DVDD3V3
16	LP8733xx PMIC Interrupt	PMIC_INT_B	Interrupt							
17	TPS6521815 PMIC Interrupt	PMIC_INT_B	Interrupt	GPIO0_45	PRG1_PRU0_GPO0	Input	High	Low	VDDSHV2	SoC_DVDD3V3
18	BTUART_RTS or Bootmode10 switch select	BTUART_RTS_SEL	Switch Selection	GPIO0_63	PRG1_PRU0_GPO18	Output	Low	High	VDDSHV2	SoC_DVDD3V3
19	VPP 1.8V regulator Enable	VPP_LDO_EN	Enable	IO Expander-P4		Output	Low	High	VDDSHV0	SoC_DVDD3V3
20	COM8 Regulator Enable	COM8_REG_EN	Enable	GPIO0_61	PRG1_PRU0_GPO16	Output	Low	High	VDDSHV2	SoC_DVDD3V3
21	Power Switch Enable for USB device	USB0_DRVBUS	Enable	GPIO1_79	USB0_DRVVBUS	Output	Low	High	VDDSHV0	SoC_DVDD3V3
22	RPI-HAT Detection	RPI_HAT_DETECT	Detection	IO Expander-P7		Input	High	Low	VDDSHV0	SoC_DVDD3V3
23	PRU Detection	PRU_DETECT	Detection	IO Expander-P2		Input	High	Low	VDDSHV0	SoC_DVDD3V3
24	PRU Power Switch Enable	PRU_3V3_En	Enable	GPIO0_64	PRG1_PRU0_GPO19	Output	Low	High	VDDSHV2	SoC_DVDD3V3
25	Rpi Power Switch Enable	RPI_PS_5V0_En	Enable	IO Expander-P6		Output	Low	High	VDDSHV0	SoC_DVDD3V3
26	Rpi Power Switch Enable	RPI_PS_3V3_En	Enable	IO Expander-P5		Output	Low	High	VDDSHV0	SoC_DVDD3V3

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Title: GPIO MAPPING TABLE

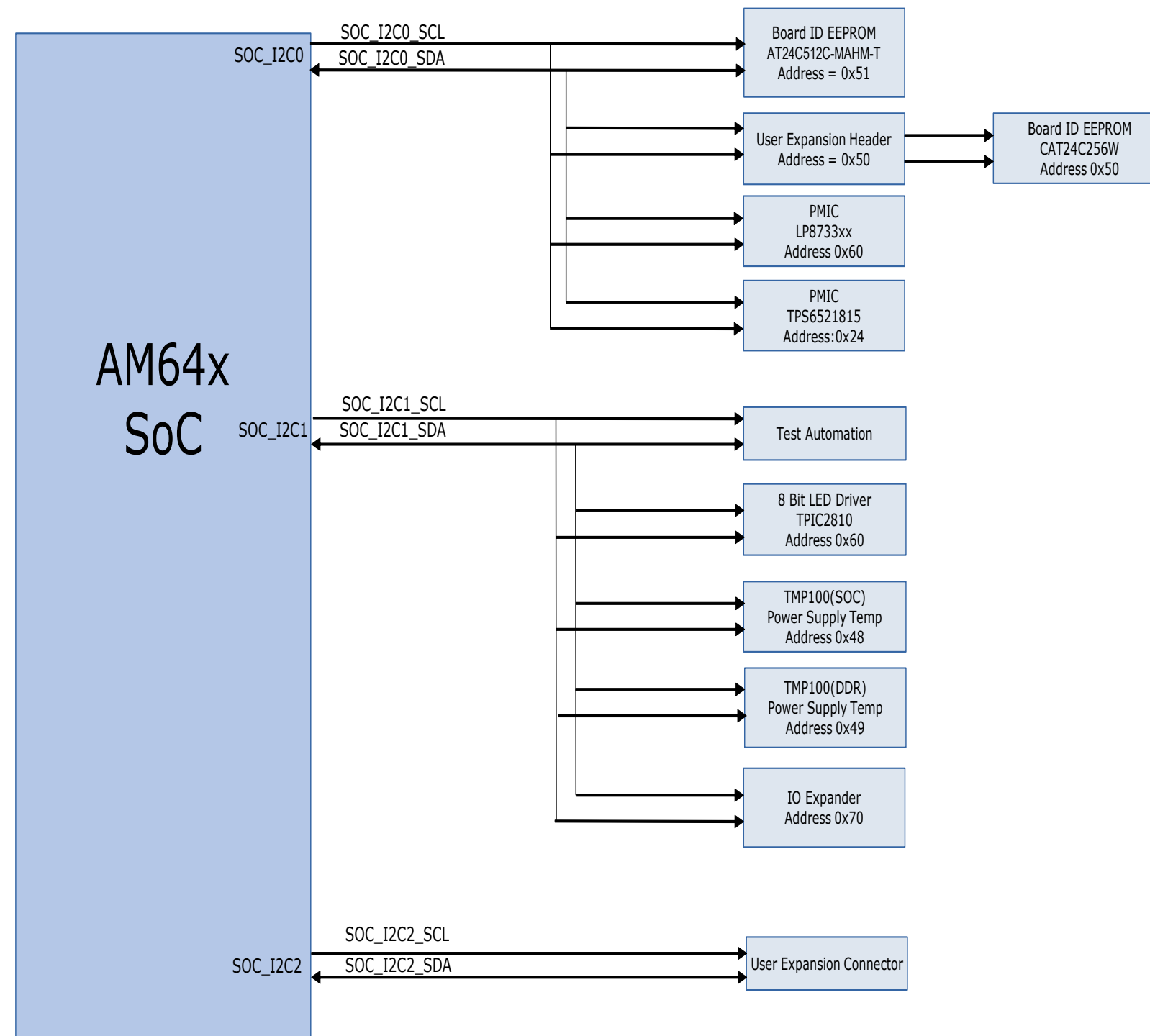
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# I2C TREE



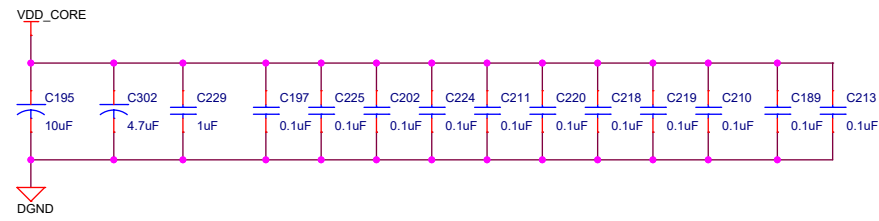
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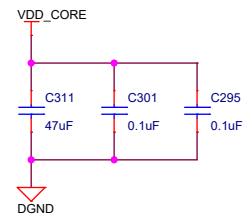
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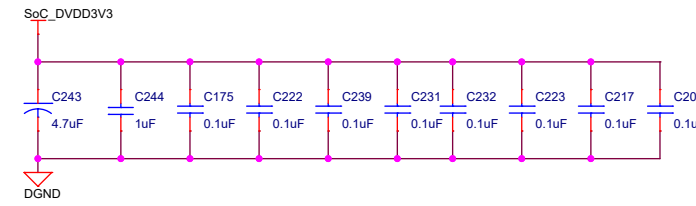
# SOC POWER DECAPS



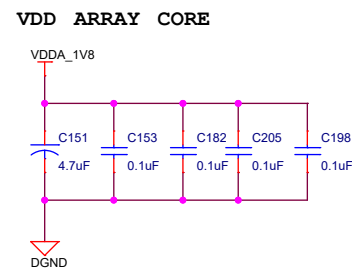
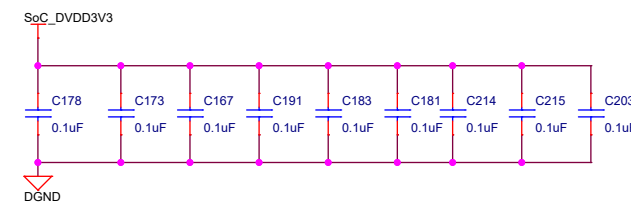
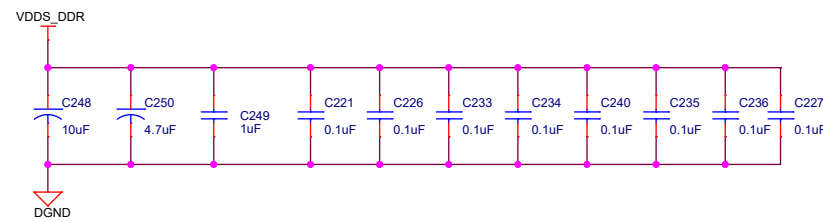
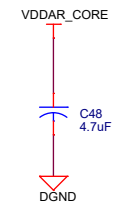
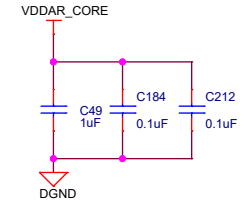
Place one 0.1uF cap near each Pin



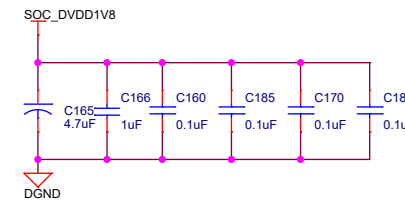
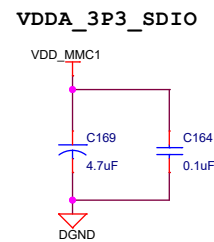
To place after current sense resistor on VDD\_CORE plane



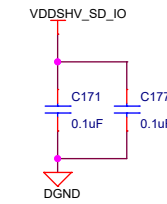
Place one 0.1uF cap near each Pin



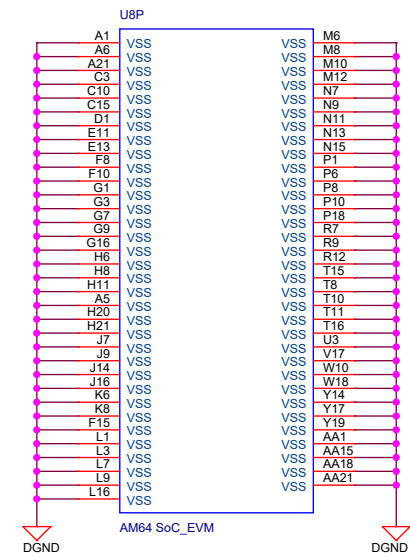
Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin



# SOC POWER - VSS



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Title SOC VSS

Size PROC100 001 SKAM64

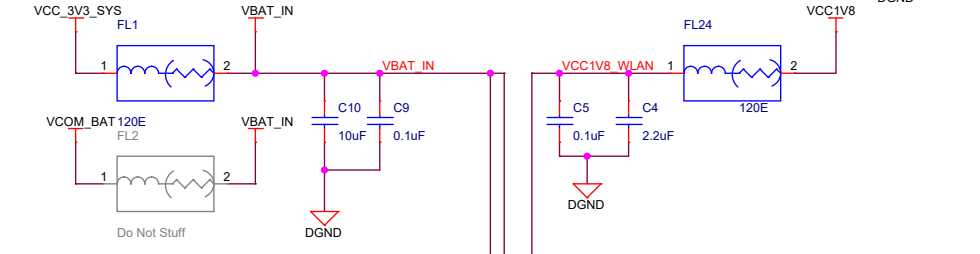
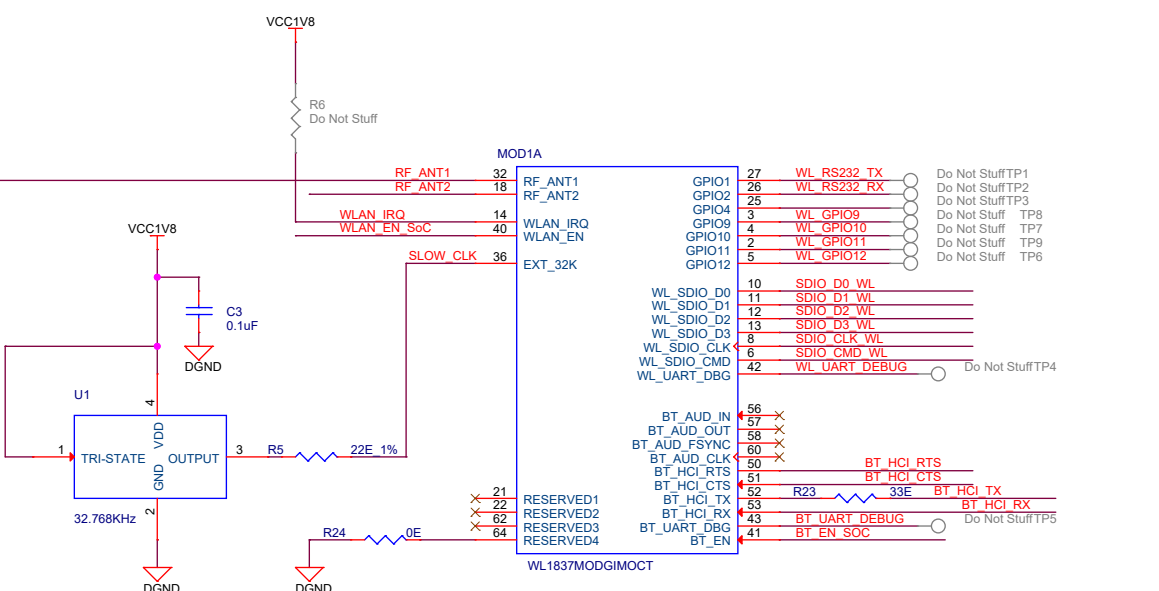
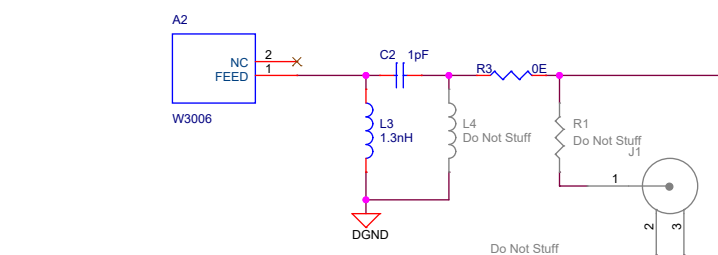
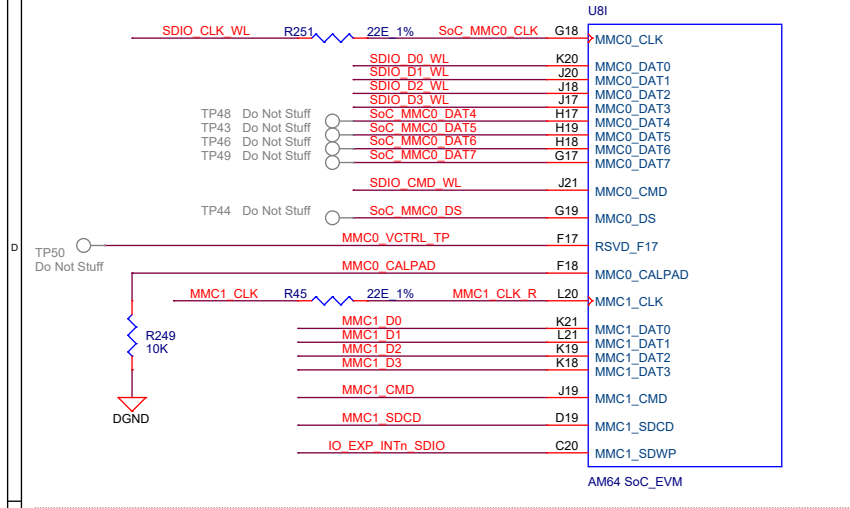
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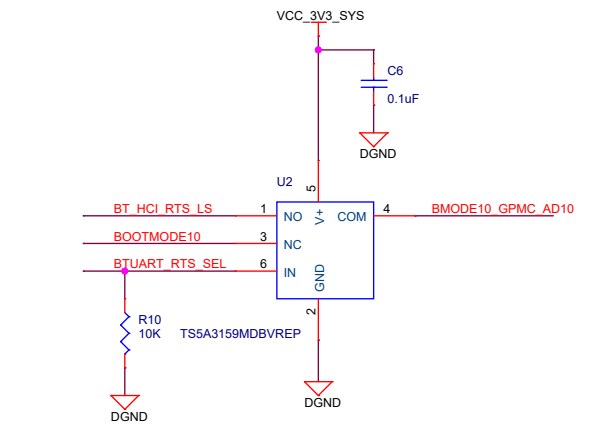
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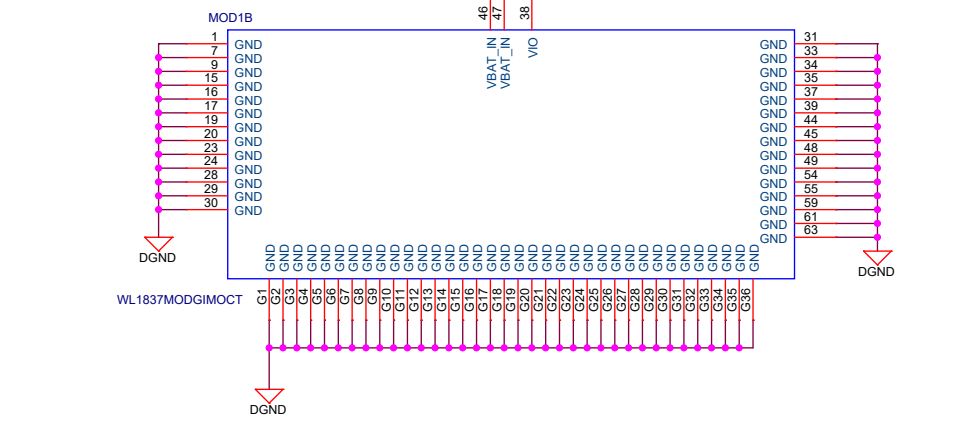
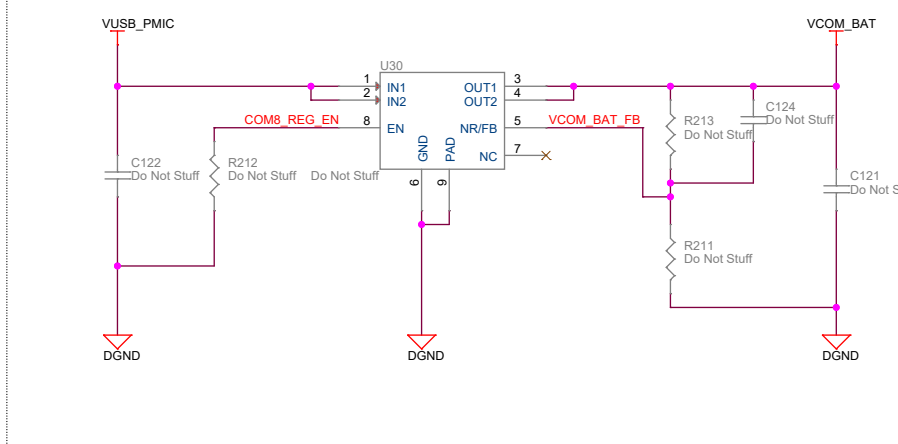
# WL1837 MODULE



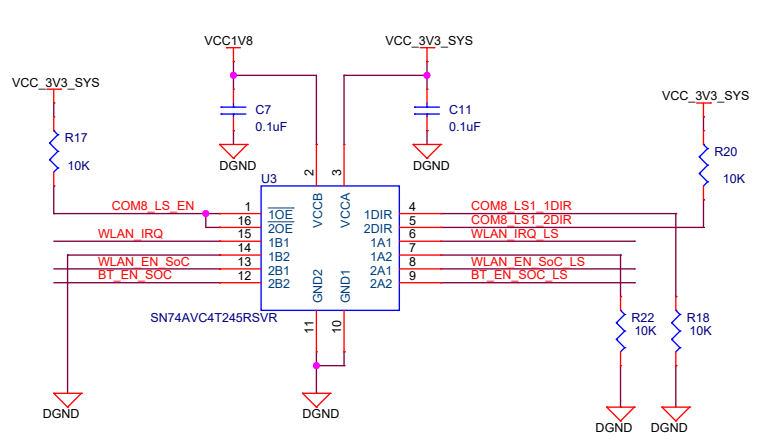
## BOOTMODE10/ BTUART RTS SELECT SWITCH



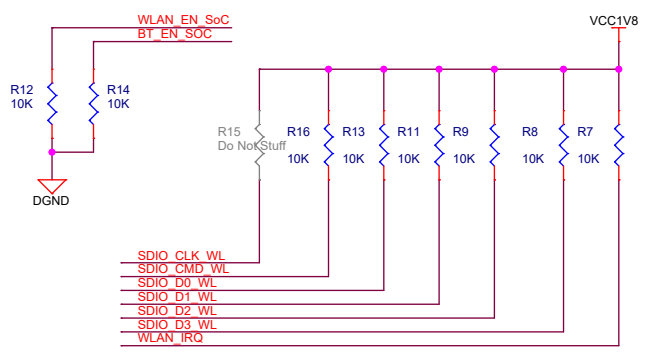
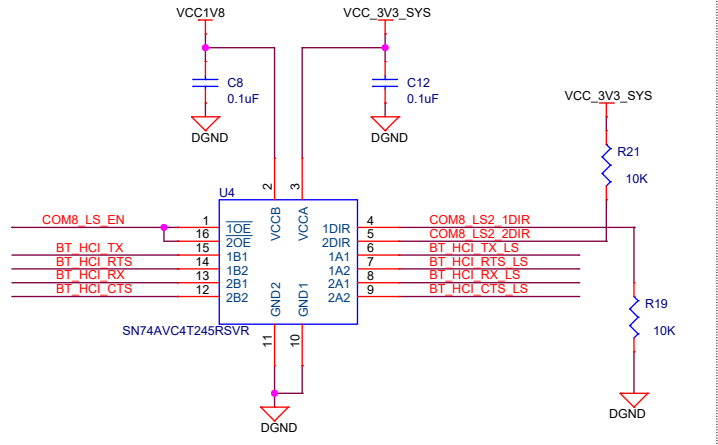
## COM8 WILINK POWER



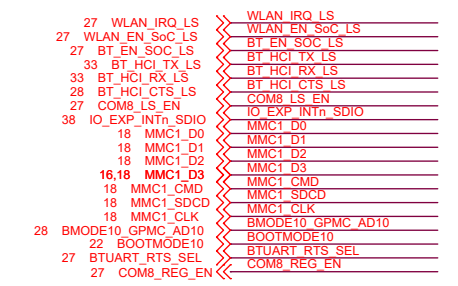
## COM8 LEVEL TRANSLATOR-1



## COM8 LEVEL TRANSLATOR-2



## OFF PAGE CONNECTIONS



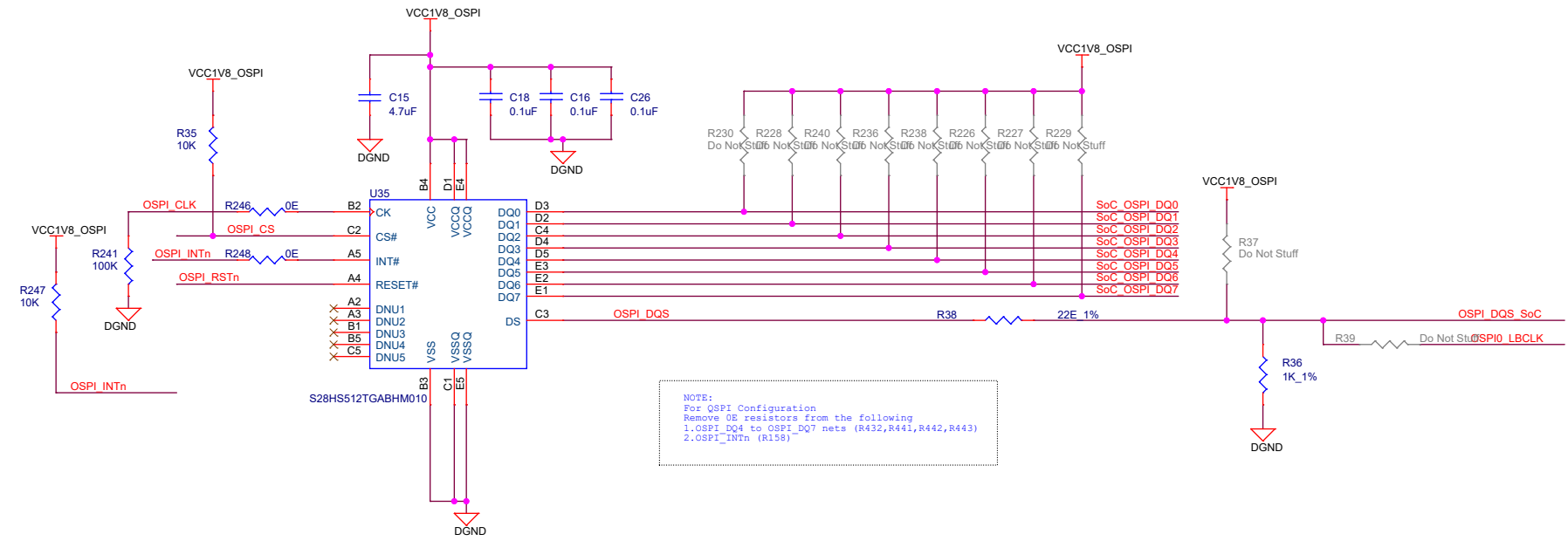
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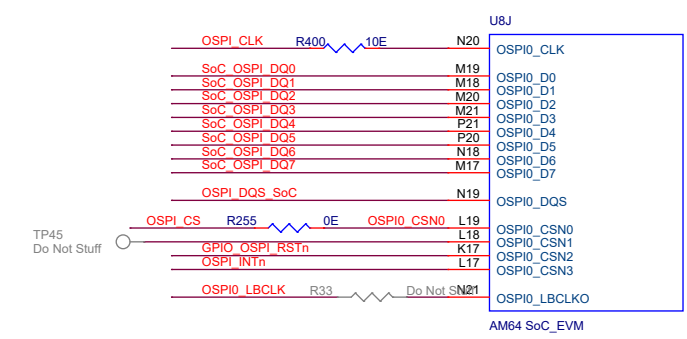
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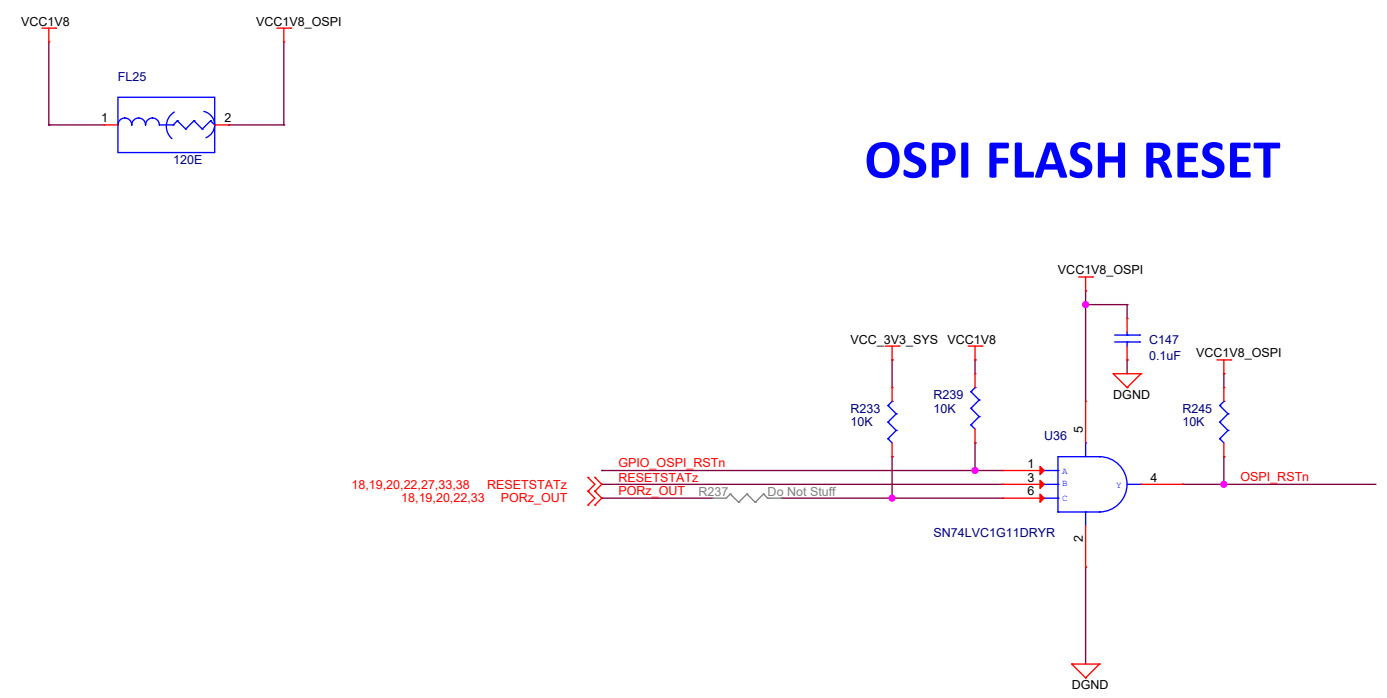
# OSPI FLASH



# SOC OSPI INTERFACE



# OSPI FLASH RESET



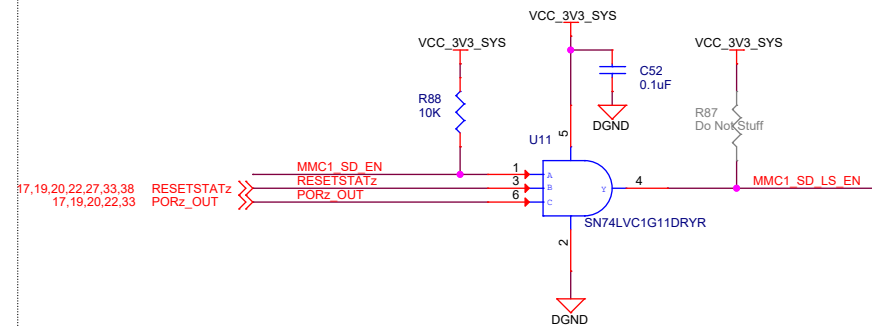
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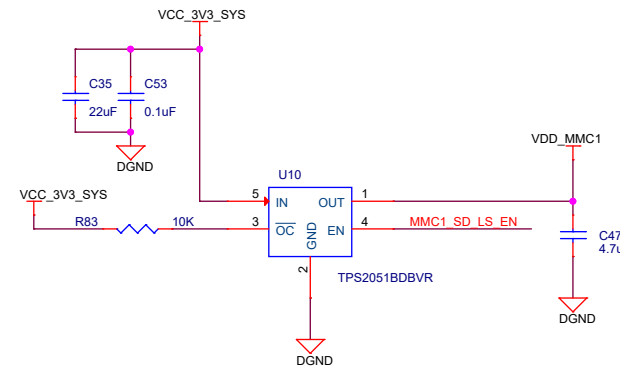
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# SD CARD INTERFACE

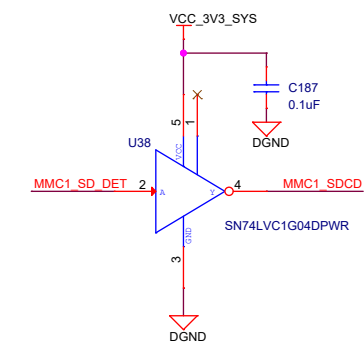
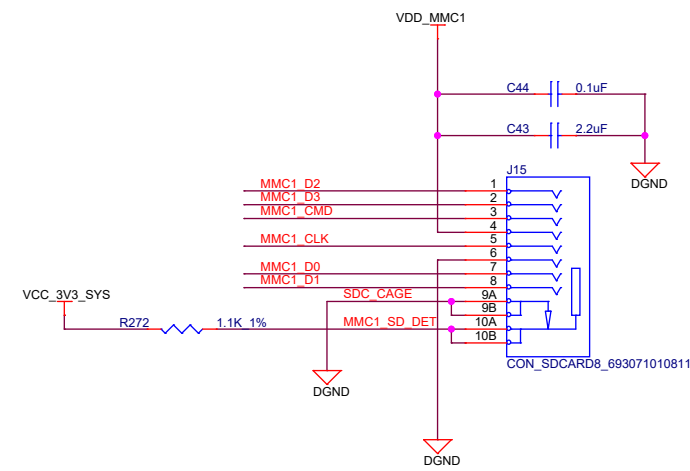
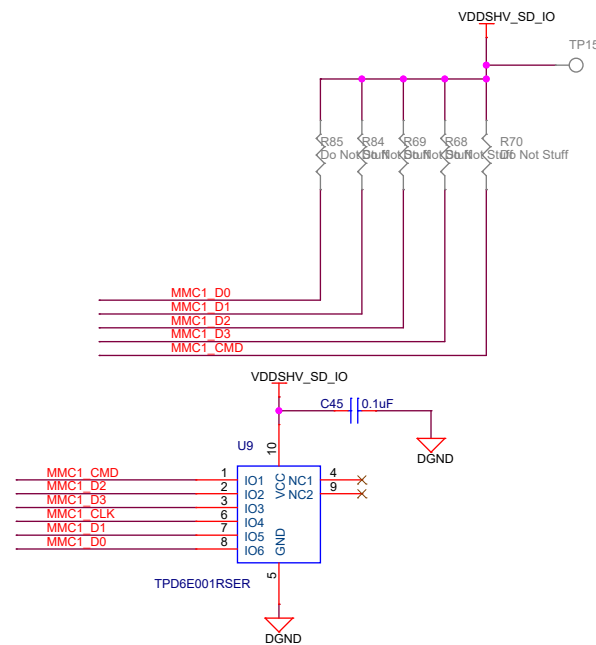
## SD CARD RESET



## POWER SWITCH



# SD CARD CONNECTOR



### OFF PAGE CONNECTIONS

16	MMC1_CLK	MMC1_CLK
38	MMC1_SD_EN	MMC1_SD_EN
16	MMC1_D0	MMC1_D0
16	MMC1_D1	MMC1_D1
16	MMC1_D2	MMC1_D2
16	MMC1_D3	MMC1_D3
16,18	MMC1_CMD	MMC1_CMD
16	MMC1_CMD	MMC1_CMD
16	MMC1_SDCD	MMC1_SDCD

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Title: SDCARD INTERFACE

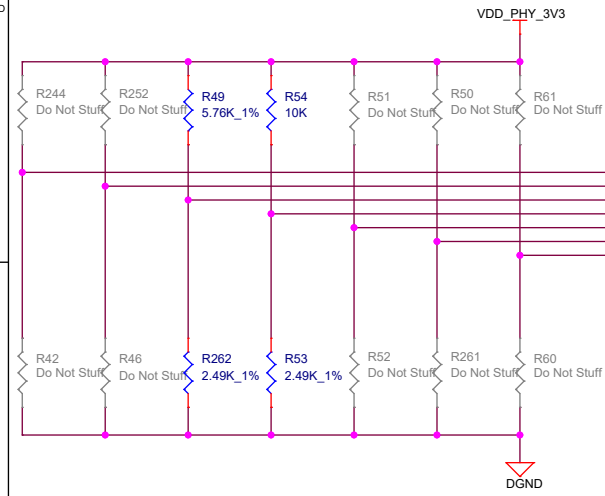
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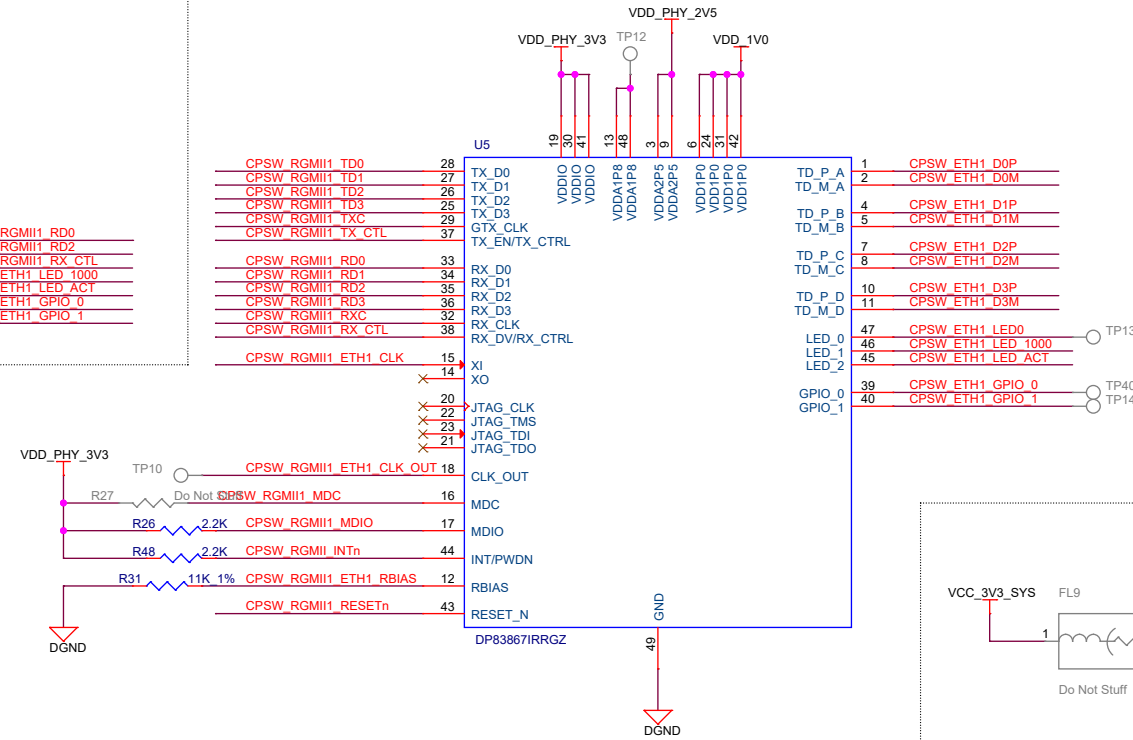
# STRAPPING RESISTORS



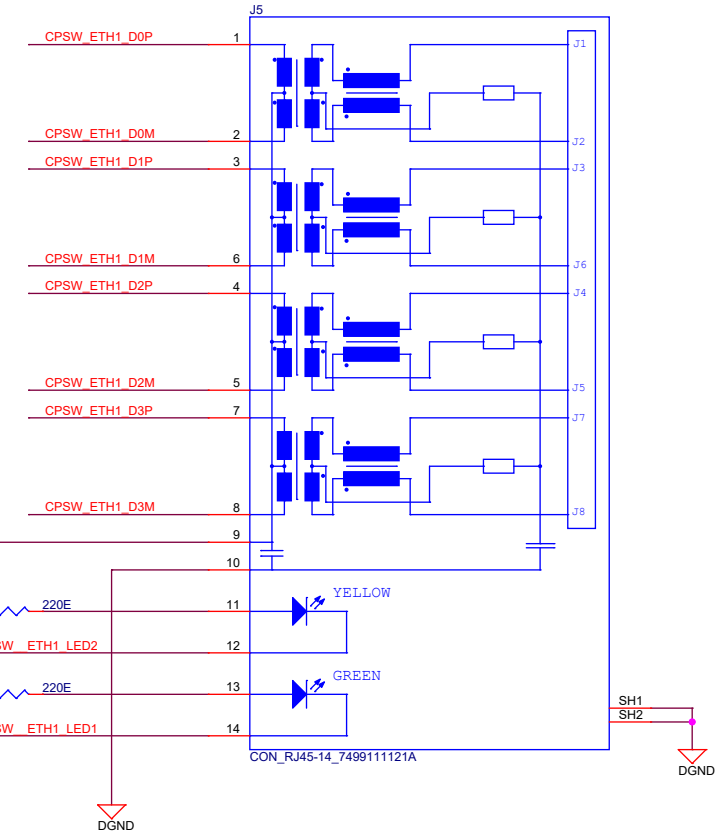
PHY ADDRESS = 00000  
 Auto-negotiation Enabled  
 10/100/1000 advertised, Auto-MDI-X  
 Tx Clock Skew = 0ns  
 Rx Clock Skew = 2ns  
 Refer 44 page for strap configuration

- CPSW\_RGMII\_INTn/PRU\_INTn R295 0E CPSW\_RGMII\_INTn
- CPSW\_RGMII2\_MDC R28 0E CPSW\_RGMII1\_MDC
- CPSW\_RGMII2\_MDIO R25 0E CPSW\_RGMII1\_MDIO

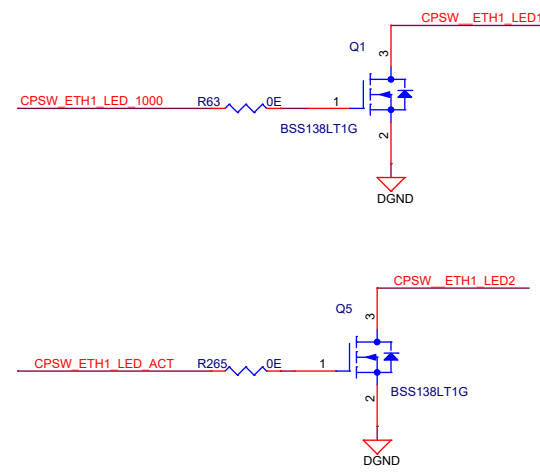
# CPSW RGMII 1 - PHY



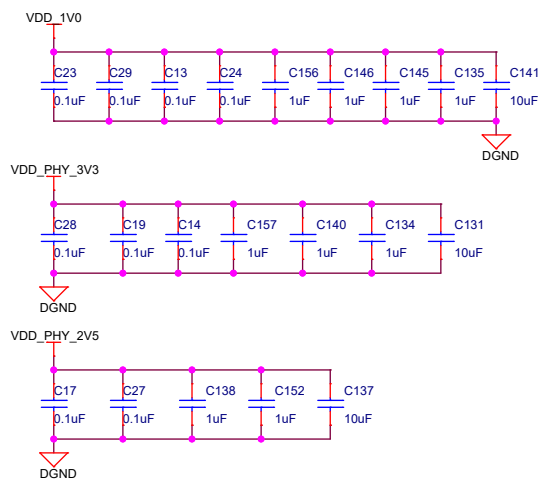
# RJ45 CONNECTOR WITH INTEGRATED MAGNETICS



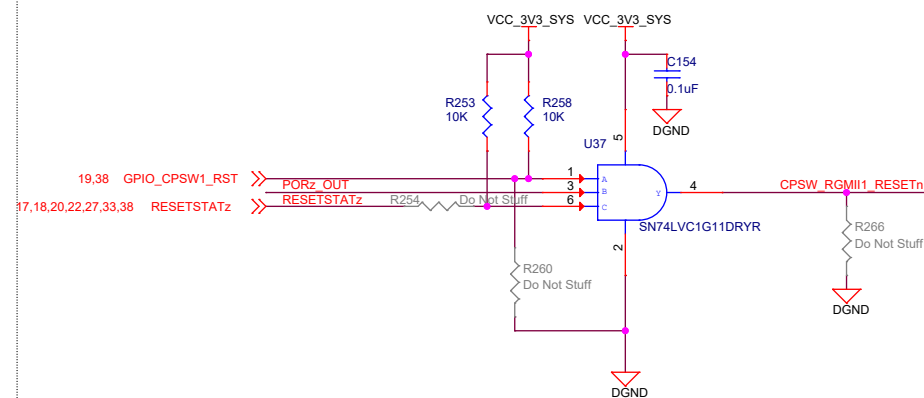
# CPSW PHY-1 SPEED AND ACTIVITY LED'S DRIVERS



# DECAPS



# CPSW PHY-1 RESET



# OFF PAGE CONNECTIONS

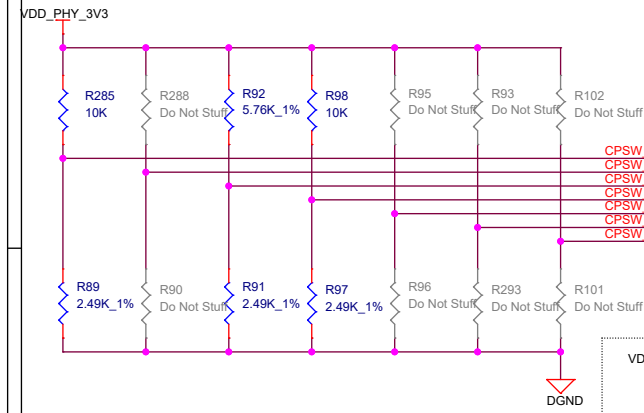
- 27 CPSW\_RGMII1\_RD0 CPSW\_RGMII1\_RD0
- 27 CPSW\_RGMII1\_RD1 CPSW\_RGMII1\_RD1
- 27 CPSW\_RGMII1\_RD2 CPSW\_RGMII1\_RD2
- 27 CPSW\_RGMII1\_RD3 CPSW\_RGMII1\_RD3
- 27 CPSW\_RGMII1\_RXC CPSW\_RGMII1\_RXC
- 27 CPSW\_RGMII1\_RX\_CTL CPSW\_RGMII1\_RX\_CTL
- 27 CPSW\_RGMII1\_TD0 CPSW\_RGMII1\_TD0
- 27 CPSW\_RGMII1\_TD1 CPSW\_RGMII1\_TD1
- 27 CPSW\_RGMII1\_TD2 CPSW\_RGMII1\_TD2
- 27 CPSW\_RGMII1\_TD3 CPSW\_RGMII1\_TD3
- 27 CPSW\_RGMII1\_TX\_CTL CPSW\_RGMII1\_TX\_CTL
- 27 CPSW\_RGMII1\_TXC CPSW\_RGMII1\_TXC
- 17,18,20,22,33 PORz\_OUT CPSW\_RGMII\_INTn/PRU\_INTn
- 27,33 CPSW\_RGMII\_INTn/PRU\_INTn GPIO\_CPSW1\_RST
- 19,38 GPIO\_CPSW1\_RST CPSW\_RGMII1\_ETH1\_CLK
- 31 CPSW\_RGMII1\_ETH1\_CLK CPSW\_RGMII2\_MDC
- 20,27 CPSW\_RGMII2\_MDC CPSW\_RGMII2\_MDIO
- 20,27 CPSW\_RGMII2\_MDIO CPSW\_RGMII\_INTn
- 20 CPSW\_RGMII\_INTn

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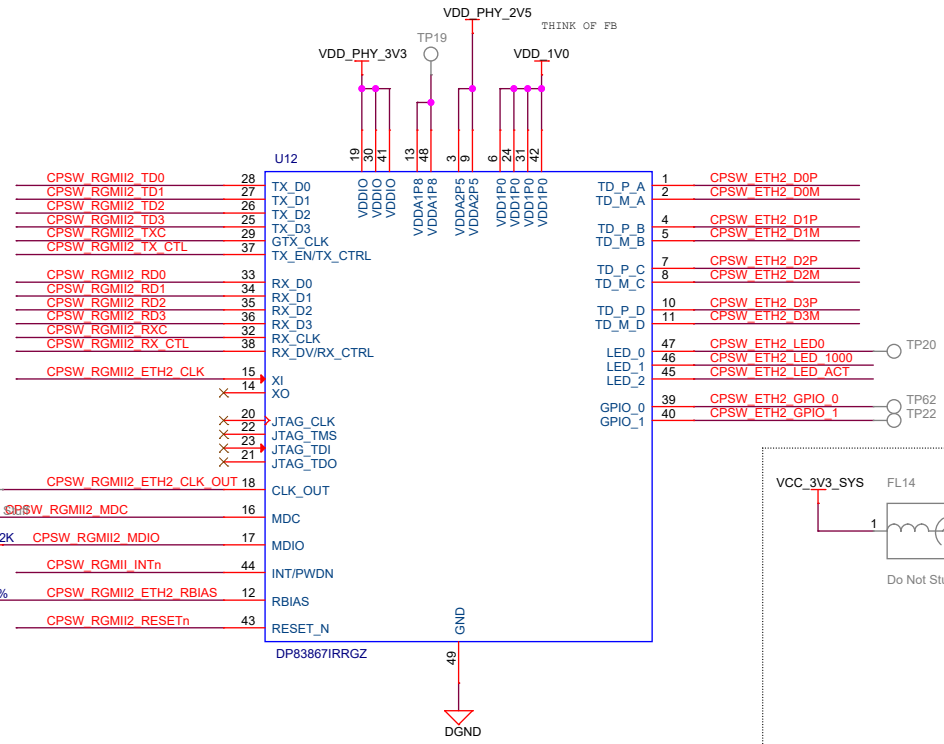
Title		CPSW_RGMII_1_ETHERNET_PHY	
Size	PROC100 001 SKAM64	Rev	E3
Date:	Thursday, July 01, 2021	Sheet	19 of 45

# STRAPPING RESISTORS

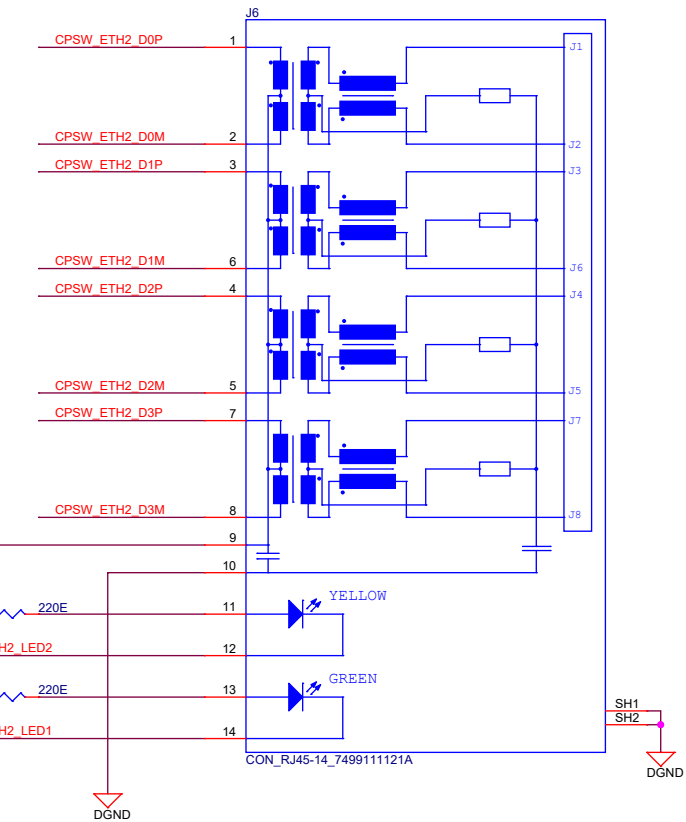


PHY ADDRESS = 00001  
 Auto-negotiation Enabled  
 10/100/1000 advertised, Auto-MDI-X  
 Tx Clock Skew = 0ns  
 Rx Clock Skew = 2ns  
 Refer 44 page for strap configuration

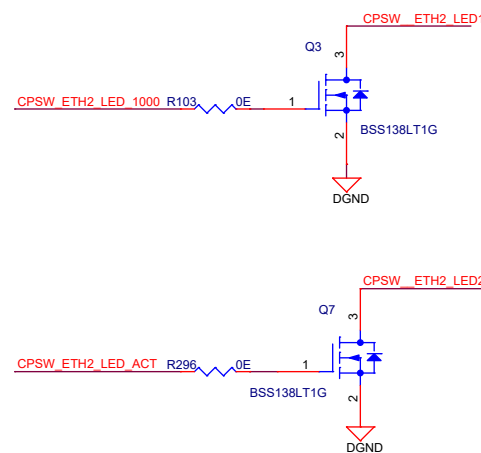
# CPSW RGMII 2 - PHY



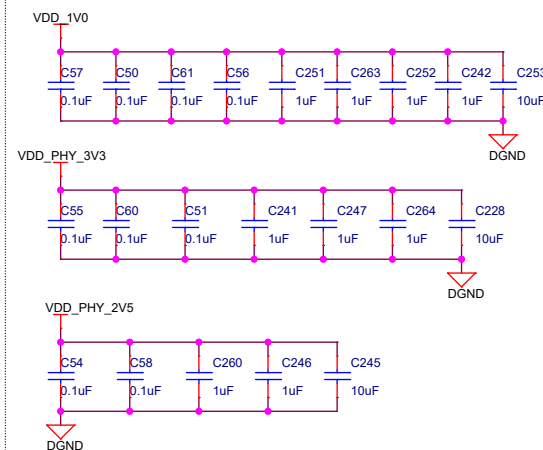
# RJ45 CONNECTOR



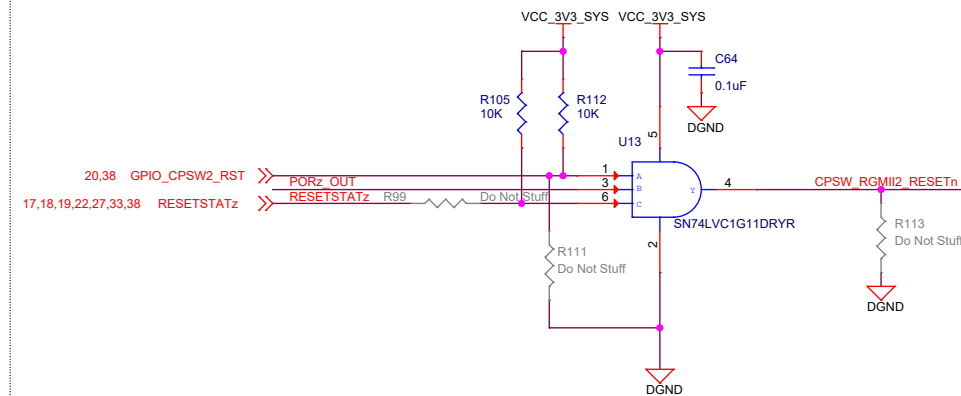
# CPSW PHY-2 SPEED AND ACTIVITY LED'S DRIVERS



# DECAPS



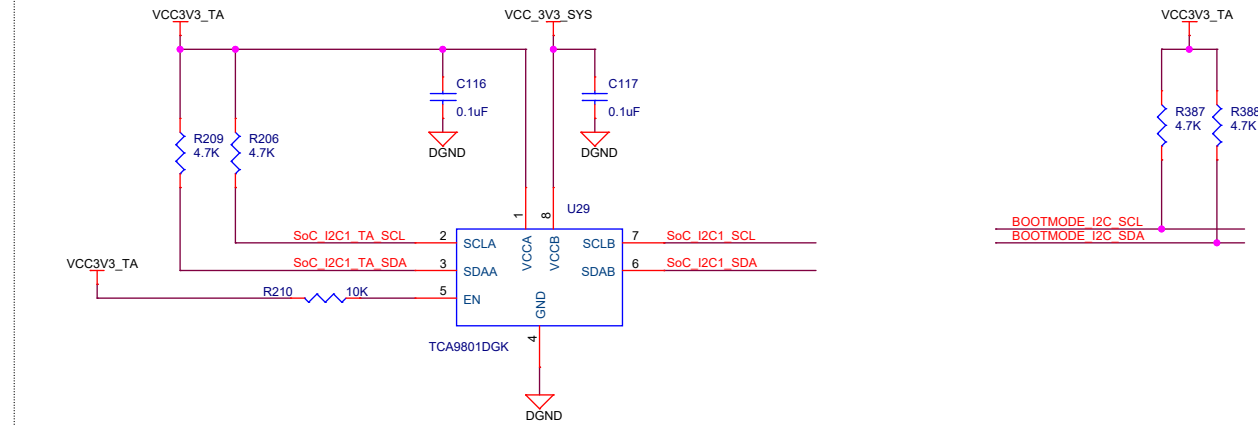
# CPSW PHY-2 RESET



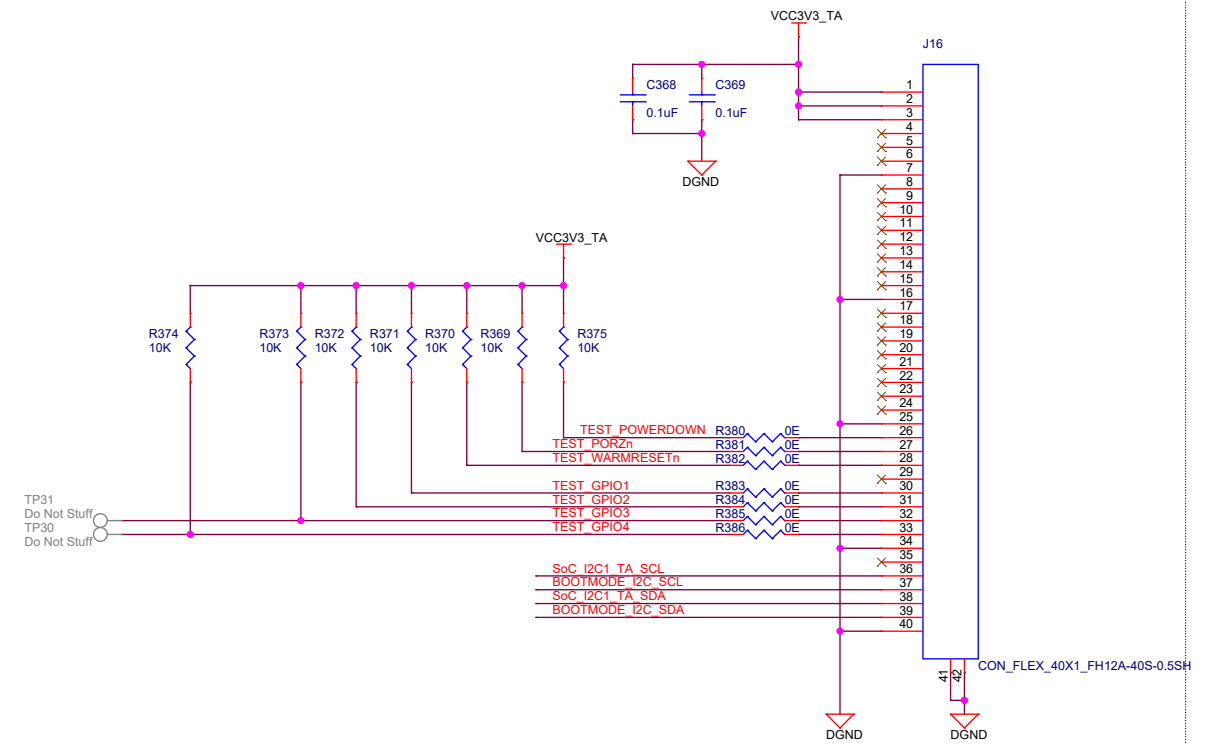
# OFF PAGE CONNECTIONS

27 CPSW_RGMII2_RD0	<<	CPSW_RGMII2_RD0
27 CPSW_RGMII2_RD1	<<	CPSW_RGMII2_RD1
27 CPSW_RGMII2_RD2	<<	CPSW_RGMII2_RD2
27 CPSW_RGMII2_RD3	<<	CPSW_RGMII2_RD3
27 CPSW_RGMII2_RXC	<<	CPSW_RGMII2_RXC
27 CPSW_RGMII2_RXC	<<	CPSW_RGMII2_RX_CTL
27 CPSW_RGMII2_RX_CTL	<<	CPSW_RGMII2_TX_CTL
27 CPSW_RGMII2_TD0	<<	CPSW_RGMII2_TD0
27 CPSW_RGMII2_TD1	<<	CPSW_RGMII2_TD1
27 CPSW_RGMII2_TD2	<<	CPSW_RGMII2_TD2
27 CPSW_RGMII2_TD3	<<	CPSW_RGMII2_TD3
27 CPSW_RGMII2_TXC	<<	CPSW_RGMII2_TXC
27 CPSW_RGMII2_TXC	<<	CPSW_RGMII2_TX_CTL
27 CPSW_RGMII2_TX_CTL	<<	PORz OUT
17,18,19,22,33	<<	PORz OUT
20,38	<<	GPIO_CPSW2_RST
31	<<	CPSW_RGMII2_ETH2_CLK
19,27	<<	CPSW_RGMII2_MDC
19,27	<<	CPSW_RGMII2_MDIO
19	<<	CPSW_RGMII2_INTn

## I2C BUS BUFFER



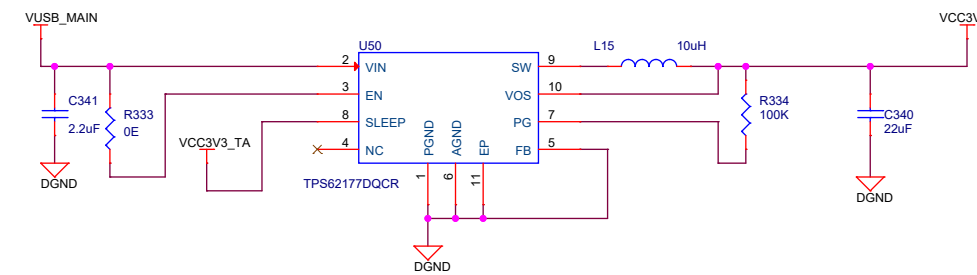
## 40-PIN AUTOMATION HEADER



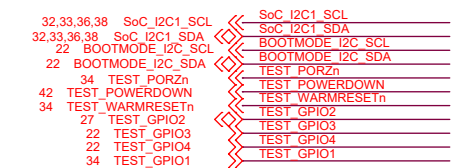
## TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO1_59_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to SoC GPIO to Communicate	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

## TEST AUTOMATION BOARD POWER



### OFF PAGE CONNECTIONS



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Title TEST AUTOMATION

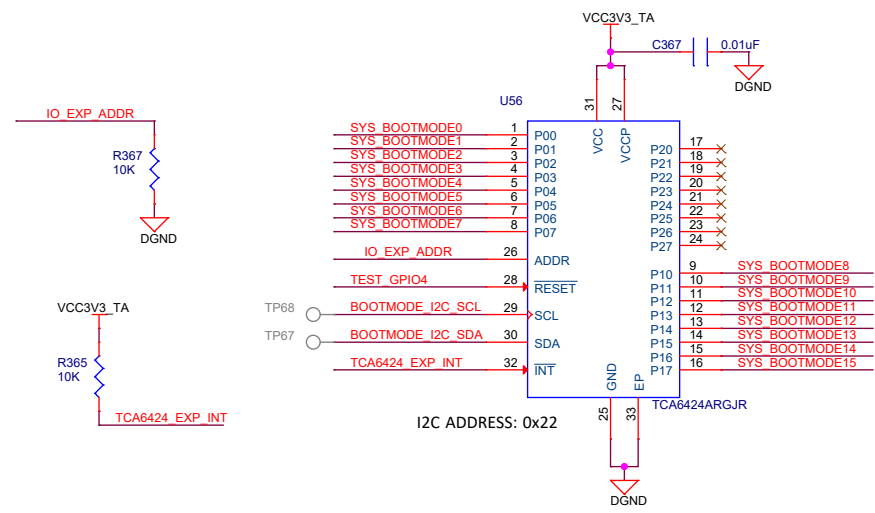
Size PROC100 001 SKAM64

Date: Thursday, July 01, 2021

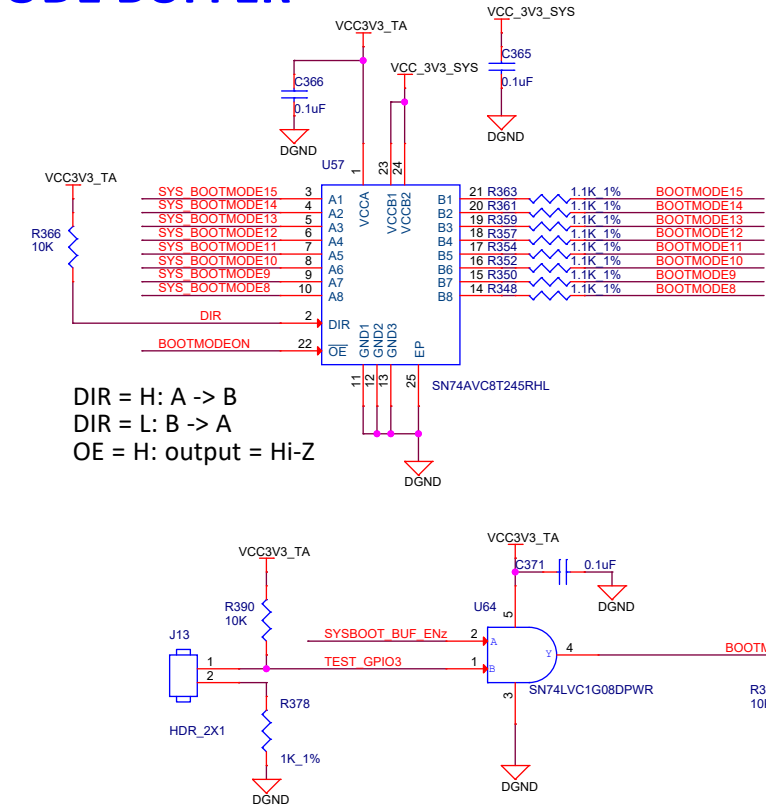
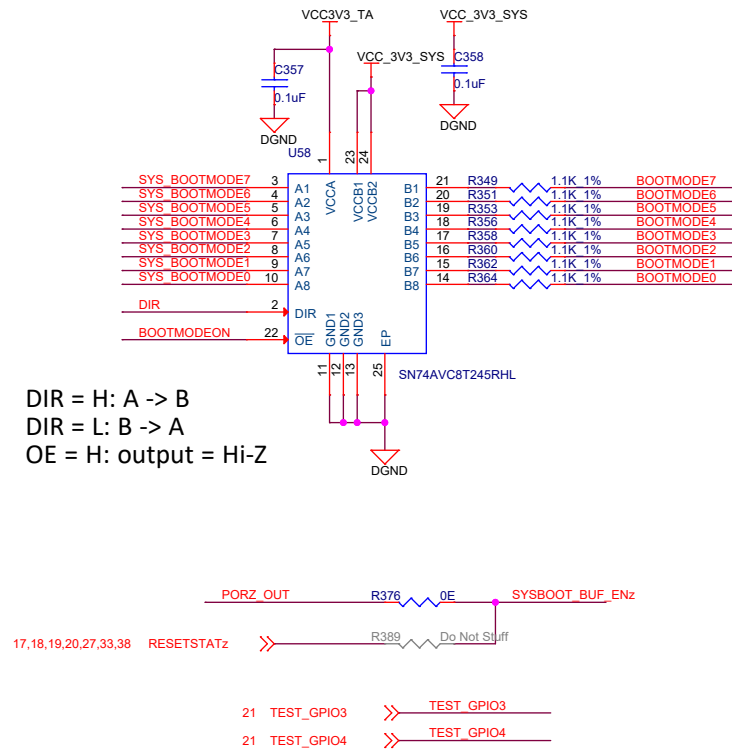
Rev E3

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## IO EXPANDER



## BOOT MODE BUFFER

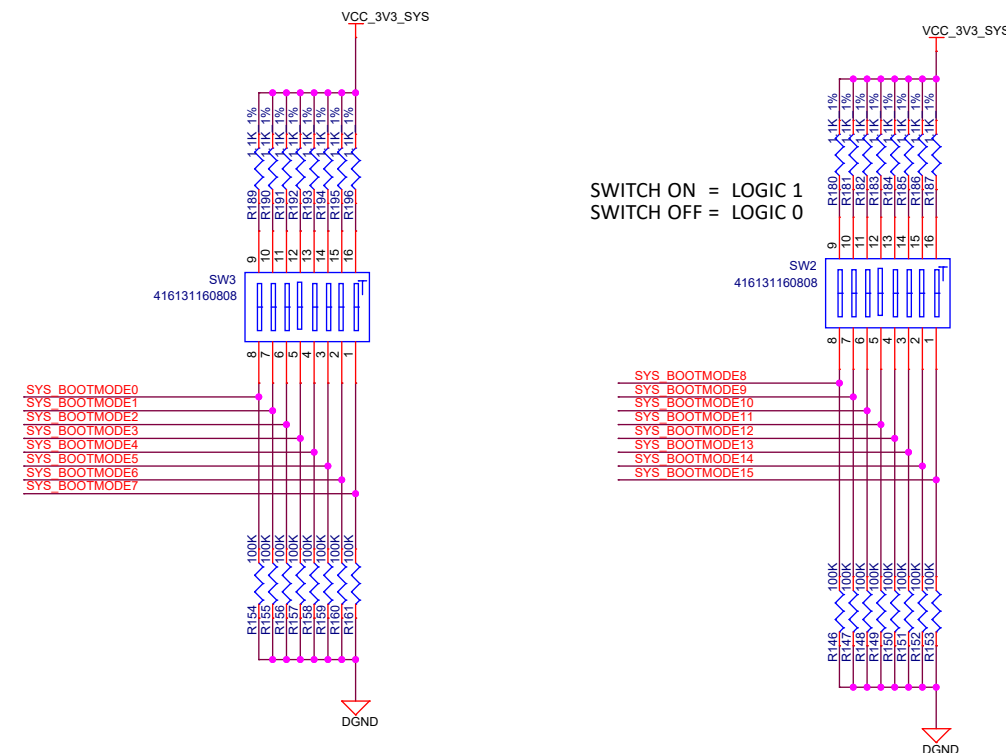


## BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. CPSW Ethernet
4. USB Device
5. Ethernet

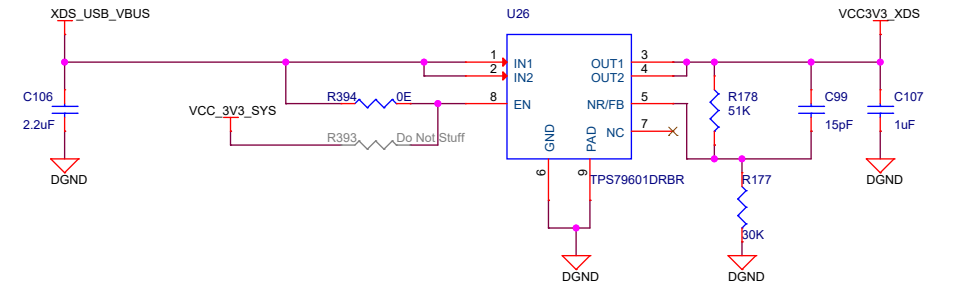
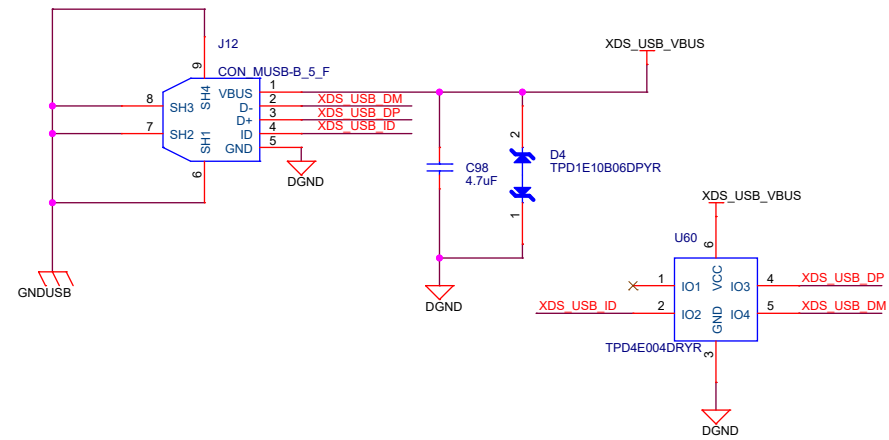
MCU Boot Mode Pins to be Finalized

## BOOT MODE SWITCHES

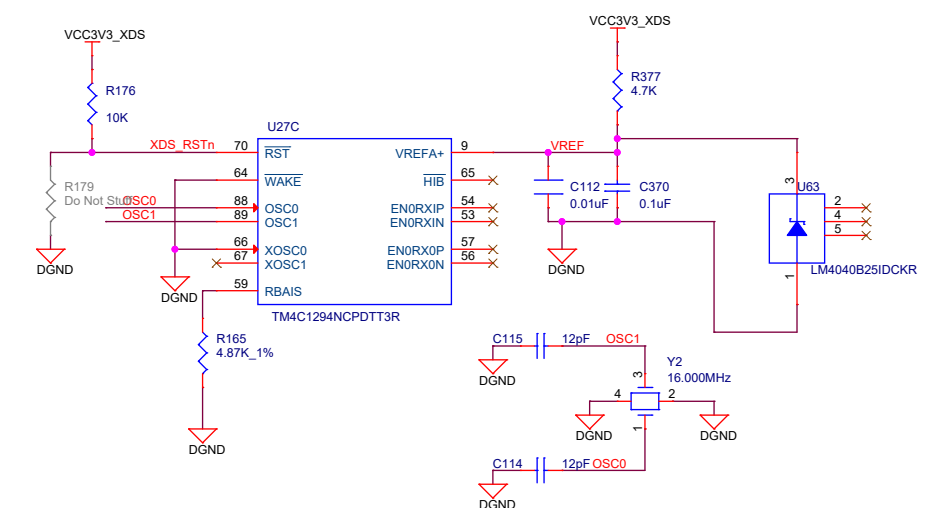
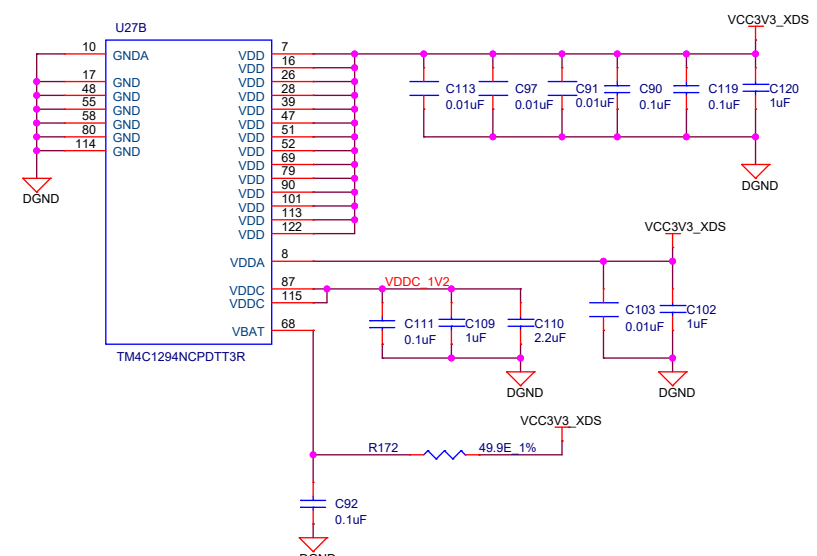
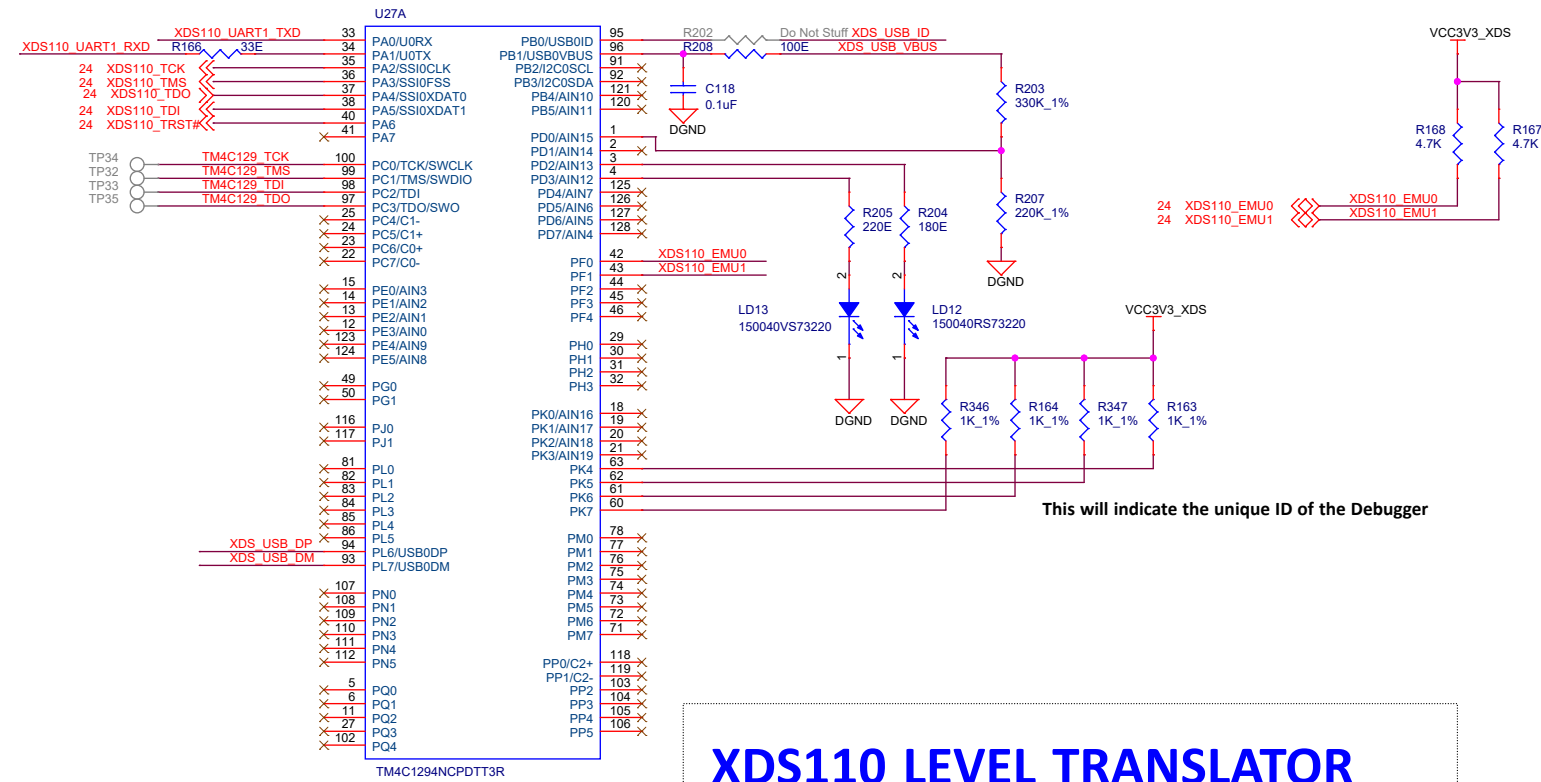


# XDS110 POWER

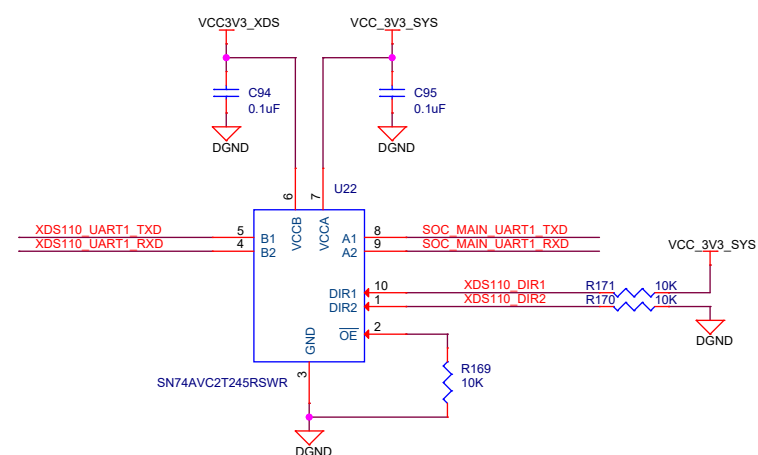
## USB Connector



# XDS110 DEBUGGER



# XDS110 LEVEL TRANSLATOR



## OFF PAGE CONNECTIONS

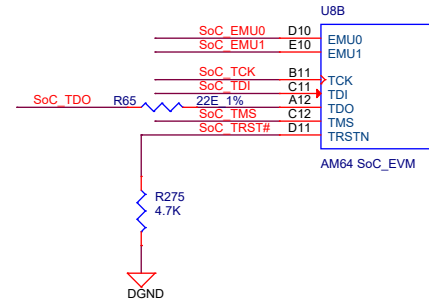


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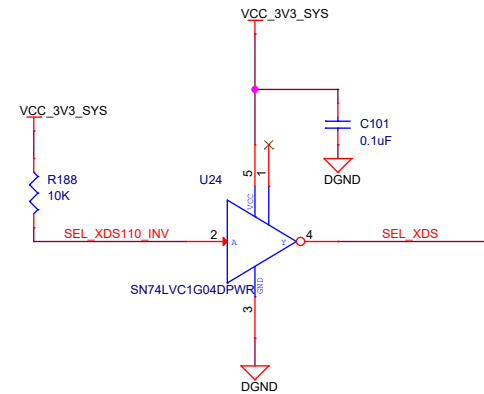


Title		XDS110 DEBUGGER	
Size	PROC100 001 SKAM64	Rev	E3
Date:	Thursday, July 01, 2021	Sheet	23 of 45

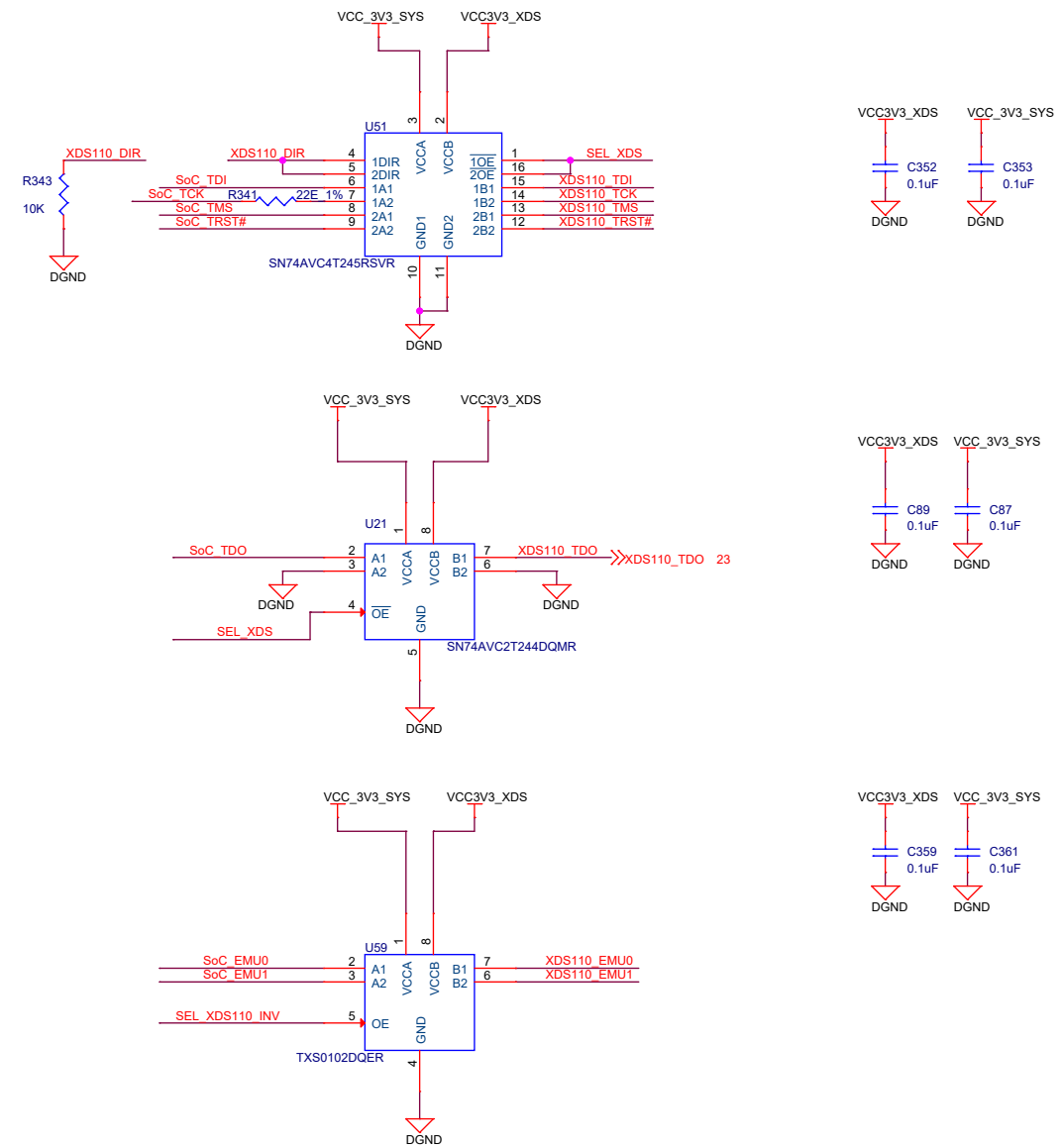
## JTAG SoC SECTION



## INVERTER



## BUFFER XDS110



### OFF PAGE CONNECTIONS

25	SEL_XDS110_INV	SEL_XDS110_INV
23	XDS110_TDI	XDS110_TDI
23	XDS110_TCK	XDS110_TCK
23	XDS110_TMS	XDS110_TMS
23	XDS110_TRST#	XDS110_TRST#
		SoC_TDO
25	SoC_TDO	SoC_TDI
25	SoC_TDI	SoC_TCK
25	SoC_TCK	SoC_TMS
25	SoC_TMS	SoC_TMS
23	XDS110_EMU0	XDS110_EMU0
23	XDS110_EMU1	XDS110_EMU1
23	XDS110_EMU1	SEL_XDS
25	SEL_XDS	SoC_EMU0
25	SoC_EMU0	SoC_EMU1
25	SoC_EMU1	SoC_EMU1
25	SoC_TRST#	SoC_TRST#

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Title: JTAG BUFFER

Size: PROC100 001 SKAM64

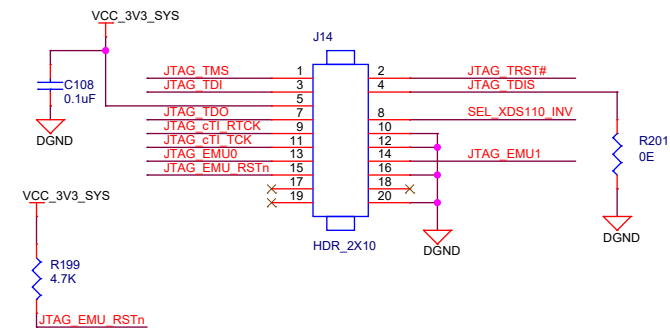
Rev: E3

Date: Thursday, July 01, 2021

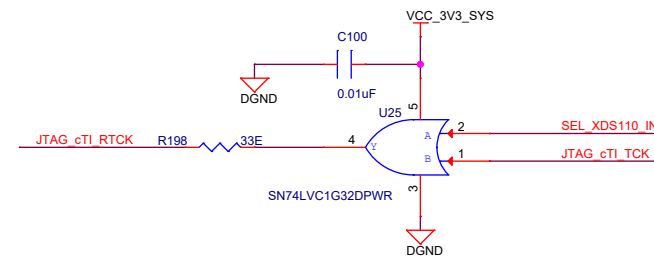
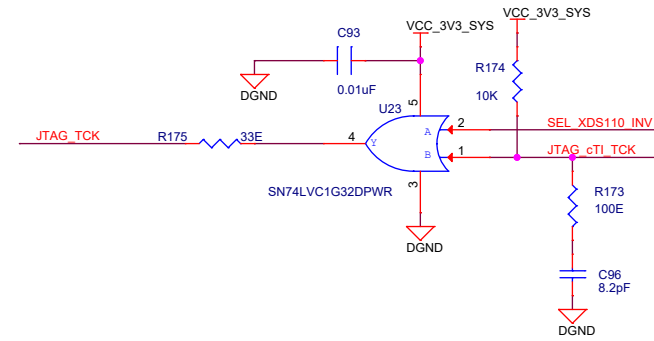
Sheet 24 of 45



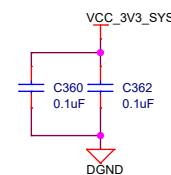
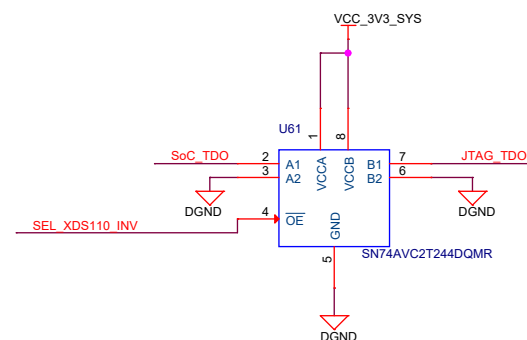
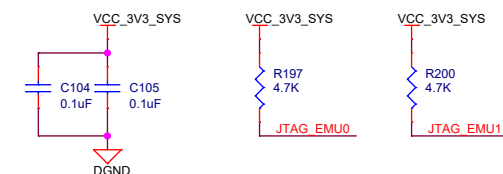
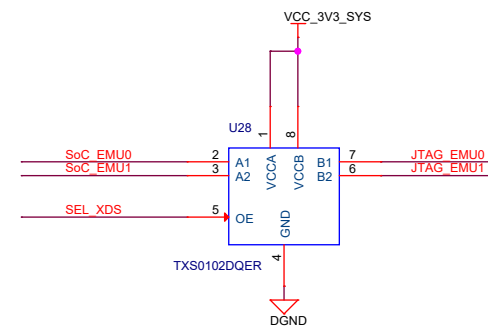
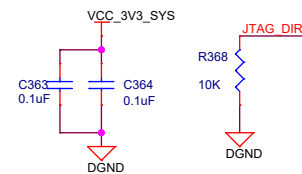
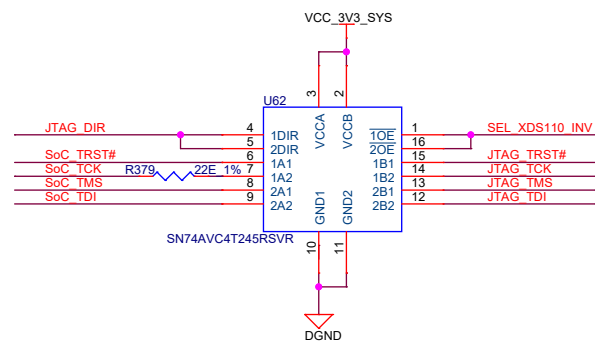
# JTAG 20 PIN cTI CONNECTOR



# JTAG CLOCK BUFFER



# 20 PIN JTAG BUFFERS



## OFF PAGE CONNECTIONS

24	SEL_XDS110_INV	SEL_XDS110_INV
24	SoC_TDO	SoC_TDO
24	SoC_TDI	SoC_TDI
24	SoC_TCK	SoC_TCK
24	SoC_TMS	SoC_TMS
24	SoC_TRST#	SoC_TRST#
34	JTAG_EMU_RSTn	JTAG_EMU_RSTn
24	SEL_XDS	SEL_XDS
24	SoC_EMU0	SoC_EMU0
24	SoC_EMU1	SoC_EMU1

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Title: JTAG 20 PIN cTI CONNECTOR

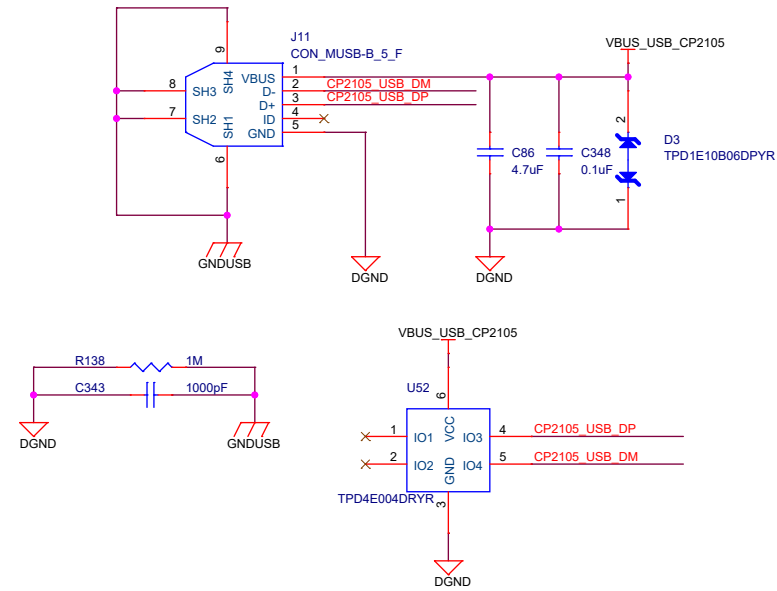
Size: PROC100 001 SKAM64

Date: Thursday, July 01, 2021

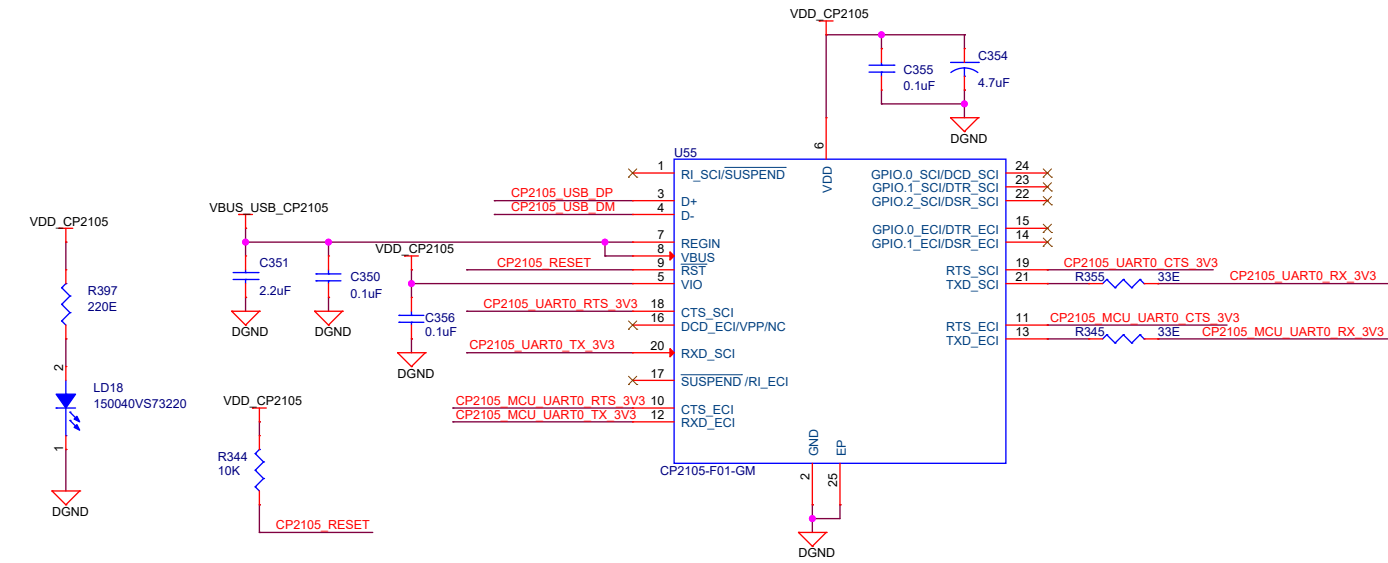
Rev: E3

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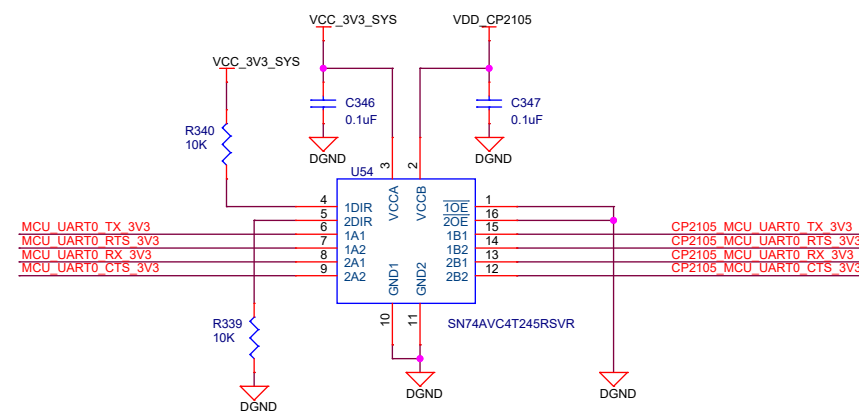
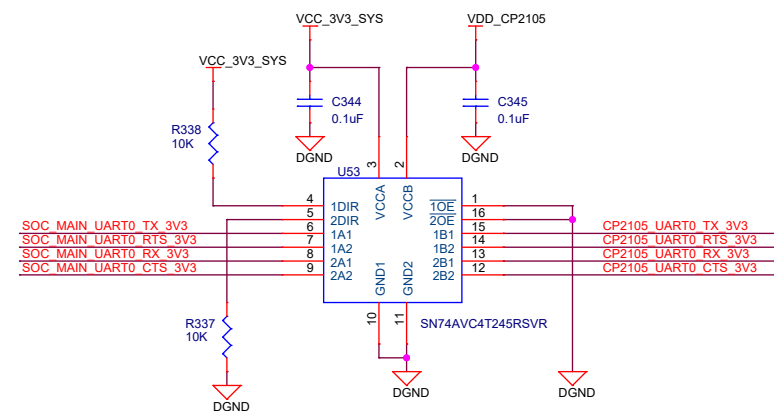
## USB Micro B CONNECTOR



## USB TO DUAL UART BRIDGE



## CP2105 LEVEL TRANSLATOR



### OFF PAGE CONNECTIONS

SOC_MAIN_UART0_RX_3V3	SOC_MAIN_UART0_RX_3V3	33
SOC_MAIN_UART0_TX_3V3	SOC_MAIN_UART0_TX_3V3	33
SOC_MAIN_UART0_RTS_3V3	SOC_MAIN_UART0_RTS_3V3	33
SOC_MAIN_UART0_CTS_3V3	SOC_MAIN_UART0_CTS_3V3	33
MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	33
MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	33
MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	33
MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	33

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Title: CP2105 UART TO USB BRIDGE

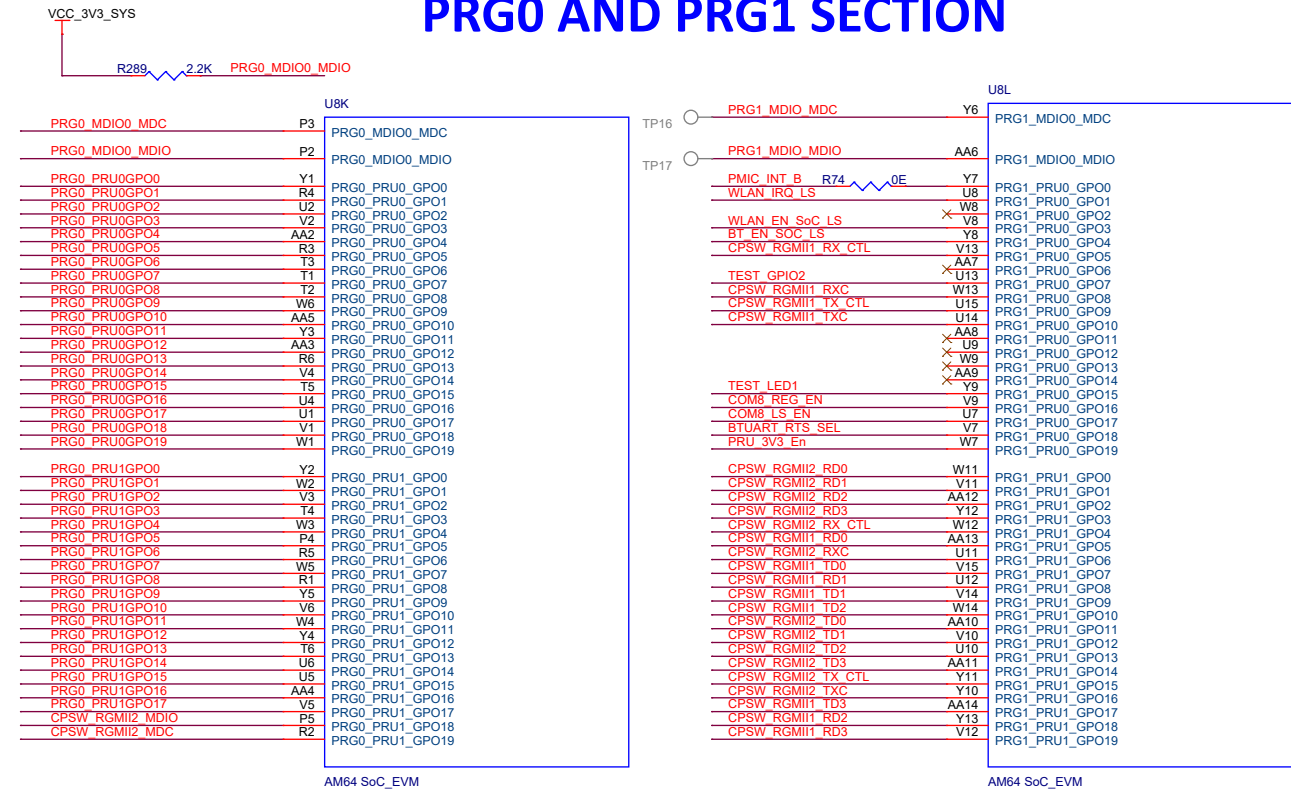
Size: PROC100 001 SKAM64

Date: Thursday, July 01, 2021

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# PRG0 AND PRG1 SECTION



# PRU CONNECTOR

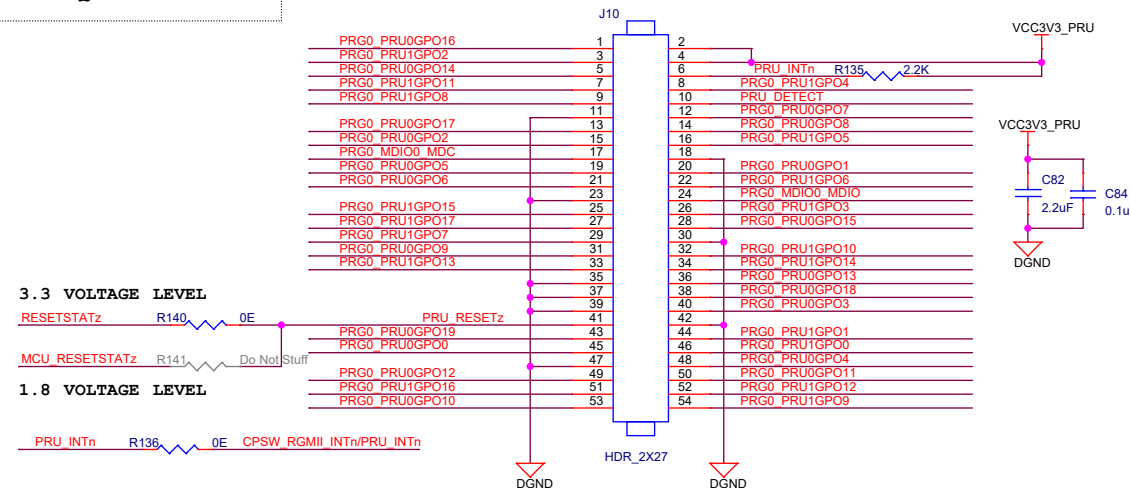
FOR LAUNCHPAD HEADER  
USE PART SSQ-127-23-L-D

## NOTE:

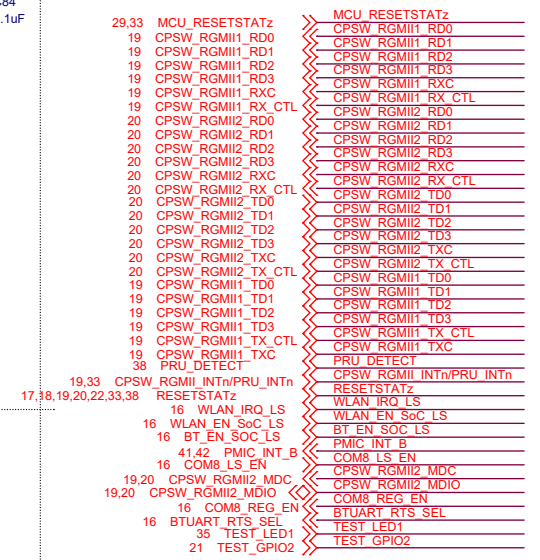
AM64x Starter Kit shall not be powered through the 3V3 pins on the PRU Connector.

PRU Connector I/O are not fail-safe and shall not be driven when AM64x Starter Kit is not powered.

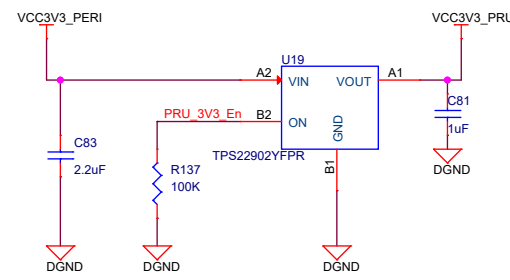
3V3 supply of User Expansion Connector is limited to sourcing 500mA max.



## OFF PAGE CONNECTIONS



# POWER SWITCH FOR 3.3V TO PRU CONNECTOR

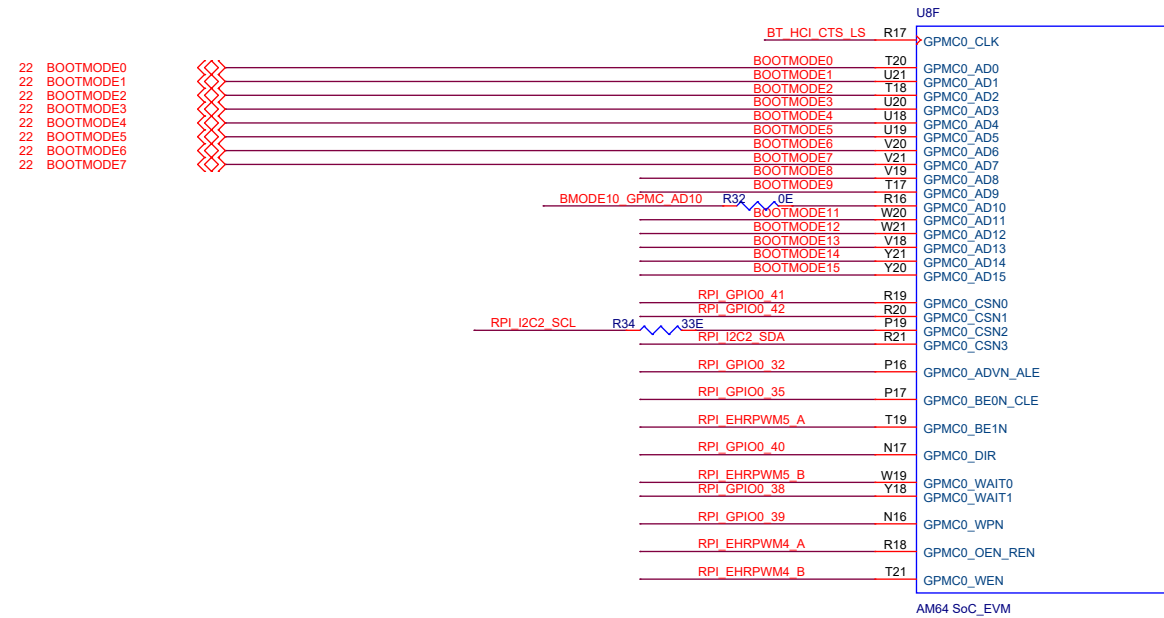


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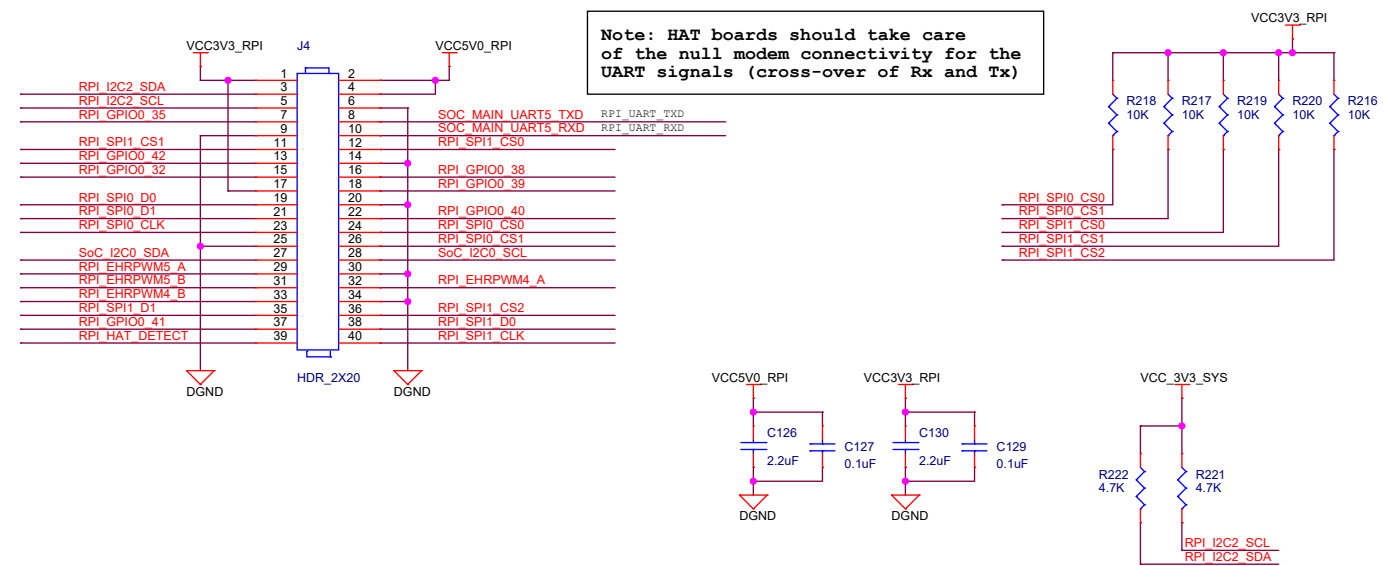


Title		PRU CONNECTOR
Size	PROC100 001 SKAM64	Rev
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Date:	Thursday, July 01, 2021	Sheet 27 of 45

## GPMC SECTION



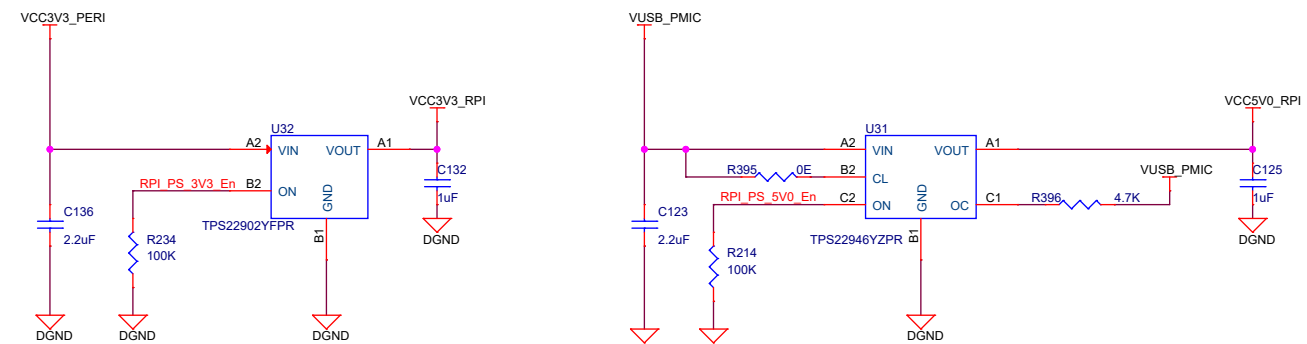
## USER EXPANSION CONNECTOR



Note: This connector is compatible to GPIO Expansion Header (J8) found on the Raspberry Pi Boards

Note: Raspberry Pi is the trademark / wordmark of Raspberry Pi Foundation

## POWER SWITCH FOR USER EXPANSION CONNECTOR



### NOTE:

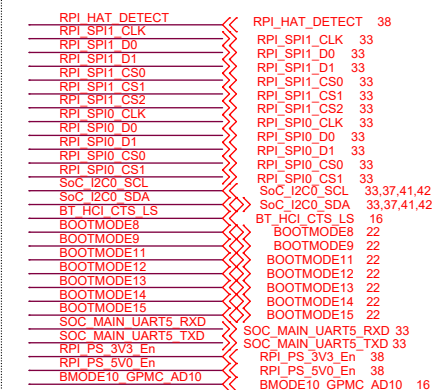
AM64x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM64x Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

### OFF PAGE CONNECTIONS



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Title USER EXPANSION CONNECTOR

Size PROC100 001 SKAM64

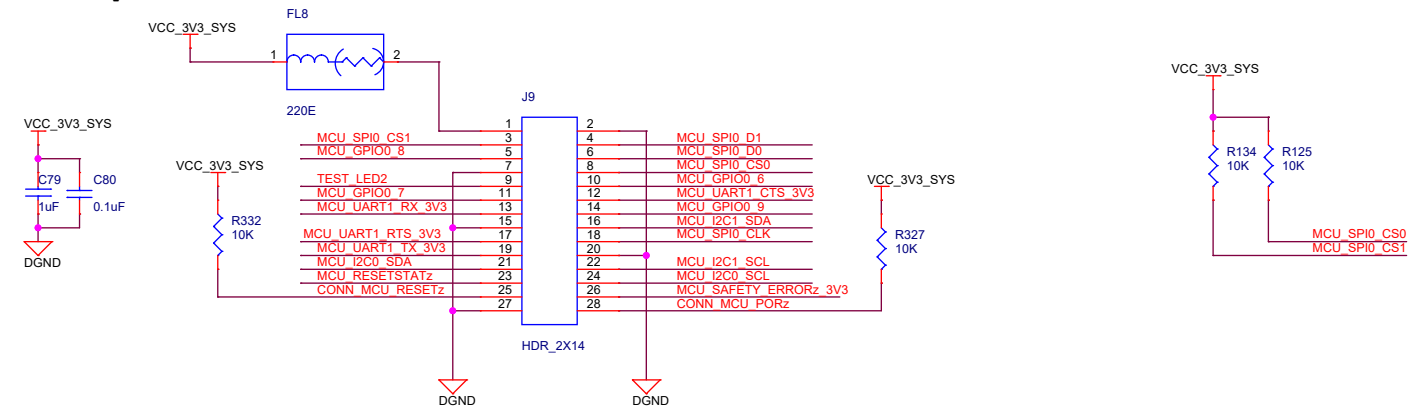
Date: Thursday, July 01, 2021

Rev E3

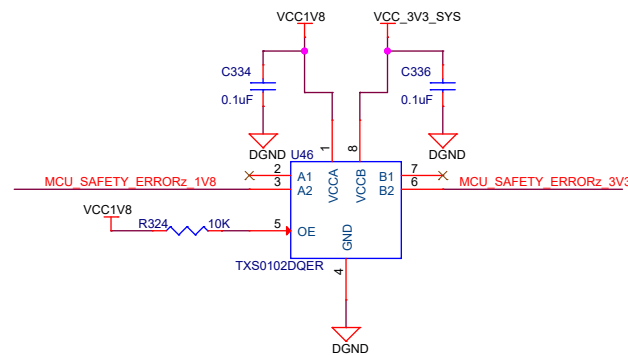
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# MCU CONNECTOR

Only 100mA supported on this pin



# LEVEL TRANSLATOR



## OFF PAGE CONNECTIONS

34	CONN_MCU_RESETz	CONN_MCU_RESETz
34	CONN_MCU_PORz	CONN_MCU_PORz
33	MCU_SPI0_CS1	MCU_SPI0_CS1
33	MCU_GPIO0_8	MCU_GPIO0_8
33,35	TEST_LED2	TEST_LED2
33	MCU_GPIO0_7	MCU_GPIO0_7
33	MCU_UART1_RX_3V3	MCU_UART1_RX_3V3
33	MCU_UART1_RTS_3V3	MCU_UART1_RTS_3V3
33	MCU_UART1_TX_3V3	MCU_UART1_TX_3V3
33	MCU_I2C0_SDA	MCU_I2C0_SDA
33	MCU_I2C0_SCL	MCU_I2C0_SCL
27,33	MCU_RESETSTATz	MCU_RESETSTATz
33	MCU_SPI0_D1	MCU_SPI0_D1
33	MCU_SPI0_D0	MCU_SPI0_D0
33	MCU_SPI0_CS0	MCU_SPI0_CS0
33,34	MCU_GPIO0_6	MCU_GPIO0_6
33	MCU_UART1_CTS_3V3	MCU_UART1_CTS_3V3
33	MCU_GPIO0_9	MCU_GPIO0_9
33	MCU_I2C1_SDA	MCU_I2C1_SDA
33	MCU_I2C1_SCL	MCU_I2C1_SCL
33	MCU_I2C0_SDA	MCU_I2C0_SDA
33	MCU_I2C0_SCL	MCU_I2C0_SCL
33	MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8

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Title MCU CONNECTOR

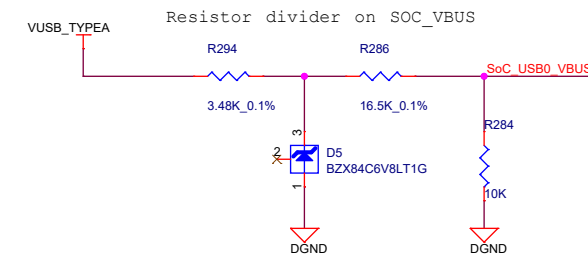
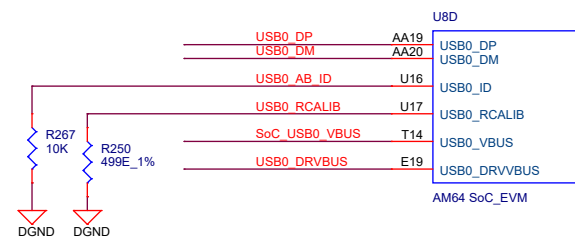
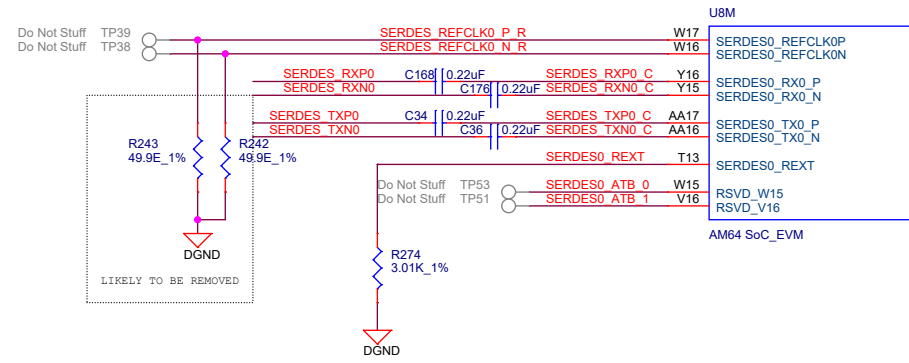
Size PROC100 001 SKAM64

Date: Thursday, July 01, 2021

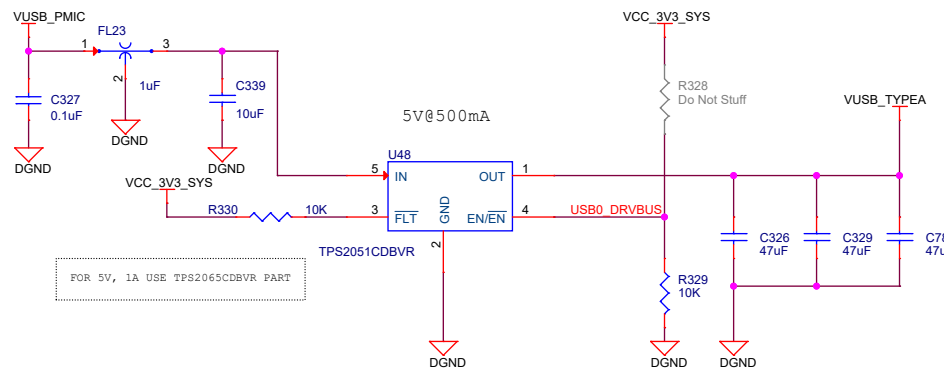
Rev E3

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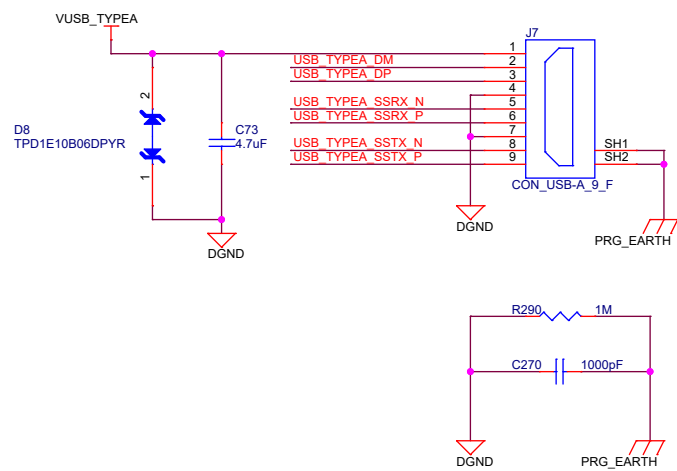
# USB 3.0 INTERFACE



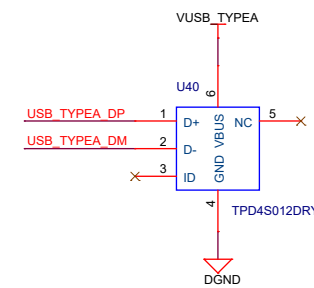
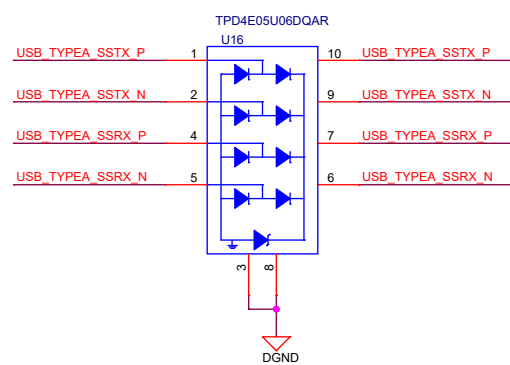
# 5V Power switch for USB 3.0 Device



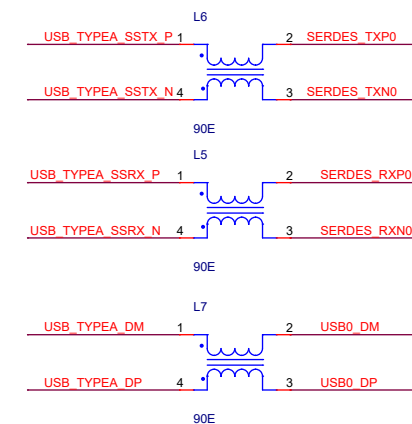
# Type-A Connector



# ESD DIODES



# CHOKES

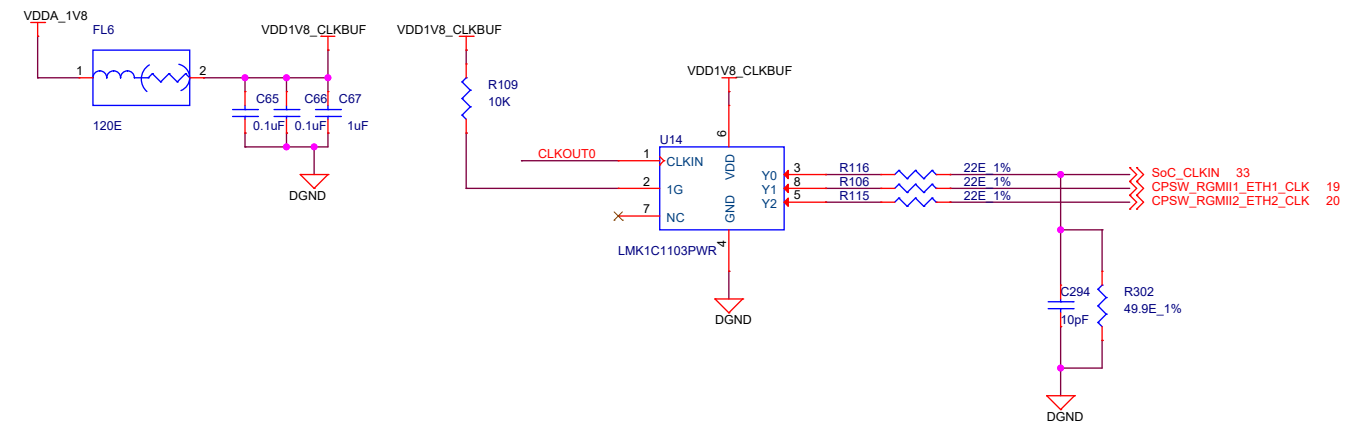


Designed for TI by Mistral Solutions Pvt Ltd



Title		USB 3.0 INTERFACE
Size	PROC100 001 SKAM64	Rev
C		E3
Date:	Thursday, July 01, 2021	Sheet 30 of 45

# ETHERNET PHY CLOCK BUFFER



## OFF PAGE CONNECTIONS

33.39 CLKOUT0 ← CLKOUT0

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Title ETHERNET PHY CLOCK BUFFER

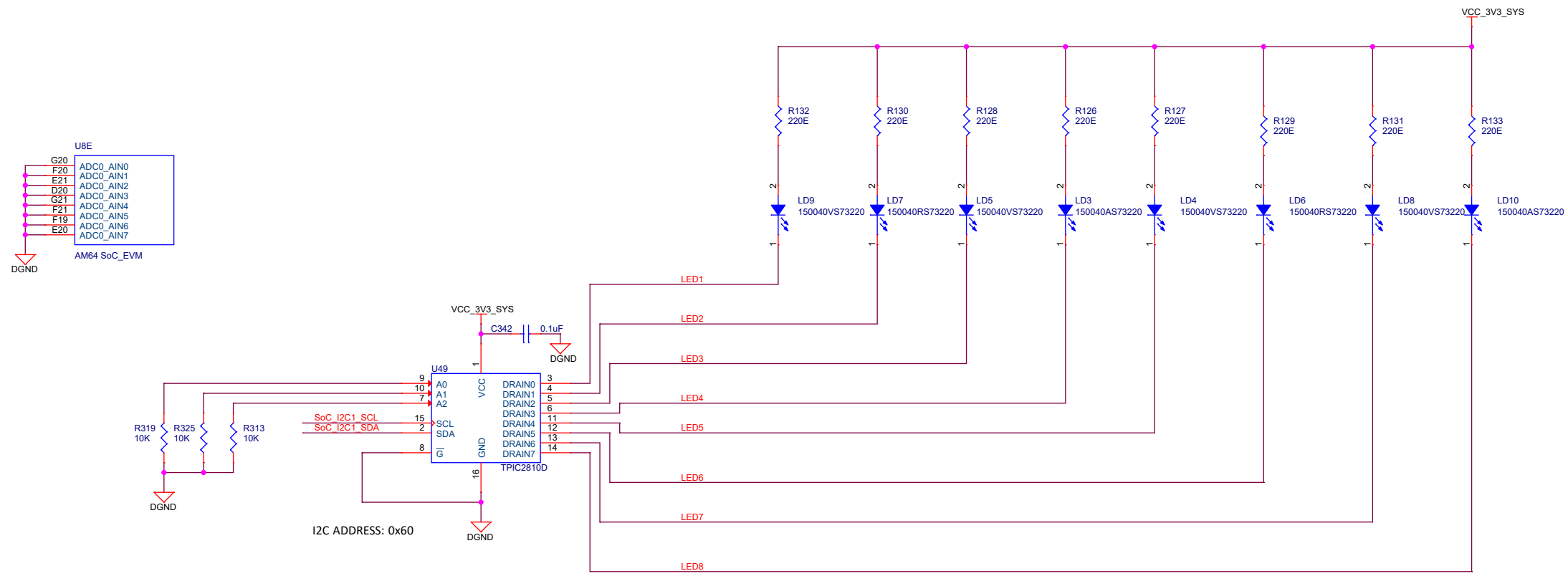
Size PROC100 001 SKAM64

Rev E3

Date: Thursday, July 01, 2021

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# INDUSTRIAL COMMUNICATION LED's

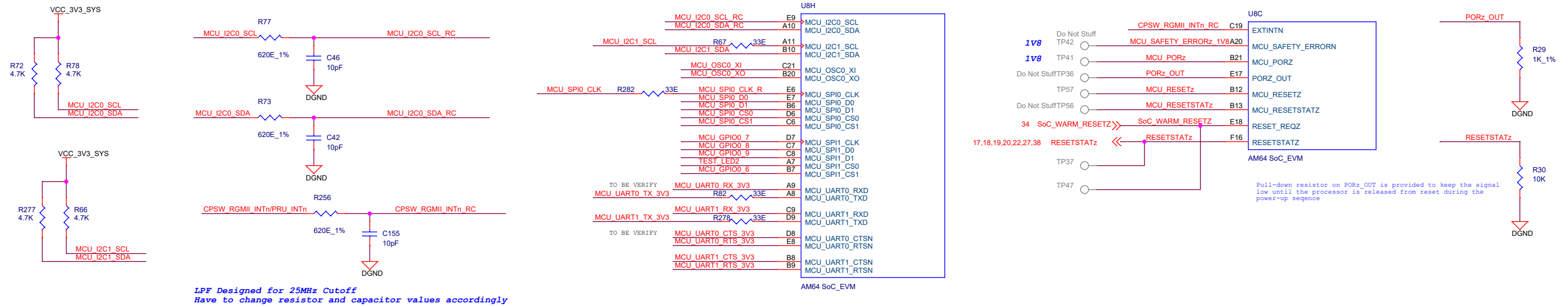


**OFF PAGE CONNECTIONS**

SoC\_I2C1\_SCL SoC\_I2C1\_SCL 21,33,36,38  
 SoC\_I2C1\_SDA SoC\_I2C1\_SDA 21,33,36,38

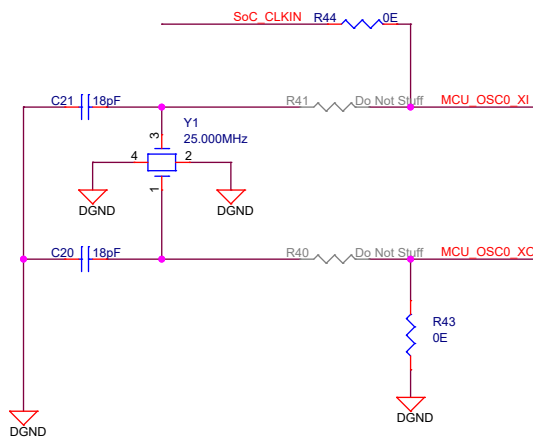


# MCU\_GENERAL

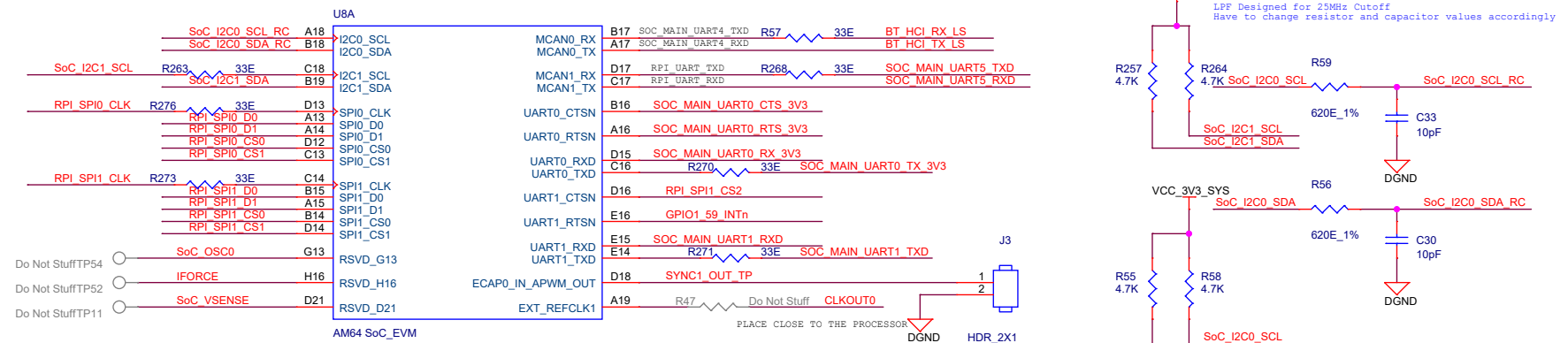


# CRYSTAL

Only Footprint option to mount the Oscillator is provided. By default the part is not mounted on the board.



# SoC MAIN DOMAIN



## OFF PAGE CONNECTIONS

34 MCU_RESETz	MCU_RESETz	29 MCU_SPI0_CS1	MCU_SPI0_CS1	BT_HCI_TX_LS	BT_HCI_TX_LS 18
34 MCU_PORz	MCU_PORz	29 MCU_GPIO0_8	MCU_GPIO0_8	BT_HCI_RX_LS	BT_HCI_RX_LS 16
27,29,33 MCU_RESETSTATz	MCU_RESETSTATz	29,33,35 TEST_LED2	TEST_LED2	SOC_MAIN_UART5_RXD	SOC_MAIN_UART5_RXD 28
17,18,19,20,22 PORz_OUT	PORz_OUT	29 MCU_UART1_RX_3V3	MCU_UART1_RX_3V3	SOC_MAIN_UART5_TXD	SOC_MAIN_UART5_TXD 28
19,27 CPSW_RGMII_INTn/PRU_INTn	CPSW_RGMII_INTn/PRU_INTn	29 MCU_UART1_RTS_3V3	MCU_UART1_RTS_3V3	RPI_SPI1_CLK	RPI_SPI1_CLK 28
29,33,35 TEST_LED2	TEST_LED2	29 MCU_UART1_TX_3V3	MCU_UART1_TX_3V3	RPI_SPI1_D0	RPI_SPI1_D0 28
29,33,34 MCU_GPIO0_6	MCU_GPIO0_6	29 MCU_I2C0_SDA	MCU_I2C0_SDA	RPI_SPI1_D1	RPI_SPI1_D1 28
31 SoC_CLKIN	SoC_CLKIN	29 MCU_I2C1_SDA	MCU_I2C1_SDA	RPI_SPI1_CS0	RPI_SPI1_CS0 28
26 MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	29 MCU_I2C1_SCL	MCU_I2C1_SCL	RPI_SPI1_CS1	RPI_SPI1_CS1 28
26 MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	29 MCU_SPI0_CLK	MCU_SPI0_CLK	RPI_SPI1_CS2	RPI_SPI1_CS2 28
26 MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	29 MCU_I2C0_SCL	MCU_I2C0_SCL	SOC_MAIN_UART0_RX_3V3	SOC_MAIN_UART0_RX_3V3 26
26 MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	29 MCU_I2C0_SDA	MCU_I2C0_SDA	SOC_MAIN_UART0_TX_3V3	SOC_MAIN_UART0_TX_3V3 26
		29 MCU_SPI0_CS0	MCU_SPI0_CS0	SOC_MAIN_UART0_RTS_3V3	SOC_MAIN_UART0_RTS_3V3 26
		29 MCU_SPI0_D0	MCU_SPI0_D0	SOC_MAIN_UART0_CTS_3V3	SOC_MAIN_UART0_CTS_3V3 26
		29 MCU_SPI0_D1	MCU_SPI0_D1	SoC_I2C0_SCL	SoC_I2C0_SCL 28,37,41,42
		29 MCU_RESETSTATz	MCU_RESETSTATz	SoC_I2C0_SDA	SoC_I2C0_SDA 28,37,41,42
		29 MCU_SPI0_CS1	MCU_SPI0_CS1	SoC_I2C1_SCL	SoC_I2C1_SCL 21,32,36,38
		29 MCU_SPI0_CS0	MCU_SPI0_CS0	SoC_I2C1_SDA	SoC_I2C1_SDA 21,32,36,38
		29,33,34 MCU_GPIO0_6	MCU_GPIO0_6	SoC_I2C1_SDA	SoC_I2C1_SDA 21,32,36,38
		29 MCU_I2C1_CTS_3V3	MCU_I2C1_CTS_3V3	CLKOUT0	CLKOUT0 31,39
		29 MCU_GPIO0_9	MCU_GPIO0_9	RPI_SPI1_CLK	RPI_SPI1_CLK 28
		29 MCU_I2C1_SDA	MCU_I2C1_SDA	RPI_SPI1_D0	RPI_SPI1_D0 28
		29 MCU_SPI0_CLK	MCU_SPI0_CLK	RPI_SPI1_D1	RPI_SPI1_D1 28
		29 MCU_I2C1_SCL	MCU_I2C1_SCL	RPI_SPI1_CS0	RPI_SPI1_CS0 28
		29 MCU_I2C0_SCL	MCU_I2C0_SCL	RPI_SPI1_CS1	RPI_SPI1_CS1 28
29 MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8			RPI_SPI1_CS2	RPI_SPI1_CS2 28
				SOC_MAIN_UART1_RXD	SOC_MAIN_UART1_RXD 23
				SOC_MAIN_UART1_TXD	SOC_MAIN_UART1_TXD 23

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Title SoC MAIN AND MCU DOMAIN

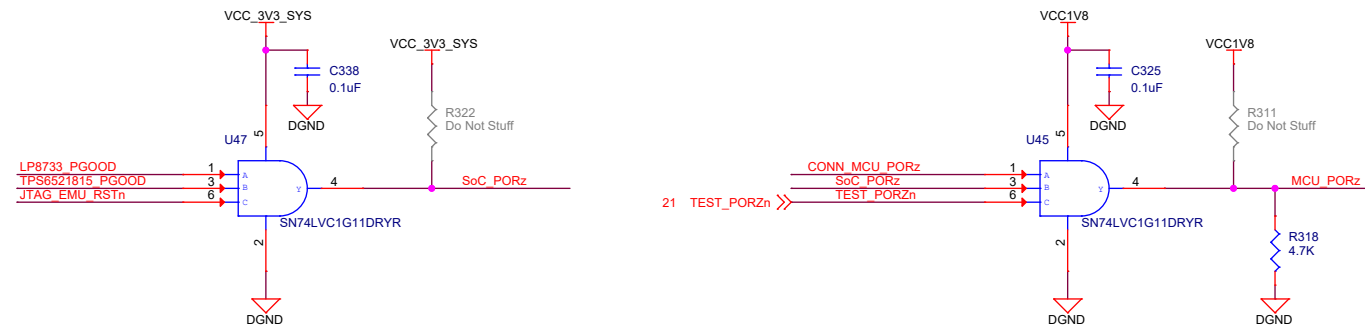
Size PROC100 001 SKAM64

C Rev E3

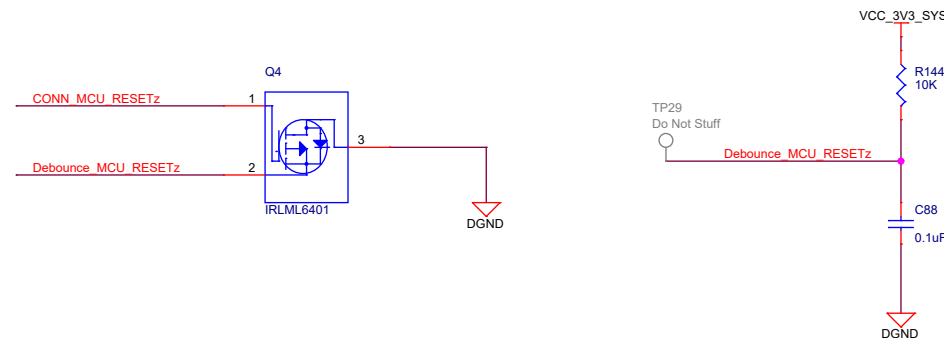
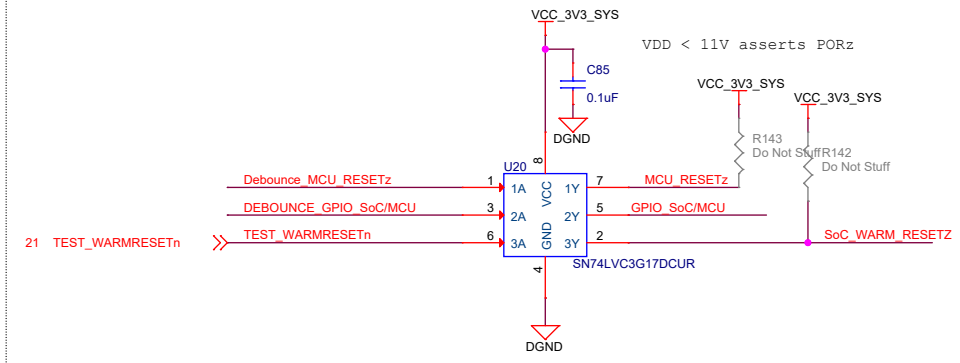
Date: Thursday, July 01, 2021

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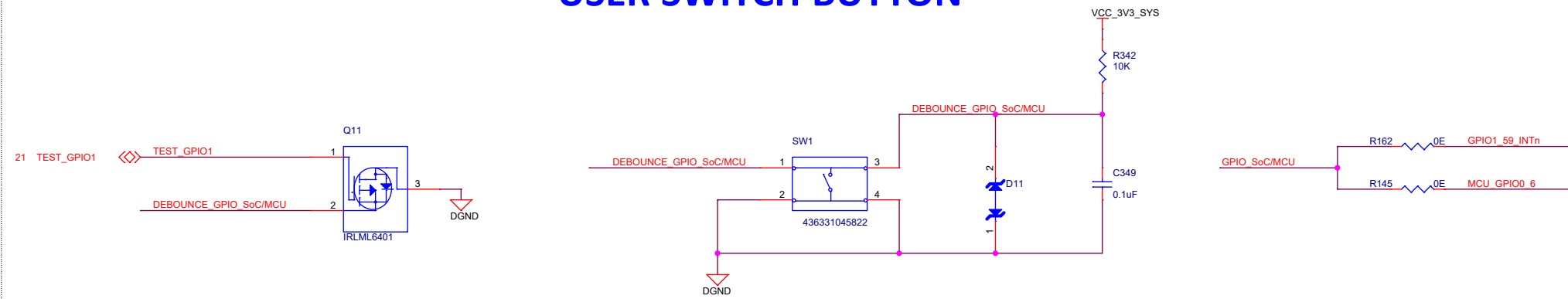
## POR



## DEBOUNCE CIRCUIT



## USER SWITCH BUTTON



### OFF PAGE CONNECTIONS

33	SoC_WARM_RESEZt	SoC_WARM_RESEZt
33	MCU_RESEZt	MCU_RESEZt
41	LP8733_PG00D	LP8733_PG00D
42	TPS6521815_PG00D	TPS6521815_PG00D
25	JTAG_EMU_RSTn	JTAG_EMU_RSTn
29	CONN_MCU_RESEZt	CONN_MCU_RESEZt
33	MCU_PORz	MCU_PORz
29,33	MCU_GPIO_6	MCU_GPIO_6
33	GPIO1_59_INTn	GPIO1_59_INTn
29	CONN_MCU_PORz	CONN_MCU_PORz

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Title: RESET CIRCUIT

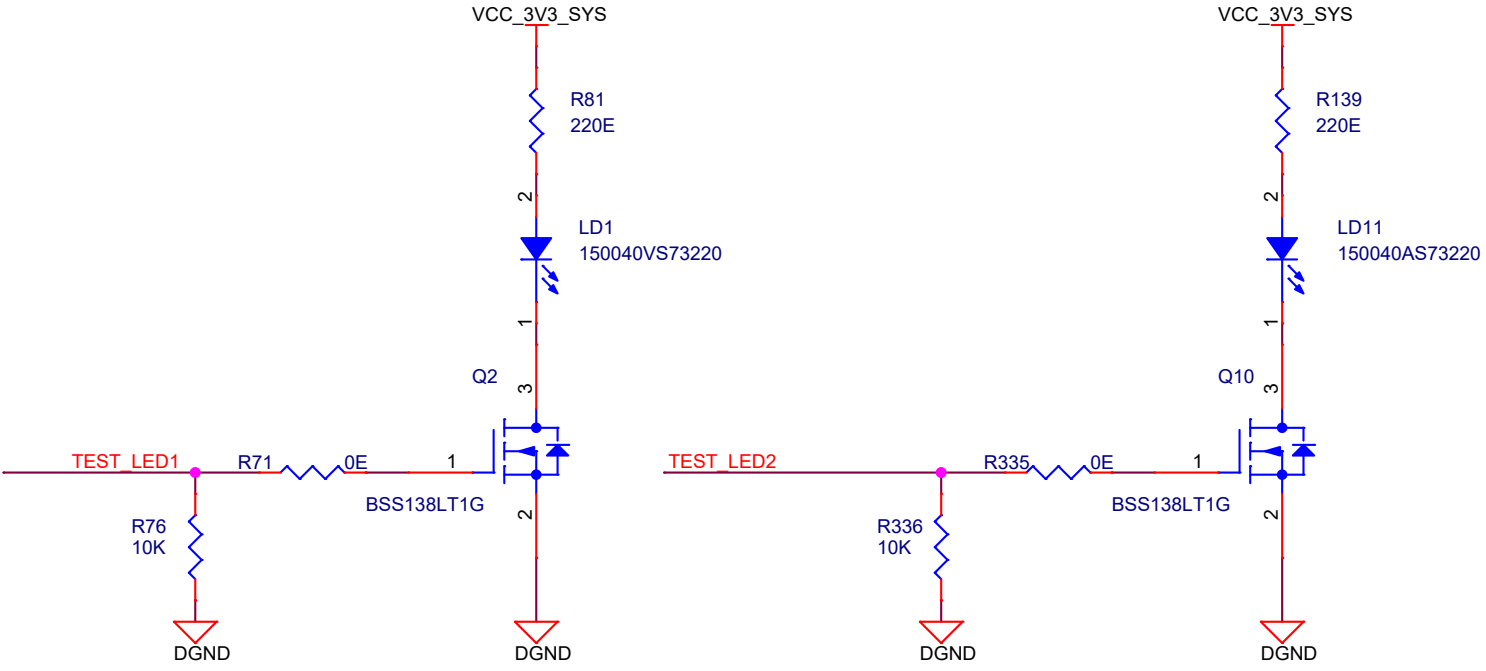
Size: PROC100 001 SKAM64

Date: Thursday, July 01, 2021

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# USER TEST LED's



## OFF PAGE CONNECTIONS

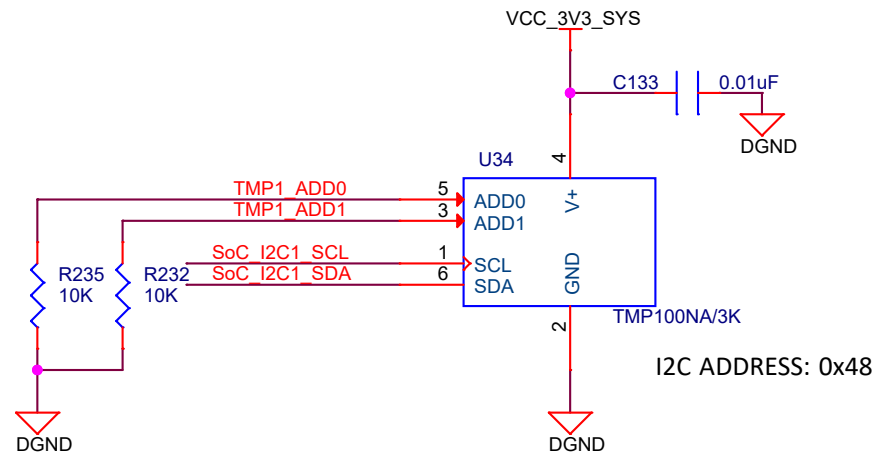


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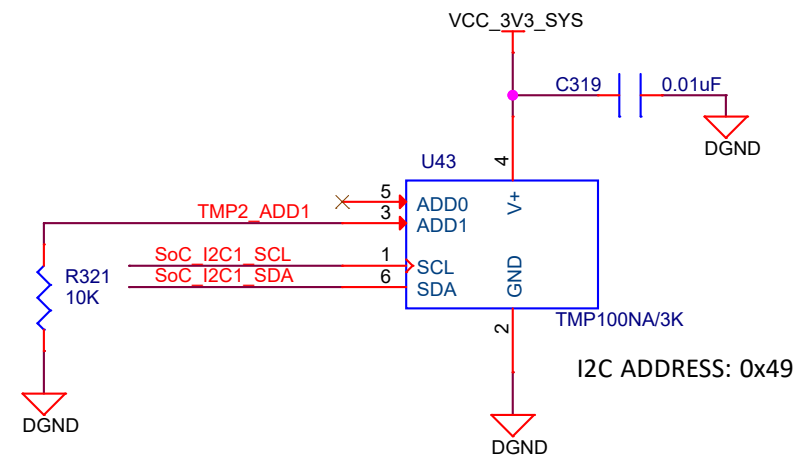


Title		USER TEST LED's	
Size	PROC100 001 SKAM64		Rev
B			E3
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# TEMPERATURE SENSORS



NOTE: PLACE TEMP SENSOR CLOSE TO SoC



NOTE: PLACE TEMP SENSOR CLOSE TO LPDDR4



## OFF PAGE CONNECTIONS



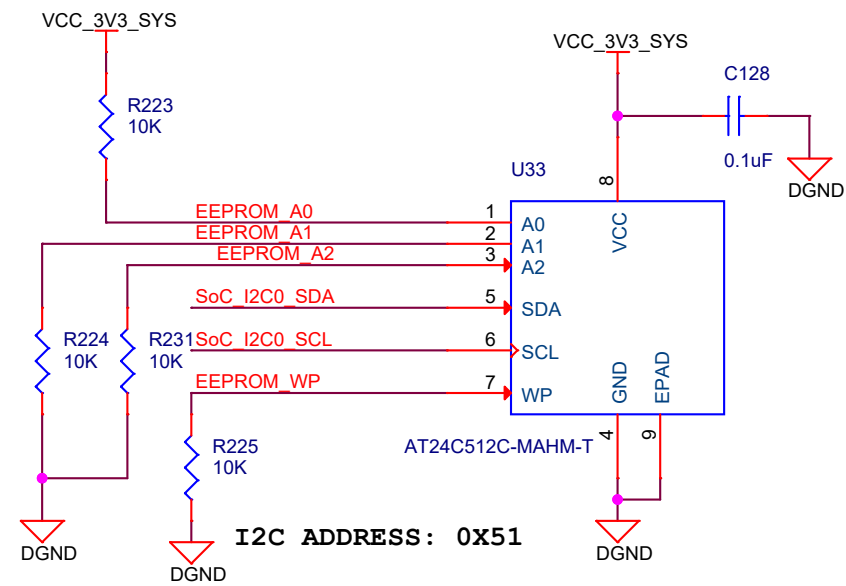
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Title TEMPERATURE SENSORS

Size	PROC100 001 SKAM64	Rev	E3
Date:	Thursday, July 01, 2021	Sheet	36 of 45

# BOARD ID EEPROM



## OFF PAGE CONNECTIONS



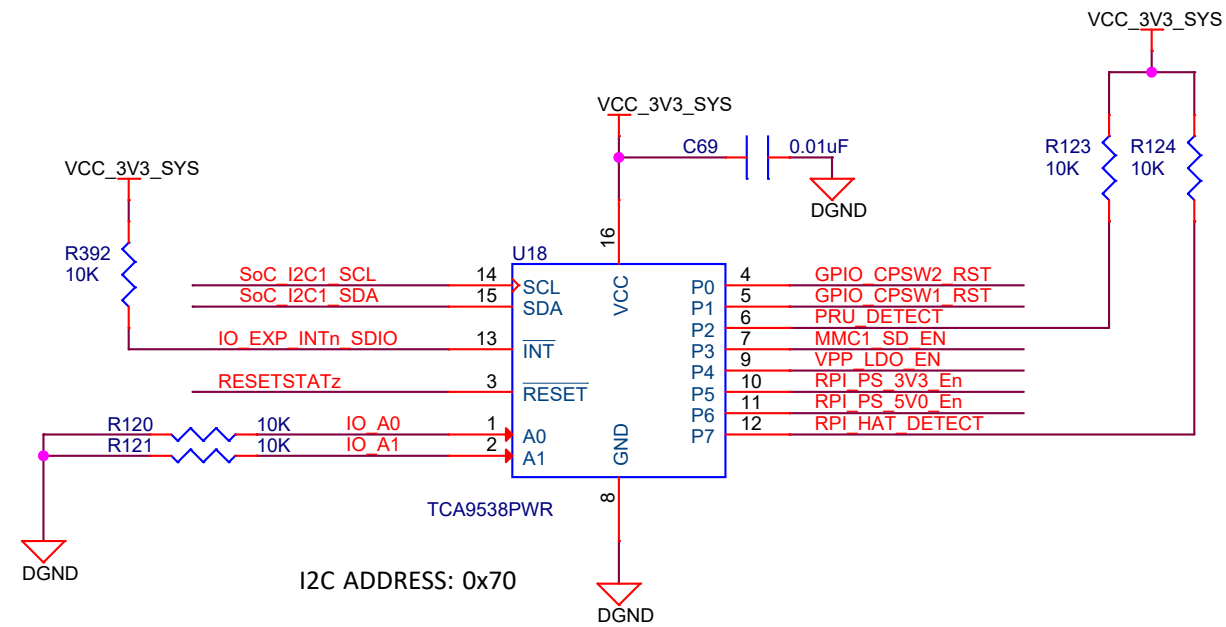
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Title BOARD ID EEPROM

Size	PROC100 001 SKAM64	Rev	E3
Date:	Thursday, July 01, 2021	Sheet	37 of 45

# IO EXPANDER



I2C ADDRESS: 0x70

## OFF PAGE CONNECTIONS

RPI_PS_3V3_En	RPI_PS_3V3_En	28
RPI_PS_5V0_En	RPI_PS_5V0_En	28
GPIO_CPSW2_RST	GPIO_CPSW2_RST	20
GPIO_CPSW1_RST	GPIO_CPSW1_RST	19
MMC1_SD_EN	MMC1_SD_EN	18
VPP_LDO_EN	VPP_LDO_EN	43
RESETSTATz	RESETSTATz	17,18,19,20,22,27,33
IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO	16
SoC_I2C1_SCL	SoC_I2C1_SCL	21,32,33,36
SoC_I2C1_SDA	SoC_I2C1_SDA	21,32,33,36
RPI_HAT_DETECT	RPI_HAT_DETECT	28
PRU_DETECT	PRU_DETECT	27

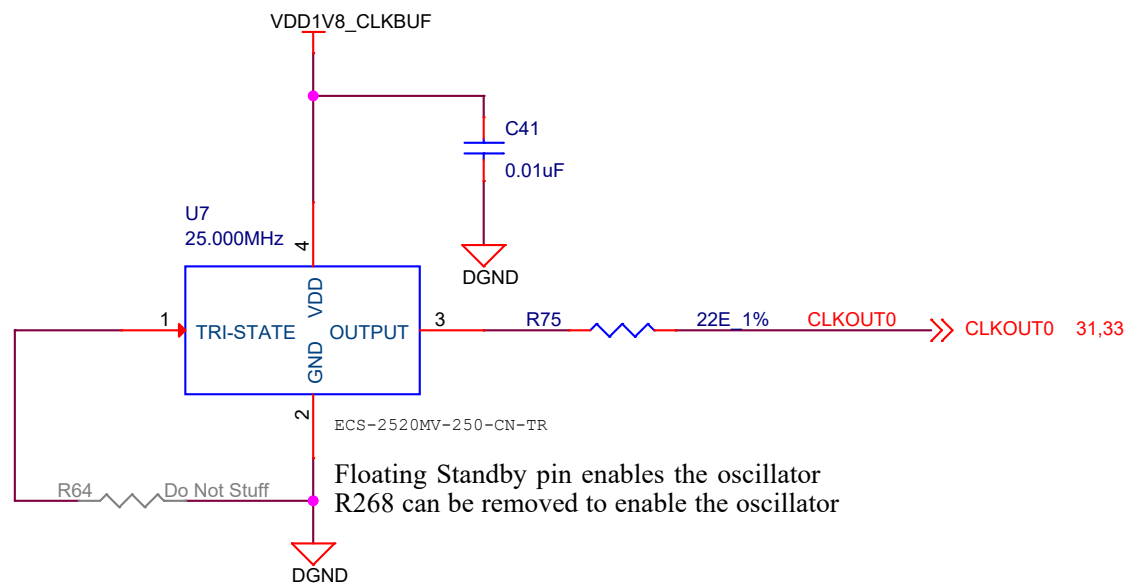
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Title IO EXPANDER

Size	PROC100 001 SKAM64	Rev	E3
Date:	Thursday, July 01, 2021	Sheet	38 of 45

# OSCILLATOR



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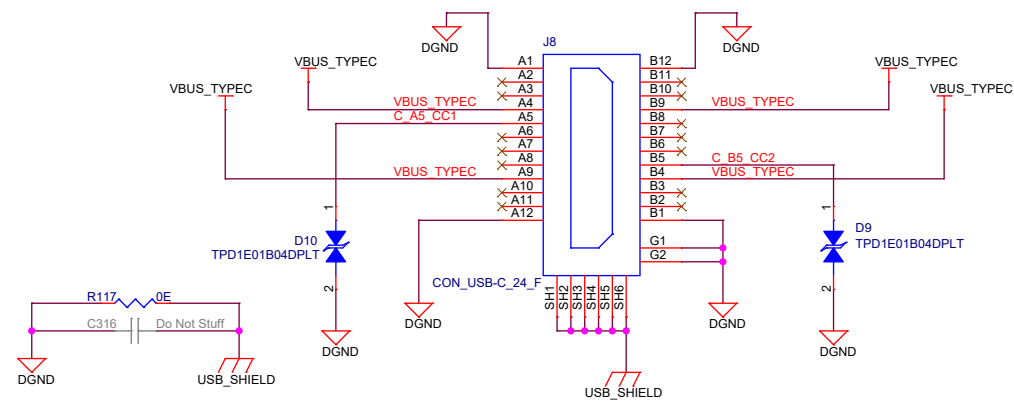


Title OSCILLATOR

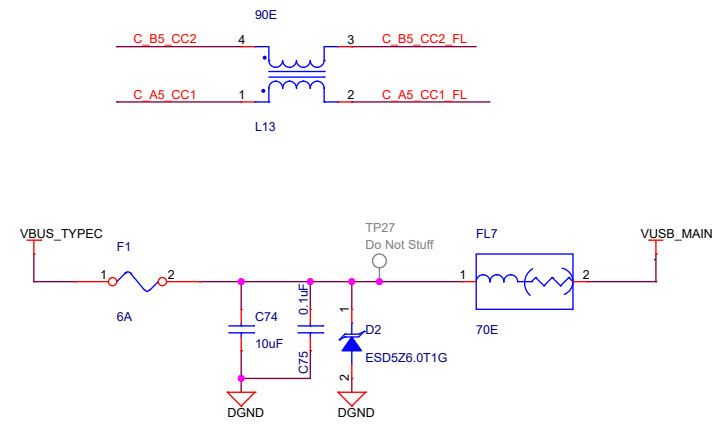
Size	PROC100 001 SKAM64	Rev	E3
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## TYPE-C CONNECTOR

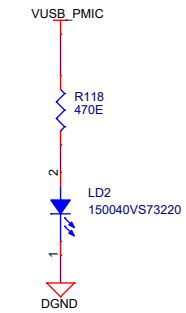
IF SPACE IS CONSTRAINT USE  
MOLEX PART: 2012670005



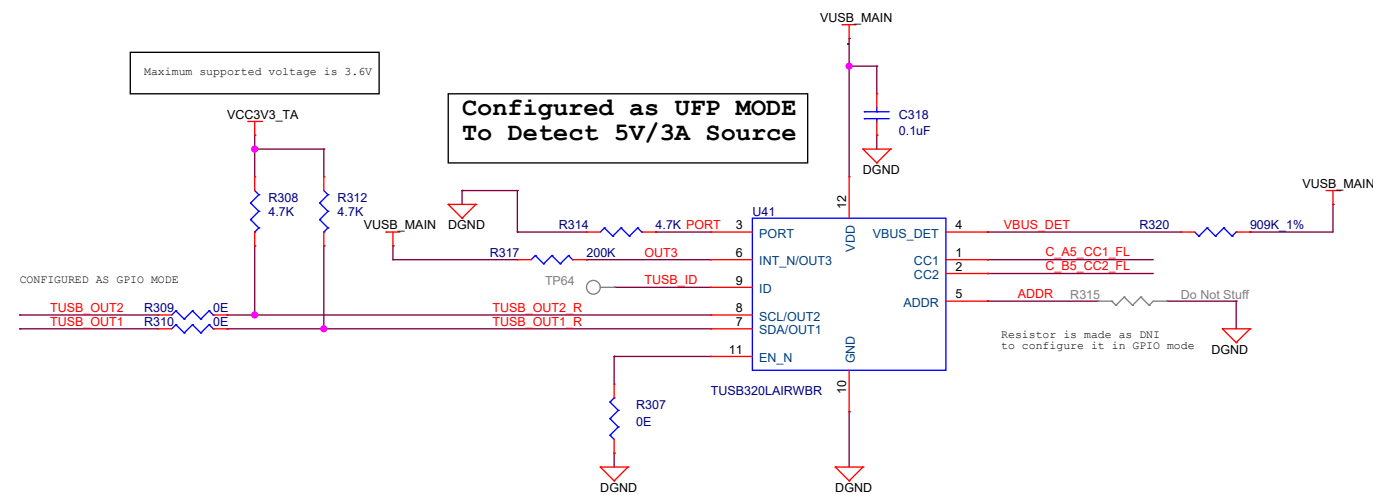
## USB MAIN INPUT 5V DC



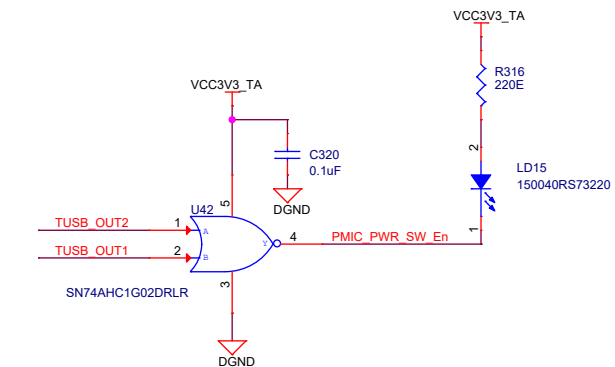
## POWER INDICATION LED: USB VBUS



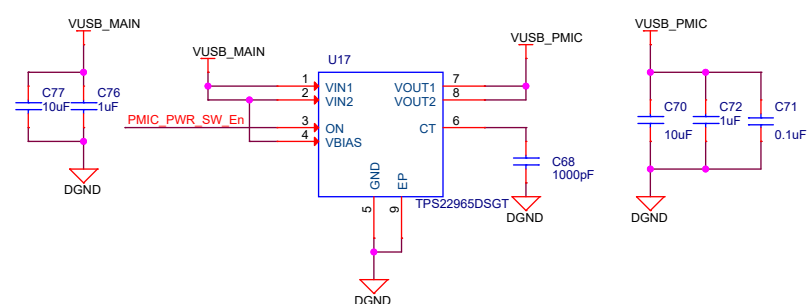
## USB TYPE C CONFIGURATION CHANNEL LOGIC AND PORT CONTROLLER



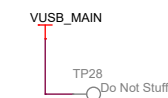
## Enable Logic for Power Switch



## POWER SWITCH ON USB VBUS MAIN SUPPLY



## TEST POINT



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Title USB MAIN 5V POWER SUPPLY

Size PROC100 001 SKAM64

Date: Thursday, July 01, 2021

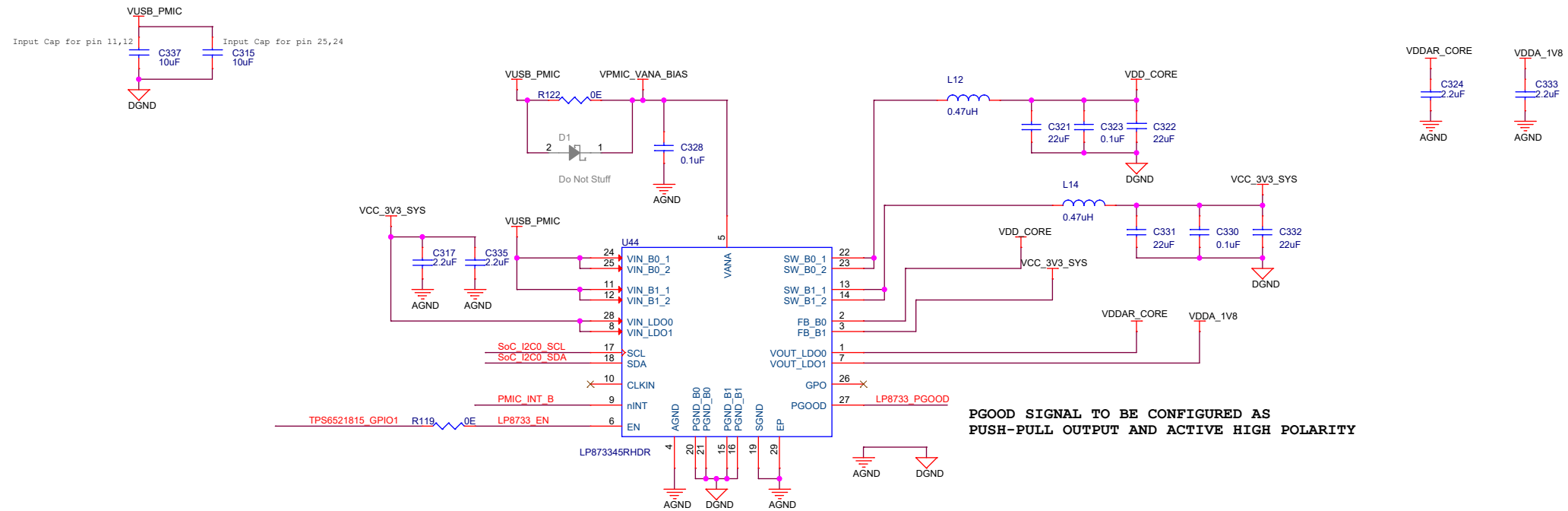
Rev E3

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# PMIC-1 POWER SUPPLY

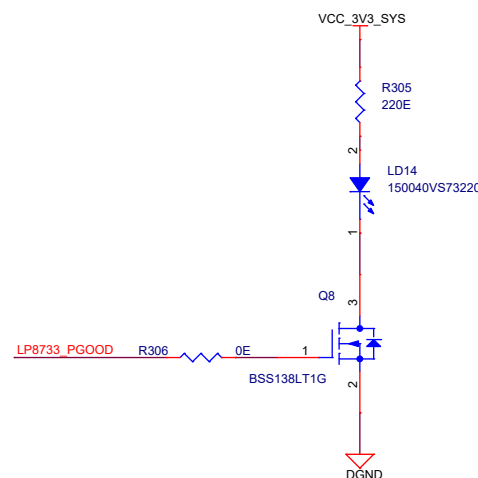
**NOTE:**  
**This power solution should not be used for a production system.**



**NOTE:** The Voltage for the following AM64x power supplies should be 0.85V typical (0.81V minimum, 0.895V maximum)  
 1. "VDDR\_CORE"  
 2. "VDDA\_CORE, VDD\_MMC0, VDD\_DLL\_MMC0, VDDAR\_0P85\_SERDES0, VDDAR\_0P85\_SERDES0\_C, VDDAR\_0P85\_USB0"

But VOUT\_LDO0 (VDDAR\_CORE) of LP873345 is programmed to 0.9V

# POWER INDICATION LED



## OFF PAGE CONNECTIONS

28.33.37.42	SoC_I2C0_SCL	SoC_I2C0_SCL
28.33.37.42	SoC_I2C0_SDA	SoC_I2C0_SDA
34	LP8733_PGOOD	LP8733_PGOOD
27.42	PMIC_INT_B	PMIC_INT_B
42	TPS6521815_GPIO1	TPS6521815_GPIO1

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Title: PMIC-1 POWER SUPPLY

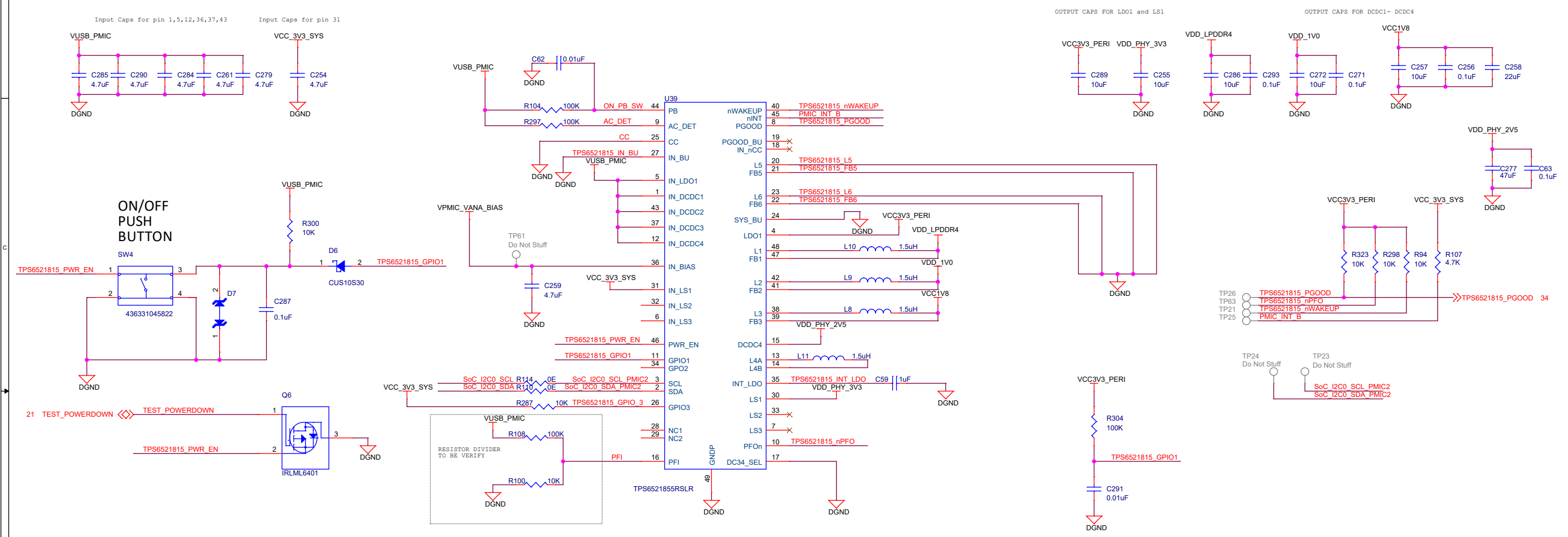
Size: PROC100 001 SKAM64

Date: Thursday, July 01, 2021

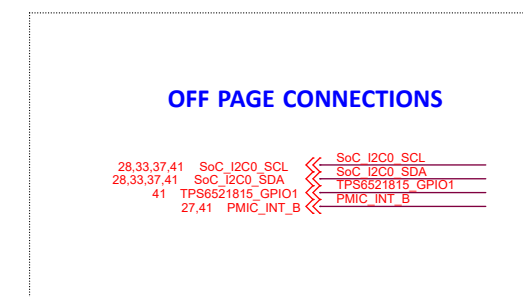
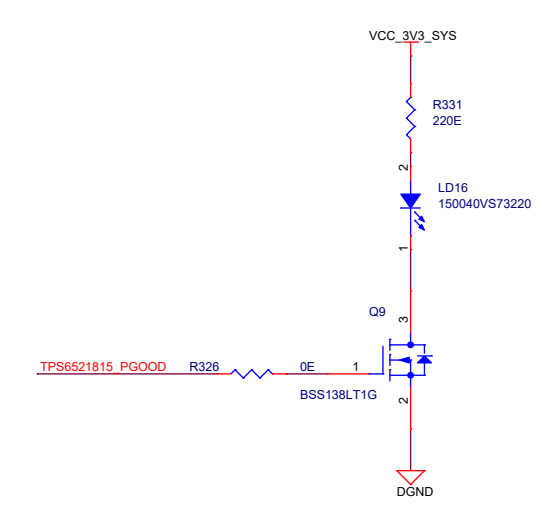
Rev: E3

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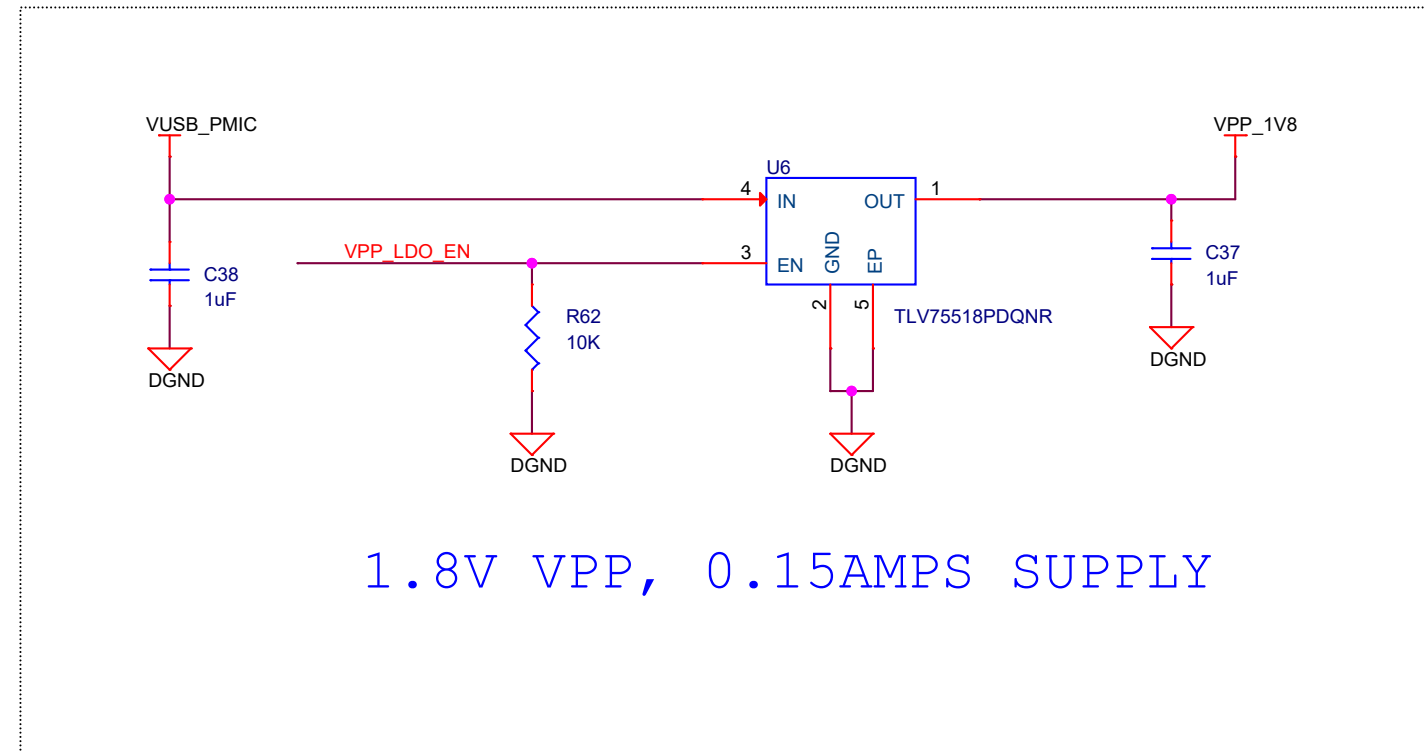
# PMIC-2 POWER SUPPLY



# POWER INDICATION LED



# eFUSE PROGRAMMING VOLTAGE TO SoC



## OFF PAGE CONNECTIONS

38 VPP\_LDO\_EN ← VPP\_LDO\_EN

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Title eFUSE PROGRAMMING PWR SOC

Size	PROC100 001 SKAM64	Rev	E3
Date:	Thursday, July 01, 2021	Sheet	43 of 45

## STRAP CONFIGURATION OF ETHERNET PHYS

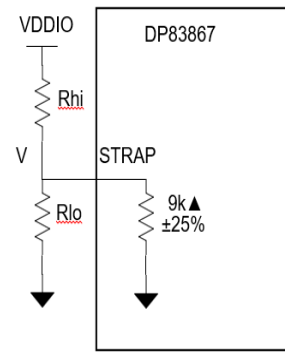


Figure 25. Strap Circuit

MODE	TARGET VOLTAGE			IDEAL R <sub>hi</sub> (kΩ)	IDEAL R <sub>lo</sub> (kΩ)
	V <sub>min</sub> (V)	V <sub>typ</sub> (V)	V <sub>max</sub> (V)		
1	0	0	0.098 × VDDIO	OPEN	OPEN
2	0.140 × VDDIO	0.165 × VDDIO	0.191 × VDDIO	10	2.49
3	0.225 × VDDIO	0.255 × VDDIO	0.284 × VDDIO	5.76	2.49
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

### Level Strap Resistor Ratios

PIN NAME	64 HTQFP PIN #	48 QFN PIN #	DEFAULT	STRAP FUNCTION		
				MODE	PHY_ADD1	PHY_ADD0
RX_D0	44	33	[00]	MODE	PHY_ADD1	PHY_ADD0
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D2	46	35	[00]	MODE	PHY_ADD3	PHY_ADD2
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D4	48		[00]	MODE	ANEG_SEL1	PHY_ADD4
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D5	49		[00]	MODE	Force MDI/X	Half-Duplex Enable (FD/HD)
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D6	50		[00]	MODE	RGMII Disable	AMDIX Disable
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D7	51		[00]	MODE	Speed Optimization Enable	Clock Out Disable
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_DV/RX_CTRL <sup>(1)</sup> (Straps Required)	53	38	[0]	MODE		Autoneg Disable
				1		N/A
				2		N/A
				3		0
				4		1
CRS <sup>(2)</sup>	56		[0]	MODE		Fast Link Drop (FLD)
				1		0
				2		1
				3		N/A

### Level Strap Pins

PIN NAME	64 HTQFP PIN #	48 QFN PIN #	DEFAULT	STRAP FUNCTION		
				MODE	RGMII Clock Skew TX[1]	RGMII Clock Skew TX[0]
LED_2 <sup>(3)</sup>		45	[00]	MODE	RGMII Clock Skew TX[1]	RGMII Clock Skew TX[0]
				1	0	0
				2	0	1
				3	1	0
				4	1	1
LED_1 (RGZ)		46	[00]	MODE	ANEG_SEL	RGMII Clock Skew TX[2]
				1	0	0
				2	0	1
				3	1	0
				4	1	1
LED_1 (PAP)	62		[0]	MODE	ANEG_SELO	
				1	0	
				2	0	
				3	1	
				4	1	
LED_0 <sup>(4)</sup>	63	47	[0]	MODE	Mirror Enable	
				1	0	
				2	N/A	
				3	1	
				4	N/A	
GPIO_0 <sup>(3)</sup>		39	[00]	MODE	RGMII Clock Skew RX[0]	
				1	0	
				2	Not Applicable	
				3	1	
				4	Not Applicable	
GPIO_1		40	[00]	MODE	RGMII Clock Skew RX[2]	RGMII Clock Skew RX[1]
				1	0	0
				2	0	1
				3	1	0
				4	1	1

### Level Strap Pins

MODE	ANEG_SEL	REMARKS
10/100/1000	0	advertise ability of 10/100/1000
100/1000	1	advertise ability of 100/1000 only

MODE	RGMII CLOCK SKEW TX[2]	RGMII CLOCK SKEW TX[1]	RGMII CLOCK SKEW TX[0]	RGMII TX CLOCK SKEW
1	0	0	0	2.0 ns
2	0	0	1	1.5 ns
3	0	1	0	1.0 ns
4	0	1	1	0.5 ns
5	1	0	0	0 ns
6	1	0	1	3.5 ns
7	1	1	0	3.0 ns
8	1	1	1	2.5 ns

MODE	RGMII CLOCK SKEW RX[2]	RGMII CLOCK SKEW RX[1]	RGMII CLOCK SKEW RX[0]	RGMII RX CLOCK SKEW
1	0	0	0	2.0 ns
2	0	0	1	1.5 ns
3	0	1	0	1.0 ns
4	0	1	1	0.5 ns
5	1	0	0	0 ns
6	1	0	1	3.5 ns
7	1	1	0	3.0 ns
8	1	1	1	2.5 ns

### RGMII Clock Skew Details

# HARDWARE SCHEMATICS

## ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

## BARE PCB



## JUMPERS



## LOGOs

PCB  
LOGO  
Do Not Stuff  
Texas Instruments

PCB  
LOGO  
Do Not Stuff  
For Evaluation only; not FCC approved for resale

PCB  
LOGO  
Do Not Stuff  
WEEE Mark

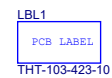
PCB  
LOGO  
Do Not Stuff  
CE Mark

## FIDUCIALS

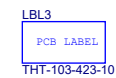


## LABELS

Board Serial No.



Assembly Revision



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Title HARDWARE SCHEMATICS

Size PROC100 001 SKAM64

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