AM625 / AM623 STARTER KIT (EVM)

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Revision Number

REV	A
VER	0.02

D-Note:-

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

R-Note:-

* Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of board design before board assembly.
* A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor.
* Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details)

KEY LINKS TO COLLATERALS

Hardware Design Guide : https://www.ti.com/lit/an/sprad05b/sprad05b.pdf
Schematic Design and Review Checklist : https://www.ti.com/lit/an/sprad21d/sprad21d.pdf
DDR Board Design and Layout Guidelines : https://www.ti.com/lit/an/sprad06/sprad06.pdf
EVM/SKs (Starter Kits) for reference : SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP

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REVISION HISTORY

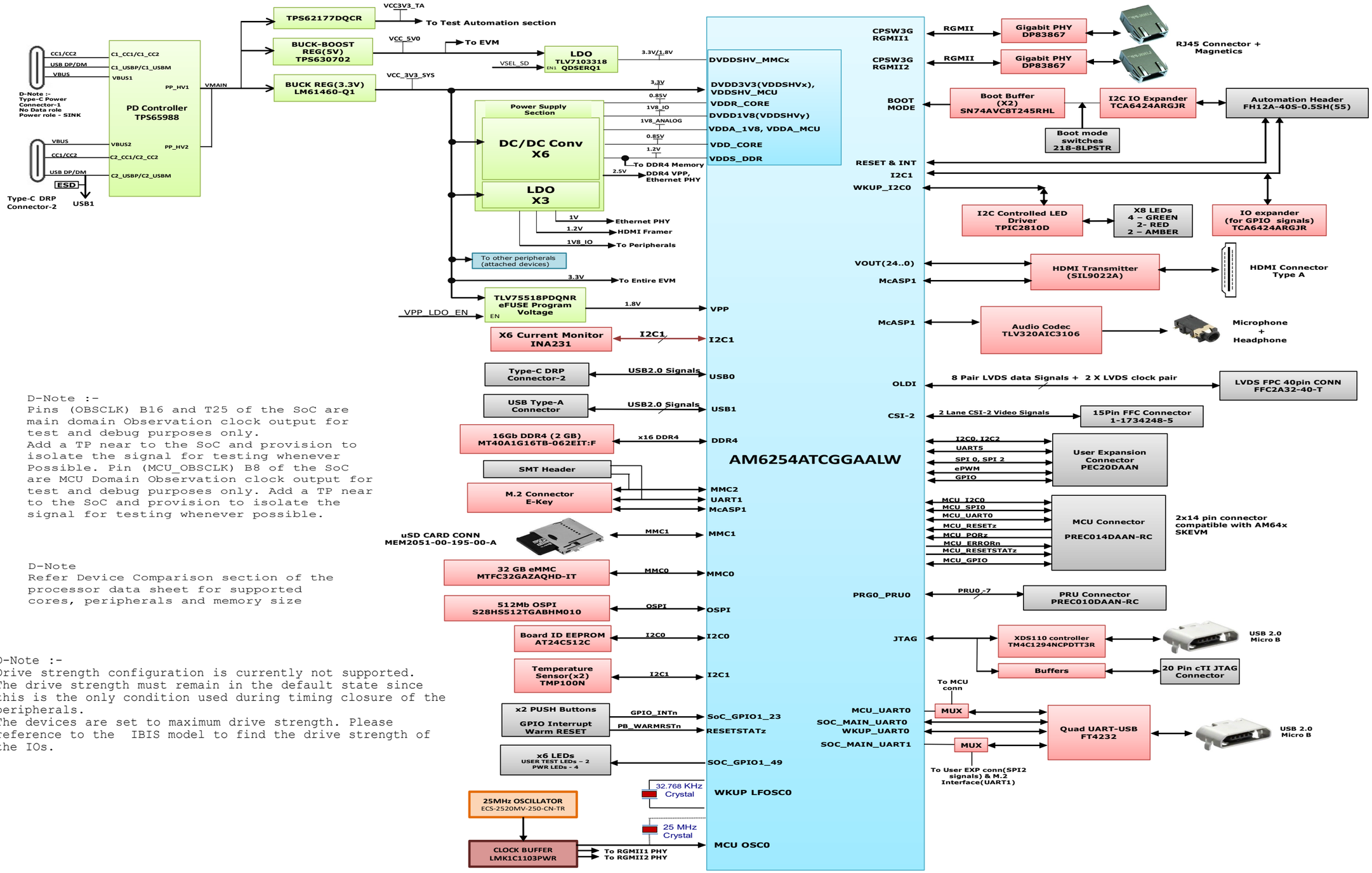
VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	11 APR 2023	Drafted from PROC114A Schematics. Changed the HDMI external swing resistance to 7.5K. Added Standoff,Screw & Washer for M.2 connector. DNI'd R650 on SoC_USB1_DRVVBUS	Mistral Design Team		
0.02	28 JUNE 2024	Updated SoC Part Number, Enabled Voltage ratings for all the capacitors and added Design Review notes Moved to DNI : U1,C5,C305,R303,Y4. Moved to Mount : R319,R309,R318,R310,R306,R307,R308,R303,R528,R572. C47 - 1uF changed to 0.1uF; C60 - 4.7uF changed to 1uF; C46 - 0.1uF changed to 4.7uF; C391,C193,C14 - 2.2uF changed to 1uF; C387,C194,C12 - 1uF changed to 0.1uF; C86 - 1uF changed to 2.2uF; C75,C79 - 9pF changed to 18pF. R56 - 0E changed to Std 22E; R408,R407 - 1K_0.1% changed to 1K_1%; R89, R354,R353,R301,R302 - 22E_1% changed to 0E; R393 - 10K_1% changed to Std 10K; R333,R12,R398 - 49.9K_1% changed to Std 10K; R152,R648 - 3.4K_1% changed to 3.48K_1%.	Mistral Design Team		

LINKS TO KEY FAQs

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1183910/faq-am625-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1184006/faq-am623-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-am62px-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1357533/faq-am625-am623-custom-board-hardware-design---design-and-review-notes-for-reuse-of-sk-am62b-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1280721/faq-am625-am623-am625sip-am625-q1-am620-q1-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit

BLOCK DIAGRAM AM62x SKEVM

Main Block Diagram



D-Note :-
Pins (OBSCLK) B16 and T25 of the SoC are main domain Observation clock output for test and debug purposes only.
Add a TP near to the SoC and provision to isolate the signal for testing whenever Possible. Pin (MCU_OBSCLK) B8 of the SoC are MCU Domain Observation clock output for test and debug purposes only. Add a TP near to the SoC and provision to isolate the signal for testing whenever possible.

D-Note
Refer Device Comparison section of the processor data sheet for supported cores, peripherals and memory size

D-Note :-
Drive strength configuration is currently not supported. The drive strength must remain in the default state since this is the only condition used during timing closure of the peripherals.
The devices are set to maximum drive strength. Please reference to the IBIS model to find the drive strength of the IOs.

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Title	BLOCK DIAGRAM AM62x SKEVM		
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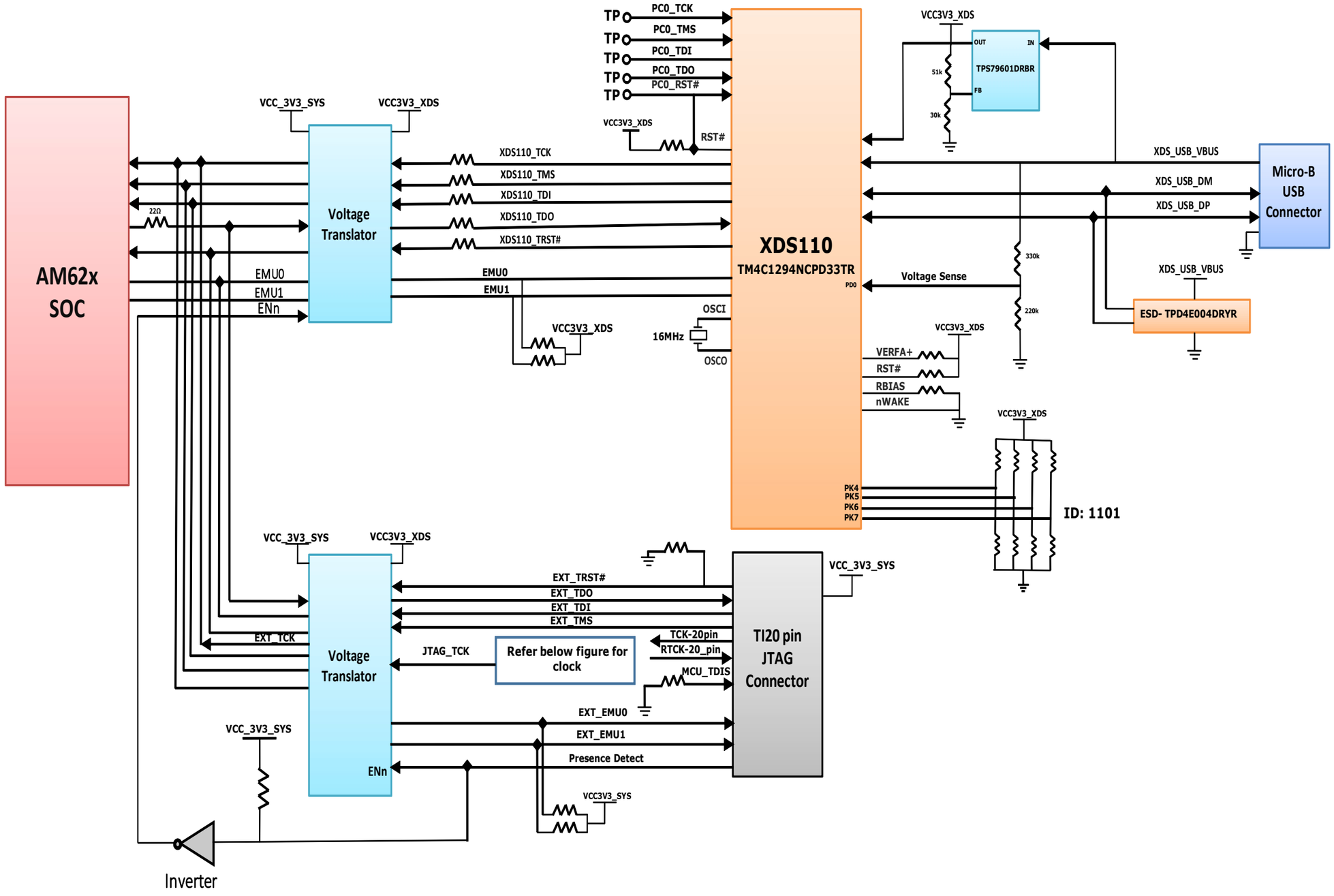
BLOCK DIAGRAM_XDS110



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Title	BLOCK DIAGRAM_XDS110	
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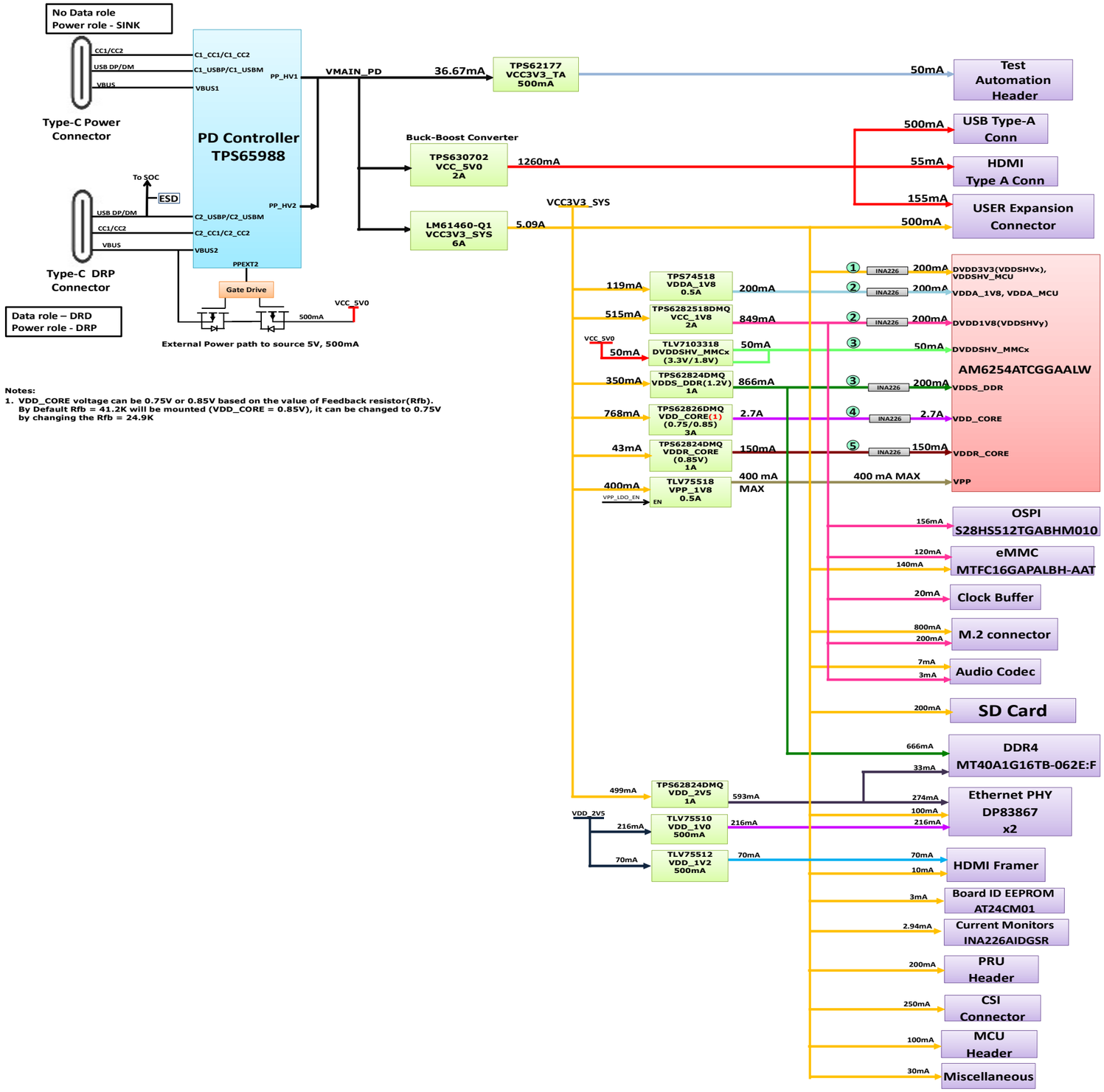
POWER ARCHITECTURE BLOCK DIAGRAM



Notes:

1. VDD_CORE voltage can be 0.75V or 0.85V based on the value of Feedback resistor(Rfb). By Default Rfb = 41.2K will be mounted (VDD_CORE = 0.85V), it can be changed to 0.75V by changing the Rfb = 24.9K

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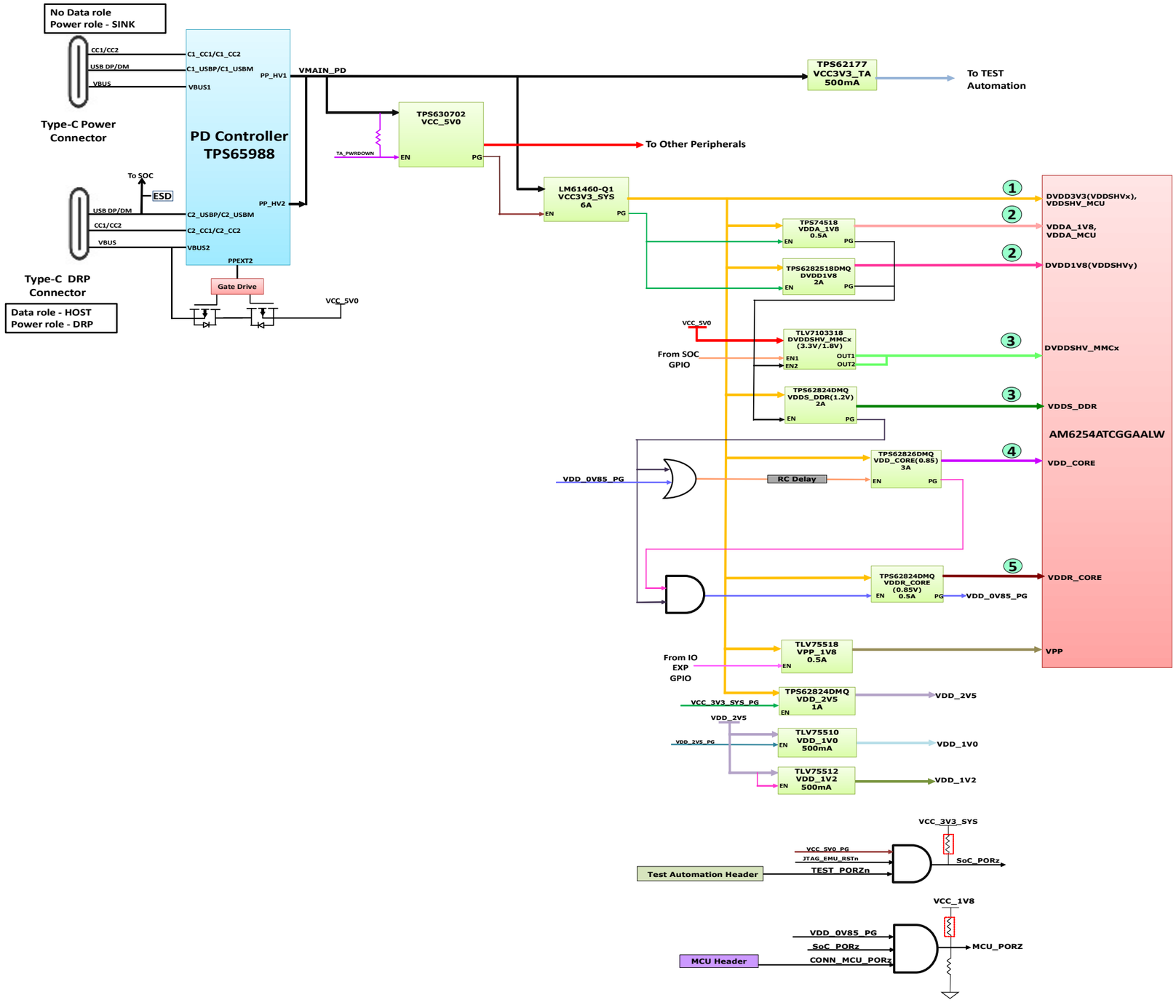
POWER SEQUENCE



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Title	POWER SEQUENCE		
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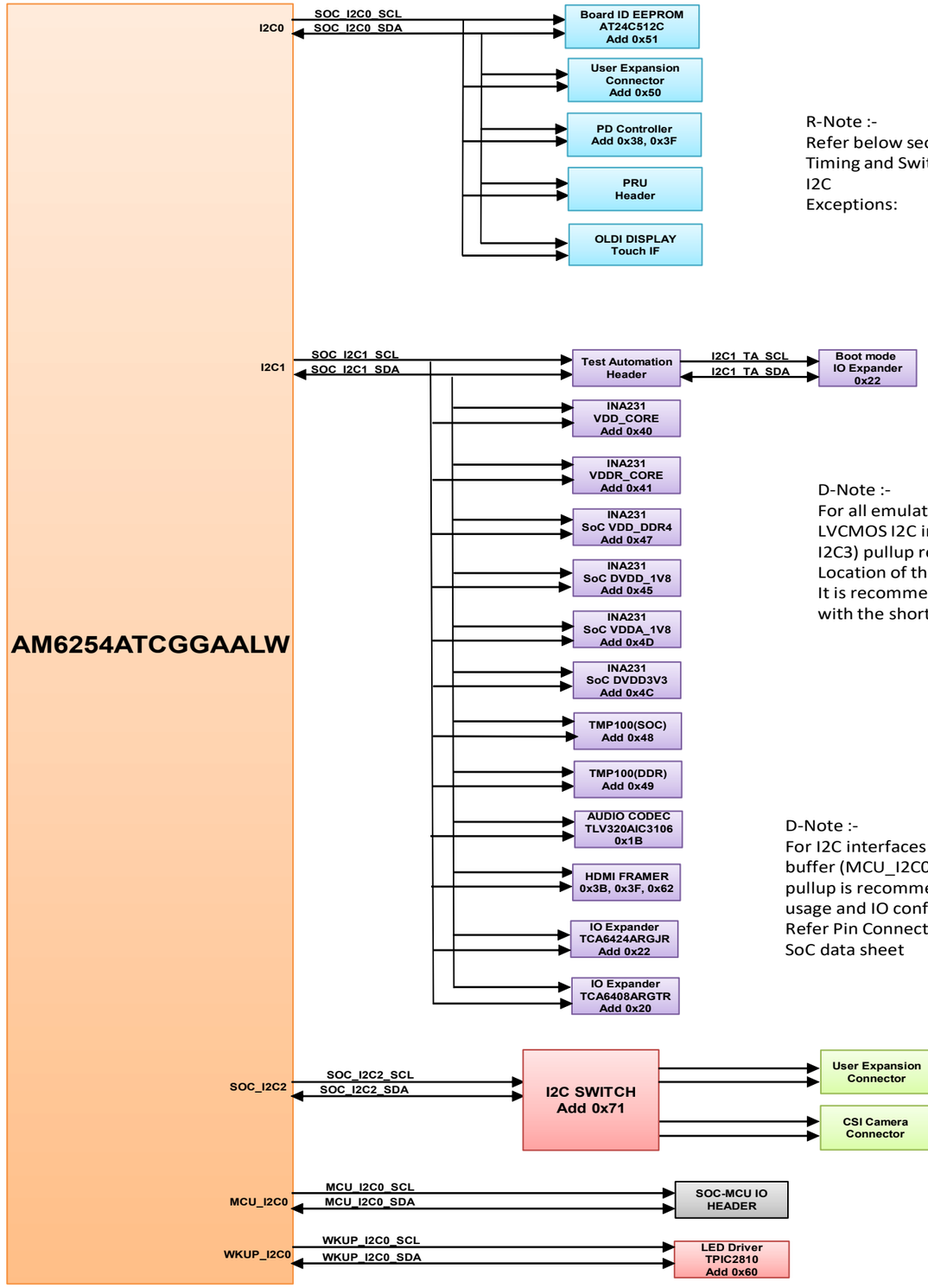
I2C TREE



R-Note :-
Add - Indicates Address

R-Note :-
Refer below section of the data sheet
Timing and Switching Characteristics
I2C
Exceptions:

D-Note :-
For all emulated open-drain output LVCMOS I2C interfaces. (I2C0, I2C1, I2C2, I2C3) pullup resistors are recommended
Location of the pullup is not a concern
It is recommended to connect the pullups with the shortest possible stub.

D-Note :-
For I2C interfaces with open-drain output type buffer (MCU_I2C0 and WKUP_I2C0), an external pullup is recommended irrespective of peripheral usage and IO configuration.
Refer Pin Connectivity Requirements section of SoC data sheet

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Title	I2C TREE	
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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	SoC_WLAN_EN_1V8	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	SoC_WLAN_IRQ_1V8	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC_3V3	ENABLE	MCU_GPIO0_1	MCU_SPI0_CS0	OUTPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt PRU Connector Interrupt PMIC_INTn	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
9	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER -P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	M.2 Connector Alert	WLAN_ALERT_3V3	ALERT	IO EXPANDER – P10		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	M.2 Connector WAKEUP	BT_UART_WAKE_SOC_3V3	WAKEUP	IO EXPANDER – P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	SOC UART1 Mux Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INT#	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 02										
1	M.2 Connector SDIO Reset Control GPIO	WLAN_SDIO_RST_3V3	RESET	IO EXPANDER – P0		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	OLDI Display Reset control	GPIO_TS_RSTn	RESET	IO EXPANDER – P1		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER – P2		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER – P3		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3

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TEXAS INSTRUMENTS MISTRAL

Title	GPIO MAPPING TABLE	
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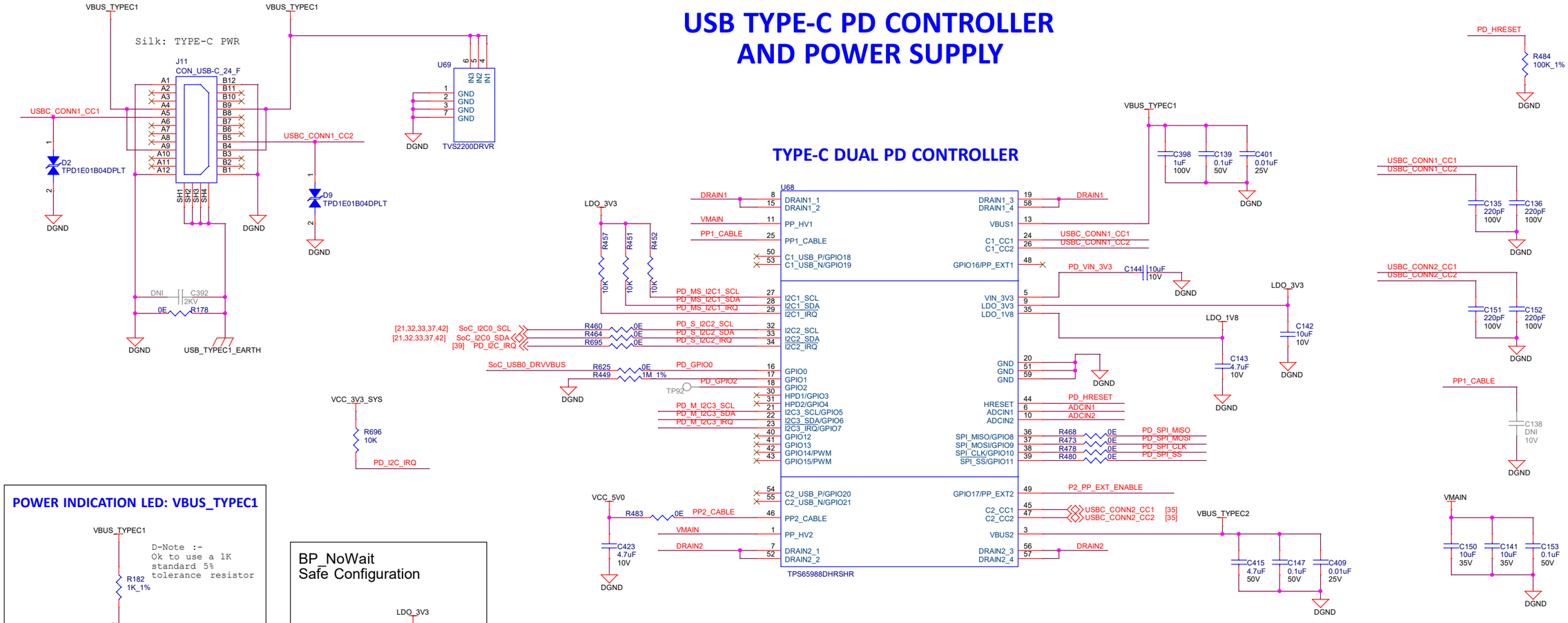
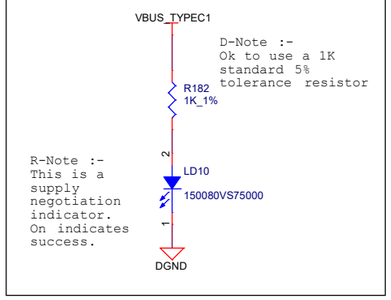
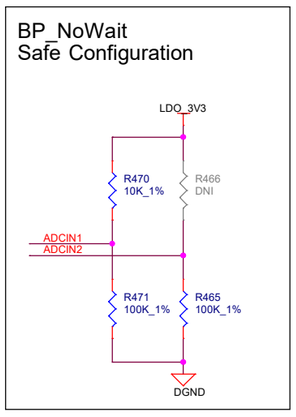
USB TYPE-C PD CONTROLLER AND POWER SUPPLY

TYPE-C DUAL PD CONTROLLER



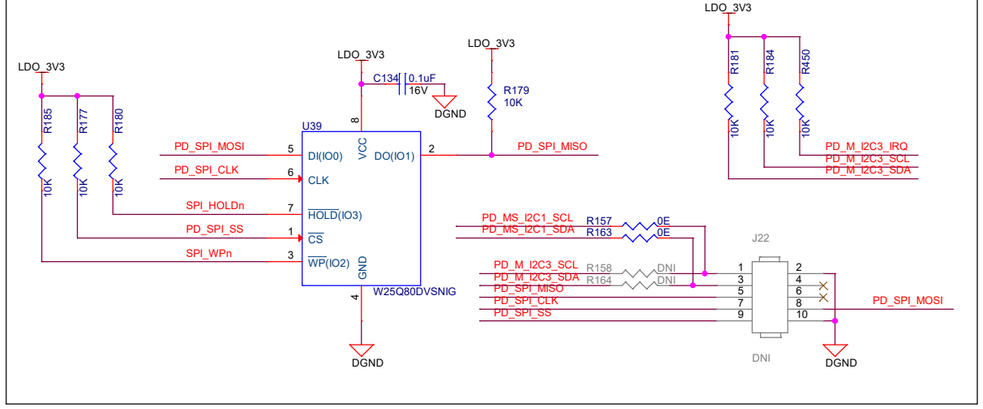
POWER INDICATION LED: VBUS_TYPEC1



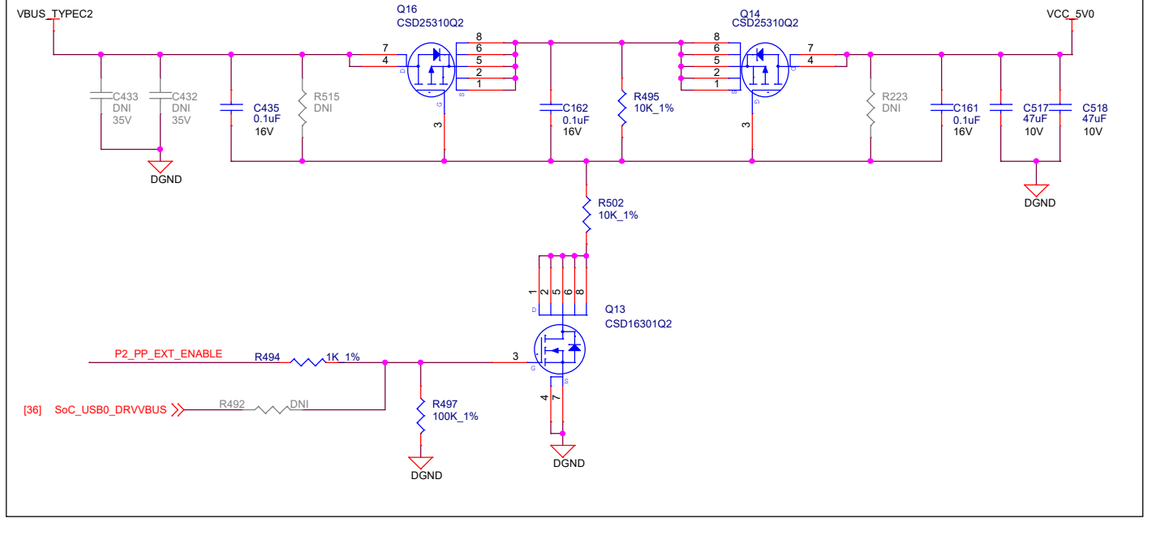


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

SPI EEPROM & PROGRAMMING HEADER



EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



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Title	USB TYPE-C POWER	
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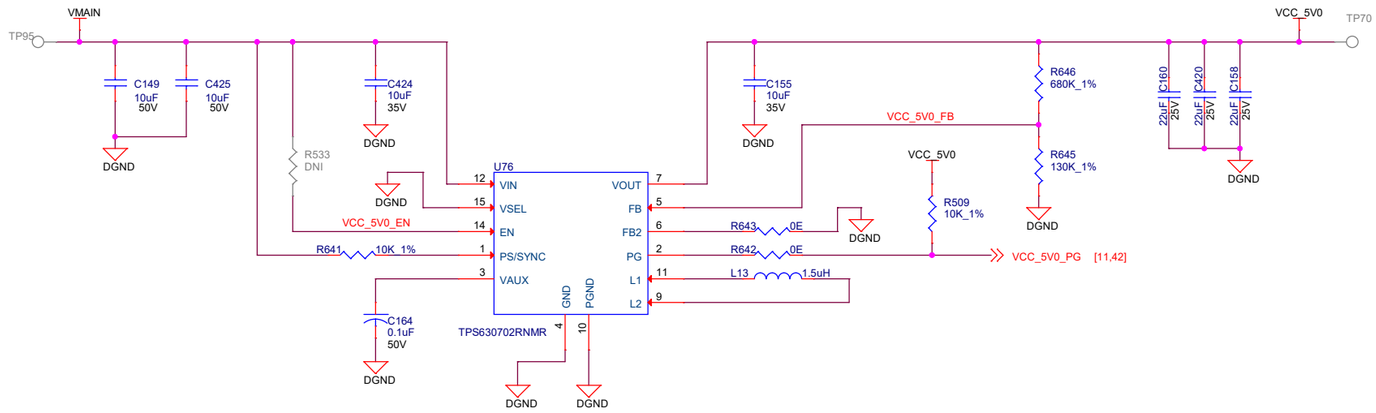
PERIPHERAL POWER SUPPLIES - 1



Power Cycle control from Test Automation

GROUND TEST POINTS

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Title	PERIPHERAL POWER SUPPLY -1	
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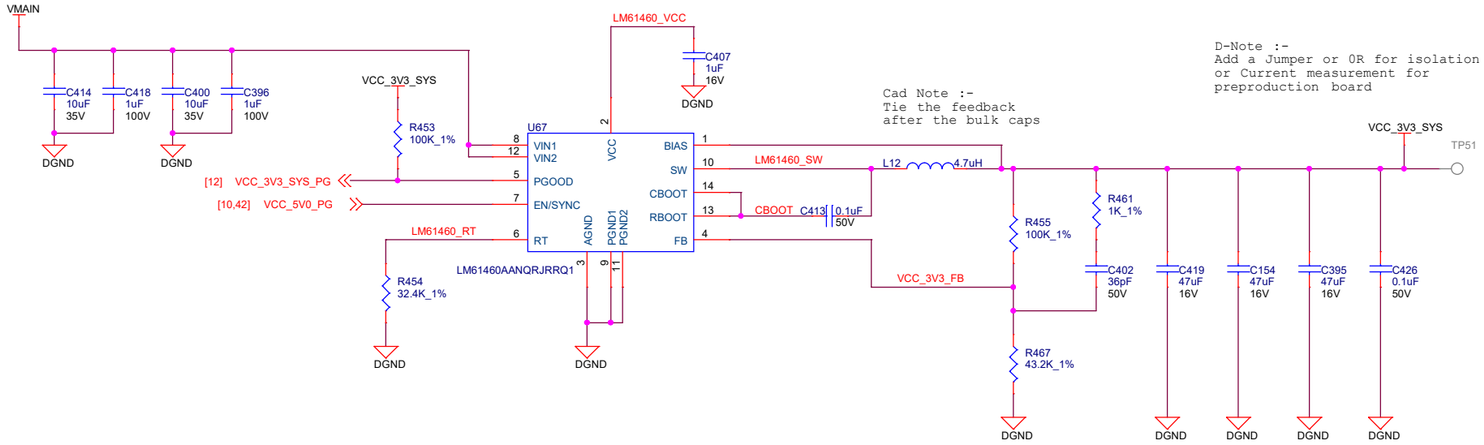
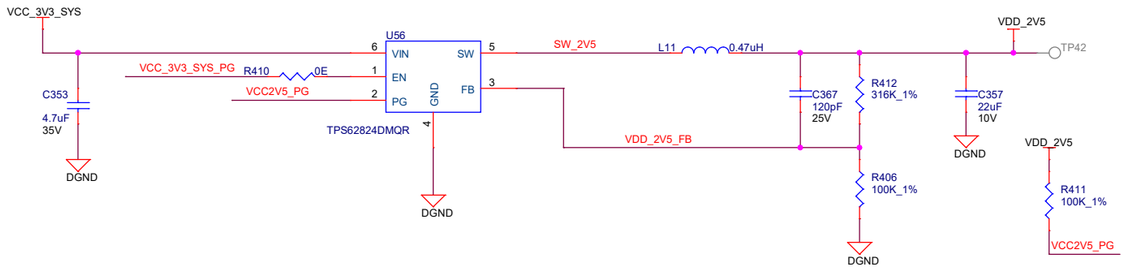
PERIPHERAL POWER SUPPLIES - 2

3.3V, 6.0 AMPS SUPPLY

VinMin = 4.5V
VinMax = 24V
Vout = 3.3V @ 6A

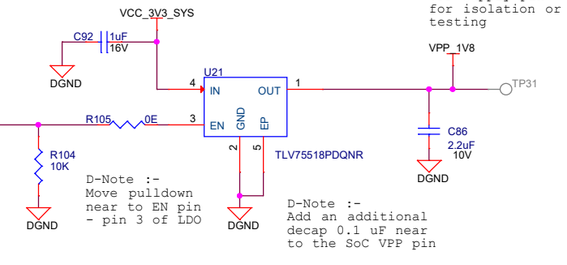


2.5V, 1.0 AMP SUPPLY



D-Note :-
It is very important to select an LDO with very fast transient response and connect its output to the VPP pin with a low loop inductance path to ensure it is able to source the high transient load, where the VPP pin never drops below the minimum operating voltage.

1.8V VPP, 0.5 AMP SUPPLY



D-Note :-
Alternate part suggestion
TPS7A21-Q1, Automotive, 500mA, low-noise ultra-low-IQ high-PSRR low-dropout (LDO) voltage regulator

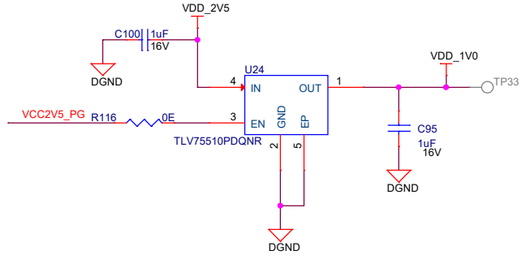
D-Note :-
Move pulldown near to EN pin - pin 3 of LDO

D-Note :-
Add an additional decap 0.1 uF near to the SoC VPP pin

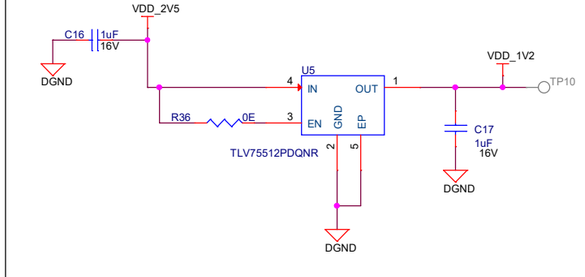
D-Note :-
Add a series resistor to the VPP supply pin for isolation or testing

PERIPHERAL SUPPLY - ETHERNET PHY

1.0V, 0.5 AMP



1.2V, 0.5 AMP SUPPLY



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Title	PERIPHERAL POWER SUPPLY-2	
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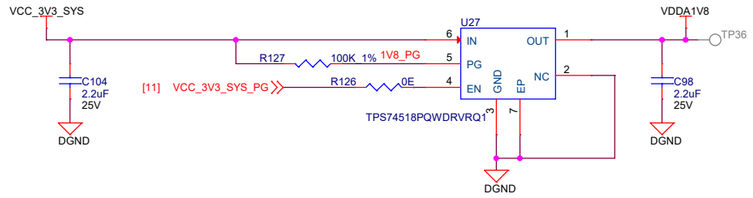
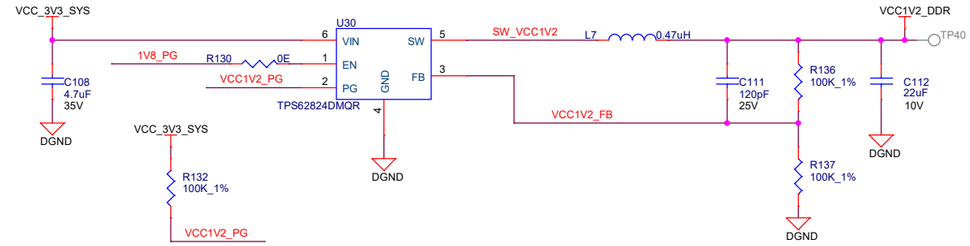
SOC POWER SUPPLIES

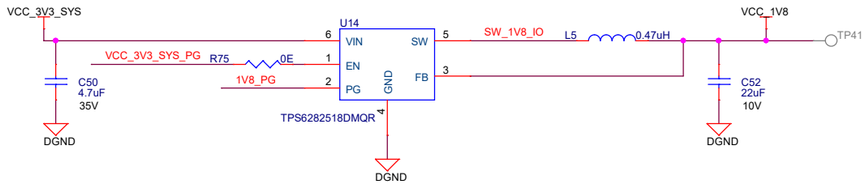
1.8V ANALOG, 0.5 AMPS SUPPLY



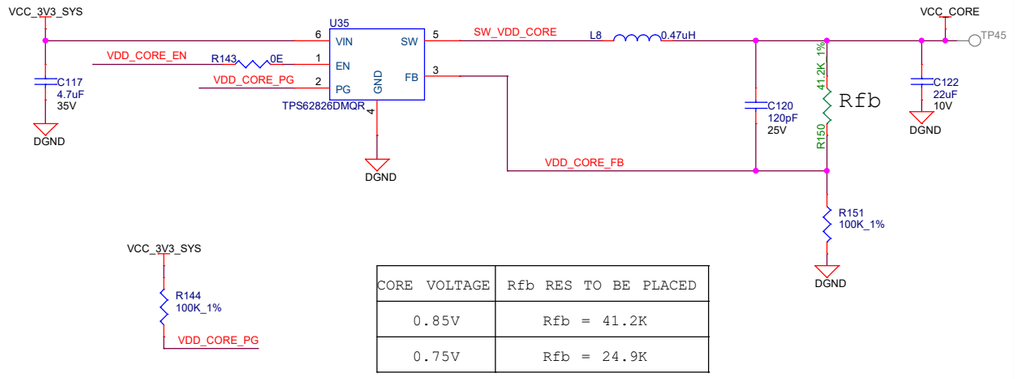
1.2V , 1.0 AMPS SUPPLY



1.8V IO, 2.0 AMPS SUPPLY



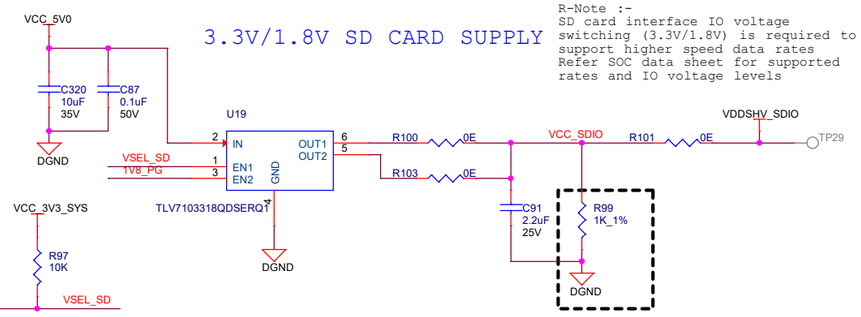
0.75V/0.85V , 3.0 AMPS SUPPLY



CORE VOLTAGE	Rfb RES TO BE PLACED
0.85V	Rfb = 41.2K
0.75V	Rfb = 24.9K

3.3V/1.8V SD CARD SUPPLY

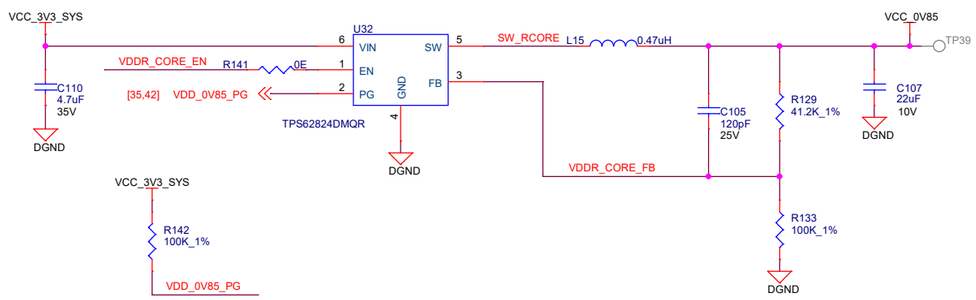
R-Note :-
SD card interface IO voltage switching (3.3V/1.8V) is required to support higher speed data rates
Refer SOC data sheet for supported rates and IO voltage levels

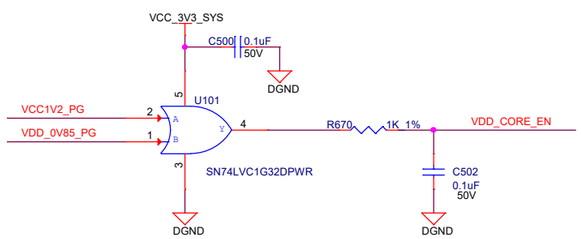


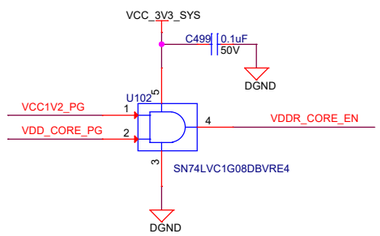
VSEL_SD	SD VOLTAGE
HIGH(DEFAULT)	3.3V
LOW	1.8V

Note: Resistor is to 'bleed' off voltage.

0.85V, 0.5 AMPS SUPPLY







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Title	SOC POWER SUPPLY	
Size: C	PROC114A1(001)	Rev: A1
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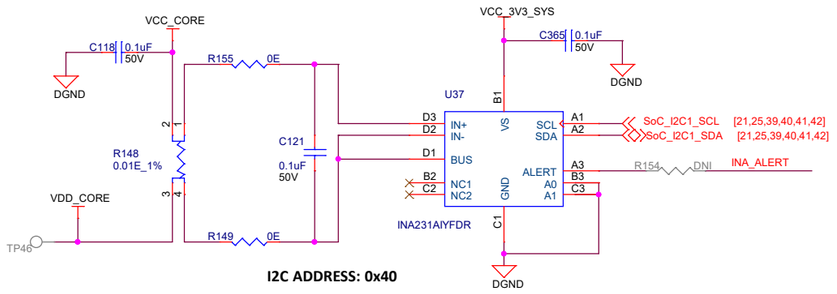
CURRENT MONITORING DEVICES

D-Note :-
Note the supply rail name change across the shunt when optimizing the design (Deleting the current sense)

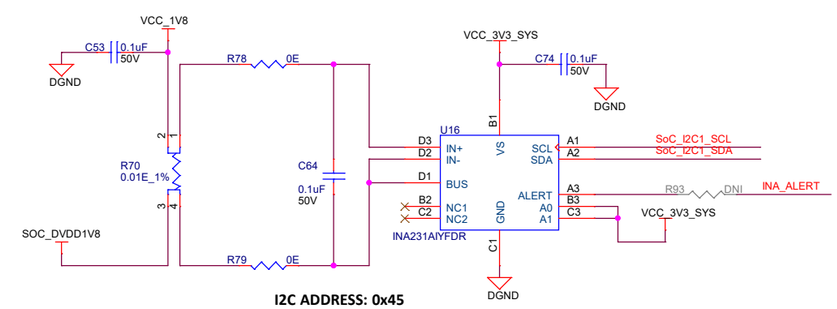
Cad Note :-
Follow Kelvin connection for Current Sensing when using 2 terminal resistors

VDD_CORE



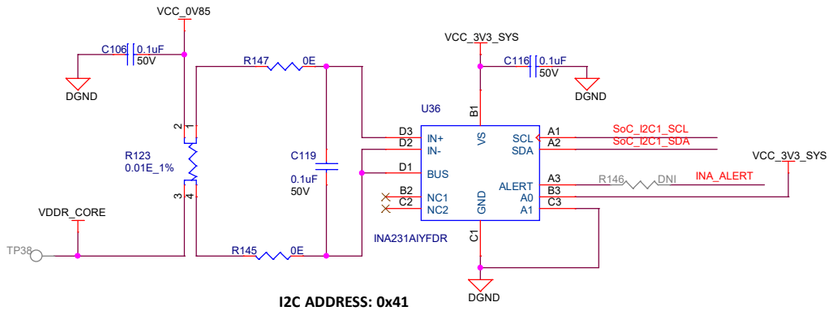
I2C ADDRESS: 0x40

SoC_DVDD1V8



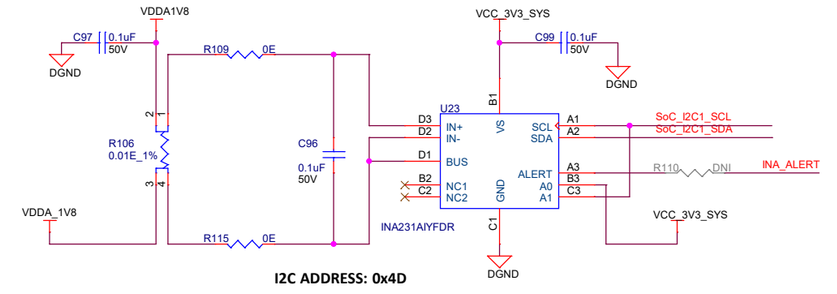
I2C ADDRESS: 0x45

VDDR_CORE



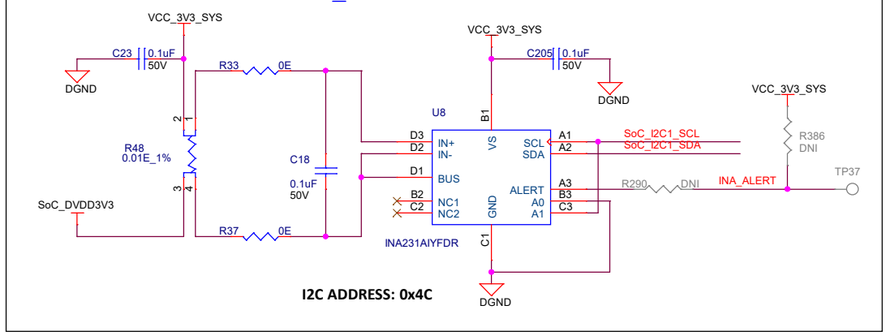
I2C ADDRESS: 0x41

VDDA_1V8



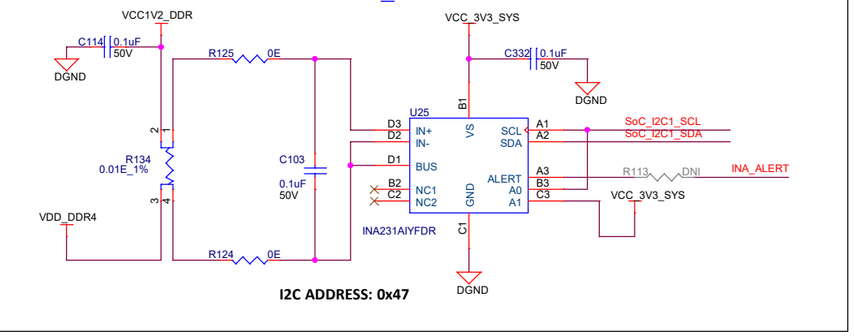
I2C ADDRESS: 0x4D

SoC_DVDD3V3



I2C ADDRESS: 0x4C

VDD_DDR4



I2C ADDRESS: 0x47

INA I2C SLAVE ADDRESS

POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V2_DDR	VDD_DDR4	47

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TEXAS INSTRUMENTS MISTRAL

Title	CURRENT MONITORING DEVICES	
Size C	PROC114A1(001)	Rev A1
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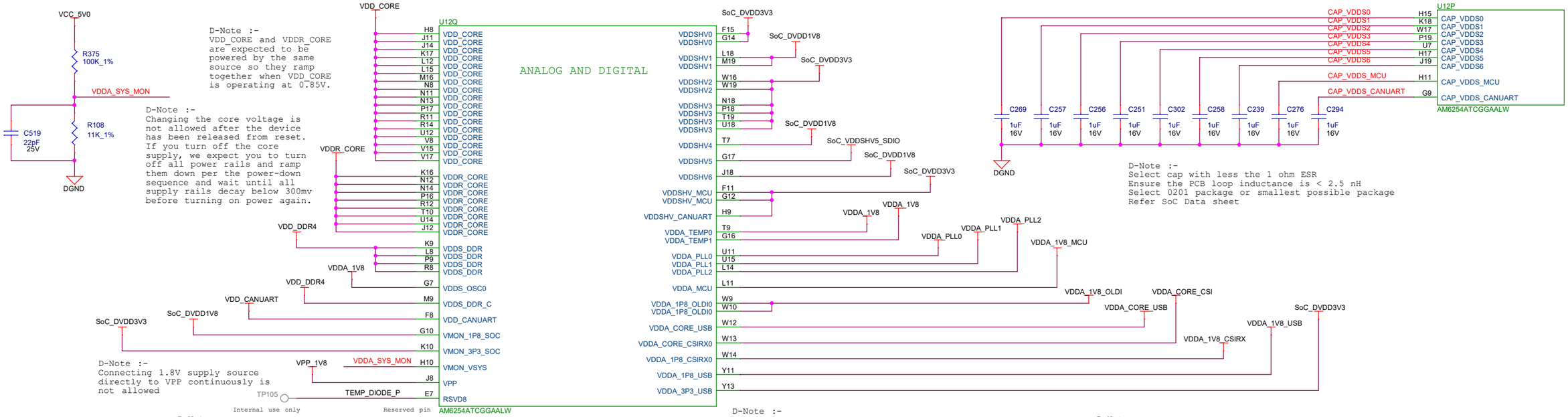
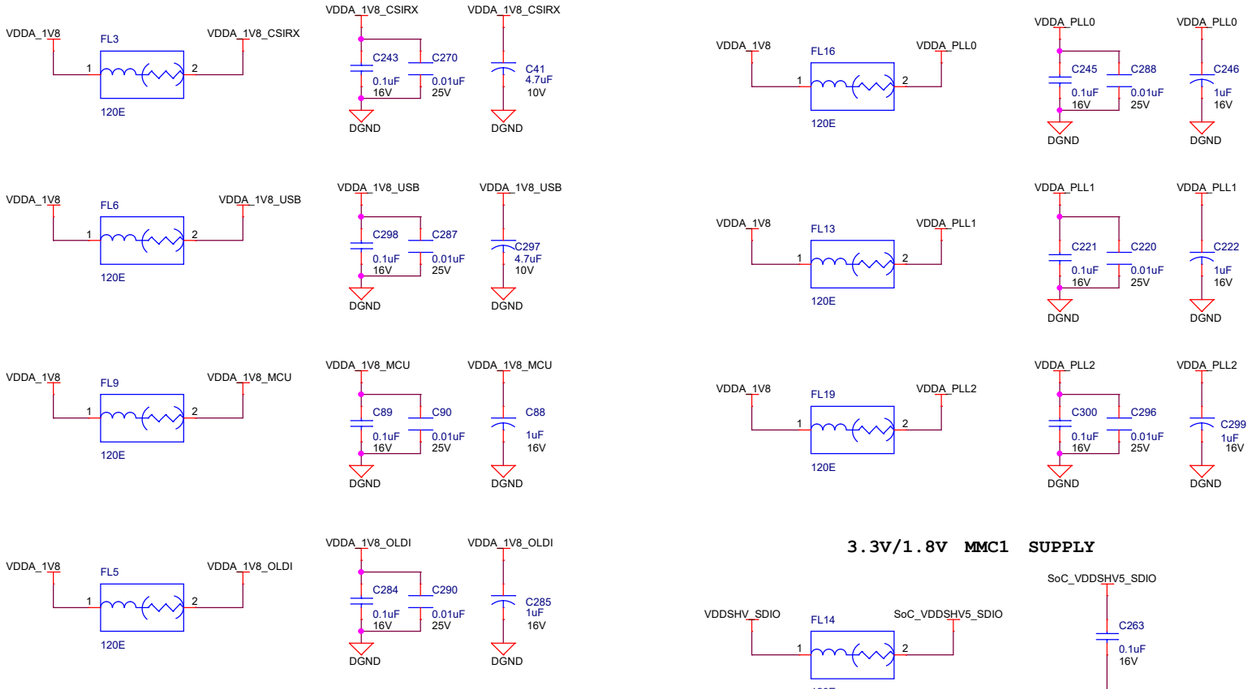
SOC POWER

D-Note :-
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure
It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts.
The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid false trigger
Refer System Power Supply Monitor Design Guidelines section of the data sheet

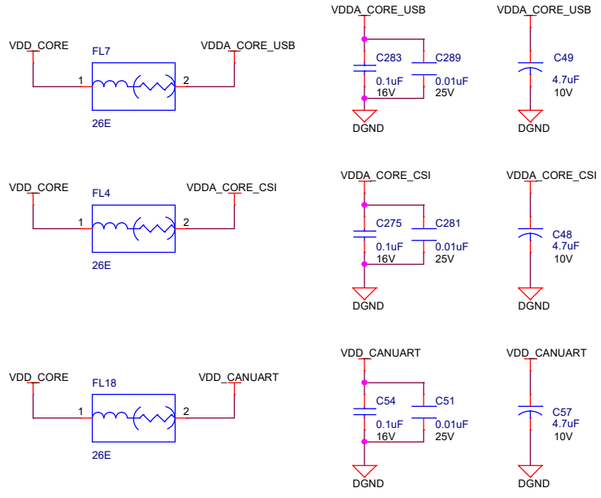


1.8V ANALOG SUPPLIES



3.3V/1.8V MMC1 SUPPLY

CORE SUPPLY



D-Note :-
A Trace connected to SOC is effectively an antenna that will pick up noise.
A potential will be generated on the signal when noise couples into the antenna.
This potential will be largest on the highest impedance end of the signal.
By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

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Title	SOC POWER	
Size	Variant Name = PROC114A1(001)	Rev
C		A1
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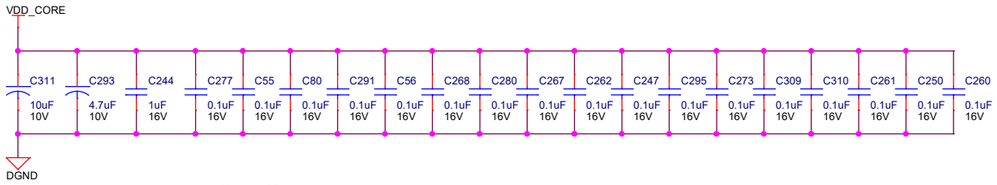
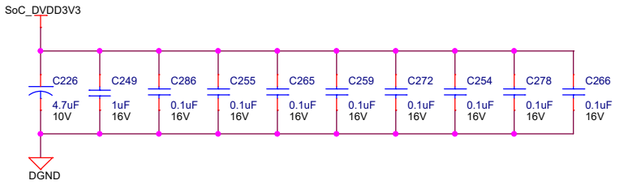
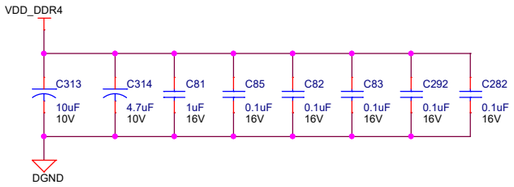
SOC POWER DECAPS



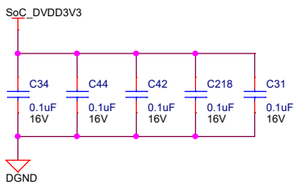
Cad Note :-
Place 0.1 uF caps near to SoC pins

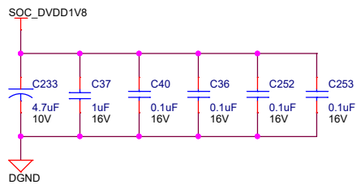


Cad Note :-
Place 0.1 uF caps near to SoC pins

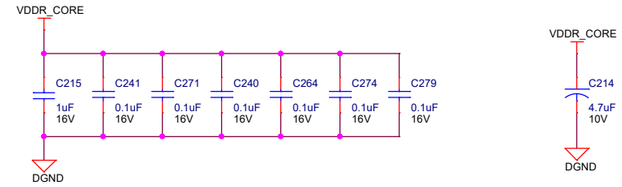


Cad Note :-
Place 0.1 uF caps near to SoC pins



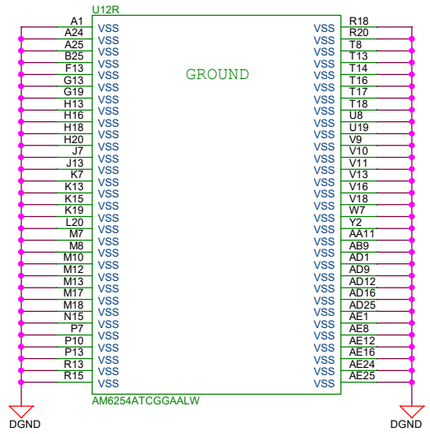


Cad Note :-
Place 0.1 uF caps near to SoC pins



Cad Note :-
Place 0.1 uF caps near to SoC pins

SOC VSS



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Title	SOC POWER CAPS & SOC VSS	
Size C	Variant Name = PROC114A1(001)	Rev
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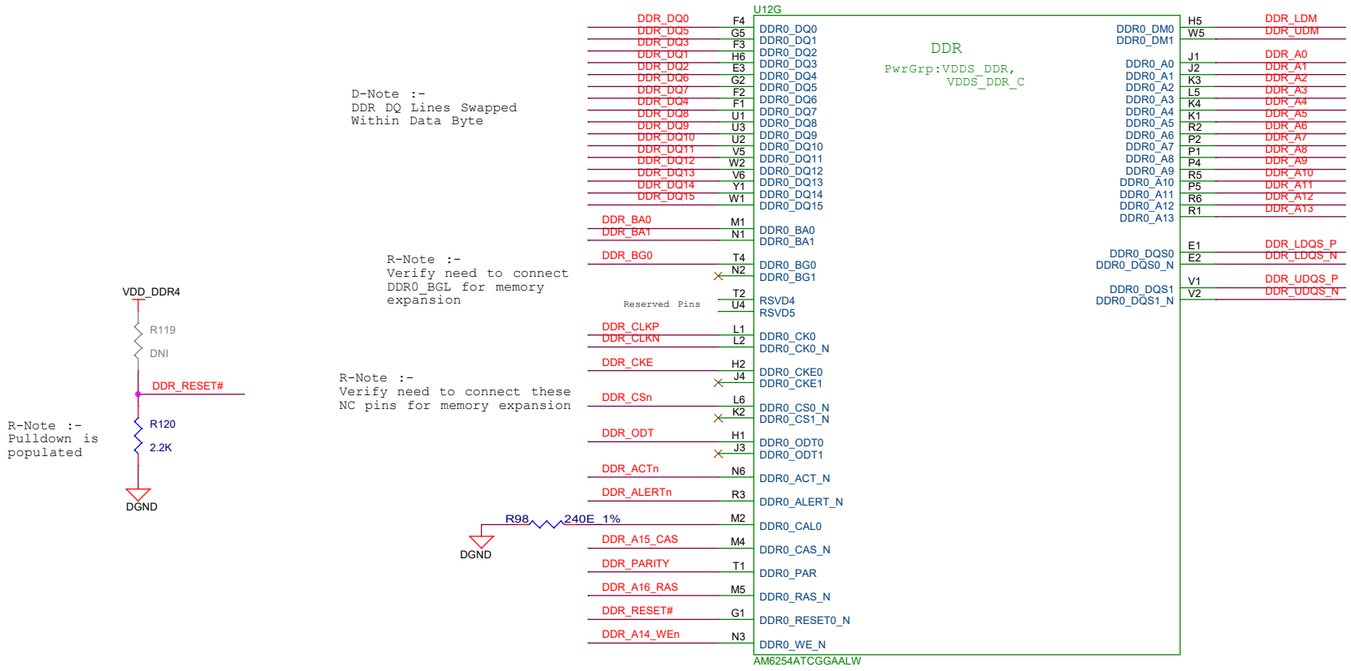
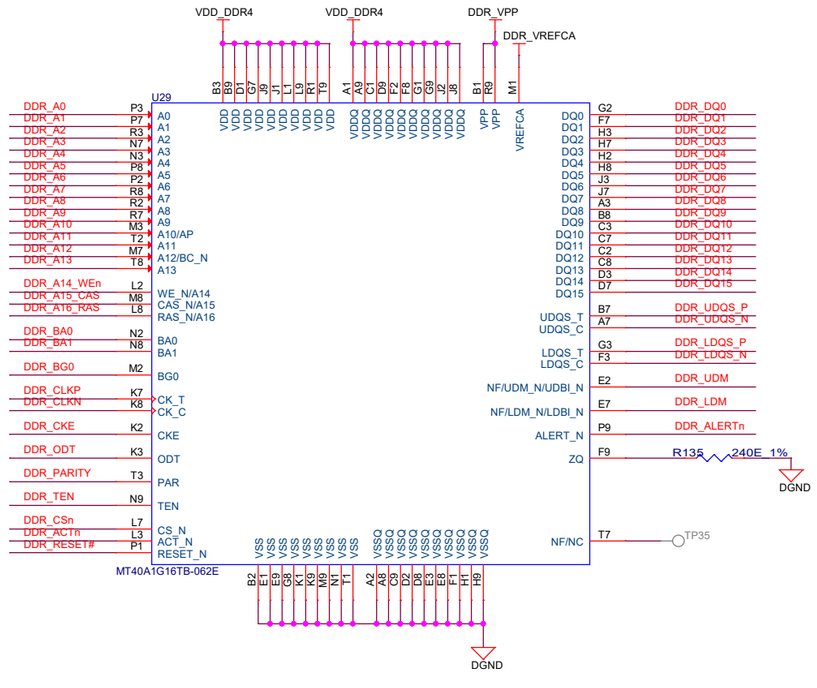
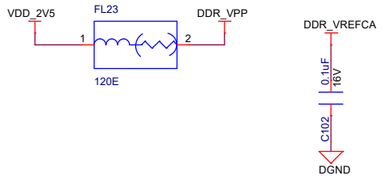
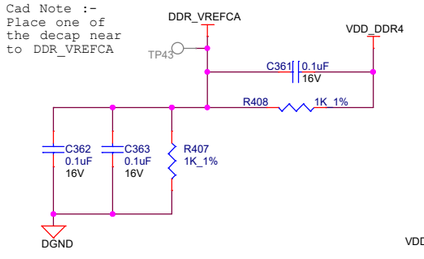
SOC DDR4 INTERFACE

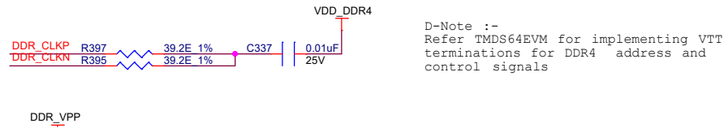


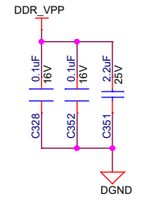
DDR4 DEVICE

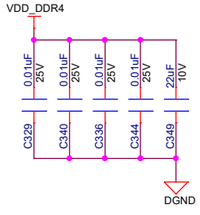


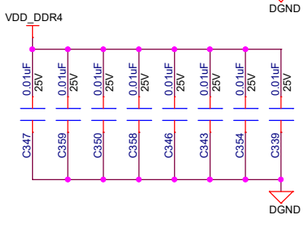


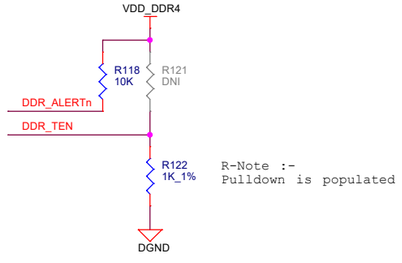


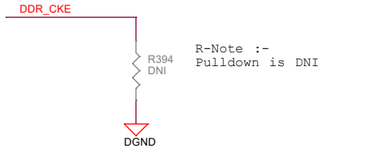












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Title	DDR4 Interface	
Size C	Variant Name = PROC114A1(001)	Rev A1
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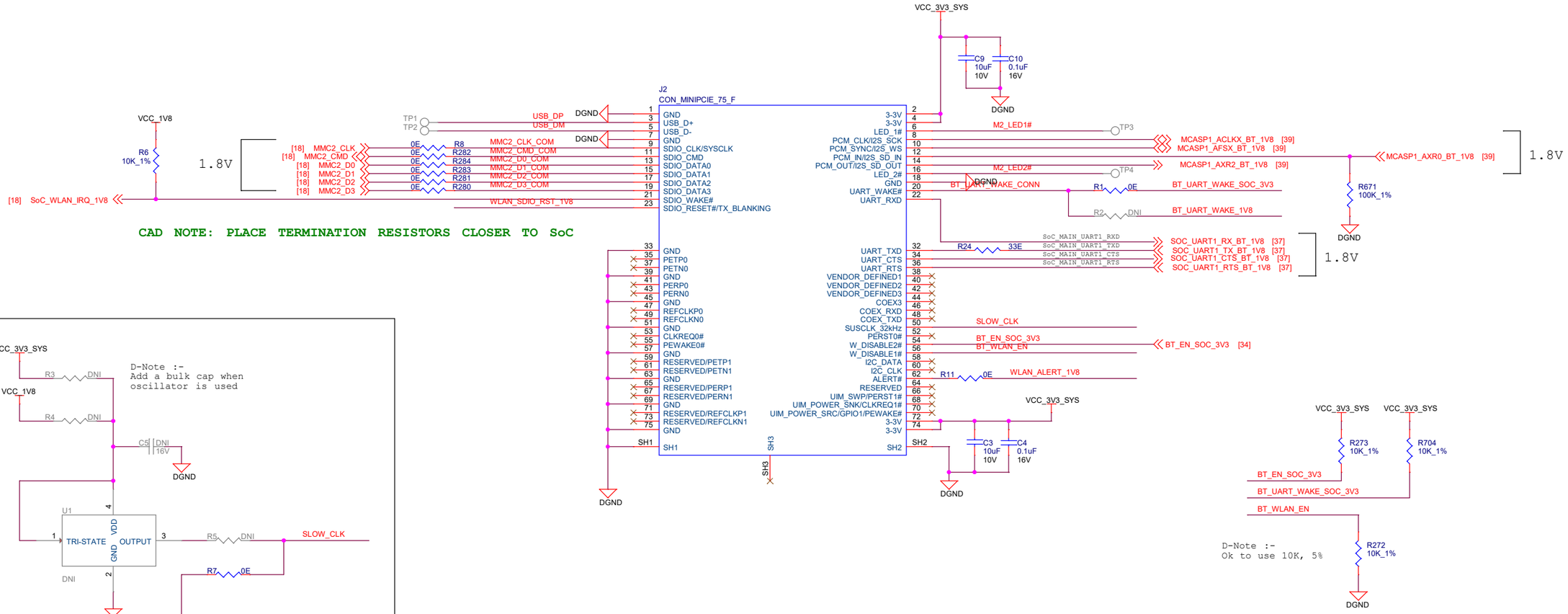
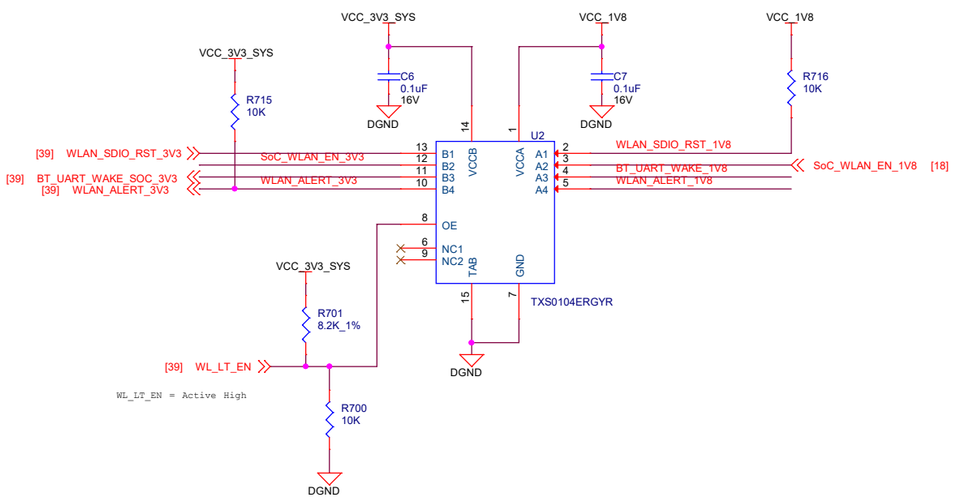
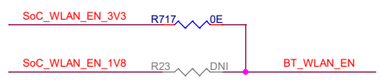
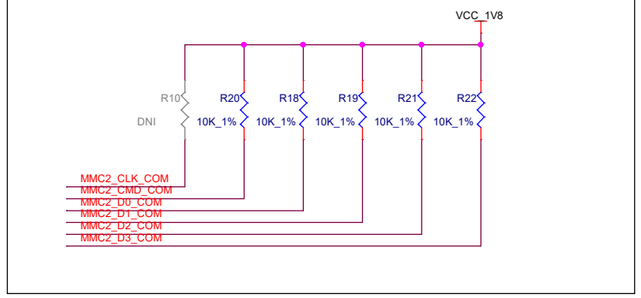
M.2 INTERFACE



CAD NOTE: PLACE TERMINATION RESISTORS CLOSER TO SoC







Designed for TI by Mistral Solutions Pvt Ltd

Title	WL1837 MODULE	
Size C	PROC114A1(001)	Rev A1
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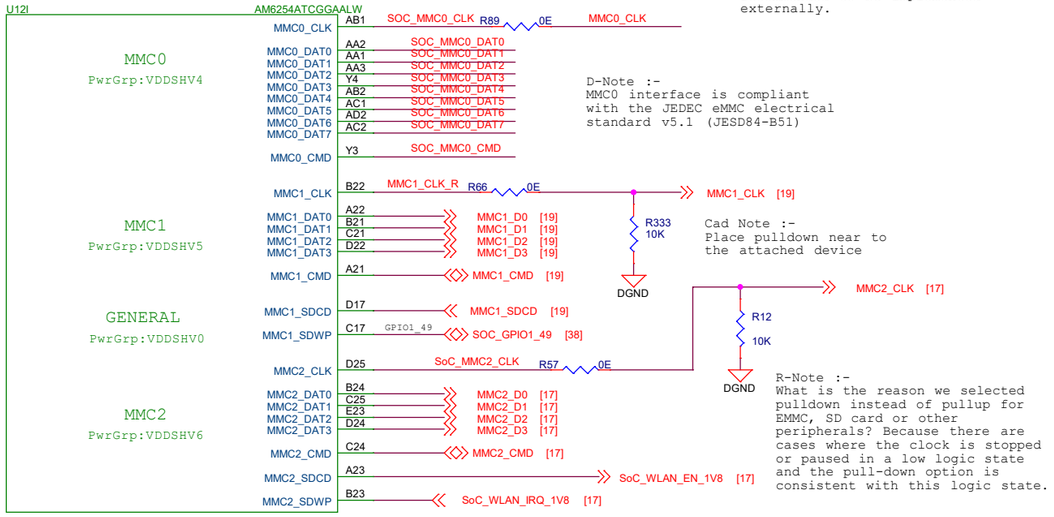
SOC - MMC Interface



D-Note :-
This family of processor implements a soft PHY for eMMC interface. The pull required for D0, Clock and other eMMC interface control signals are recommended to be implemented externally.

D-Note :-
MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)

Cad Note :-
Place pulldown near to the attached device

R-Note :-
What is the reason we selected pulldown instead of pullup for EMMC, SD card or other peripherals? Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

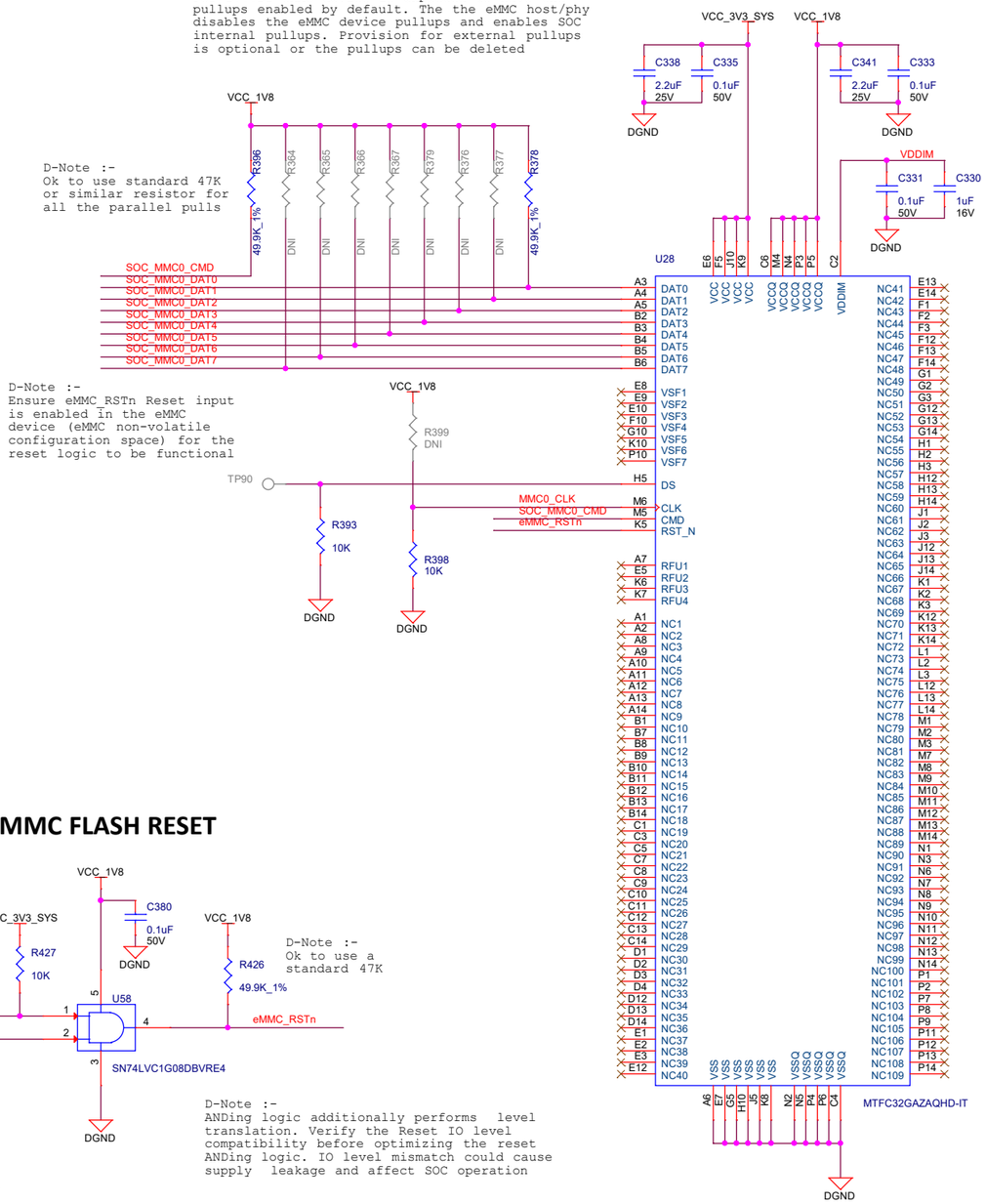
D-Note :-
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or OLDI0 or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

D-Note :-
You could eliminate the GPIO option and only use the reset output (Warm or cold), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.

eMMC FLASH

D-Note :-
For D7..D1 eMMC device is expected to have the pullups enabled by default. The the eMMC host/phy disables the eMMC device pullups and enables SOC internal pullups. Provision for external pullups is optional or the pullups can be deleted

D-Note :-
Add additional decaps as required
Refer SK-AM62P-LP schematics



D-Note :-
Ensure eMMC_RSTn Reset input is enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional

D-Note :-
Ok to use standard 47K or similar resistor for all the parallel pulls

eMMC FLASH RESET

D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

D-Note :-
Ok to use a standard 47K

D-Note :-
In case ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level.
A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is selected.
If too high the rise/fall time of the eMMC reset input could be slow and introduce too much delay.
If too low it will cause the AM62x to source too much steady-state current during normal operation.

D-Note :-
ANDing logic additionally performs level translation. Verify the Reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch could cause supply leakage and affect SOC operation

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Title	eMMC FLASH INTERFACE	
Size C	PROC114A1(001)	Rev A1
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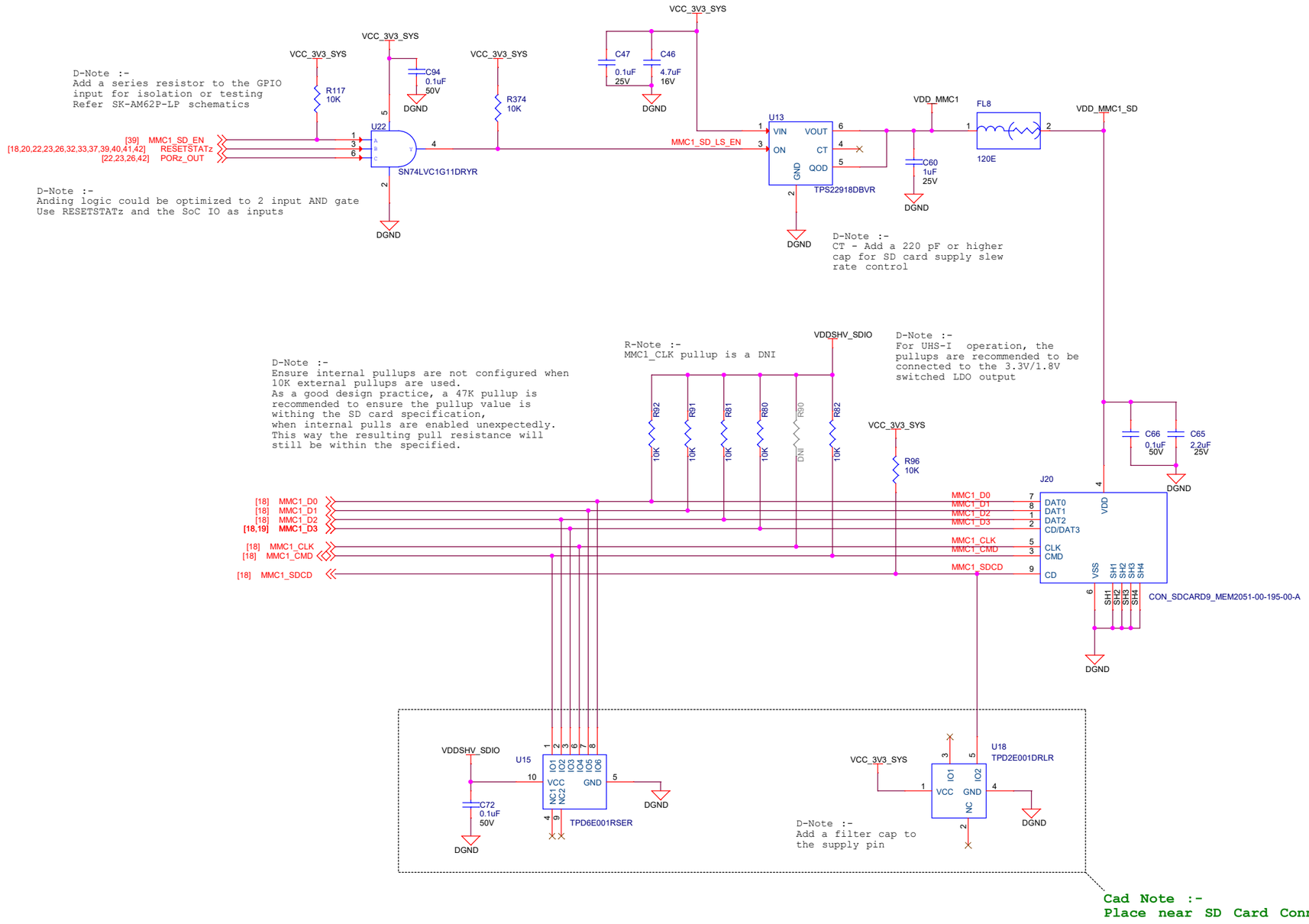
SD CARD INTERFACE

D-Note :-
This power switch, along with the reset logic, and the host IO power supply circuit is required to support UHS-I SD Cards which begins communications
using 3.3V signal levels and later change to 1.8V signal levels when changing to one of the faster data transfer speeds.
Cycling power to the SD Card is the only way to put it back into 3.3V mode since SD Cards do not have a reset pin.
The host IO power supply must power off/on and change voltage at the same time as the SD Card. These circuits and the software driver operating
the signals sourcing these circuits ensure both devices are off, or on and operating at the same IO voltage at the same time.

SD CARD LOAD SWITCH RESET LOGIC

LOAD SWITCH



Cad Note :-
Place near SD Card Connector

Designed for TI by Mistral Solutions Pvt Ltd

Title	SD CARD INTERFACE		
Size	PROC114A1(001)		Rev
C			A1
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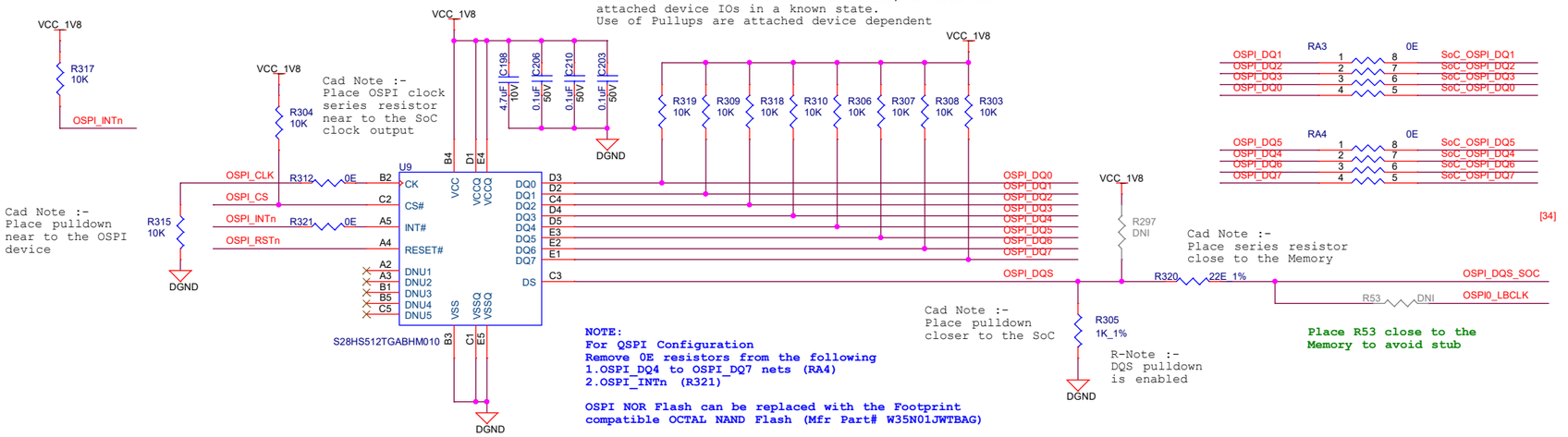
OSPI FLASH

R-Note :-
SOC IO buffers are off during power-up. A pullup is recommended near to the attached device, to hold the attached device IOs in a known state.
Use of Pullups are attached device dependent

D-Note :-
These 0R resistors are used for configuring QSPI and OSPI
This is optional during custom board design

D-Note :-
Connecting OSPI interface to multiple devices is not recommended or supported

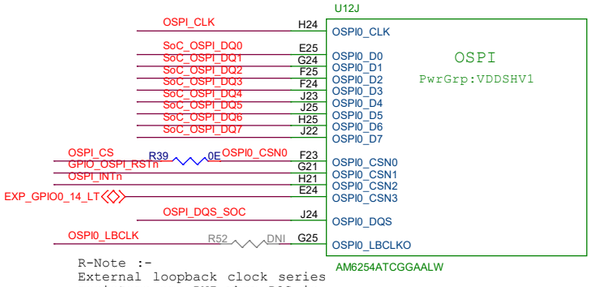


NOTE:
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (RA4)
2.OSPI_INTn (R321)

OSPI NOR Flash can be replaced with the Footprint compatible OCTAL NAND Flash (Mfr Part# W35N01JWTBAG)

Place R53 close to the Memory to avoid stub

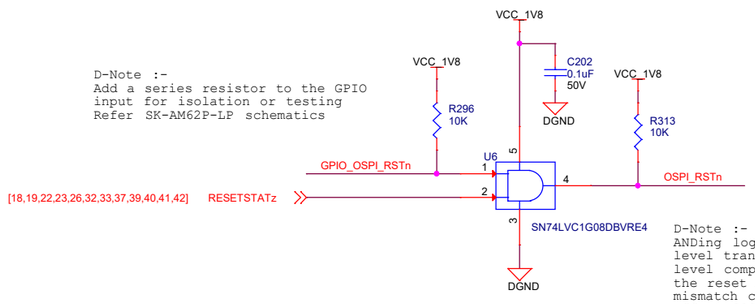
SOC OSPI INTERFACE



R-Note :-
External loopback clock series resistors are DNI when DQS is connected

Cad Note :-
Place R52 close to the SOC Ball with as little trace as possible

OSPI FLASH RESET



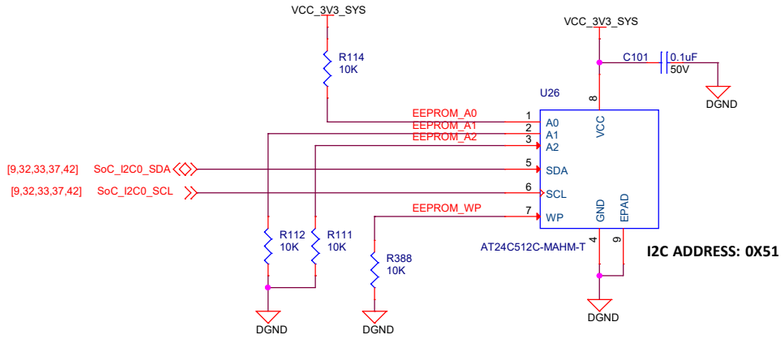
D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

D-Note :-
ANDing logic additionally performs level translation. Verify the Reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch could cause supply leakage and affect SOC operation

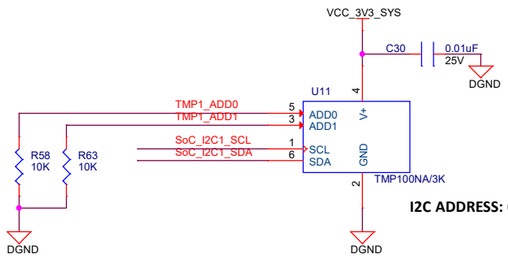
Designed for TI by Mistral Solutions Pvt Ltd

Title	OSPI INTERFACE		
Size C	PROC114A1(001)		Rev A1
Date: Friday, June 28, 2024		Sheet 20 of 44	

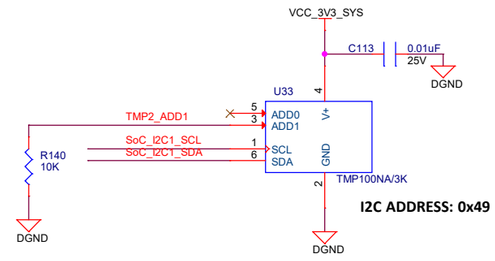
BOARD ID EEPROM



DIGITAL TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR CLOSE TO SoC



CAD NOTE: PLACE TEMP SENSOR CLOSE TO DDR4

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOARD ID EEPROM & TEMPERATURE SENSORS	
Size: C	PROC114A1(001)	Rev: A1
Date: Friday, June 28, 2024	Sheet 21 of 44	

CPSW3G RGMII 1 - ETHERNET PHY

D-Note :-
The caps and values used are as per the EPHY data sheet recommendations.

VCC_3V3_SYS: C301 0.1uF 16V, C315 0.1uF 16V, C76 0.1uF 16V, C316 1uF 16V, C307 1uF 16V, C58 1uF 16V, C319 10uF 10V, C84 0.01uF 25V → DGND

VDD_1V0: C73 0.1uF 16V, C70 0.1uF 16V, C63 0.1uF 16V, C318 0.1uF 16V, C306 1uF 16V, C317 1uF 16V, C62 1uF 16V, C71 1uF 16V, C69 10uF 10V, C61 0.01uF 25V → DGND

VDD_2V5: C68 0.1uF 16V, C304 0.1uF 16V, C78 1uF 16V, C308 1uF 16V, C77 10uF 10V, C67 0.01uF 25V → DGND

VCC_3V3_SYS, VDD_2V5, VDD_1V0; TP100, TP30

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

U51 DP83867IRRGZ

[24] CPSW_RGMII1_TD0	28	TX_D0
[24] CPSW_RGMII1_TD1	27	TX_D1
[24] CPSW_RGMII1_TD2	26	TX_D2
[24] CPSW_RGMII1_TD3	25	TX_D3
[24] CPSW_RGMII1_TXC	29	GTX_CLK
[24] CPSW_RGMII1_TX_CTL	37	TX_EN/TX_CTRL
[24] CPSW_RGMII1_RD0	33	RX_D0
[24] CPSW_RGMII1_RD1	34	RX_D1
[24] CPSW_RGMII1_RD2	35	RX_D2
[24] CPSW_RGMII1_RD3	36	RX_D3
[24] CPSW_RGMII1_RXC	32	RX_CLK (R359 0E)
[24] CPSW_RGMII1_RX_CTL	38	RX_DV/RX_CTRL
[24] CPSW_RGMII1_ETH1_CLK	15	XI
	14	XO (TP102)
	20	JTAG_CLK
	22	JTAG_TMS
	23	JTAG_TDI
	21	JTAG_TDO
CPSW_RGMII1_ETH1_CLK_OUT	18	CLK_OUT (TP32)
CPSW_RGMII1_MDC	16	MDC (R362 DNI)
CPSW_RGMII1_MDIO	17	MDIO (R363 DNI)
CPSW_RGMII_INTn	44	INT/PWDN (R352 2.2K 1%)
CPSW_RGMII1_ETH1_RBIAS	12	RBIAS (R361 10K 1%, C312 22pF 25V)
	43	RESET_N
	49	GND → DGND
	19, 30, 41	VDDIO
	13, 48	VDDA1P8
	3, 9	VDDA2P5
	6, 24, 31, 42	VDD1P0

TD_P_A	1	CPSW_ETH1_D0P
TD_M_A	2	CPSW_ETH1_D0N
TD_P_B	4	CPSW_ETH1_D1P
TD_M_B	5	CPSW_ETH1_D1M
TD_P_C	7	CPSW_ETH1_D2P
TD_M_C	8	CPSW_ETH1_D2M
TD_P_D	10	CPSW_ETH1_D3P
TD_M_D	11	CPSW_ETH1_D3M
LED_0	47	CPSW_ETH1_LED0 (TP26)
LED_1	46	CPSW_ETH1_LED_1000 (TP27)
LED_2	45	CPSW_ETH1_LED_ACT (TP22)
GPIO_0	39	R354 0E — CPSW_ETH1_GPIO_0 (TP23)
GPIO_1	40	R353 0E — CPSW_ETH1_GPIO_1 (TP24)

D-Note :-
Refer EPHY EVM for JTAG connection

R-Note :-
Ferrite is DNI

VCC_3V3_SYS → FL20 DNI

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

J6

TD_P_A	2
TD_M_A	9
TD_P_B	10
TD_M_B	7
TD_P_C	8
TD_M_C	5
TD_P_D	6
TD_M_D	3
	1 → DGND
SH1	15
SH2	16

VCC_3V3_SYS → R342 220E → 11 YELLOW / GREEN RIGHT LED; 12 CPSW1_LED_1000; YELLOW / GREEN LEFT LED; 13 CPSW1_LED_ACT; 14 CPSW1_GPIO_0

CON_RJ45-14_LPJG16314A4NL

C327 DNI 2KV, R339 0E → DGND, ETH1_EARTH

R-Note :-
Pullup is enabled for GPIO input
RESETSTATz series resistor is DNI

[23] CPSW_RGMII_INTn	CPSW_RGMII_INTn	
[32,42] CPSW_RGMII_INTn/PRU_INTn	R72 0E	CPSW_RGMII_INTn
[23,32] SoC_RGMII_MDC	R102 0E	CPSW_RGMII1_MDC
[23,32] SoC_RGMII_MDIO	R64 0E	CPSW_RGMII1_MDIO

D-Note :-
Add a isolation resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

VCC_3V3_SYS → R192 10K, R191 10K; C148 0.1uF 16V → DGND

U40 SN74LVC1G11DRYR

[39] GPIO_CPSW1_RST	1	A
[19,23,26,42] PORz_OUT	3	B
[18,19,20,23,26,32,33,37,39,40,41,42] RESETSTATz	6	C
	4	Y → CPSW_RGMII1_RESETn
	5	VCC_3V3_SYS
	2	DGND

R189 DNI, R190 DNI, R481 10K → DGND

D-Note :-
Anding logic could be optimized to 2 input AND gate
Use RESETSTATz and the SoC IO as inputs

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

VCC_3V3_SYS

R357 DNI	R356 DNI	R349 5.76K_1%
R351 10K	R76 DNI	R347 DNI
R344 DNI		
R86 DNI	R85 DNI	R350 2.49K_1%
R84 2.49K_1%	R348 DNI	R346 DNI
R345 DNI		

→ CPSW_RGMII1_RD0, CPSW_RGMII1_RD2, CPSW_RGMII1_RX_CTL, CPSW_ETH1_LED_1000, CPSW_ETH1_LED_ACT, CPSW_ETH1_GPIO_0, CPSW_ETH1_GPIO_1 → DGND

CPSW_ETH1_LED_1000 — R335 0E — Q7 CSD16301Q2 → DGND

VCC_3V3_SYS → R371 220E → CPSW1_GPIO_0

CPSW_ETH1_GPIO_0 — R387 0E — Q9 CSD16301Q2 → DGND

VCC_3V3_SYS → R341 220E → CPSW1_LED_ACT

CPSW_ETH1_LED_ACT — R383 0E — Q8 CSD16301Q2 → DGND

PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 2ns
Rx Clock Skew = 2ns

Silk: CPSW PHY-1

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_1 ETHERNET PHY	
Size	PROC114A1(001)	Rev
C		A1
Date:	Friday, June 28, 2024	Sheet 22 of 44

CPSW3G RGMII 2 - ETHERNET PHY

D-Note :-
The caps and values used are as per
the EPHY data sheet recommendations.

VCC_3V3_SYS: C235 0.1uF 16V, C32 0.1uF 16V, C208 0.1uF 16V, C236 1uF 16V, C19 1uF 16V, C227 1uF 16V, C242 10uF 10V, C38 0.01uF 25V → DGND

VDD_1V0: C27 0.1uF 16V, C238 0.1uF 16V, C22 0.1uF 16V, C29 0.1uF 16V, C237 1uF 16V, C224 1uF 16V, C21 1uF 16V, C28 1uF 16V, C39 10uF 10V, C26 0.01uF 25V → DGND

VDD_2V5: C216 0.1uF 16V, C25 0.1uF 16V, C35 1uF 16V, C228 1uF 16V, C33 10uF 10V, C24 0.01uF 25V → DGND

VCC_3V3_SYS, TP101, TP19, VDD_2V5, VDD_1V0

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

U49 DP83867IRRGZ

Pin	Name	Net
19	VDDIO	VCC_3V3_SYS
30	VDDIO	VCC_3V3_SYS
41	VDDIO	VCC_3V3_SYS
13	VDDA1P8	VCC_3V3_SYS
48	VDDA1P8	VCC_3V3_SYS
3	VDDA2P5	VDD_2V5
9	VDDA2P5	VDD_2V5
6	VDD1P0	VDD_1V0
24	VDD1P0	VDD_1V0
31	VDD1P0	VDD_1V0
42	VDD1P0	VDD_1V0
28	TX_D0	[24] CPSW_RGMII2_TD0
27	TX_D1	[24] CPSW_RGMII2_TD1
26	TX_D2	[24] CPSW_RGMII2_TD2
25	TX_D3	[24] CPSW_RGMII2_TD3
29	GTX_CLK	[24] CPSW_RGMII2_TXC
37	TX_EN/TX_CTRL	[24] CPSW_RGMII2_TX_CTL
33	RX_D0	[24] CPSW_RGMII2_RD0
34	RX_D1	[24] CPSW_RGMII2_RD1
35	RX_D2	[24] CPSW_RGMII2_RD2
36	RX_D3	[24] CPSW_RGMII2_RD3
32	RX_CLK	[24] CPSW_RGMII2_RXC
38	RX_DV/RX_CTRL	[24] CPSW_RGMII2_RX_CTL
15	XI	[24] CPSW_RGMII2_ETH2_CLK
14	XO	TP103
20	JTAG_CLK	
22	JTAG_TMS	
23	JTAG_TDI	
21	JTAG_TDO	
18	CLK_OUT	CPSW_RGMII2_ETH2_CLK_OUT
16	MDC	CPSW_RGMII2_MDC
17	MDIO	CPSW_RGMII2_MDIO
44	INT/PWDN	CPSW_RGMII_INTn
12	RBIAS	CPSW_RGMII2_ETH2_RBIAS
43	RESET_N	
49	GND	DGND
1	TD_P_A	CPSW_ETH2_D0P
2	TD_M_A	CPSW_ETH2_D0N
4	TD_P_B	CPSW_ETH2_D1P
5	TD_M_B	CPSW_ETH2_D1M
7	TD_P_C	CPSW_ETH2_D2P
8	TD_M_C	CPSW_ETH2_D2M
10	TD_P_D	CPSW_ETH2_D3P
11	TD_M_D	CPSW_ETH2_D3M
47	LED_0	CPSW_ETH2_LED0
46	LED_1	CPSW_ETH2_LED_1000
45	LED_2	CPSW_ETH2_LED_ACT
39	GPIO_0	CPSW_ETH2_GPIO_0
40	GPIO_1	CPSW_ETH2_GPIO_1

D-Note :-
Provision for Series resistor based on EPHY for RX signals near to EPHY

R324 0E

VCC_3V3_SYS: R330 1.5K, R329 DNI, R672 DNI

TP20

R328 10K 1%, C234 22pF 25V → DGND

[22] CPSW_RGMII_INTn

[22,32] SoC_RGMII_MDC — R673 0E — CPSW_RGMII2_MDC

[22,32] SoC_RGMII_MDIO — R674 0E — CPSW_RGMII2_MDIO

R-Note :-
Pullup is enabled for GPIO input
RESETSTATz series resistor is DNI

D-Note :-
Add a isolation resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

VCC_3V3_SYS: R197 10K, R196 10K, C157 0.1uF 16V → DGND

U41 SN74LVC1G11DRYR

[39] GPIO_CPSW2_RST
[19,22,26,42] PORz_OUT
[18,19,20,22,26,32,33,37,39,40,41,42] RESETSTATz
R194 DNI
CPSW_RGMII2_RESETn
R35 10K → DGND
R195 DNI → DGND

D-Note :-
Anding logic could be optimized to 2 input AND gate
Use RESETSTATz and the SoC IO as inputs

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

VCC_3V3_SYS: R322 10K, R311 DNI, R298 5.76K_1%, R300 10K, R38 DNI, R294 DNI, R291 DNI

CPSW_RGMII2_RD0
CPSW_RGMII2_RD2
CPSW_RGMII2_RX_CTL
CPSW_ETH2_LED_1000
CPSW_ETH2_LED_ACT
CPSW_ETH2_GPIO_0
CPSW_ETH2_GPIO_1

R54 2.49K_1%, R49 DNI, R299 2.49K_1%, R47 2.49K_1%, R295 DNI, R293 DNI, R292 DNI → DGND

PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 2ns
Rx Clock Skew = 2ns

R-Note :-
Ferrite is DNI

VCC_3V3_SYS — FL15 DNI

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

J4

Pin	Net
2	CPSW_ETH2_D0P
9	CPSW_ETH2_D0N
10	CPSW_ETH2_D1P
7	CPSW_ETH2_D1M
8	CPSW_ETH2_D2P
5	CPSW_ETH2_D2M
6	CPSW_ETH2_D3P
3	CPSW_ETH2_D3M
4	CPSW_ETH2_LED0
1	DGND
11	CPSW2_LED_1000
12	CPSW2_LED_ACT
13	CPSW2_GPIO_0
14	DGND
SH1	15
SH2	16

VCC_3V3_SYS: R286 220E → CPSW2_LED_1000 → YELLOW / GREEN (RIGHT LED)
CPSW2_LED_ACT → YELLOW / GREEN (LEFT LED)
CPSW2_GPIO_0

CON_RJ45-14_LPJG16314A4NL

C195 DNI 2KV
R29 0E → DGND
ETH2_EARTH

Silk: CPSW PHY-2

CPSW2_LED_1000 — R289 0E — Q4 CSD16301Q2 → DGND

CPSW_ETH2_GPIO_0 — R340 0E — Q6 CSD16301Q2 → DGND

CPSW_ETH2_LED_ACT — R338 0E — Q5 CSD16301Q2 → DGND

VCC_3V3_SYS: R334 220E → CPSW2_GPIO_0

VCC_3V3_SYS: R288 220E → CPSW2_LED_ACT

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_2 ETHERNET PHY		
Size	C	PROC114A1(001)	Rev A1
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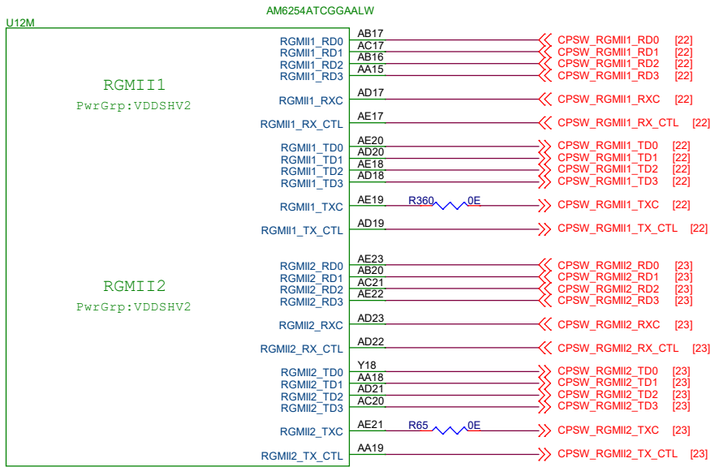
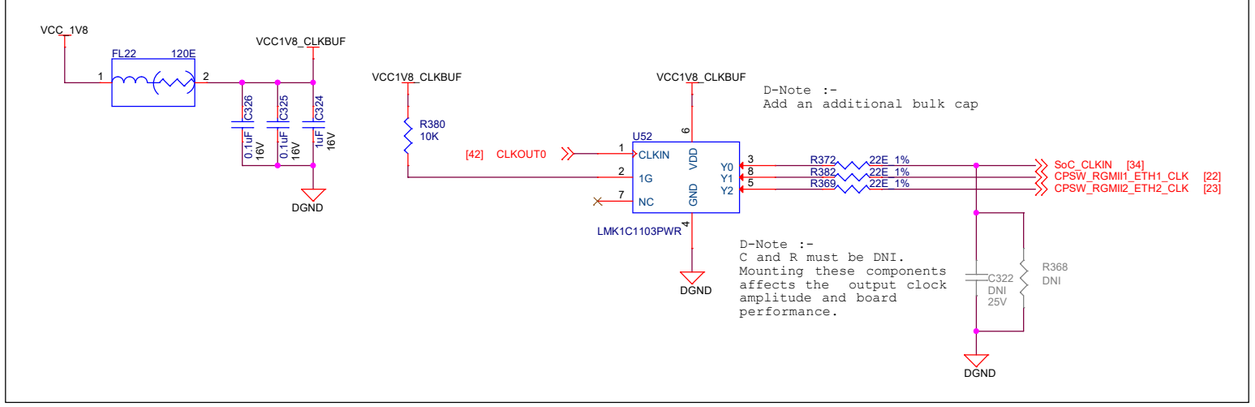
SOC MAC INTERFACE

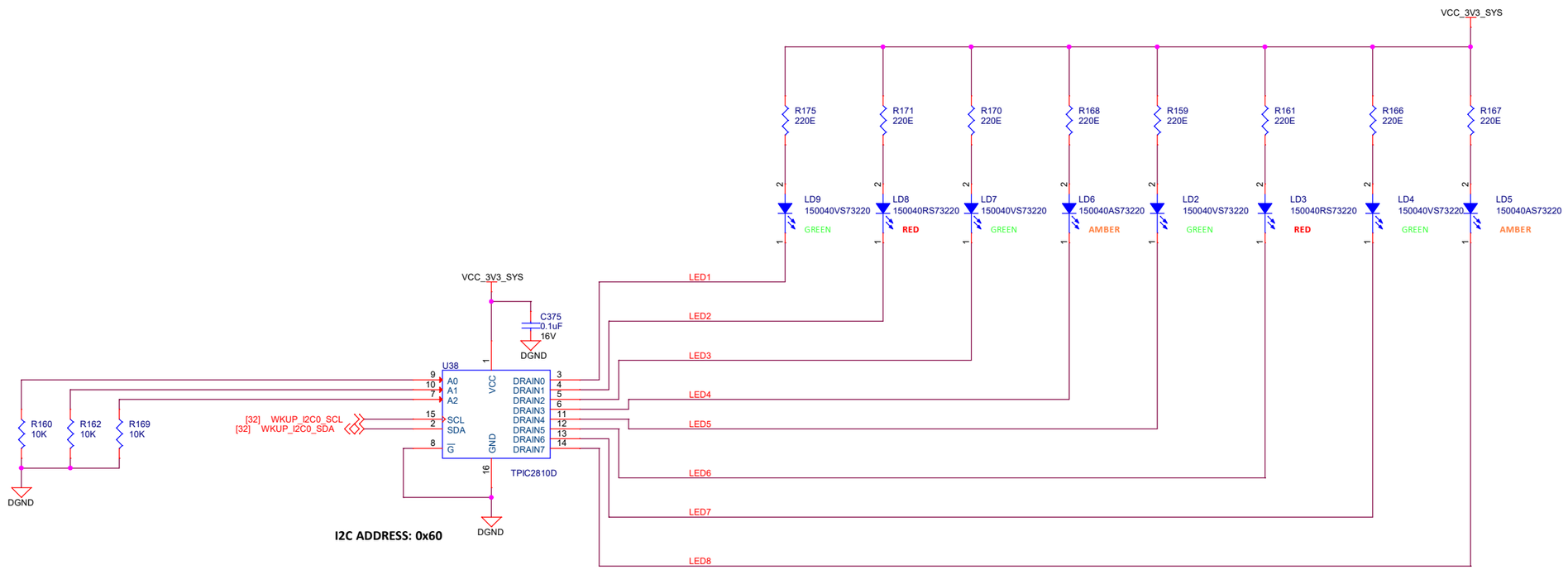
D-Note :-
Add series resistors 22 R on the Ethernet interface TX (TDx) signals near to the SoC



CLOCK BUFFER FOR SOC AND ETHERNET PHYs



LED DRIVER



Designed for TI by Mistral Solutions Pvt Ltd

Title	ETHERNET PHY CLOCK BUFFER & LED DRIVER	
Size C	PROC114A1(001)	Rev A1
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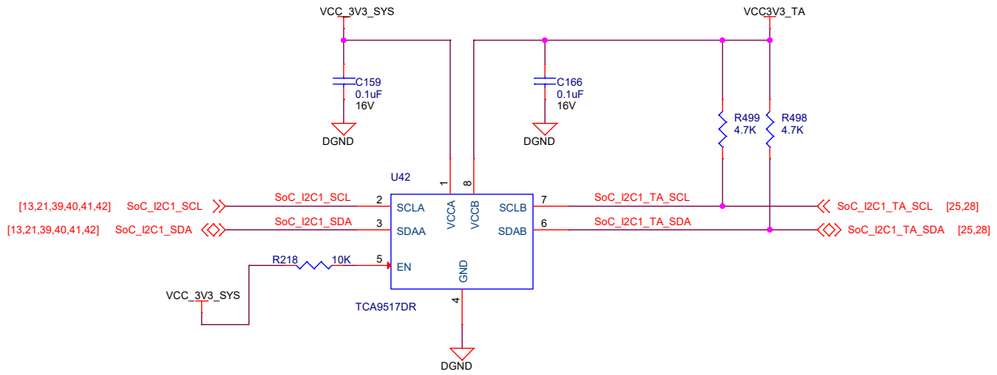
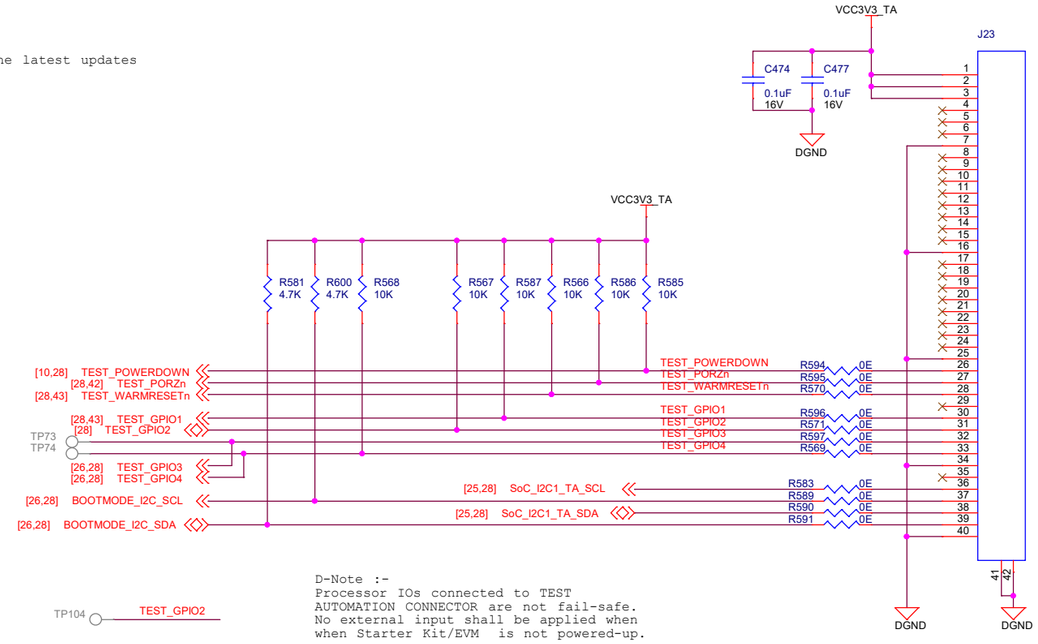
40-PIN TEST AUTOMATION HEADER

I2C BUS BUFFER



D-Note :-
Refer SK-AM62P-LP for the latest updates



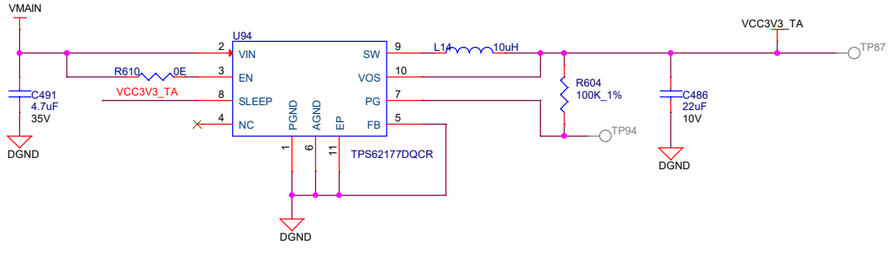
D-Note :-
Processor IOs connected to TEST
AUTOMATION CONNECTOR are not fail-safe.
No external input shall be applied when
when Starter Kit/EVM is not powered-up.

CON_FLEX_40X1_FH12A-40S-0.5SH

Silk: AUTOMATION HDR

TEST AUTOMATION BOARD POWER

VinMin = 4.75V
VinMax = 24V
Vout = 3.3V @ 0.5A



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SoC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

Designed for TI by Mistral Solutions Pvt Ltd

Title	TEST AUTOMATION		
Size C	PROC114A1(001)		Rev A1
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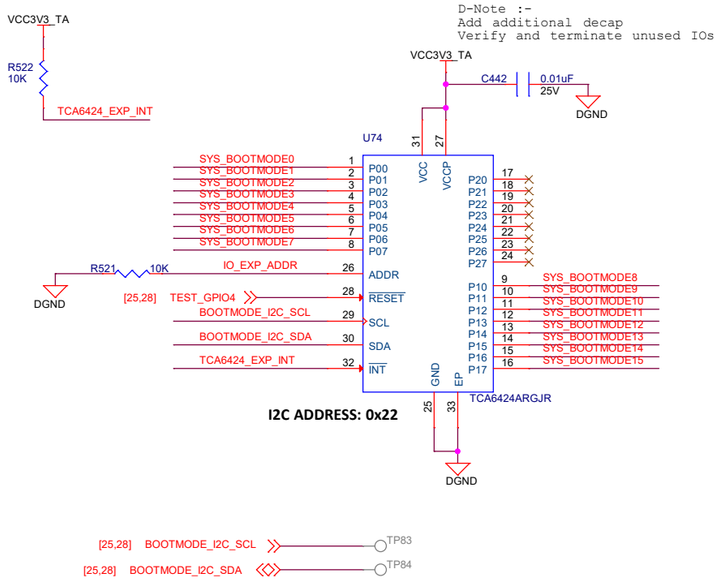
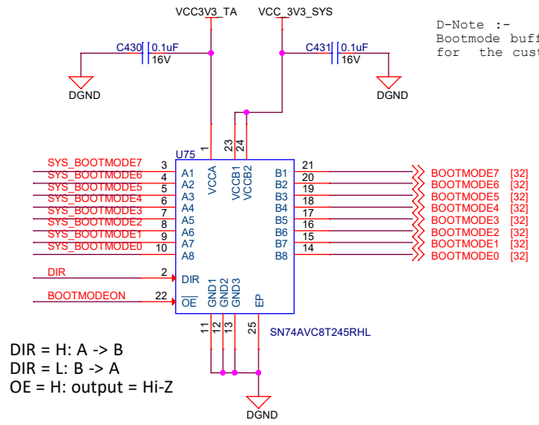
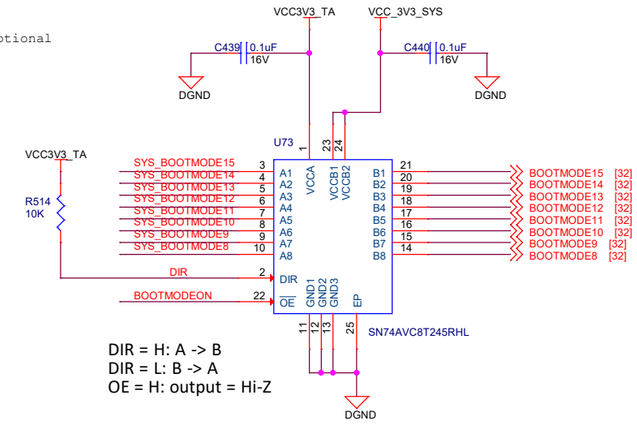
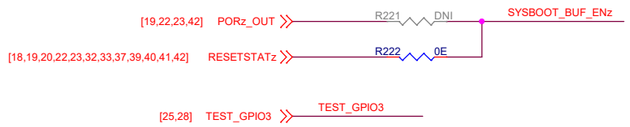
BOOTMODE IO EXPANDER

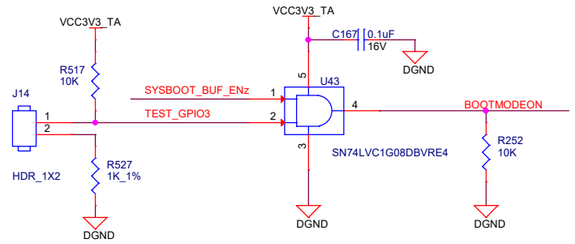


BOOT MODE BUFFERS







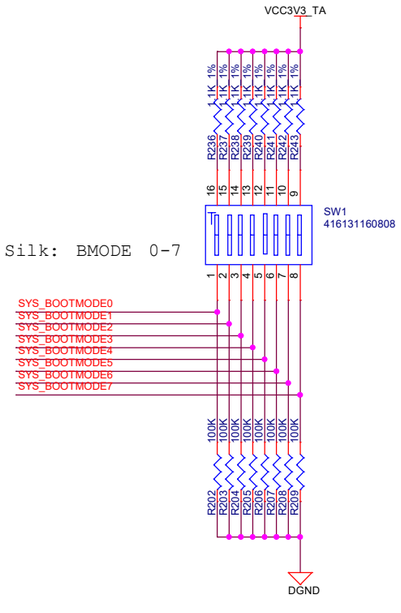


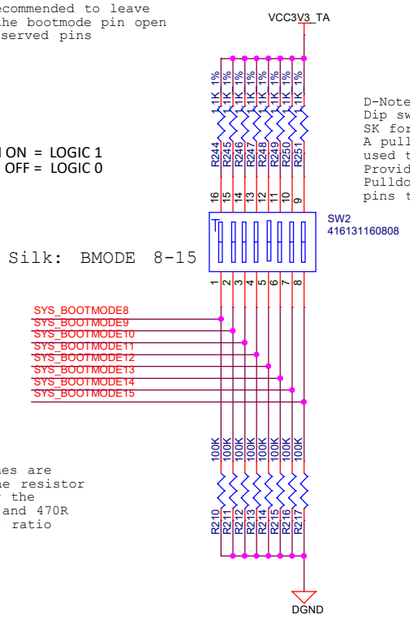
BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES

D-Note :-
VCC3V3_XDS_TA supply is used for test automation. Connect SoC_DVDD3V3 in the custom board design when buffers are not used

D-Note :-
it is not recommended to leave any of the the bootmode pin open including reserved pins

SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0





D-Note :-
When DIP switches are used, reduce the resistor values used for the divider to 47K and 470R maintaining the ratio

D-Note :-
Dip switch is optional and used on the SK for ease of configuration
A pullup or pulldown resistor can be used to set the BOOTMODE configuration
Provide provision for Pullup and Pulldown resistors for the bootmode pins that have configuration capability

BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. BACKUP BOOT OPTION

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOOT MODE BUFFER & SWITCHES		
Size	PROC114A1(001)		Rev A1
C			
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XDS110 DEBUGGER

D-Note :-
Please follow SK-AM62P-LP EVM implementations
for latest updates on XDS110

TP86
XDS_USB_VBUS
C180 4.7uF 10V
D8 TPD1E10B06DPYR
C455 2.2uF 25V
R540 0E
U79
IN1 IN2 EN GND OUT1 OUT2 NR/FB PAD NC
TPS79601DRBR
R520 51K
R519 30K
C441 15pF 25V
C443 1uF 16V
VCC3V3_XDS
TP77
C454 1uF 16V
C468 0.1uF 16V
C173 0.1uF 16V
C181 0.01uF 25V
C176 0.01uF 25V
C191 0.01uF 25V
U45B
VDD GNDA GND VDDA VDDC VBAT
TM4C1294NCPDTT3R
C192 1uF 16V
C189 0.01uF 25V
C179 2.2uF 25V
C178 1uF 16V
C449 0.1uF 16V
VDDC_1V2
R228 49.9E_1%
C169 0.1uF 16V
DGND

Silk: JTAG

J16
VBUS D- D+ ID GND SH1 SH2 SH3 SH4
CON_MUSB-B_5_F
XDS_USB_DM
XDS_USB_DP
XDS_USB_ID
D-Note :-
Add a filter
cap (0.1uF)
U89
IO1 IO2 IO3 IO4 VCC GND
TPD4E004DRYR
R256 0E
C185 DNI 2KV
XDS_SHIELD

U45A
PA0/U0RX PA1/U0TX PA2/SSI0CLK PA3/SSI0FSS PA4/SSI0XDAT0 PA5/SSI0XDAT1 PA6 PA7
PC0/TCK/SWCLK PC1/TMS/SWDIO PC2/TDI PC3/TDO/SWO PC4/C1- PC5/C1+ PC6/C0+ PC7/C0-
PE0/AIN3 PE1/AIN2 PE2/AIN1 PE3/AIN0 PE4/AIN9 PE5/AIN8
PG0 PG1
PJ0 PJ1
PL0 PL1 PL2 PL3 PL4 PL5 PL6/USB0DP PL7/USB0DM
PN0 PN1 PN2 PN3 PN4 PN5
PQ0 PQ1 PQ2 PQ3 PQ4
TM4C1294NCPDTT3R
PB0/USB0ID PB1/USB0VBUS PB2/I2C0SCL PB3/I2C0SDA PB4/AIN10 PB5/AIN11
PD0/AIN15 PD1/AIN14 PD2/AIN13 PD3/AIN12 PD4/AIN7 PD5/AIN6 PD6/AIN5 PD7/AIN4
PF0 PF1 PF2 PF3 PF4
PH0 PH1 PH2 PH3
PK0/AIN16 PK1/AIN17 PK2/AIN18 PK3/AIN19 PK4 PK5 PK6 PK7
PM0 PM1 PM2 PM3 PM4 PM5 PM6 PM7
PP0/C2+ PP1/C2- PP2 PP3 PP4 PP5
[29] XDS110_TCK
[29] XDS110_TMS
[29] XDS110_TDO
[29] XDS110_TDI
[29] XDS110_TRST#
TP82 TP81 TP80 TP79
TM4C129_TCK
TM4C129_TMS
TM4C129_TDI
TM4C129_TDO
[28] BOOTMODE_XDS_I2C_SCL
[28] BOOTMODE_XDS_I2C_SDA
[28] SoC_I2C1_XDS_SDA
[28] SoC_I2C1_XDS_SCL
XDS_USB_DP
XDS_USB_DM
XDS110_EMU0
XDS110_EMU1
R530 100E_1%
R235 DNI
C170 0.1uF 16V
XDS_USB_ID
XDS_USB_VBUS
R268 30K
R269 20K_1%
R267 220E
R271 220E
LD14 150080VS75000 GREEN
LD15 150040RS73220 RED
TEST_POWERDOWN_XDS [28]
TEST_PORZn_XDS [28]
TEST_WARMRESETn_XDS [28]
TEST_GPIO1_XDS [28]
TEST_GPIO2_XDS [28]
TEST_GPIO3_XDS [28]
TEST_GPIO4_XDS [28]
TP76
R563 1K_1%
R560 1K_1%
R556 1K_1%
R552 1K_1%
R260 DNI
R259 DNI
R258 DNI
R255 DNI

Sets the unique ID of the Debugger

VCC3V3_XDS
R539 10K
TP75
R546 DNI
XDS_RSTn
U45C
RST WAKE HIB OSC0 OSC1 XOSC0 XOSC1 RBAIS VREFA+ EN0RXIP EN0RXIN EN0RX0P EN0RX0N
TM4C1294NCPDTT3R
R270 4.7K
XDS_VREF
C186 0.01uF 25V
C190 0.1uF 16V
U47
LM4040B25IDCKR
C172 12pF 25V
C171 12pF 25V
Y2 16.000MHz
R261 4.87K_1%
R264 4.7K
R265 4.7K
XDS110_EMU0 [29]
XDS110_EMU1 [29]
DGND

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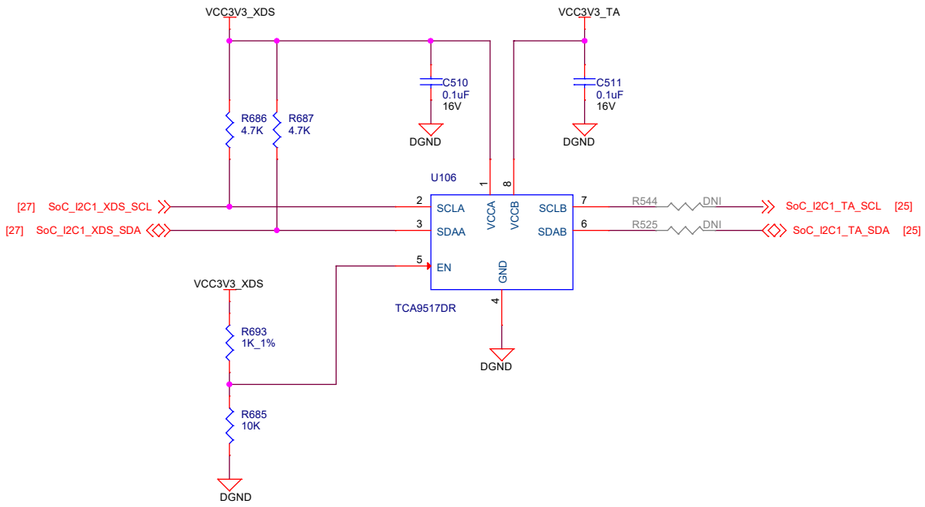
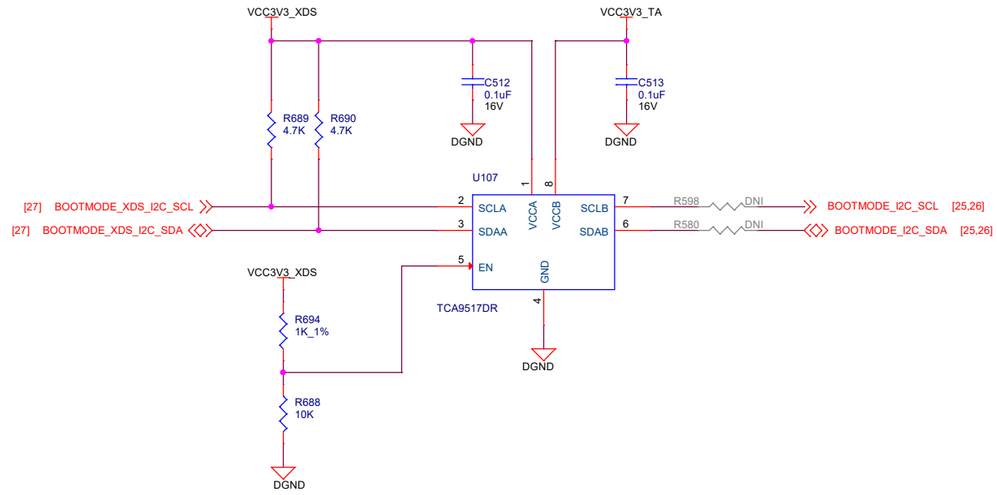
Title	XDS110 DEBUGGER		
Size	PROC114A1(001)		Rev
C			A1
Date:	Friday, June 28, 2024	Sheet 27 of 44	

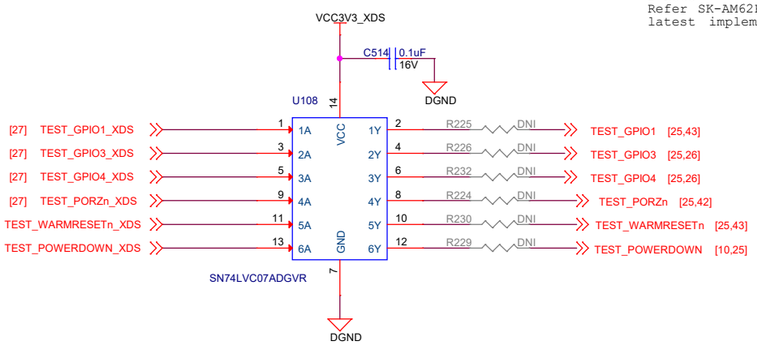
I2C_TA BUS BUFFER

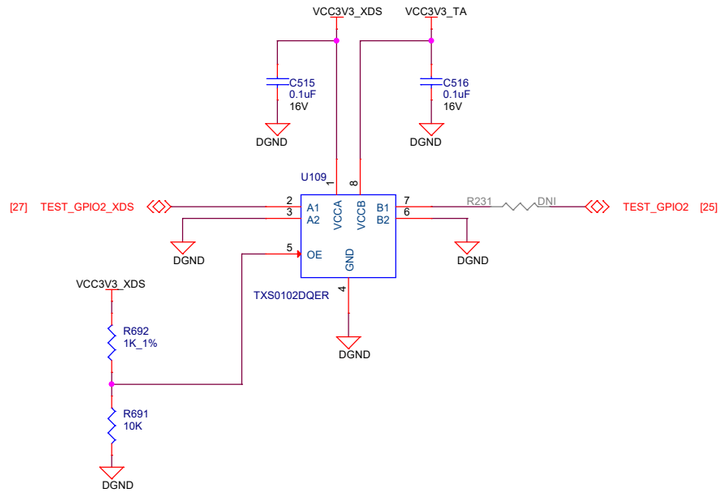


BOOTMODE_I2C_TA BUFFER



ISOLATION BUFFERS FOR TA SIGNALS





D-Note :-
Refer SK-AM62P-LP for the latest implementation

Pull ups(R567, R587, R517, R568, R585, R586 & R566) to VCC3V3_TA are present

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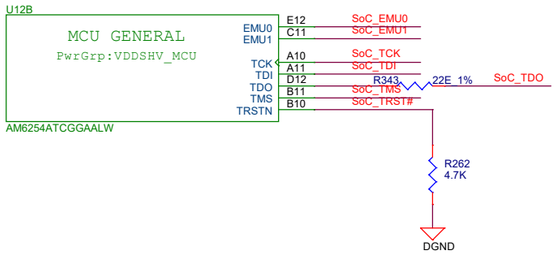
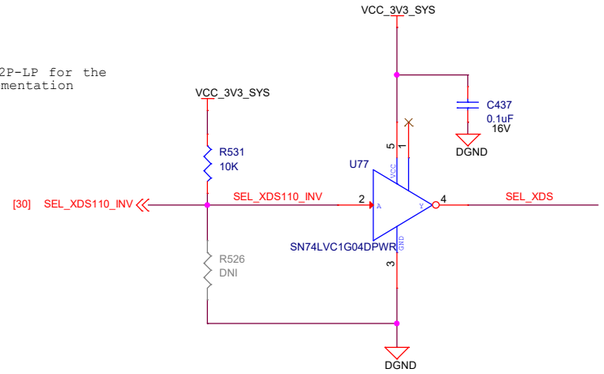
Title	AUTOMATION SIGNALS BUFFER	
Size C	PROC114A1(001)	Rev A1
Date: Friday, June 28, 2024	Sheet 28 of 44	

JTAG SOC SECTION

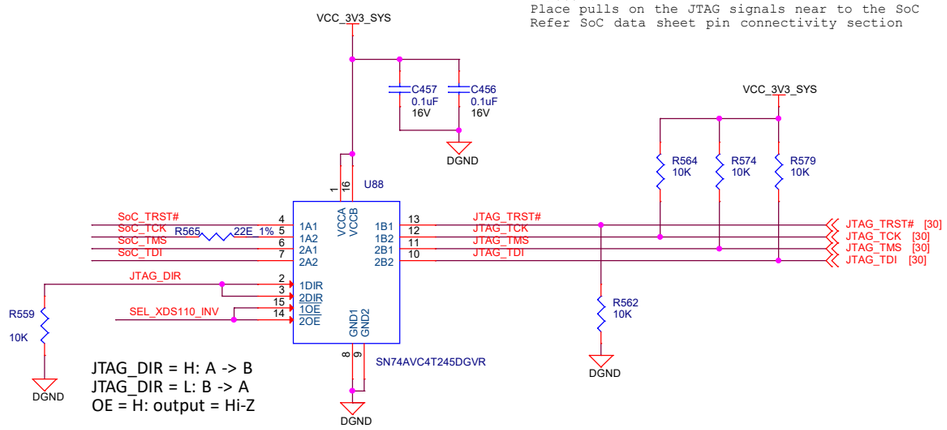
D-Note :-
Refer SK-AM62P-LP for the
latest implementation



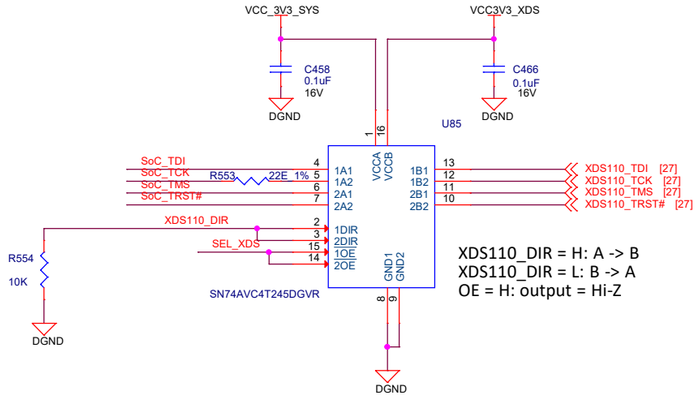


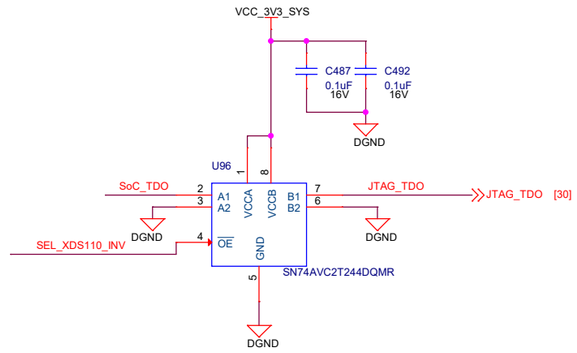
cTI20 JTAG BUFFERS

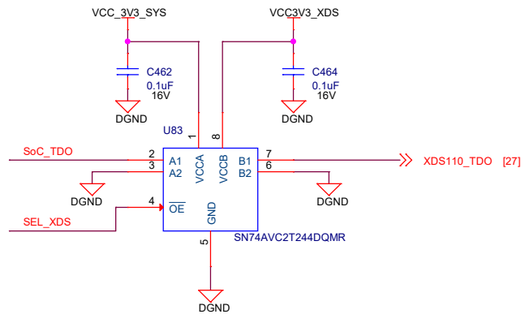
D-Note :-
Place pulls on the JTAG signals near to the SoC
Refer SoC data sheet pin connectivity section



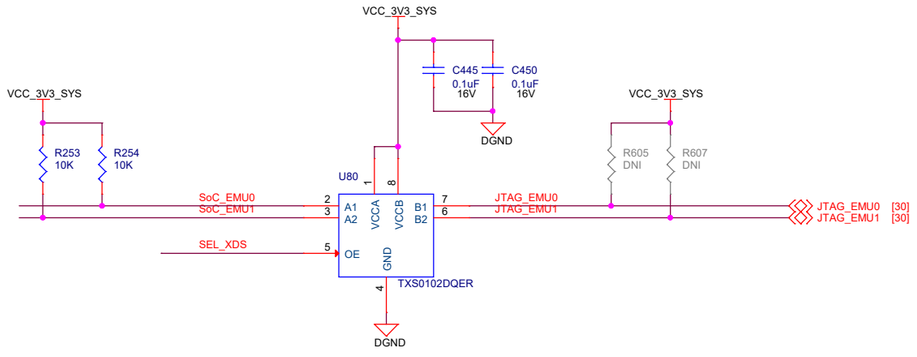
BUFFER XDS110

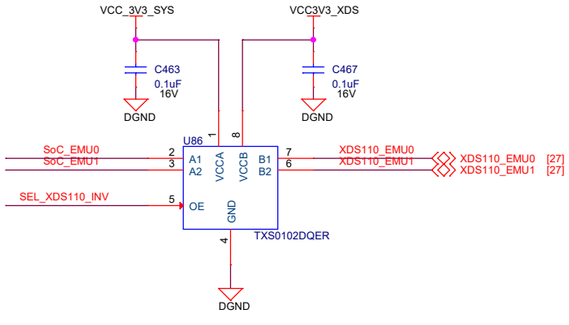






CAD NOTE: Buffers U88 and U96
need to be placed closer to the
cTI-20pin connector J17 to reduce Stub length of the JTAG signals.





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Title	JTAG BUFFER	
Size: C	PROC114A1(001)	Rev: A1
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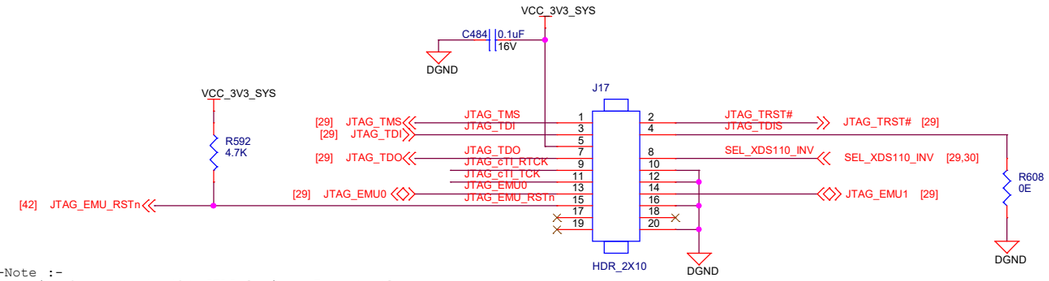
JTAG 20 PIN cTI CONNECTOR

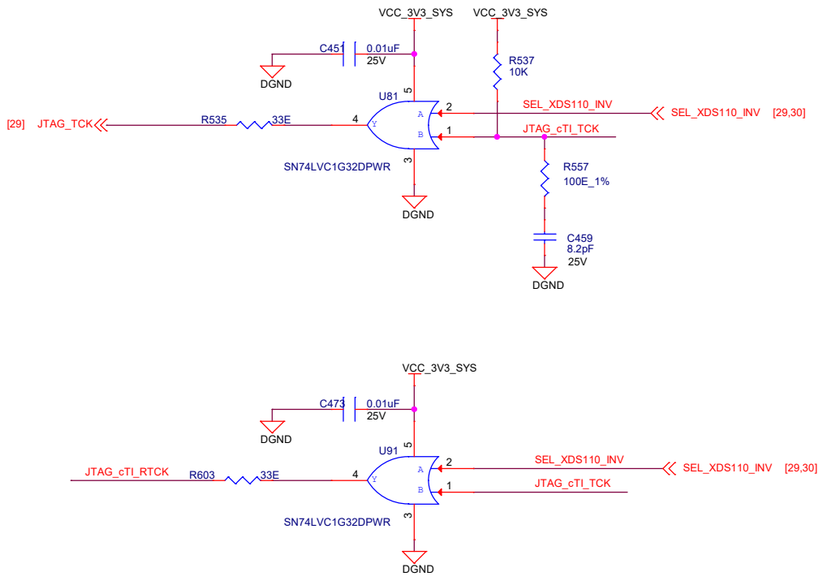


D-Note :-
TRSTn is the reset to the JTAG logic. For normal operation, this is pulled low, and thus the JTAG remains in reset as it is not being used.
When a JTAG pod is connected, the pod will eventually drive this signal high to release the JTAG logic from reset and enable a JTAG connection.

Silk: cTI

D-Note :-
Add an external ESD protection to provide system level ESD protection when external connector is used for debug
Add Test points and ESD protection when JATG connector is not used

JTAG CLOCK BUFFER



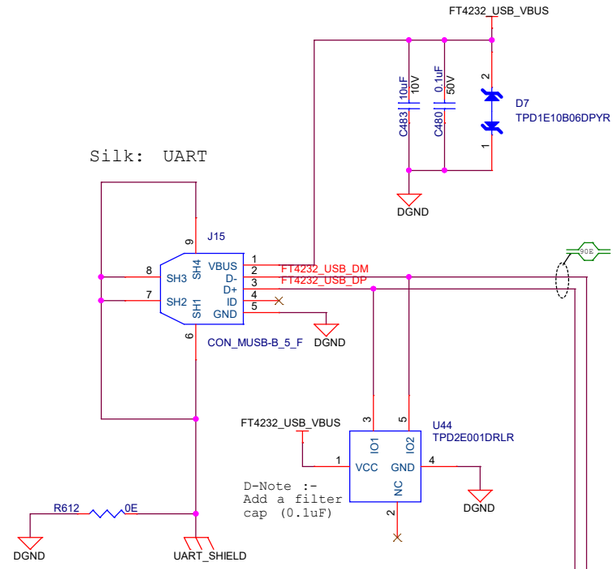
Designed for TI by Mistral Solutions Pvt Ltd

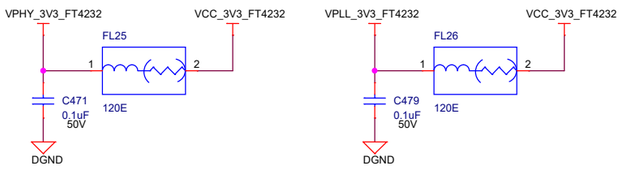
Title	JTAG 20 PIN cTI CONNECTOR	
Size C	PROC114A1(001)	Rev A1
Date: Friday, June 28, 2024	Sheet 30 of 44	

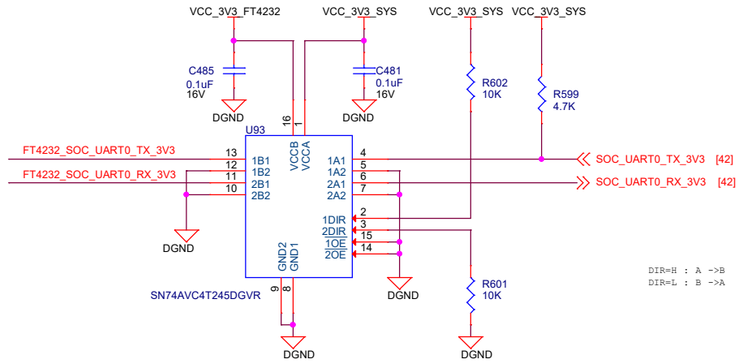
FT4232 UART

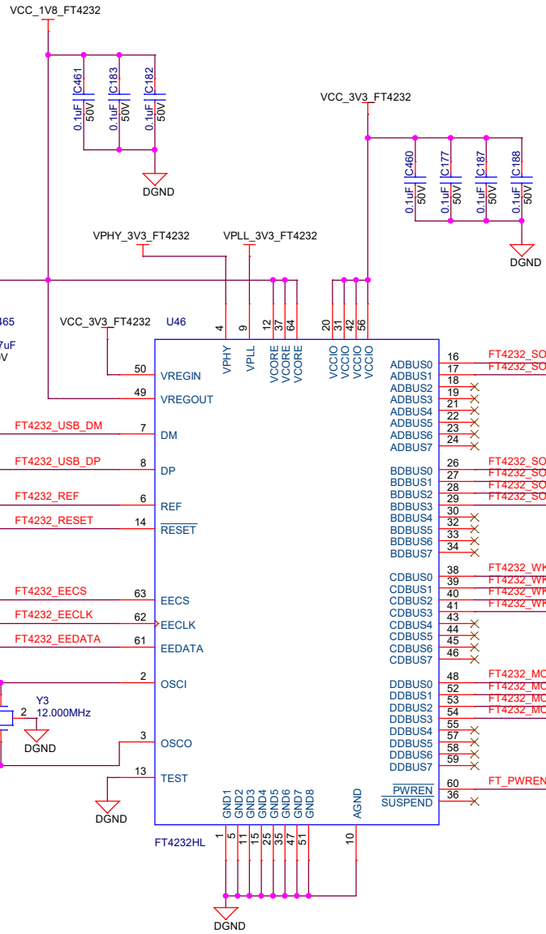
D-Note :-
Follow SK-AM62P-LP for latest
FT4232 implementations

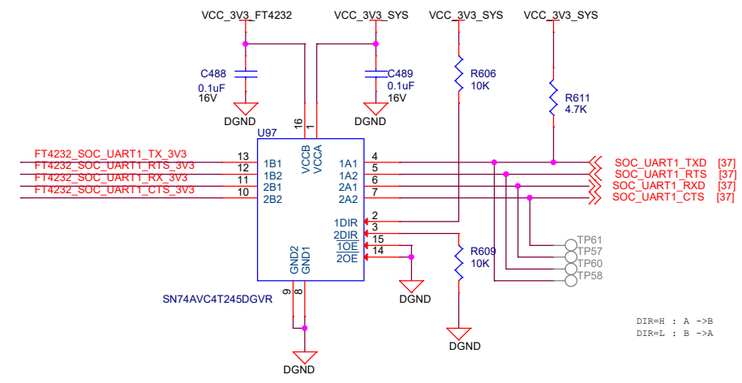
Silk: UART

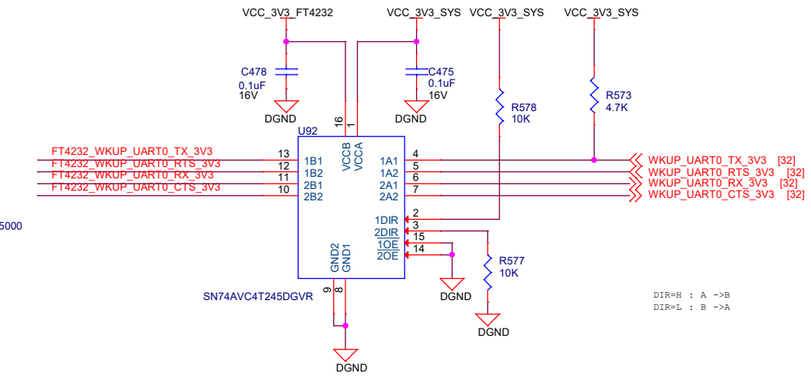


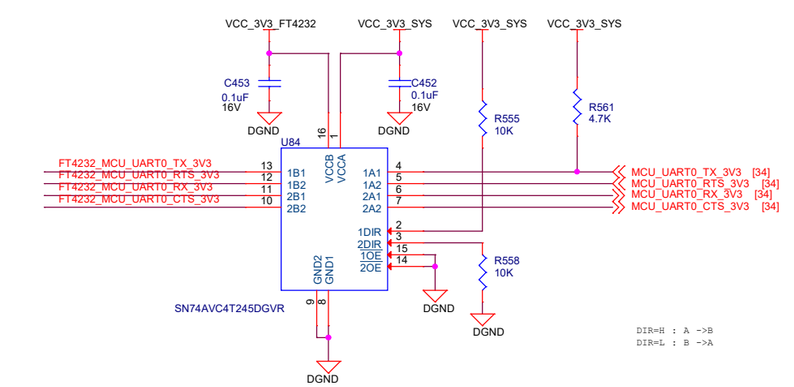




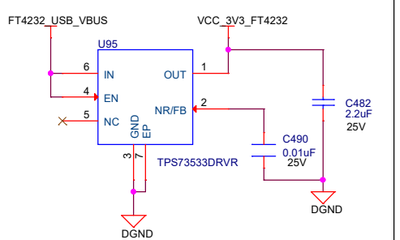




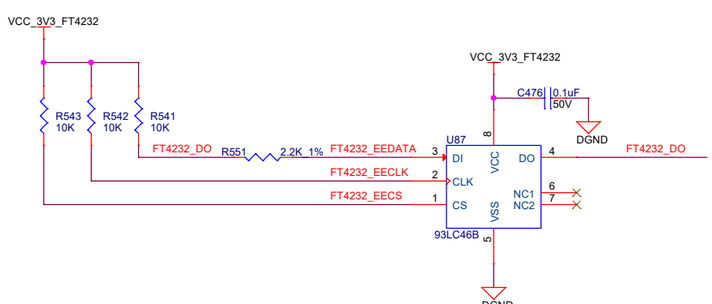




FT4232: 5V to 3.3V@500mA LDO



EEPROM



R-Note :-
Verify the implementation
with the device manufacturer

Designed for TI by Mistral Solutions Pvt Ltd

Title	FT4232 UART TO USB BRIDGE		
Size	PROC114A1(001)		Rev
C			A1
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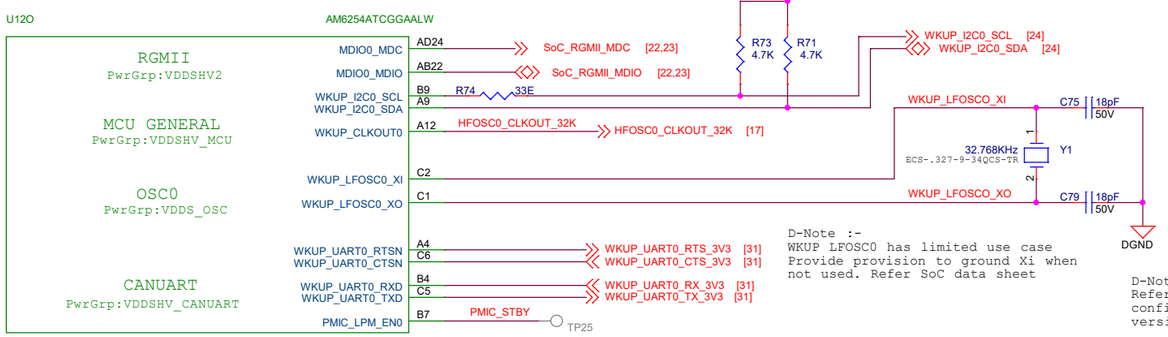
SOC WKUP DOMAIN

D-Note :-
A pullup is recommended for Open-drain output type I2C interfaces irrespective of the IO configuration. Refer pin connectivity table of SOC data sheet

D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V
An RC is recommended for slew rate control
Refer SK-AM62P-LP schematics



D-Note :-
The only LFOSC0 register bits that should be changed by the customer are BP_C, PD_C, and CTRLMMR_WKUP_LFXOSC_TRIM[18:16], where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source.The CTRLMMR_WKUP_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the Load Capacitance Equation. The load capacitance range of the crystal will be half of the recommended capacitor value range since there are connected in series with the crystals resonate circuit.

D-Note :-
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot
Shorting the bootmode pins directly to VCC or ground directly is not recommended. Connect each of the bootmode pins through separate resistor
Choose the bootmode resistor value based on the use case (10K or similar)

D-Note :-
WKUP LFOSC0 has limited use case
Provide provision to ground Xi when not used. Refer SoC data sheet

D-Note :-
Refer SoC data sheet for the recommended circuit configuration during initial prototype and the final version

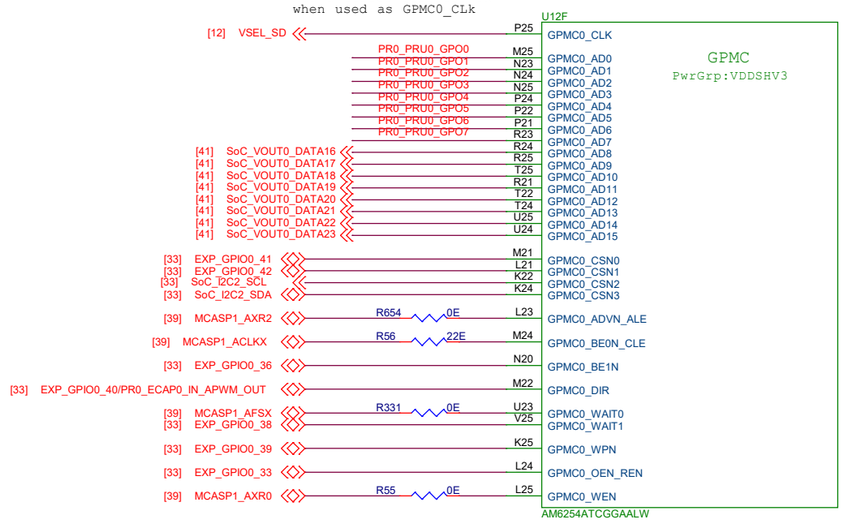
D-Note :-
Reduce the series resistor value when buffer is not used to 0R
These resistors are used to isolate the alternate function during testing

D-Note :-
WKUP_CLKOUT0 is a buffered output of the high frequency oscillator (HFOSC0) available during power-up as default.

D-Note :-
SOC IO buffers used for GPMC interface signals are disabled during reset
The required pulls for the interfaced signals are provided on the GPMC interface card

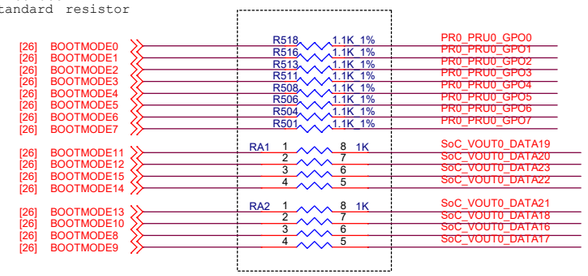
SOC GPMC INTERFACE

D-Note :-
Add a series resistor 0R when used as GPMC0_CLk



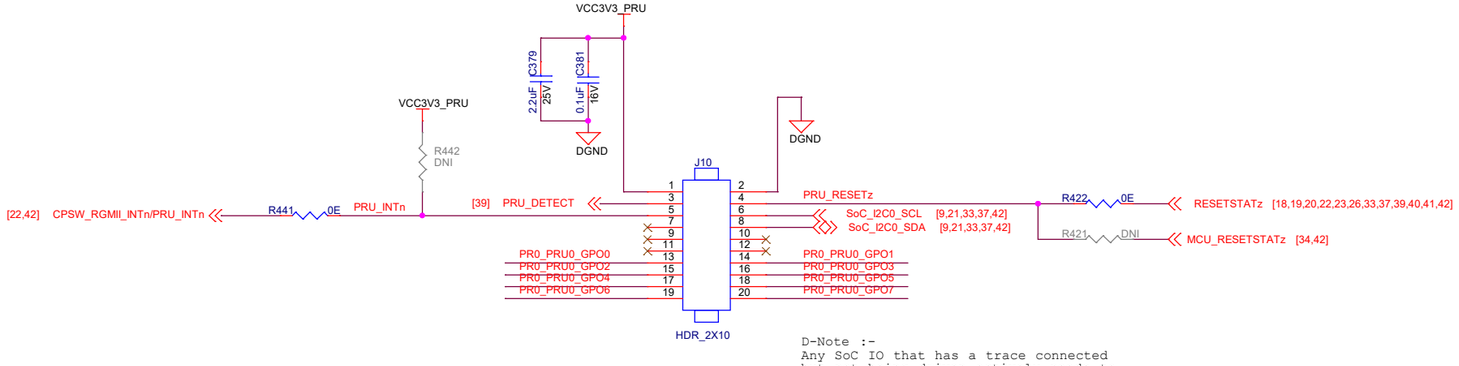
BOOTMODE PINS

D-Note :-
Ok to use 1K standard resistor



D-Note :-
Resistors are used to isolate the BOOTMODE control logic after the value is latched

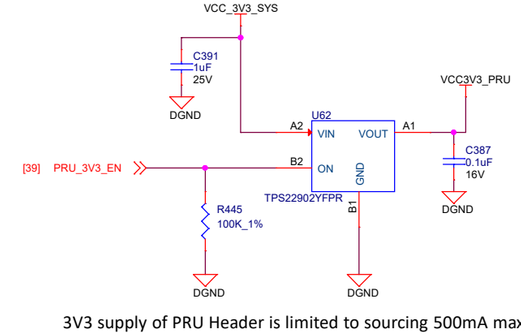
PRU HEADER



D-Note :-
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull

Silk: PRU HDR

LOAD SWITCH FOR PRU HEADER



3V3 supply of PRU Header is limited to sourcing 500mA max.

D-Note :-
Processor IOs connected to PRU Header are not fail-safe.
No external input shall be driven when when Starter Kit is not powered-up.

Designed for TI by Mistral Solutions Pvt Ltd

Title	PRU HEADER	
Size C	PROC114A1(001)	Rev A1
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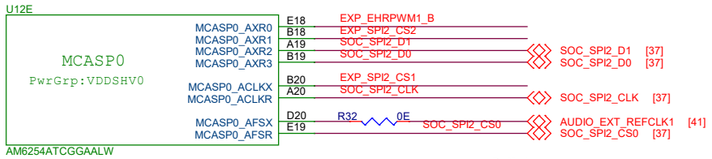
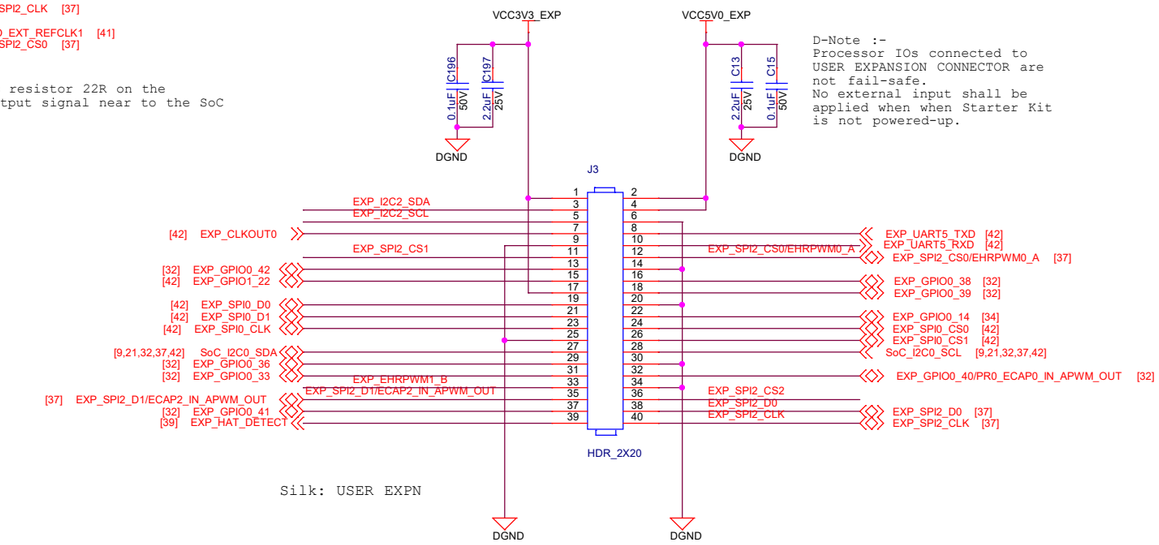
USER EXPANSION CONNECTOR



R32(Series damping resistor) should be placed close to SoC

D-Note :-
Add a series resistor 22R on the
SPI clock output signal near to the SoC

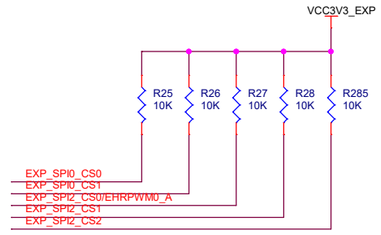
User Note :-
These supplies are off by default
The supplies are controlled by the below
load switches and needs to be enabled



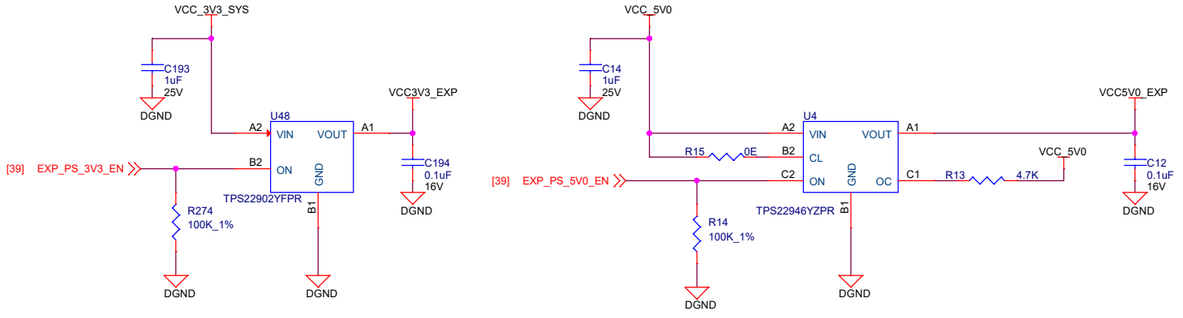
Silk: USER EXPN

D-Note :-
Processor IOs connected to
USER EXPANSION CONNECTOR are
not fail-safe.
No external input shall be
applied when when Starter Kit
is not powered-up.

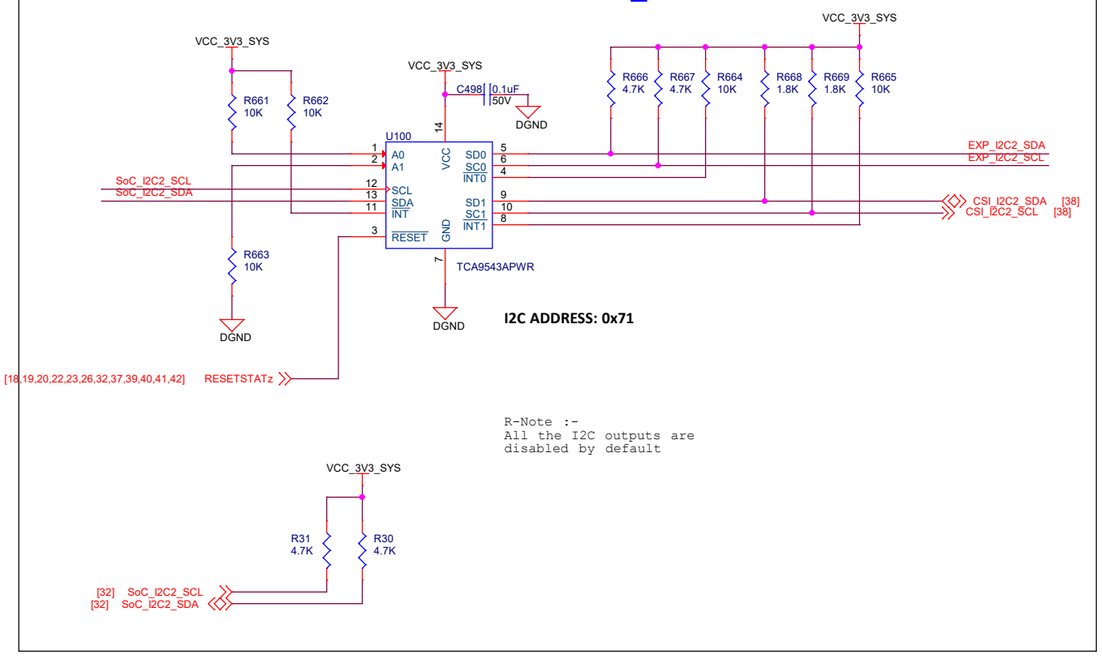
Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



LOAD SWITCHES FOR USER EXPANSION CONNECTOR



I2C SWITCH FOR SoC_I2C2



R-Note :-

AM62x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

Designed for TI by Mistral Solutions Pvt Ltd

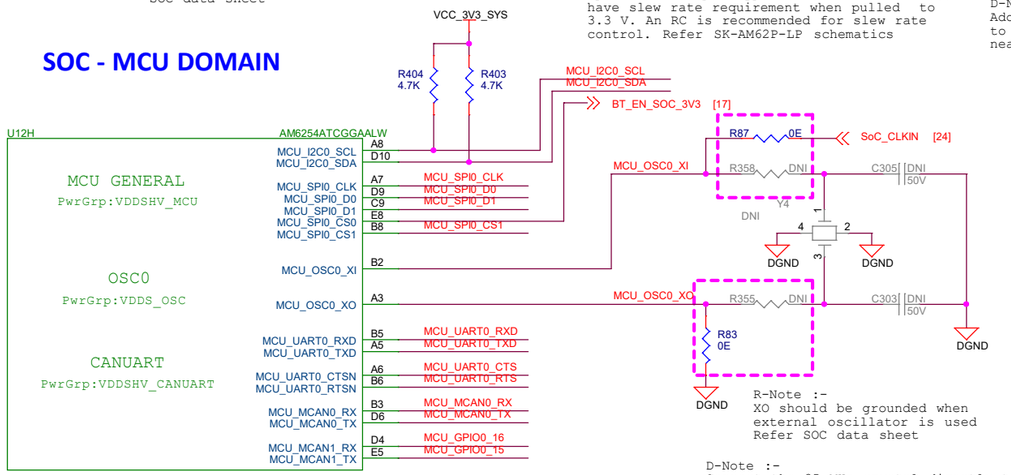
Title	USER EXPANSION CONNECTOR		
Size C	PROC114A1(001)		Rev A1
Date:	Friday, June 28, 2024	Sheet 33 of 44	

SOC - MCU DOMAIN

D-Note :-
A pullup is recommended for Open-drain output type I2C interfaces irrespective of the IO configuration. Refer pin connectivity table of SOC data sheet

D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V. An RC is recommended for slew rate control. Refer SK-AM62P-LP schematics

D-Note :-
Add a series resistor 22R to the SPI0 clock output near to the SoC



D-Note :-
No HFOSC0 registers are required to be changed. These registers should remain in their default state. Select the appropriate crystal circuit components that are compliant to the values defined in the MCU_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

D-Note :-
Refer Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:
Clock Routing Guidelines
Oscillator Routing

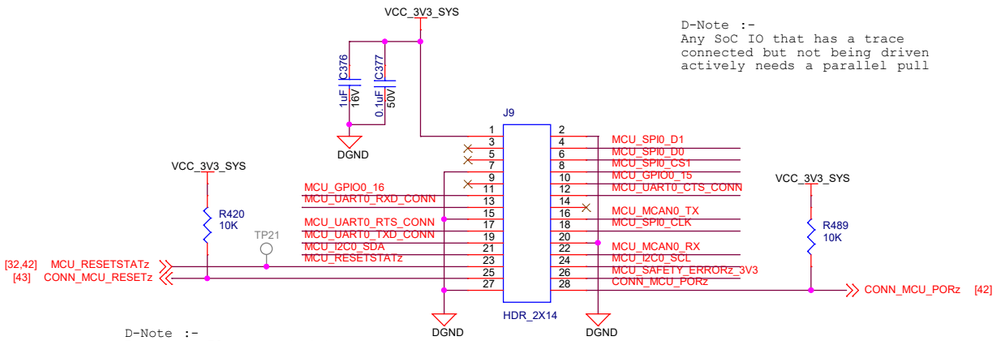
D-Note :-
MCU_OSC0 has been validated only with a 25 MHz clock source, so that is the only frequency supported. The datasheet shows MCU_OSC0 not starting until after the core voltage because there are some cases where the oscillator may not start until VDD_CORE is valid. In most cases it will start as early as VDDS_OSC0, but this may not always be the case.
This diagram in the datasheet is showing the maximum start-up time, which must include the case where the delay is based on VDD_CORE being valid.

R-Note :-
XO should be grounded when external oscillator is used
Refer SOC data sheet

D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

D-Note :-
Connect the 25 MHz crystal directly to the SOC Xi and Xo pins (No Series or parallel resistors are recommended). The internal oscillator implements AGC (Automatic Gain Control) for amplitude control. Match the SOC and the EPHY crystal specs

SOC-MCU HEADER

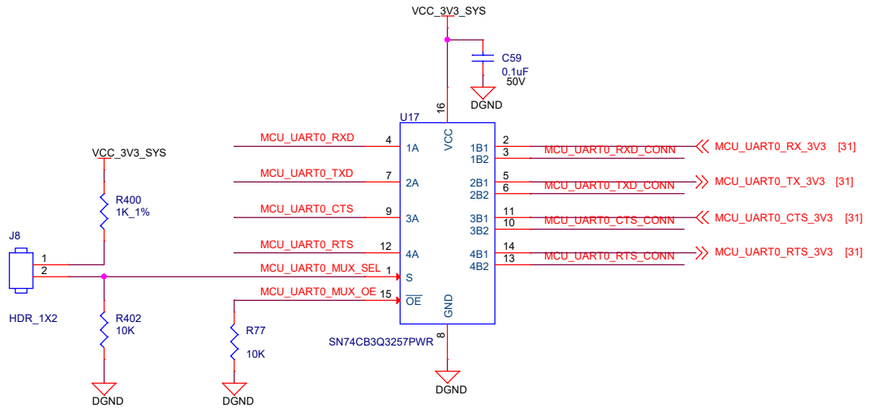


D-Note :-
Any SoC IO that has a trace connected but not being driven actively needs a parallel pull

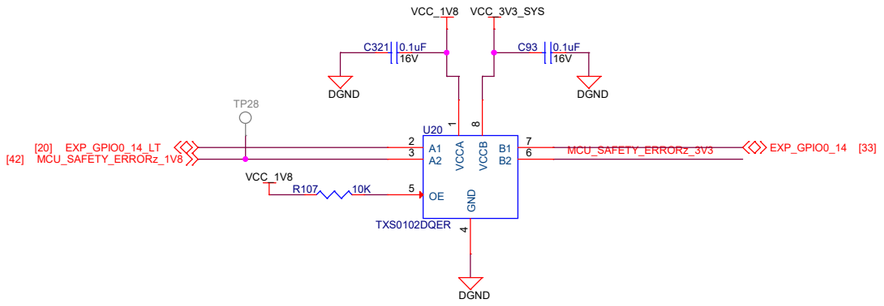
D-Note :-
Processor IOs connected to MCU expansion CONNECTOR are not fail-safe.
No external input shall be applied when when Starter Kit/EVM is not powered-up.

Silk: MCU HDR

SOC - MCU_UART0 MUX



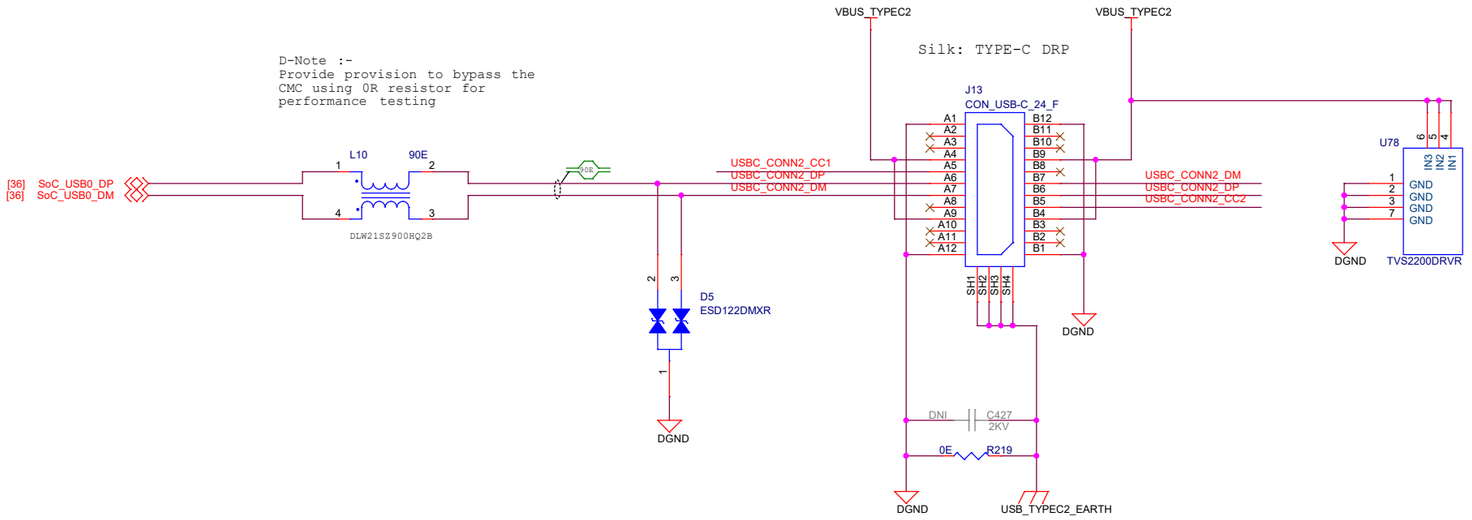
OEn	SEL	INPUT/OUTPUT An	
L	L(DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

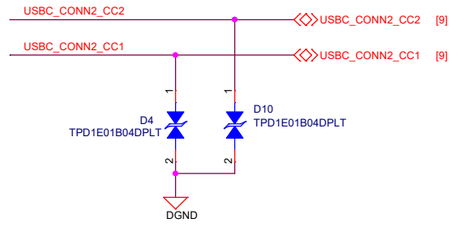


Designed for TI by Mistral Solutions Pvt Ltd

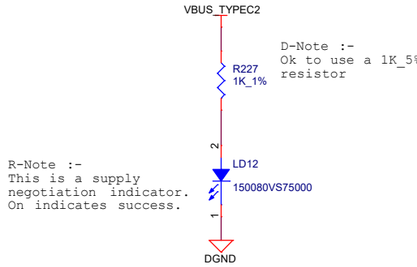
Title	MCU HEADER	
Size: C	PROC114A1(001)	Rev: A1
Date: Friday, June 28, 2024	Sheet 34 of 44	

USB0 TYPE-C DRP

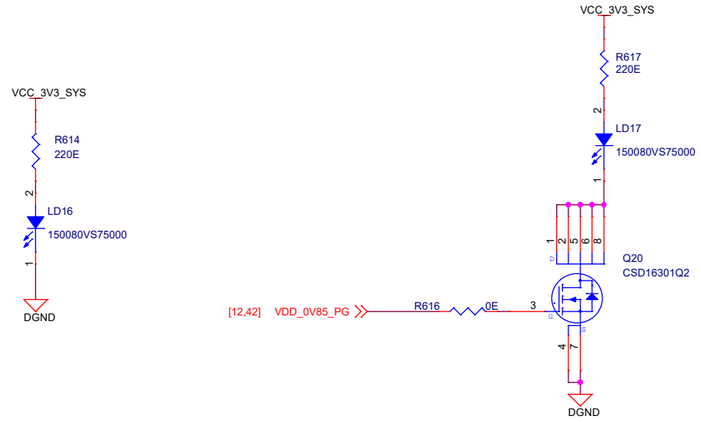




POWER INDICATION LED: VBUS_TYPEC2



POWER RAIL LEDS



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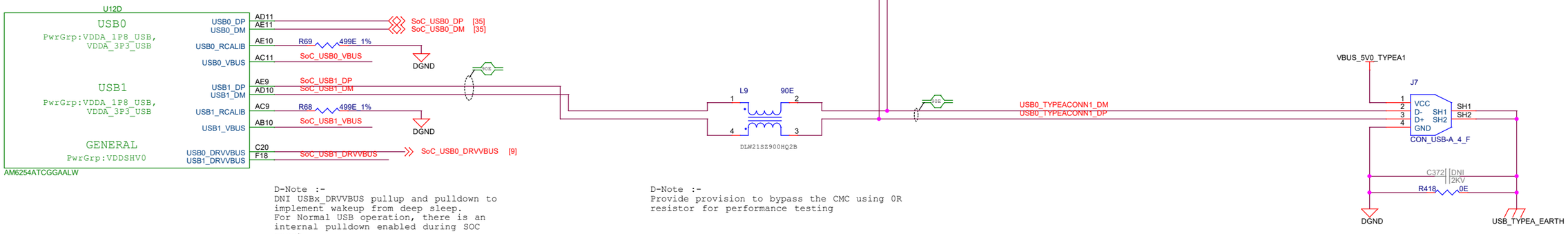
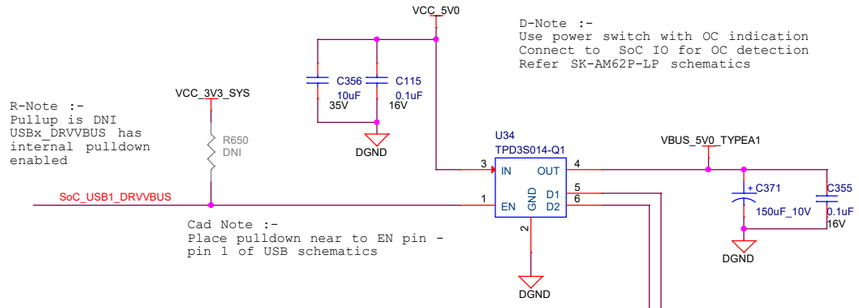
Title	USB0 TYPE-C DRP	
Size: C	PROC114A1(001)	Rev: A1
Date: Friday, June 28, 2024	Sheet 35 of 44	

USB1 TYPE-A





D-Note :-
Use power switch with OC indication
Connect to SoC IO for OC detection
Refer SK-AM62P-LP schematics

R-Note :-
Pullup is DNI
USBx_DRVVBUS has
internal pulldown
enabled

Cad Note :-
Place pulldown near to EN pin -
pin 1 of USB schematics

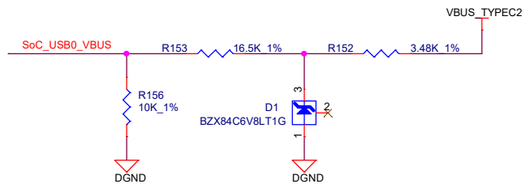
D-Note :-
DNI USBx_DRVVBUS pullup and pulldown to
implement wakeup from deep sleep.
For Normal USB operation, there is an
internal pulldown enabled during SOC
reset

D-Note :-
Provide provision to bypass the CMC using 0R
resistor for performance testing

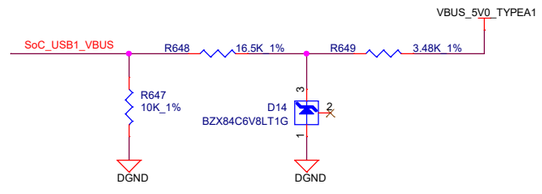
Silk: TYPE-A

D-Note :-
VBUS connection is optional for
Host configuration

D-Note :-
Refer USB VBUS Design Guidelines section of SoC data sheet



D-Note :-
Refer USB VBUS Design Guidelines section of SoC data sheet



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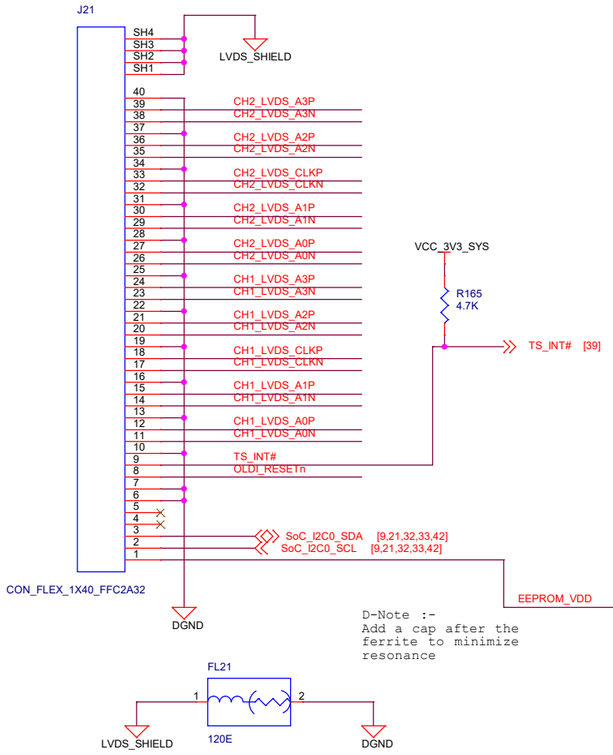
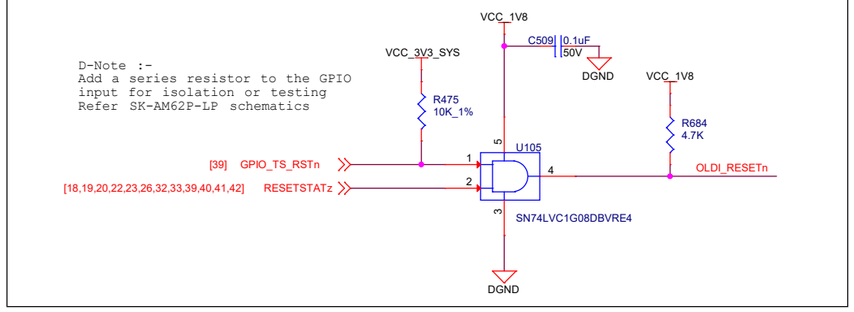
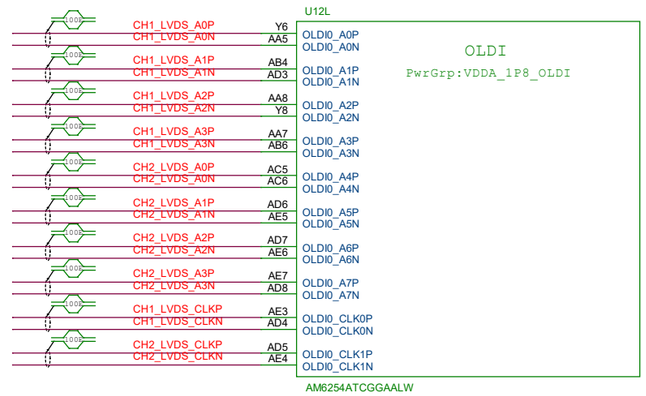
Title	USB1 TYPE-A		
Size C	PROC114A1(001)		Rev A1
Date:	Friday, June 28, 2024	Sheet 36 of 44	

OLDI DISPLAY INTERFACE

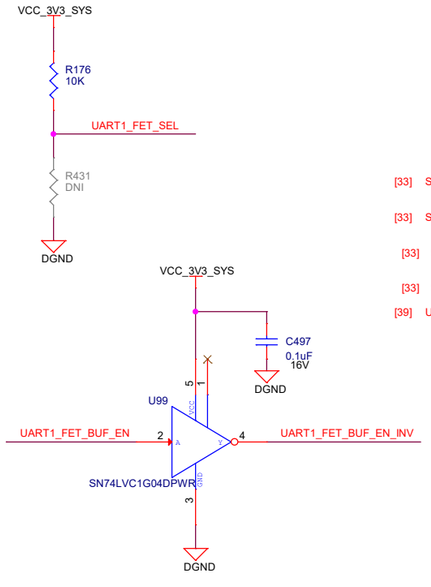


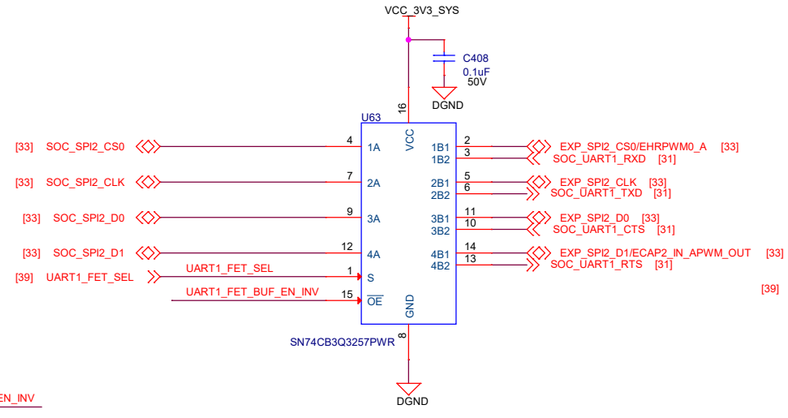
OLDI RESET

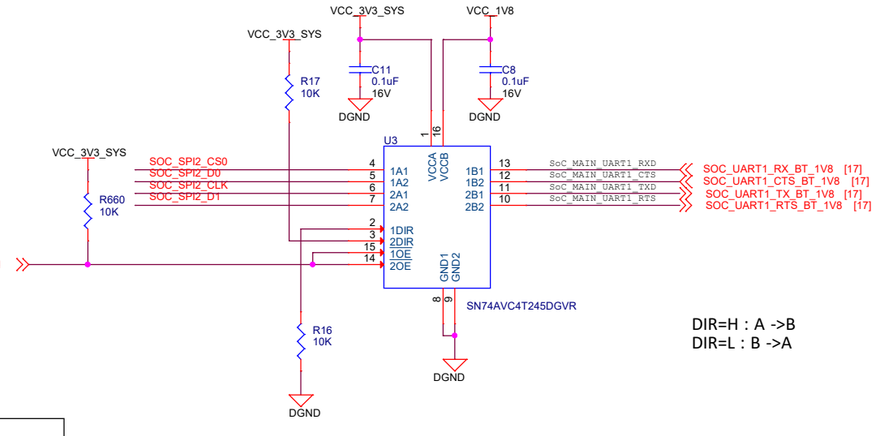




SoC UART1 FET SWITCH & BUFFER







OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	FT4232
L	L	An=nB1	User EXPANSION CONNECTOR

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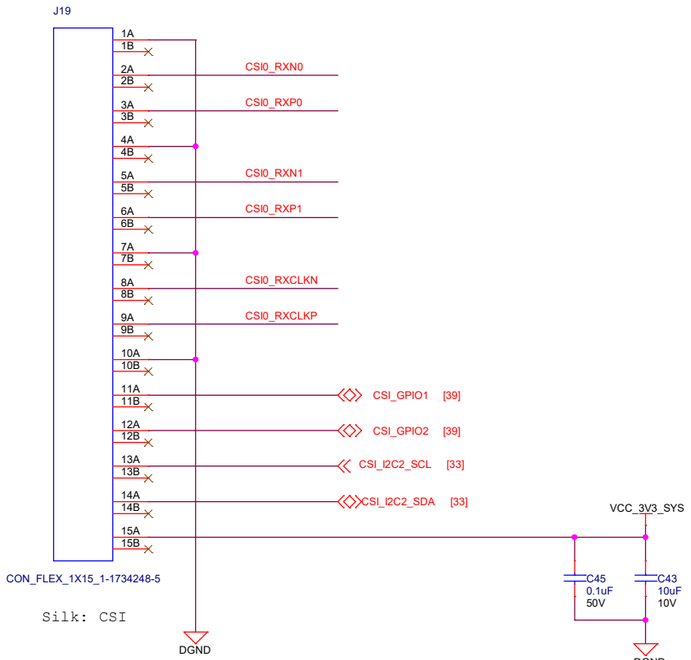
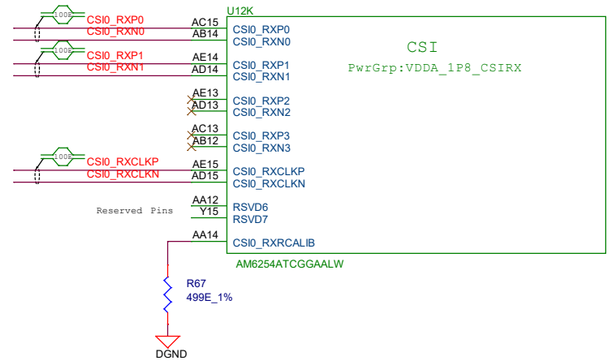
Title	OLDI DISPLAY INTERFACE	
Size C	PROC114A1(001)	Rev A1
Date: Friday, June 28, 2024	Sheet 37 of 44	

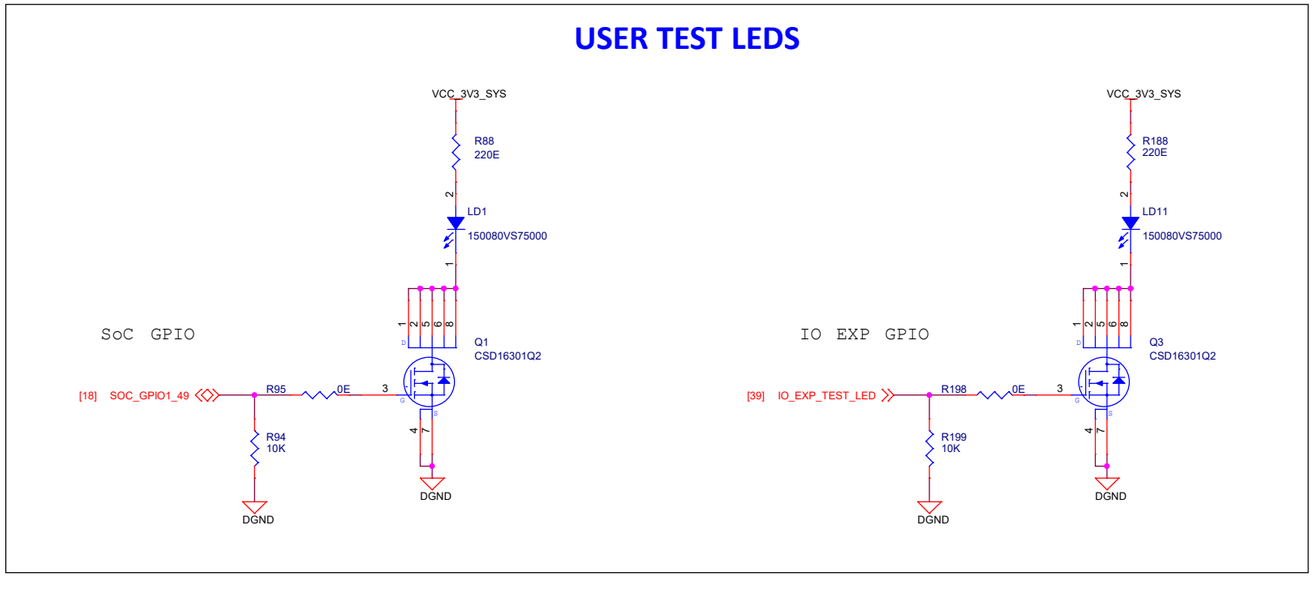
CSI INTERFACE

CSI CAMERA HEADER





USER TEST LEDS



Designed for TI by Mistral Solutions Pvt Ltd

Title	CSI INTERFACE & USER TEST LEDS	
Size C	PROC114A1(001)	Rev A1
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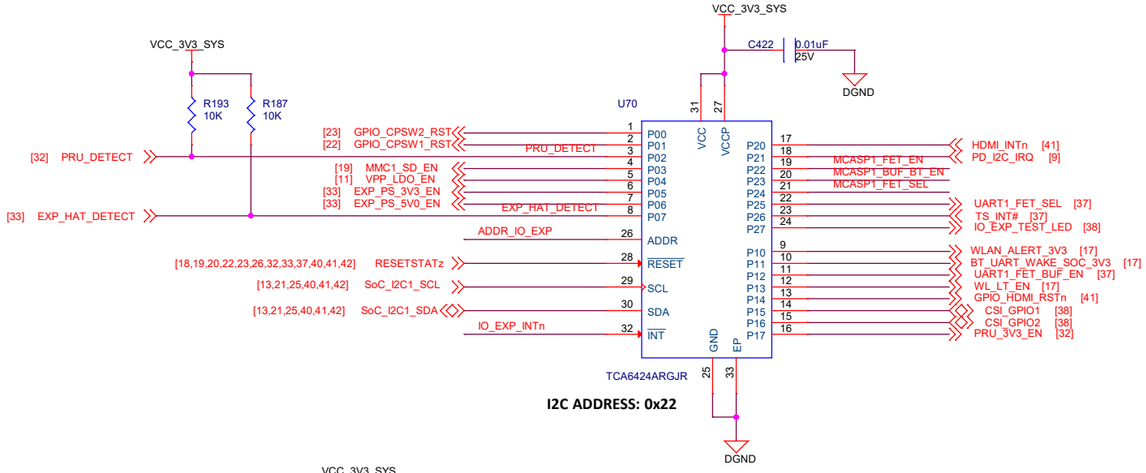
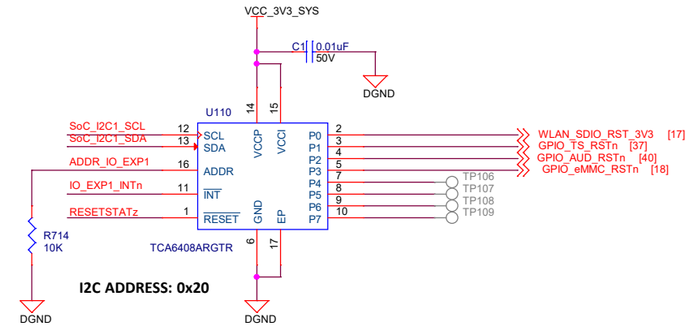
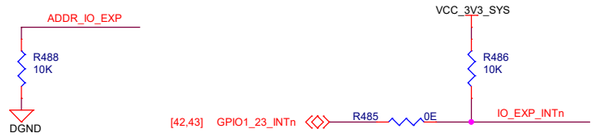
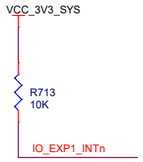
IO EXPANDER

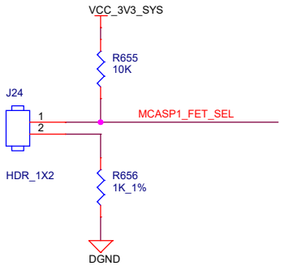


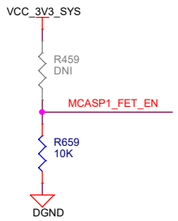


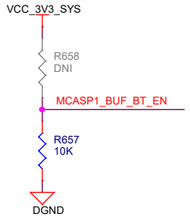


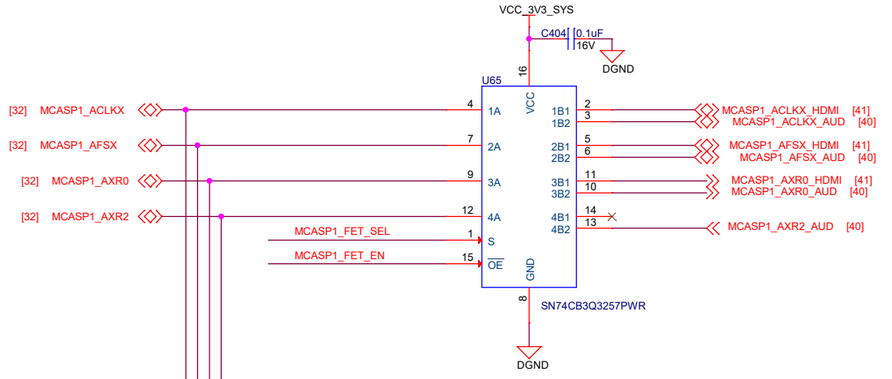


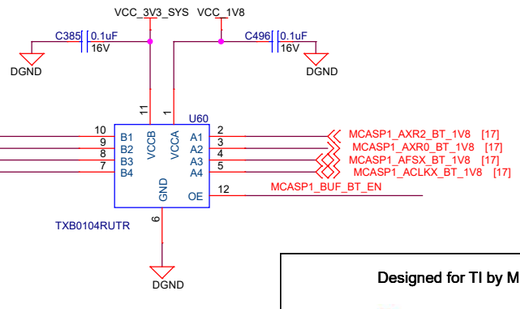
MCASP1 FET SWITCH & BUFFER











OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

Designed for TI by Mistral Solutions Pvt Ltd

Title	IO EXPANDER		
Size	PROC114A1(001)		Rev
C			A1
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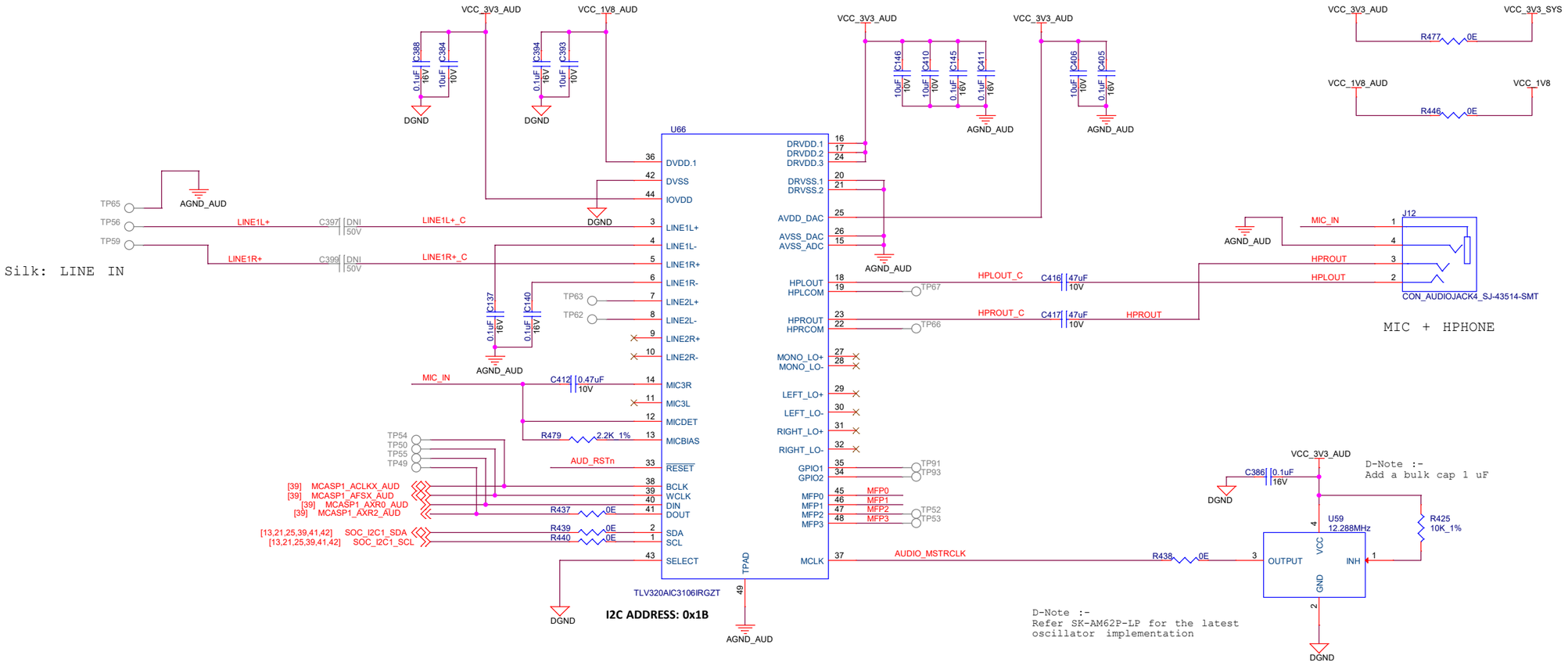
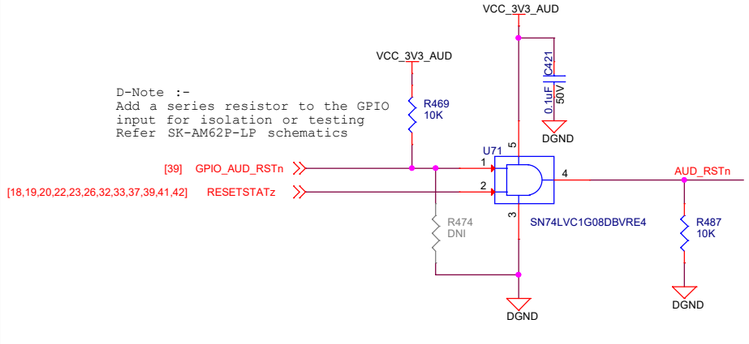
AUDIO CODEC

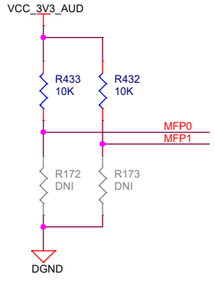


AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



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Title	AUDIO CODEC		
Size	C	PROC114A1(001)	Rev A1
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HDMI INTERFACE

U12N AM6254ATCGGAALW

VOUT0
PwrGrp:VDDSHV3

VOUT0_DATA0	U22	SoC_VOUT0_DATA0
VOUT0_DATA1	V24	SoC_VOUT0_DATA1
VOUT0_DATA2	W25	SoC_VOUT0_DATA2
VOUT0_DATA3	W24	SoC_VOUT0_DATA3
VOUT0_DATA4	Y25	SoC_VOUT0_DATA4
VOUT0_DATA5	Y24	SoC_VOUT0_DATA5
VOUT0_DATA6	Y23	SoC_VOUT0_DATA6
VOUT0_DATA7	AA25	SoC_VOUT0_DATA7
VOUT0_DATA8	V21	SoC_VOUT0_DATA8
VOUT0_DATA9	W21	SoC_VOUT0_DATA9
VOUT0_DATA10	V20	SoC_VOUT0_DATA10
VOUT0_DATA11	AA23	SoC_VOUT0_DATA11
VOUT0_DATA12	AB25	SoC_VOUT0_DATA12
VOUT0_DATA13	AA24	SoC_VOUT0_DATA13
VOUT0_DATA14	Y22	SoC_VOUT0_DATA14
VOUT0_DATA15	AA21	SoC_VOUT0_DATA15
VOUT0_PCLK	AC24	SoC_VOUT0_PCLK
VOUT0_DE	Y20	SoC_VOUT0_DE
VOUT0_VSYNC	AC25	SoC_VOUT0_VSYNC
VOUT0_HSYNC	AB24	SoC_VOUT0_HSYNC

SoC_VOUT0_PCLK — R60 0E — HDMI_PCLK

D-Note :-
Refer SK-AM62P-LP for the latest
oscillator implementation

D-Note :-
Add a bulk cap

VCC_3V3_SYS — C20 0.1uF 16V — DGND

R41 10K_1%

U7 12.288MHz
VCC, INH, OUTPUT, GND
1 — 3 — 4 — 2

DGND

R-Note :-
M_CLK is not used

R34 DNI

[33] AUDIO_EXT_REFCLK1

Cad Note :-
Move the net after the 0R and
add a 0R to choose the required
configuration

VDD_1V2 — FB3 300E — VHDMI_AVCC_1V2
C232 22uF 10V — DGND
C230 10uF 10V, C231 0.1uF 16V, C229 0.1uF 16V — DGND

VHDMI_CVCC_1V2 — FB2 300E — VDD_1V2
C213, C209, C200, C207, C225, C217: 0.1uF 16V — DGND
C201 10uF 10V — DGND

VHDMI_IOVCC_3V3 — FB1 300E — VCC_3V3_SYS
C223 0.1uF 16V, C212 0.1uF 16V, C199 10uF 10V — DGND
C204 10uF 10V — DGND

D-Note :-
Add an additional decap

VHDMI_IOVCC_3V3 — R61 4.7K

[13,21,25,39,40,42] SoC_I2C1_SCL
[13,21,25,39,40,42] SoC_I2C1_SDA

HDMI_RSTn
HDMI_PCLK

SoC_VOUT0_DATA0 … SoC_VOUT0_DATA23 [32]

SoC_VOUT0_HSYNC
SoC_VOUT0_VSYNC
SoC_VOUT0_DE

HDMI_MSTRCLK
[39] MCASP1_ACLKX_HDMI
[39] MCASP1_AFSX_HDMI

U10 Sil9022ACNU

CSCL	1	
CSDA	2	
CI2CA	72	
RESET#	51	HDMI_RSTn
IDCK	22	HDMI_PCLK
D0 … D23	32 … 13	SoC_VOUT0_DATA0 … SoC_VOUT0_DATA23
HSYNC	34	SoC_VOUT0_HSYNC
VSYNC	35	SoC_VOUT0_VSYNC
DE	33	SoC_VOUT0_DE
SPDIF	36	
MCLK	38	HDMI_MSTRCLK
SCK	45	MCASP1_ACLKX_HDMI
WS	44	MCASP1_AFSX_HDMI
AVCC12_1, AVCC12_2	60, 66	VHDMI_CVCC_1V2
CVCC12_1 … CVCC12_6	5, 12, 28, 42, 47, 53	VHDMI_CVCC_1V2
IOVCC1, IOVCC2, IOVCC3	3, 21, 46	VHDMI_IOVCC_3V3
DSDA	48	HDMI_I2C_SDA
DSCL	49	HDMI_I2C_SCL
INT	52	HDMI_INTn [39]
HPD	54	HDMI_HPD
EXT_SWING	56	HDMI_EXTSWING
TXC+, TXC-	59, 58	HDMI_CLK+, HDMI_CLK-
TX0+, TX0-	62, 61	HDMI_TX0+, HDMI_TX0-
TX1+, TX1-	65, 64	HDMI_TX1+, HDMI_TX1-
TX2+, TX2-	68, 67	HDMI_TX2+, HDMI_TX2-
CEC_A	71	HDMI_CEC
CEC_D	50	HDMI_CEC_D
RSVDL	55	
IO_SEL	69	R62 0E — DGND
VDDQ	70	
SD0, SD1, SD2, SD3	41, 40, 39, 37	MCASP1_AXR0_HDMI [39]; HDMI_AUDD1, HDMI_AUDD2, HDMI_AUDD3
IOGND, CGND, AGND, PAD	57, 43, 63, 73	DGND

VHDMI_IOVCC_3V3 — R316 DNI, R323 DNI, R325 10K

R287 0E — DGND

R327 7.5K — DGND
R326 DNI — DGND

TP18, TP16, TP14, TP88

I2C ADDRESS: 0x3B, 0x3F, 0x62

D-Note :-
REXT_SWING modified to 7.5K_5%
Value changed for internal testing
(Radiated Emission)
Refer device data sheet for the
recommended value

D-Note :-
Add bulk caps

HDMI ESD DEVICE

VCC_3V3_SYS — C248 10uF 10V — DGND
VCC_5V0 — C219 10uF 10V — DGND
VCC_3V3_SYS — R314 0E
VCC_5V0_HDMICONN — C211 10uF 10V — DGND

U50 TPD12S016PWR

HDMI_TX0+	18	D0+
HDMI_TX0-	17	D0-
HDMI_TX1+	21	D1+
HDMI_TX1-	20	D1-
HDMI_TX2+	23	D2+
HDMI_TX2-	22	D2-
HDMI_CLK+	16	CLK+
HDMI_CLK-	15	CLK-
HDMI_CONN_I2CSCL	8	SCL_B
HDMI_CONN_I2CSDA	9	SDA_B
HDMICONN_HPD	10	HPD_B
HDMI_CONNCEC	7	CEC_B
VCCA	24	
VCC5V	11	
5V_OUT	13	
CT_HPD	12	
LS_OE	5	
SCL_A	2	HDMI_I2C_SCL
SDA_A	3	HDMI_I2C_SDA
HPD_A	4	HDMI_HPD
CEC_A	1	HDMI_CEC
GND1, GND2, GND3	6, 14, 19	DGND

R-Note :-
TPD12S016PWR has integrated pullup or pulldown resistors on the
I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR

J5 CON_HDMI_1X19_F

HDMI_TX2+	1
HDMI_TX2-	3
HDMI_TX1+	4
HDMI_TX1-	6
HDMI_TX0+	7
HDMI_TX0-	9
HDMI_CLK+	10
HDMI_CLK-	12
HDMI_CONNCEC	13
HDMI_CONN_I2CSCL	15
HDMI_CONN_I2CSDA	16
VCC_5V0_HDMICONN	18
HDMICONN_HPD	19
2, 5, 8, 11, 14, 17	DGND
20, 21, 22, 23	DGND

FL17 120E — DGND, HDMI_EARTH

Silk: HDMI

HDMI RESET

D-Note :-
Add a series resistor to the GPIO
input for isolation or testing
Refer SK-AM62P-LP schematics

VCC_3V3_SYS — R389 10K
VCC_3V3_SYS — C323 0.1uF 50V — DGND

U54 SN74LVC1G08DBVRE4

[39] GPIO_HDMI_RSTz	1	
[18,19,20,22,23,26,32,33,37,39,40,42] RESETSTATz	2	
	3	R390 DNI
	4	HDMI_RSTn
	5	

R373 10K — DGND

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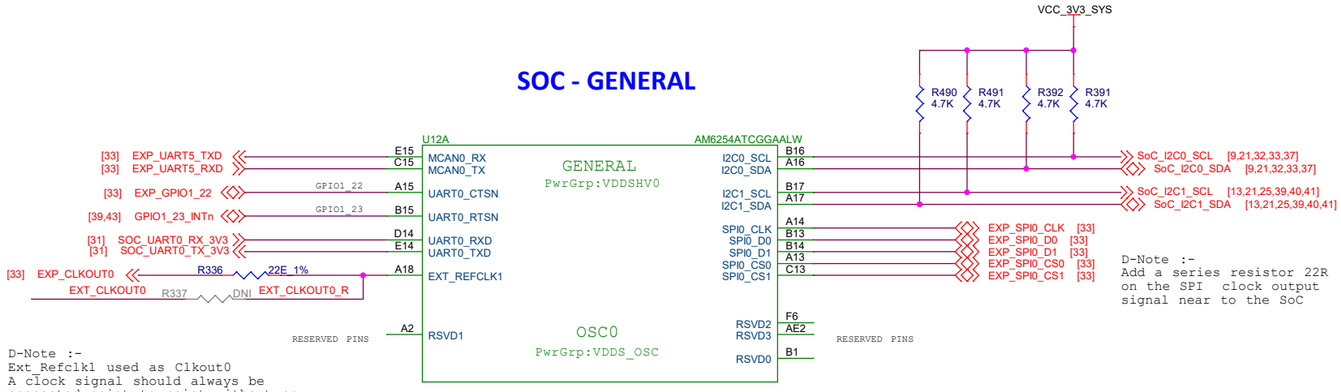
Title	HDMI INTERFACE	
Size C	PROC114A1(001)	Rev A1
Date: Friday, June 28, 2024	Sheet 41 of 44	

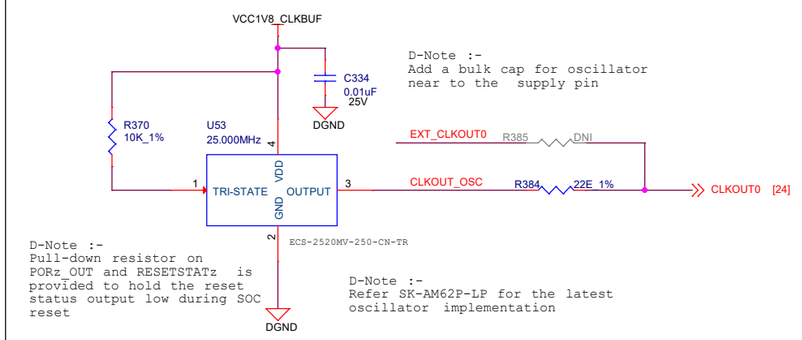
SOC - GENERAL



D-Note :-
Add a series resistor 22R on the SPI clock output signal near to the SoC

D-Note :-
Ext_Refclk1 used as Clkout0
A clock signal should always be connected point to point without any branches. When connecting Clkout0 to more than one (multiple) clock inputs, use a buffer with one input and multiple outputs.

OSCILLATOR



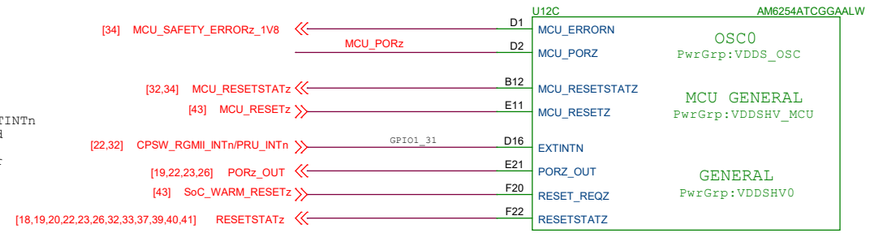
D-Note :-
Add a bulk cap for oscillator near to the supply pin

D-Note :-
Pull-down resistor on PORz_OUT and RESETSTATz is provided to hold the reset status output low during SOC reset

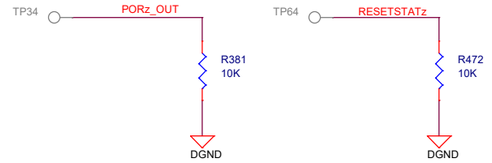
D-Note :-
Refer SK-AM62P-LP for the latest oscillator implementation

D-Note :-
Provision for a pulldown. Populate when attached device is connected. Refer SOC data sheet pin connectivity requirements

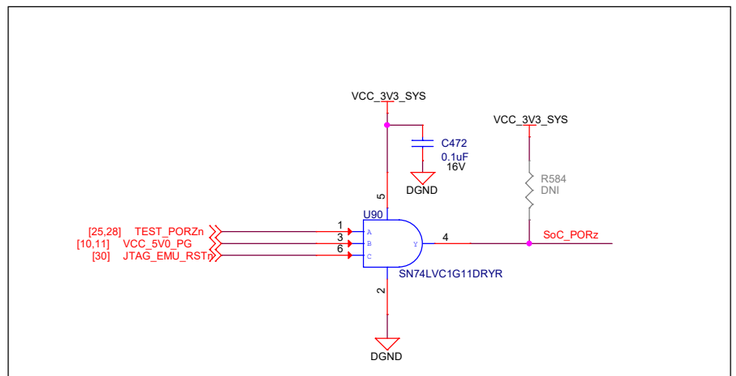
SOC - RESET

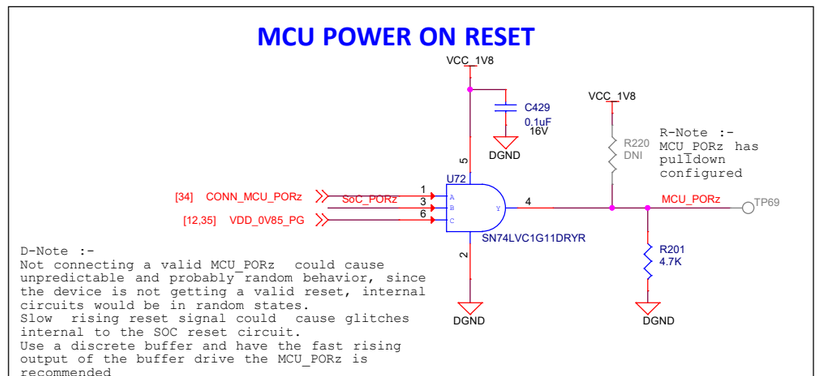


D-Note :-
Open drain output type IO EXTINTn has slew rate limit specified when pulled to 3.3V supply. Add an RC at the input. Refer TMDS64EVM.



D-Note :-
Pull-down resistor on PORz_OUT and RESETSTATz is provided to hold the attached device in reset condition during SOC reset and power-up





D-Note :-
Not connecting a valid MCU_PORz could cause unpredictable and probably random behavior, since the device is not getting a valid reset, internal circuits would be in random states.
Slow rising reset signal could cause glitches internal to the SOC reset circuit.
Use a discrete buffer and have the fast rising output of the buffer drive the MCU_PORz is recommended

D-Note :-
It is recommended to connect the output from logic gate or discrete buffer (with fast rise time) as MCU_PORz input rather than slow rising open drain output (could glitch internally).

D-Note :-
A delay circuit recommended in the below section of the data sheet may be required when crystal is used as clock source
MCU_PORz Timing Requirements

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Title	OSCILLATOR	
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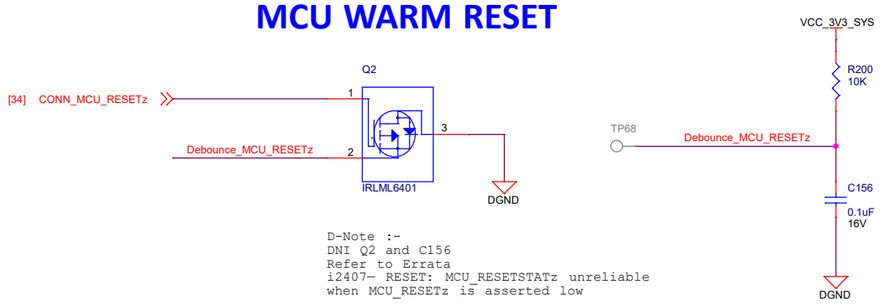
EXTERNAL RESET INPUT AND SCHMITT TRIGGER DEBOUNCE LOGIC

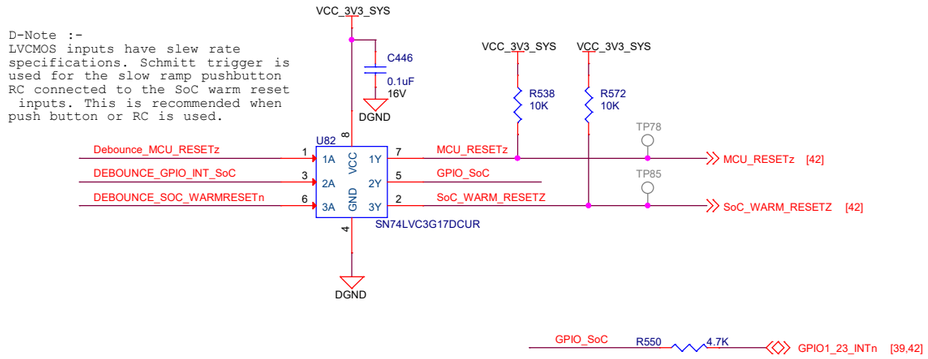
MCU WARM RESET



D-Note :-
DNI Q2 and C156
Refer to Errata
i2407– RESET: MCU_RESETSTATz unreliable
when MCU_RESETz is asserted low

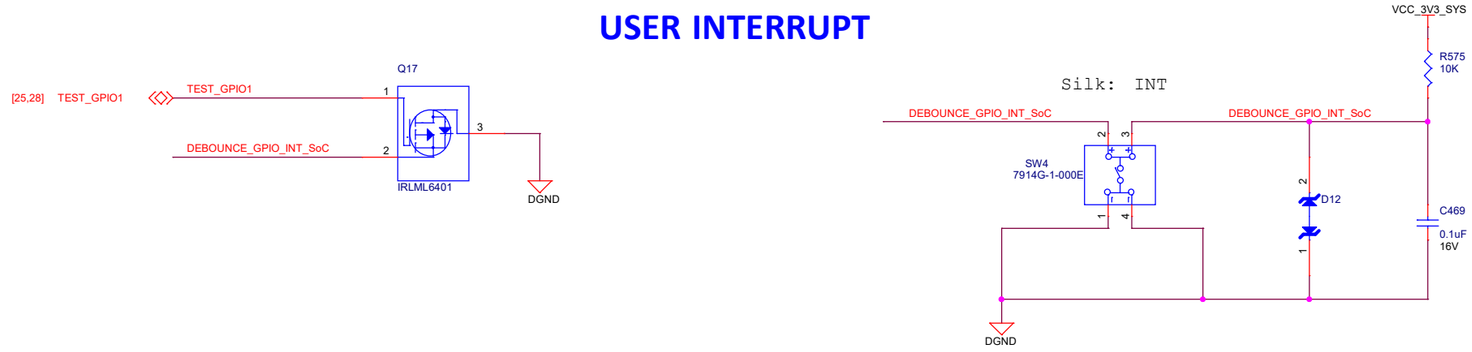
DEBOUNCE CIRCUIT

D-Note :-
LVCMOS inputs have slew rate specifications. Schmitt trigger is used for the slow ramp pushbutton RC connected to the SoC warm reset inputs. This is recommended when push button or RC is used.



SOC WARM RESET

USER INTERRUPT



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Title	RESET	
Size	PROC114A1(001)	Rev
C		A1
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MOUNTING HARDWARE

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and
packed securely before shipment.

BARE PCB

PROC114

PROC114E1

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

LABELS

Board Serial No.

LBL1
PCB LABEL
DNI

Assembly Revision

LBL2
PCB LABEL
DNI

STANDOFF,SCREW & WASHER FOR PCIe M.2

ACC1
9774015243R

MH1
FLAT WASHER_M2
3356

MH2
PAN HEAD_M2 X 5
MPMS 002 0005 PH

FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

ORDERABLE PART NO

LBL3
PCB LABEL
DNI

Oderable Part Number	
Variant	**Label Text**
001	SK-AM62
002	SK-AM62B

R-Note :-
Refer STRAP CONFIGURATION OF ETHERNET PHYS page from SK-AM64B schematics

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TEXAS INSTRUMENTS
MISTRAL

Title	HARDWARE SCHEMATICS	
Size: C	PROC114A1(001)	Rev: A1
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