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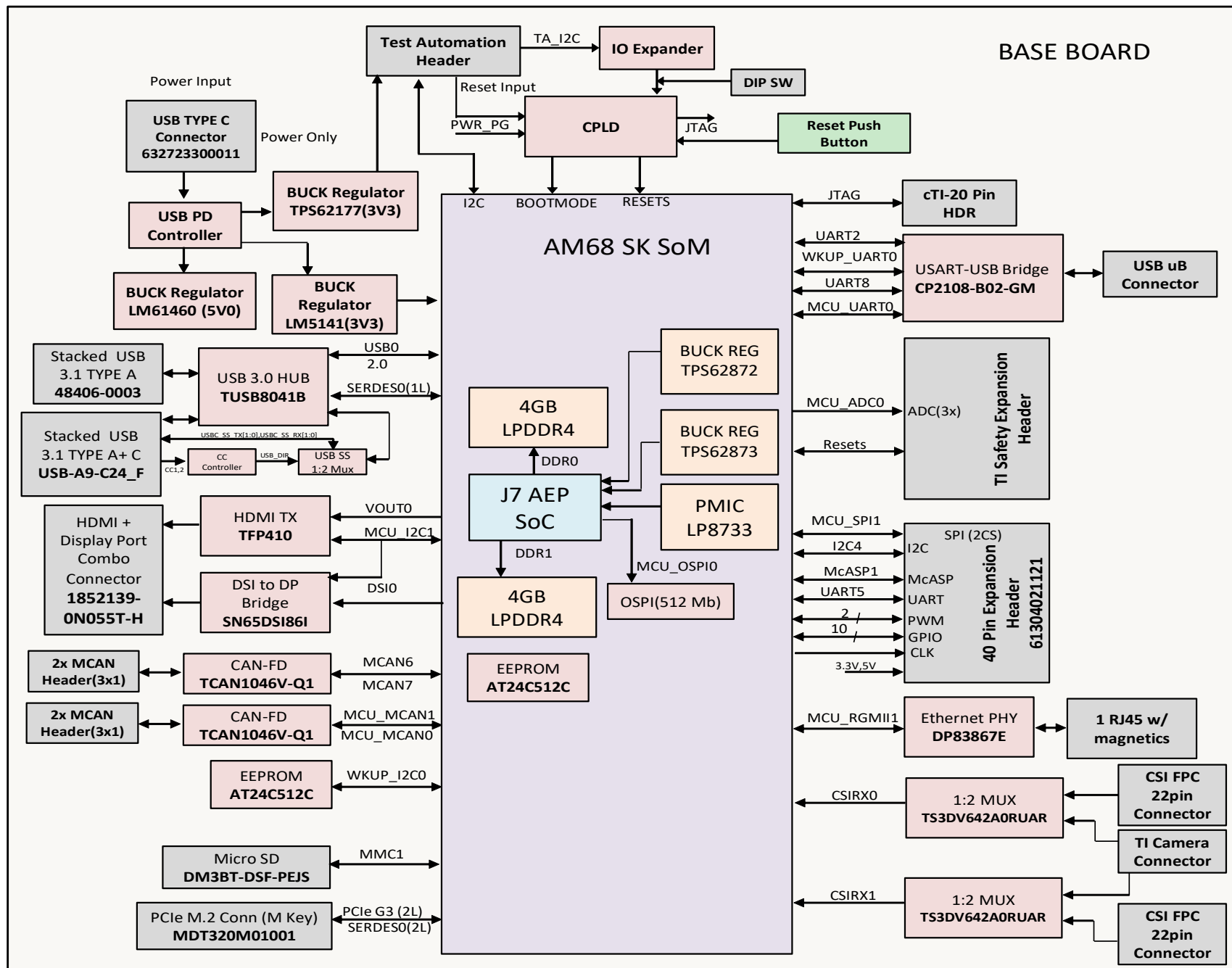
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## REVISION HISTORY

| REV # | DATE        | DESCRIPTION OF CHANGES                                                                                                                                                                   | AUTHOR              | REVIEWED BY | APPROVED BY |
|-------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-------------|-------------|
| E1    | 12-OCT-2021 | Initial Draft                                                                                                                                                                            | Mistral Design Team |             |             |
|       | 03-NOV-2021 | Updated for GPIO Assignment given by TI                                                                                                                                                  | Mistral Design Team |             |             |
|       | 09-NOV-2021 | Updated for Power pins and rearranged signal pins in sodimm connector<br>Changed C1163 to 100uF and removed C1162                                                                        | Mistral Design Team |             |             |
|       | 11-NOV-2021 | Updated variant list and added GND test points                                                                                                                                           | Mistral Design Team |             |             |
|       | 16-NOV-2021 | Updated to latest PDN v0.4                                                                                                                                                               | Mistral Design Team |             |             |
|       | 18-NOV-2021 | Swapped CSI signals on DIMM connector for routing ease<br>Updated GPIO mapping table                                                                                                     | Mistral Design Team |             |             |
|       | 24-NOV-2021 | Moved VSYS_IO_3V3 INA to Base board<br>Changed Board ID EEPROM to AT24C512C-MAHM-T device<br>Swapped SODIMM connectors for routing ease                                                  | Mistral Design Team |             |             |
|       | 29-NOV-2021 | Added Mounting hole                                                                                                                                                                      | Mistral Design Team |             |             |
|       | 1-DEC-2021  | Updated Tripad capacitors footprint<br>Updated VSYS_IO_3V3 supply connection                                                                                                             | Mistral Design Team |             |             |
|       | 1-DEC-2021  | Changed U12 to TXS0102<br>Changed R119 to 10K                                                                                                                                            | Mistral Design Team |             |             |
|       | 5-AUG-2022  | Changed U12 to TXS0102                                                                                                                                                                   | Mistral Design Team |             |             |
|       | 10-AUG-2022 | Updated SoC symbol                                                                                                                                                                       | Mistral Design Team |             |             |
|       | 17-AUG-2022 | DNI'd capacitors C67,C365, C351<br>Changed pin assignment for VDD_SD_DV                                                                                                                  | Mistral Design Team |             |             |
|       | 19-AUG-2022 | Removed TP16                                                                                                                                                                             | Mistral Design Team |             |             |
|       | 24-AUG-2022 | Updated PMIC part number                                                                                                                                                                 | Mistral Design Team |             |             |
|       | 29-AUG-2022 | Updated block diagrams<br>Updated DDR part number to MT53E2G32D4DE-046 AUT:C                                                                                                             | Mistral Design Team |             |             |
|       | 29-AUG-2022 | Updated for TI review comments                                                                                                                                                           | Mistral Design Team |             |             |
|       | 12-SEP-2022 | Updated murata capacitors part numbers                                                                                                                                                   | Mistral Design Team |             |             |
|       | 04-OCT-2022 | Updated Title block and board name                                                                                                                                                       | Mistral Design Team |             |             |
| E1A   | 16-JAN-2023 | Updated schematic revision to E1A for HS SOC build<br>Updated SOC symbol to XJ721S25AALZ<br>Changed resistor R119 to 1K ( Pull up resistor for PORz)                                     | Mistral Design Team |             |             |
| E2    | 19-JAN-2023 | Updated schematic revision to E2<br>Updated FL7 & FL13 to BLM21SP111BH1D<br>Changed C53, C54, C232, C33 to 47uF<br>Changed C45, C174 to GCM32ED70G107MEC4<br>and deleted caps C44 & C176 | Mistral Design Team |             |             |
|       | 31-JAN-2023 | Changed 0.01uF cap from C0402C103K5RACTU to GCM155R71H103KA55D                                                                                                                           | Mistral Design Team |             |             |
|       | 06-FEB-2023 | Added fan assembly components and assembled Baseboard as accessories                                                                                                                     | Mistral Design Team |             |             |
|       | 27-MAR-2023 | Changed C5, C6, 127 & 128 to 47uF - GCM31CD70G476ME02<br>Removed C39, C390 & C391                                                                                                        | Mistral Design Team |             |             |
| E2A   | 07-AUG-2025 | Updated SCH pgs 4, 16 & 18 to add PDN mapping notes for new product designs for improved SoC pwr seq.                                                                                    | TI EVM Team         |             |             |

|                                                            |  |                           |  |                           |         |
|------------------------------------------------------------|--|---------------------------|--|---------------------------|---------|
| Project :<br><div style="text-align: center;">J7 EVM</div> |  |                           |  | Title<br>REVISION HISTORY |         |
| Size                                                       |  | <Core Design>             |  |                           | Rev     |
| C                                                          |  |                           |  |                           | E2A     |
| Date:                                                      |  | Thursday, August 07, 2025 |  | Sheet                     | 2 of 21 |

# SYSTEM BLOCK DIAGRAM



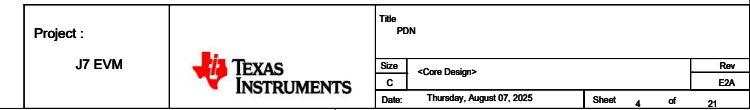
NOTE: New designs should apply following SCH & PCB updates for improved power sequencing. An updated PDN-6H v0.1.1 diag is available in source zip file to show these updates. There are no SoC reliability concerns for designs released using original PDN power mapping.

1. SoC's VDD\_MCU and VDD\_MCU\_WAKE1 should be supplied by VDD\_CORE\_0V8 power rail.
- a. MCU (1.1A) + VDD\_CORE (12.3A) = 13.4A peak load, maintaining +10.5 margin on power rail.
2. SoC's VDDAR\_MCU, VDDAR\_CPU and VDDAR\_CORE input supplies should continue to be sourced from LP8733's Buck0.

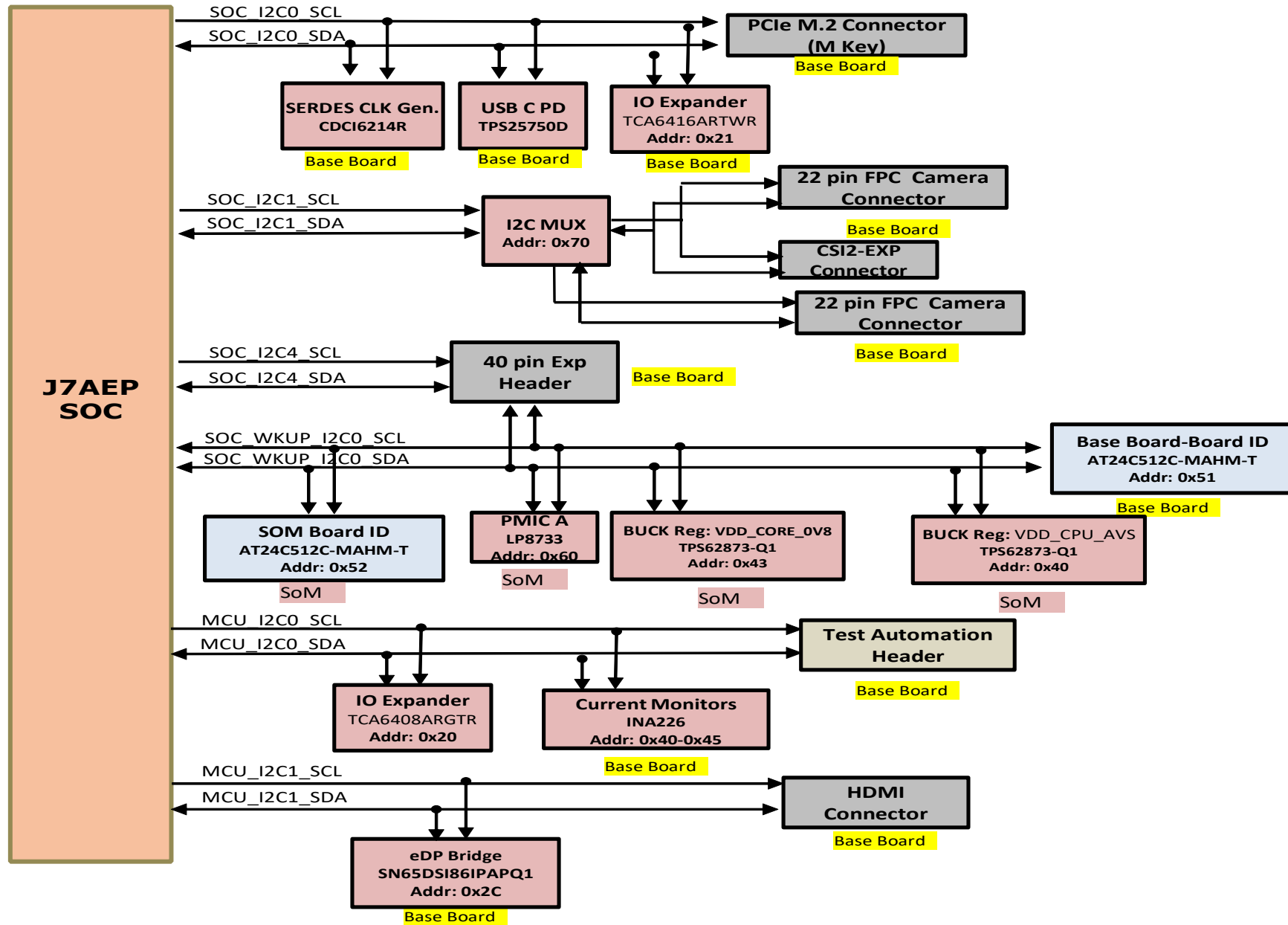
Flex PMIC, PN LP87334ERHDR-Q1 (TI OTP ID = 4E)  
Tulip Buck, PN TPS62873Y1QWRXSR  
Tulip Buck, PN TPS62872Y1QWRXSR

1. J721S2 Superset Use-Case Performance with 2.0GHz clock and Peak Power est.
2. Supports J721S2 Junction Temperature (Tj) up to 105C
3. 32Gb LPDDR4 Memory, Dual 32b Interfaces at 4266MT/s
4. Supports both 3.3V and 1.8V digital IO

- 5. Includes capacity on IO rails to support variety of peripherals (xSPI Flash, eMMC, etc)
- 6. Supports UHS-I compliant SD cards (Dual-Voltage IO)
- 7. High Secure/Field Securable Device Support
- 8. No Low/Partial Power Modes Support (MCU-only, Retention, etc)



# SoM I2C TREE DIAGRAM



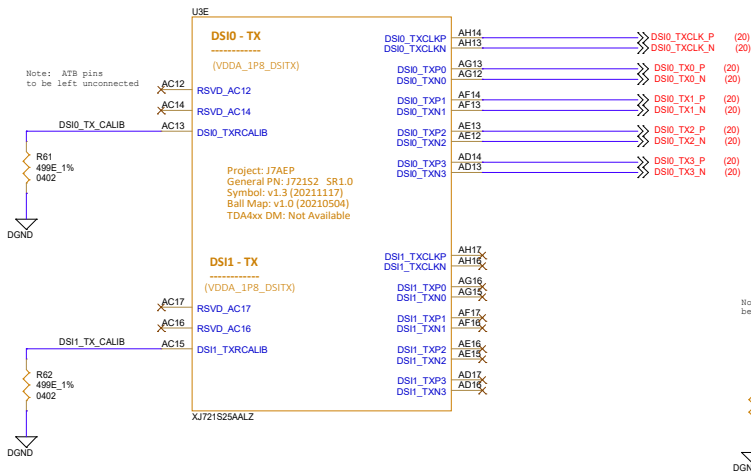
## SoM I2C ADDRESS TABLE

| Board   | Interface name           | Part#                 | Address                       | J7AEP Port mapping |
|---------|--------------------------|-----------------------|-------------------------------|--------------------|
| EVM/SoM | Board ID EEPROM          | CAV24C256WE-GT3       | 0x51                          | WKUP_I2C0          |
| EVM/CPB | Board ID EEPROM          | AT24C512C-MAHM-T      | 0x52                          |                    |
| EVM/CPB | 40 pin Expansion Header  |                       |                               |                    |
| EVM/SoM | PMIC and BUCK's          | PMIC A: LP7733        | 0x60                          |                    |
|         |                          | BUCK: TPS62873        | 0x40                          |                    |
|         |                          | BUCK: TPS62873        | 0x43                          |                    |
| EVM/CPB | 16 bit I2C GPIO Expander | TCA6424ARGJR          | 0X21                          | Main I2C0          |
| EVM/CPB | SerDes Clock gen         | CDCI6214              | Optional                      |                    |
| EVM/CPB | PCIe M.2 M Key           |                       |                               |                    |
| EVM/CPB | USC C PD controller      | TPS25750DRJKR         | 0x20                          |                    |
| EVM/CPB | I2C MUX                  | TCA9543APWR           | 0x70                          | Main I2C1          |
| EVM/CPB | CSI2 Expansion Connector | QSH-020-01-L-D-DP-A-K |                               |                    |
| EVM/CPB | CSI FPC Connector        | 22_1734248            |                               |                    |
| EVM/CPB | 40 pin Expansion Header  |                       |                               | Main I2C4          |
| EVM/SoM | CURRENT MONITORs         | INA231AIYFDR          | 0x40,0x41,0x41,0x43,0x44,0x45 | MCU I2C0           |
| EVM/CPB | Test automation header   |                       |                               |                    |
| EVM/CPB | Bootmode IO Expander     | TCA6408ARGTR          | 0x20                          |                    |
| EVM/CPB | eDP Bridge               | SN65DSI86IPAPQ1       | 0x2C                          | MCU I2C1           |

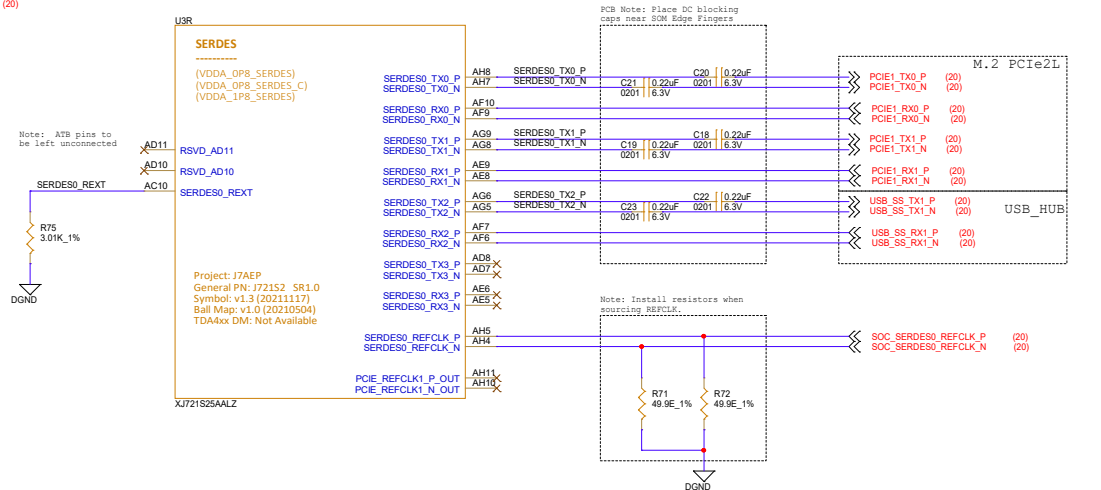
# SoC GPIO MAPPING TABLE

| J7x SoM - GPIO Mapping Table |                       |                                            |                  |          |             |                                                                                    |
|------------------------------|-----------------------|--------------------------------------------|------------------|----------|-------------|------------------------------------------------------------------------------------|
| J7AEP Mapping                |                       | WKUP Domain                                |                  |          |             |                                                                                    |
| Package Signal Name          | GPIO Number           | Net name                                   | Input/<br>Output | Default  | State       | Remarks                                                                            |
| MCU_OSPiO_CSn1               | WKUP_GPIO0_28         | EN_EFUSE_VPP                               | Output           | PU       | Active High | Enable pin for VPP_EFUSE supply                                                    |
| MCU_OSPiO_CS2                | WKUP_GPIO0_29         | CPLD_TMS/USER_LED1                         | Output           | NA       | NA          | JTAG signals for CPLD & USER LED enable signal.<br>1:2 Mux on base board           |
| MCU_OSPi1_CLK                | WKUP_GPIO0_31         | CPLD_TCK/MCU_RGMII_INTz                    | Input            | PD       | NA          | JTAG signals for CPLD & MCU_RGMII_INT signal.<br>1:2 Mux on base board             |
| MCU_OSPi1_CSNO               | WKUP_GPIO0_38         | CSI_EXP_GPIO_4                             | I/O              | NA       | NA          | GPIO Signals for CSI expansion connector                                           |
| MCU_OSPi1_CSNI               | WKUP_GPIO0_39         | PMIC_INTn_1V8                              | Input            | PU       | Active low  | Interrupt signal from PMIC                                                         |
| MCU_OSPi1_D0                 | WKUP_GPIO0_34         | CPLD_TDI/ eDP_IRQ                          | Input            | NA       | NA          | JTAG signals for CPLD & Interrupt signal from eDP bridge.<br>1:2 Mux on base board |
| MCU_OSPi1_D1                 | WKUP_GPIO0_35         | CSI_EXP_GPIO_5                             | I/O              | NA       | NA          | GPIO Signals for CSI expansion connector                                           |
| MCU_OSPi1_D2                 | WKUP_GPIO0_36         | CSI_EXP_GPIO_2                             | I/O              | NA       | NA          | GPIO Signals for CSI expansion connector                                           |
| MCU_OSPi1_D3                 | WKUP_GPIO0_37         | CSI_EXP_GPIO_3                             | I/O              | NA       | NA          | GPIO Signals for CSI expansion connector                                           |
| MCU_OSPi1_DQS                | WKUP_GPIO0_33         | CPLD_TDO/ SOC_WAKE                         | Output           | NA       | NA          | JTAG signals for CPLD                                                              |
| MCU_OSPi1_LBCLKO             | WKUP_GPIO0_32         | CSI_EXP_GPIO_1                             | I/O              | NA       | NA          | GPIO Signals for CSI expansion connector                                           |
| MCU_SPIO_CLK                 | WKUP_GPIO0_54         | WKUP_GPIO0_54                              | Output           | BOOTMODE | Active low  | CPLD_JTAG/GPIOOn_SEL.                                                              |
| MCU_SPIO_CS0                 | WKUP_GPIO0_70         | WKUP_GPIO0_70                              | I/O              | BOOTMODE | NA          | Mux select signal for CPLD JTAG and GPIO's                                         |
| MCU_SPIO_D1                  | WKUP_GPIO0_69         | SYS_MCU_PWRDN                              | Output           | BOOTMODE | Active High | FPC Camera GPIO signals                                                            |
|                              |                       |                                            |                  |          |             | System Power Down ('0' - normal operation,<br>'1' - system power down)             |
| WKUP_GPIO0_10                | WKUP_GPIO0_10         | MCU_ADC_EXT_TRIGGER0/PCIE<br>1_M.2_CLKREQ# |                  |          |             | ADC external trigger from TI safety header(Default<br>connection)/CLKREQ#          |
| WKUP_GPIO0_11                | WKUP_GPIO0_11         | MCU_CLKOUT0                                | Output           | NA       | NA          | 25MHz reference clock for CSI expansion connector                                  |
| WKUP_GPIO0_15                | WKUP_GPIO0_15         | MCU_SPI1_CS2                               | Output           | BOOTMODE | Active low  | MCU SPI1 signals                                                                   |
| WKUP_GPIO0_49                | WKUP_GPIO0_49         | WKUP_GPIO0_49                              | I/O              | NA       | NA          | GPIO signal for 40 pin expansion header                                            |
| WKUP_GPIO0_57                | WKUP_GPIO0_57         | WKUP_GPIO0_57                              | I/O              | BOOTMODE | NA          | GPIO signal for 40 pin expansion header                                            |
| WKUP_GPIO0_56                | WKUP_GPIO0_56         | WKUP_GPIO0_56                              | I/O              | BOOTMODE | NA          | GPIO signal for 40 pin expansion header                                            |
| WKUP_GPIO0_66                | WKUP_GPIO0_66         | WKUP_GPIO0_66                              | I/O              | BOOTMODE | NA          | GPIO signal for 40 pin expansion header                                            |
| WKUP_GPIO0_67                | WKUP_GPIO0_67         | WKUP_GPIO0_67                              | I/O              | BOOTMODE | NA          | GPIO signal for 40 pin expansion header                                            |
| PMIC_POWER_EN1               | WKUP_GPIO0_88         | WKUP_GPIO0_88                              | I/O              | NA       | NA          | FPC Camera GPIO signals                                                            |
| MCU_ADC1_AIN0                | WKUP_GPIO0_79         | SOC_INT1z                                  | Input            | PU       | Active low  | Test automation INT signal                                                         |
| MCU_ADC1_AIN1                | WKUP_GPIO0_80         | SOC_INT2z                                  | Input            | PU       | Active low  | Test automation INT signal                                                         |
|                              |                       |                                            |                  |          |             |                                                                                    |
| Main Domain                  |                       |                                            |                  |          |             |                                                                                    |
| ECAP0_IN_APWM_OUT            | GPIO0_49              | SEL_SDIO_3v3_1v8n                          | Output           | PU       | Active low  | VDD_SD_DV 1.8V or 3.3V selection control                                           |
| TIMER_IO0                    | GPIO0_58              | MMCI1_SDIO                                 | Input            | PU       | Active low  | SD card detect signal                                                              |
| TIMER_IO1                    | GPIO0_59              | USB0_DRVVBUS                               | Output           | NA       | Active High | USB VBUS Drive signal                                                              |
| EXTINTN                      | GPIO0_0               | HDMI_HPD                                   | Input            | NA       | Active High | HDMI hot plug detect signal                                                        |
| MCAN1_TX                     | GPIO0_27              | GPIO0_27                                   | I/O              | NA       | NA          | GPIO signal for 40 pin expansion header                                            |
| MCAN13_TX                    | GPIO0_3               | GPIO0_3                                    | I/O              | NA       | NA          | GPIO signal for 40 pin expansion header                                            |
| MCASPO_AXR8                  | GPIO0_36              | GPIO0_36                                   | I/O              | NA       | NA          | GPIO signal for 40 pin expansion header                                            |
| MCASPO_AXR13                 | GPIO0_41              | GPIO0_41/UART5_CTSn                        | I/O              | NA       | NA          | GPIO signal for 40 pin expansion header/ UART5_CTS Signal                          |
| MCASPO_AXR14                 | GPIO0_42              | GPIO0_42/UART5_RTSn                        | I/O              | NA       | NA          | GPIO signal for 40 pin expansion header/ UART5_RTS Signal                          |
| GPIO Expander on Base Board  |                       |                                            |                  |          |             |                                                                                    |
| Port NO                      |                       | I2C Instance                               | Input/O<br>utput | Default  | State       | Usage                                                                              |
| P00                          | CSI_VIO_SEL           | I2C0 ADDR: 0x21                            | Output           | PD       | Active High | Enable for VCC_CSI_IO supply generation load switch                                |
| P01                          | CSI_SEL_FPC_EXPn      |                                            | Output           | PD       | Active High | CSI MUX selection                                                                  |
| P02                          | HDMI_PDn              |                                            | Output           | PD       | Active Low  | Power down signal for HDMI Transmitter                                             |
| P03                          | HDMI_LS_OE            |                                            | Output           | PU       | Active High | HDMI current limit load switch enable                                              |
| P04                          | DP0_3V3_EN            |                                            | Output           | PD       | Active High | Enable signal for Display port load switch                                         |
| P05                          | BOARDID_EEPROM_WP     |                                            | Output           | PD       | Active High | Board id Eeprom Write protect signal                                               |
|                              |                       |                                            |                  |          |             | Standby signals for MAIN & MCU domain                                              |
| P06                          | CAN_STB               |                                            | Output           | PD       | Active High | CAN Transceivers                                                                   |
| P10                          | GPIO_uSD_PWR_EN       |                                            | Output           | PU       | Active High | Micro SD card Load switch enable                                                   |
| P11                          | eDP_ENABLE            |                                            | Output           | PD       | Active High | Used for Enable of DSI to eDP Bridge                                               |
| P12                          | IO_EXP_PCIE1_M.2_RTSz |                                            | Output           | NA       | Active Low  | PCIe Reset input to CPLD                                                           |
| P13                          | IO_EXP_MCU_RGMII_RST# |                                            | Output           | NA       | Active Low  | MCU_RGMII reest input to CPLD                                                      |
| P14                          | IO_EXP_CSI2_EXP_RSTz  |                                            | Output           | PD       | Active Low  | CSI expansion connector reset                                                      |
| P16                          | CSIO_B_GPIO1          |                                            | Output           | NA       | NA          | FPC Camera1 GPIO signal                                                            |
| P17                          | CS11_B_GPIO1          |                                            | Output           | NA       | NA          | FPC Camera2 GPIO signal                                                            |

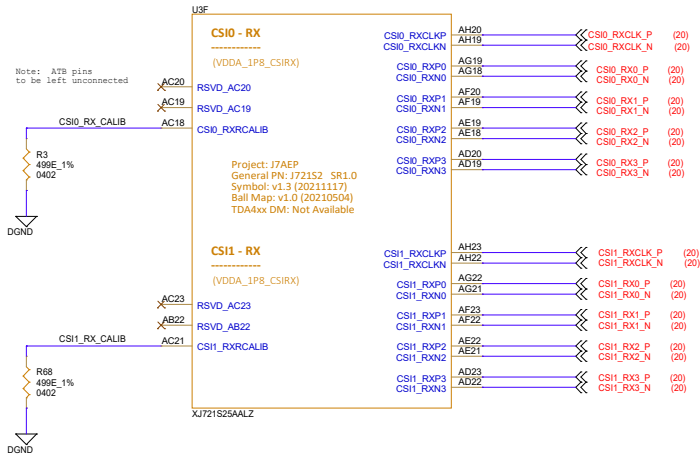
## DSI Interface



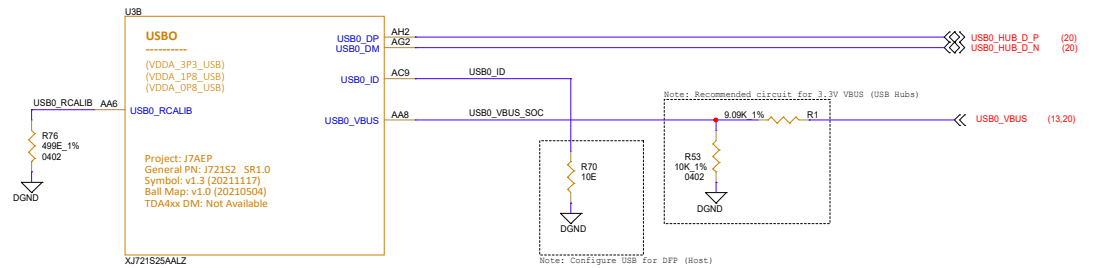
## SERDES Interface (PCIE/USB)



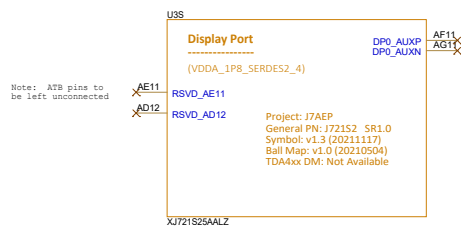
## CSI Interface



## USB2.0 Interface

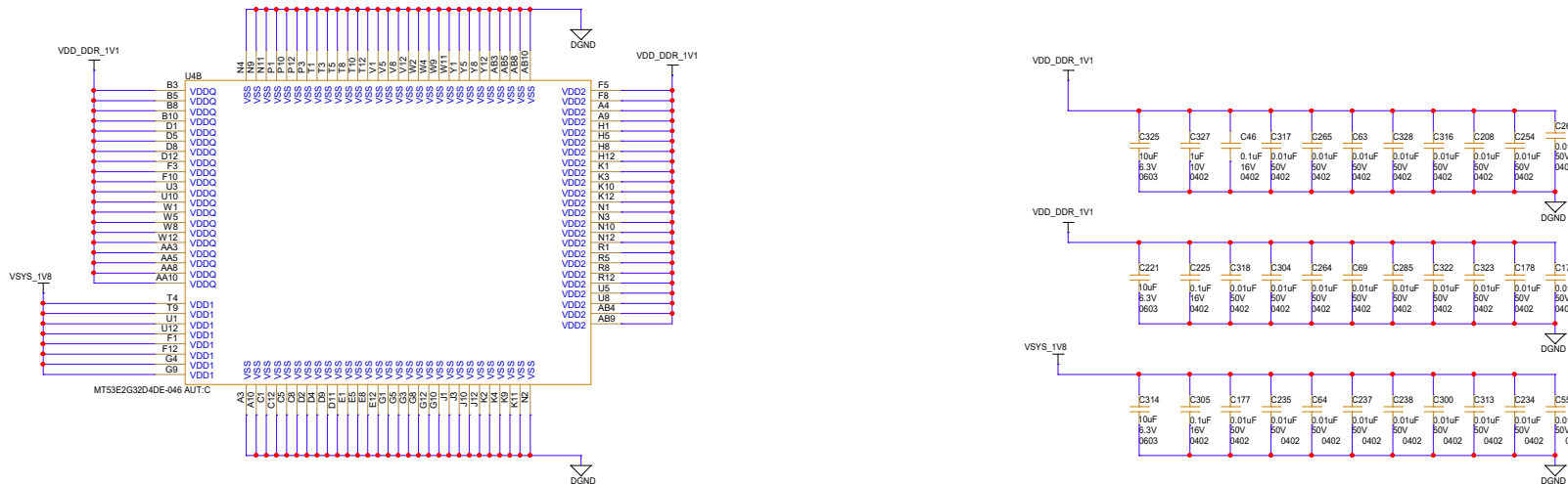
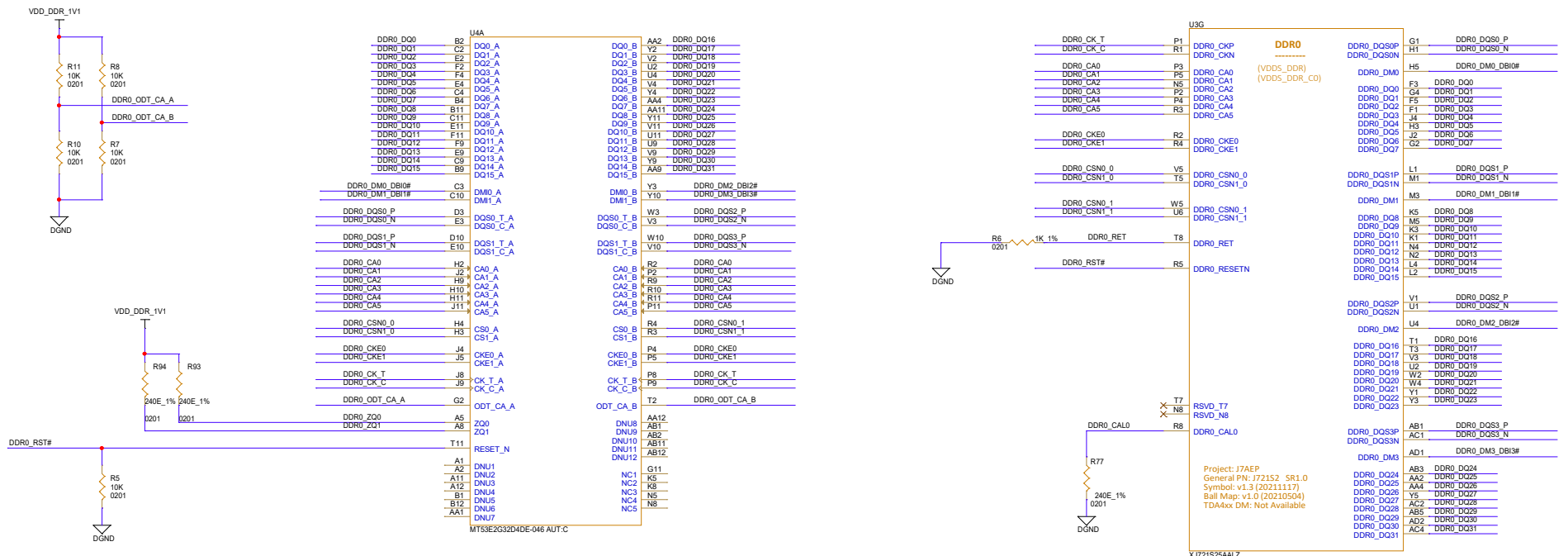


## DP Aux

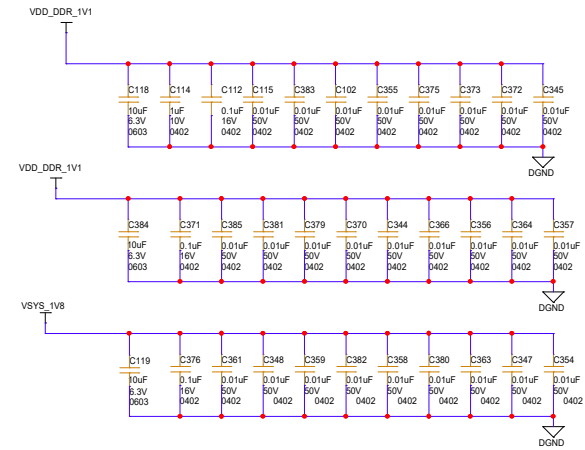
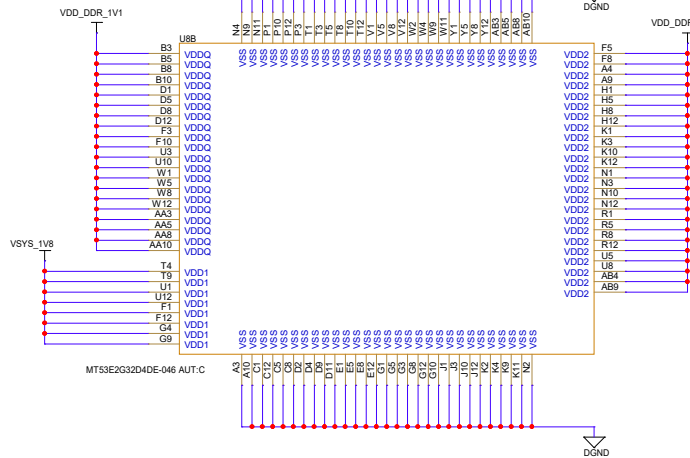
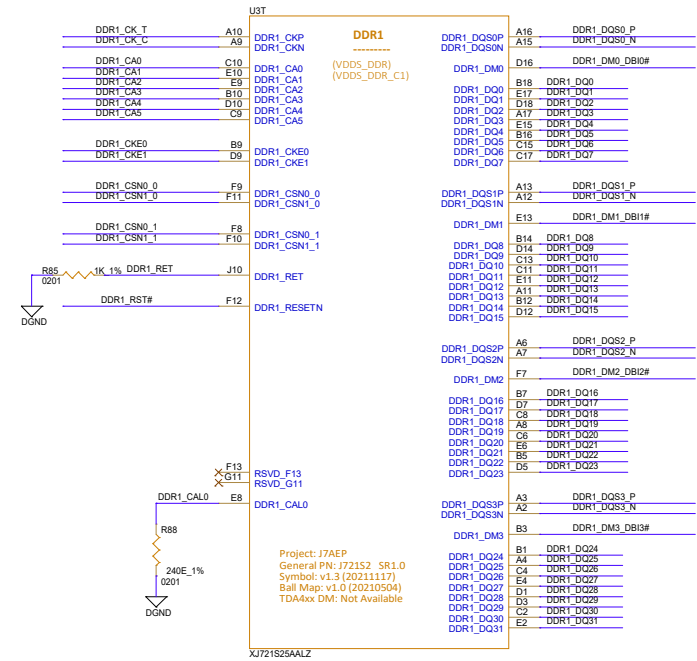
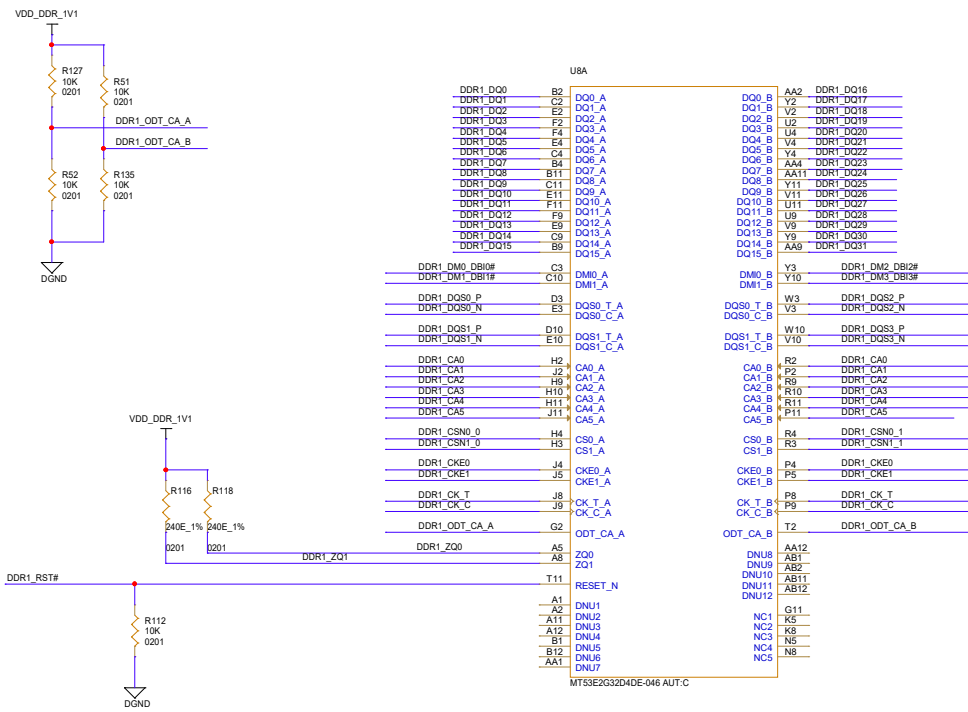


|                                 |  |                              |  |
|---------------------------------|--|------------------------------|--|
| Project :<br>J7 EVM             |  | Title<br>DSI & CSI INTERFACE |  |
| Size<br>C                       |  | Rev<br>E2A                   |  |
| Date: Thursday, August 07, 2025 |  | Sheet 8 of 21                |  |

## LPDDR4 Inteface (Bank 0)



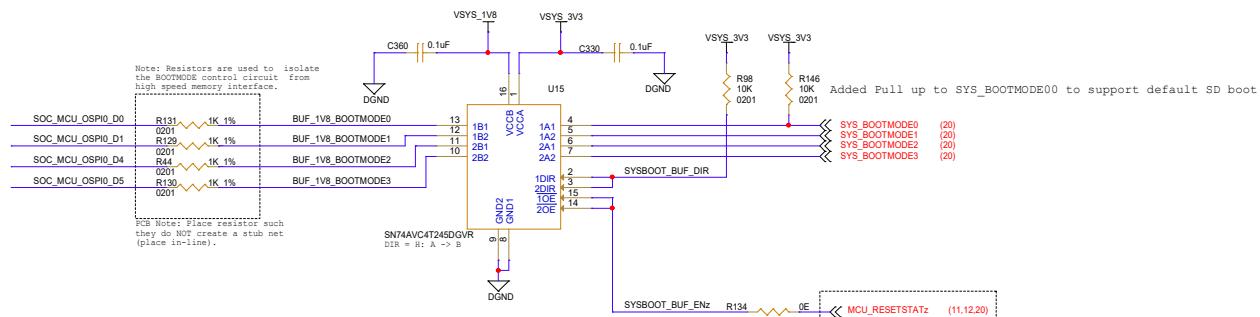
## LPDDR4 Interface (Bank 1)



[illegible]

Note: Logic used to configure BOOTMODE settings during reset. This is four (4) of a total of eighteen (18) boot pins. Specific value is user configured (dip switch).

Note: Logic used to configure BOOTMODE settings during reset. This is four (4) of a total of eighteen (18) boot pins. Specific value is user configured (dip switch).



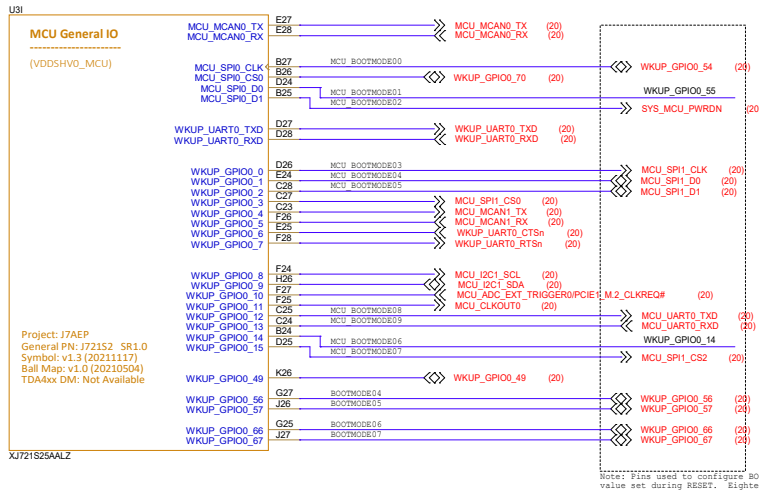
The diagram shows the L2934T package with pins 1 through 28. Pins 1-14 are labeled 'MCU-ADC0' and pins 15-28 are labeled 'MCU-ADC1'. The connections are as follows:

| Pin | Label          |
|-----|----------------|
| 1   | MCU_ADC0_AIN0  |
| 2   | MCU_ADC0_AIN1  |
| 3   | MCU_ADC0_AIN2  |
| 4   | MCU_ADC0_AIN3  |
| 5   | MCU_ADC0_AIN4  |
| 6   | MCU_ADC0_AIN5  |
| 7   | MCU_ADC0_AIN6  |
| 8   | MCU_ADC0_AIN7  |
| 9   | MCU_ADC0_AIN8  |
| 10  | MCU_ADC0_AIN9  |
| 11  | MCU_ADC0_AIN10 |
| 12  | MCU_ADC0_AIN11 |
| 13  | MCU_ADC0_AIN12 |
| 14  | MCU_ADC0_AIN13 |
| 15  | MCU_ADC1_AIN0  |
| 16  | MCU_ADC1_AIN1  |
| 17  | MCU_ADC1_AIN2  |
| 18  | MCU_ADC1_AIN3  |
| 19  | MCU_ADC1_AIN4  |
| 20  | MCU_ADC1_AIN5  |
| 21  | MCU_ADC1_AIN6  |
| 22  | MCU_ADC1_AIN7  |
| 23  | MCU_ADC1_AIN8  |
| 24  | MCU_ADC1_AIN9  |
| 25  | MCU_ADC1_AIN10 |
| 26  | MCU_ADC1_AIN11 |
| 27  | MCU_ADC1_AIN12 |
| 28  | MCU_ADC1_AIN13 |

Project: I7AEP  
 General PN: J71252 SR1.0  
 Symbol: v1.3 (20211117)  
 Bill Maps: v1.0 (20210504)  
 D24xx4 DM: Not Available

|                         |                                                                                       |                                 |                |
|-------------------------|---------------------------------------------------------------------------------------|---------------------------------|----------------|
| Project :<br><br>J7 EVM |  | Title<br>MCU FLASH IF           |                |
|                         |                                                                                       | Size<br>C                       | <Core Design>  |
|                         |                                                                                       | Date: Thursday, August 07, 2025 | Sheet 11 of 24 |

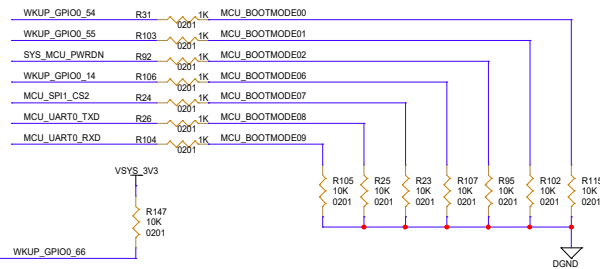
## MCU GENERAL IO



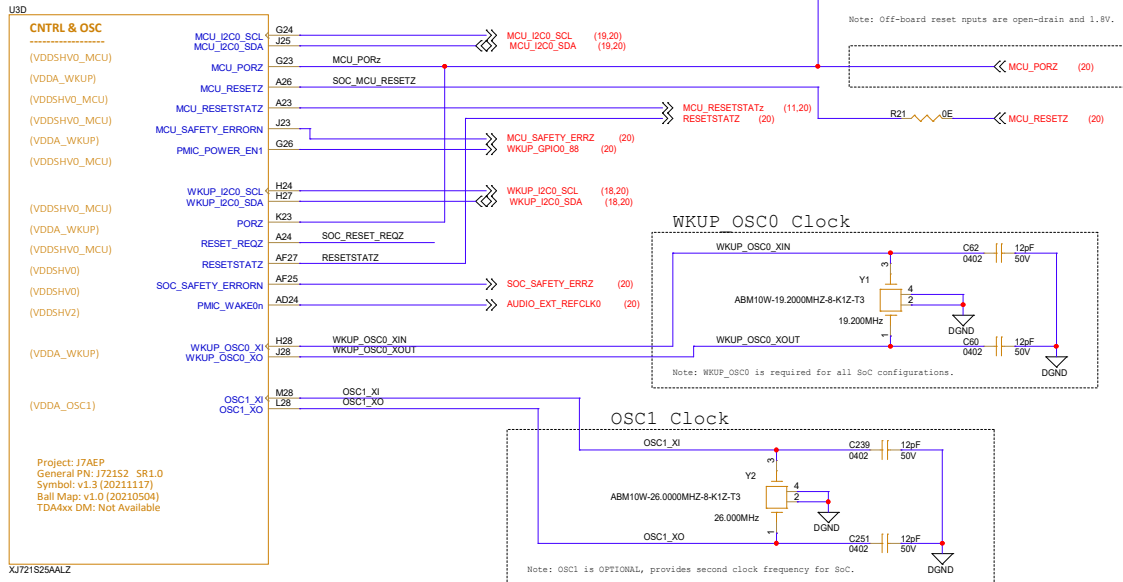
### BOOTMODE Control Logic

Note: Logic used to configure BOOTMODE settings during reset. This is seven(7) of a total of eighteen (18) boot pins. These settings configure for:

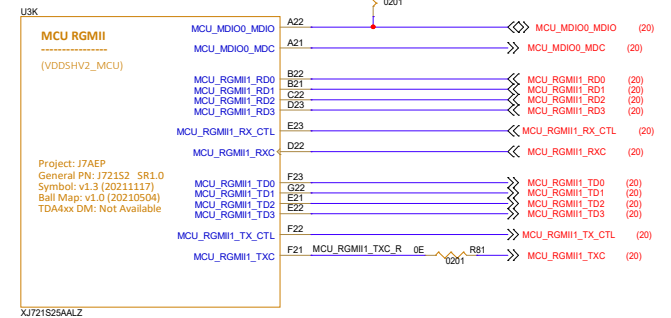
MCU\_BOOTMODE[2:0] set '000' for WKUP\_OSC0 of 19.2MHz  
MCU\_BOOTMODE[6] set '0' for Normal Boot  
MCU\_BOOTMODE[7] set '0' for Reserved  
MCU\_BOOTMODE[9:8] set '00' for LBIST + PBIST



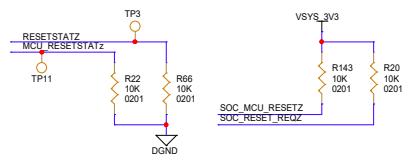
## MCU CNTRL and OSC



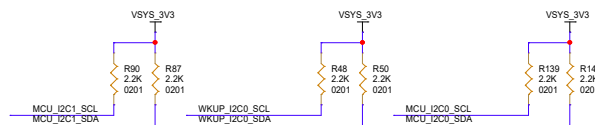
## MCU RGMII



### RESET Pull Resistors



### MCU I2C Pull-Ups



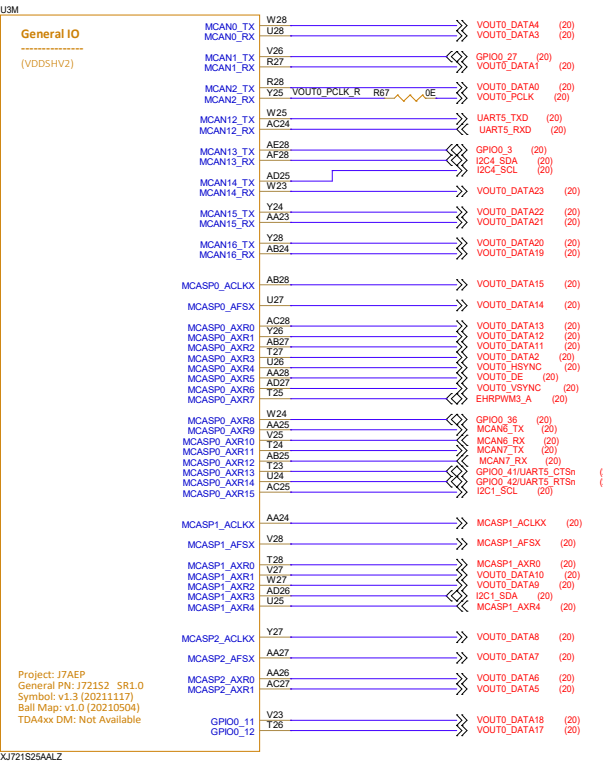
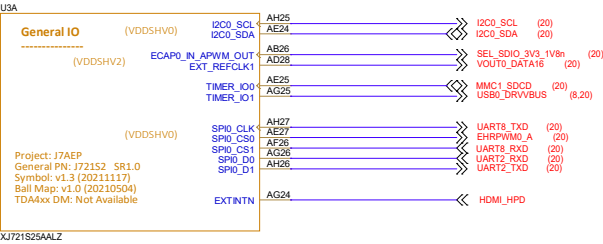
Project :

J7 EVM

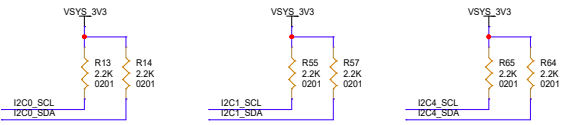


| Title                   |                           | Rev   |          |
|-------------------------|---------------------------|-------|----------|
| SOC_GENERAL&MCU_GENERAL |                           | E2A   |          |
| Size                    | <Core Design>             |       |          |
| C                       |                           |       |          |
| Date:                   | Thursday, August 07, 2025 | Sheet | 12 of 21 |

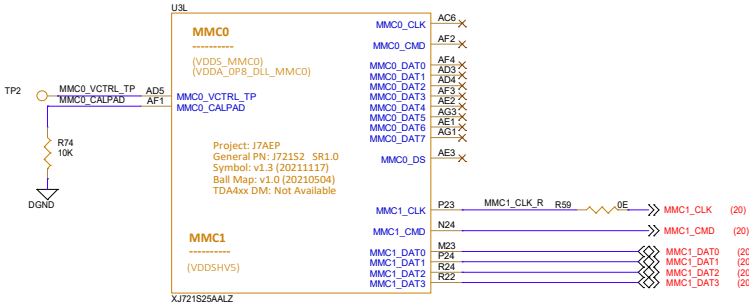
# GENERAL IO



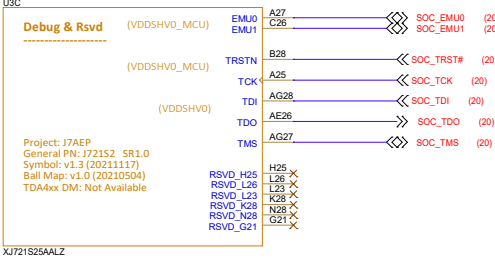
## I2C Pull-Ups



# MMC Interface



# DEBUG

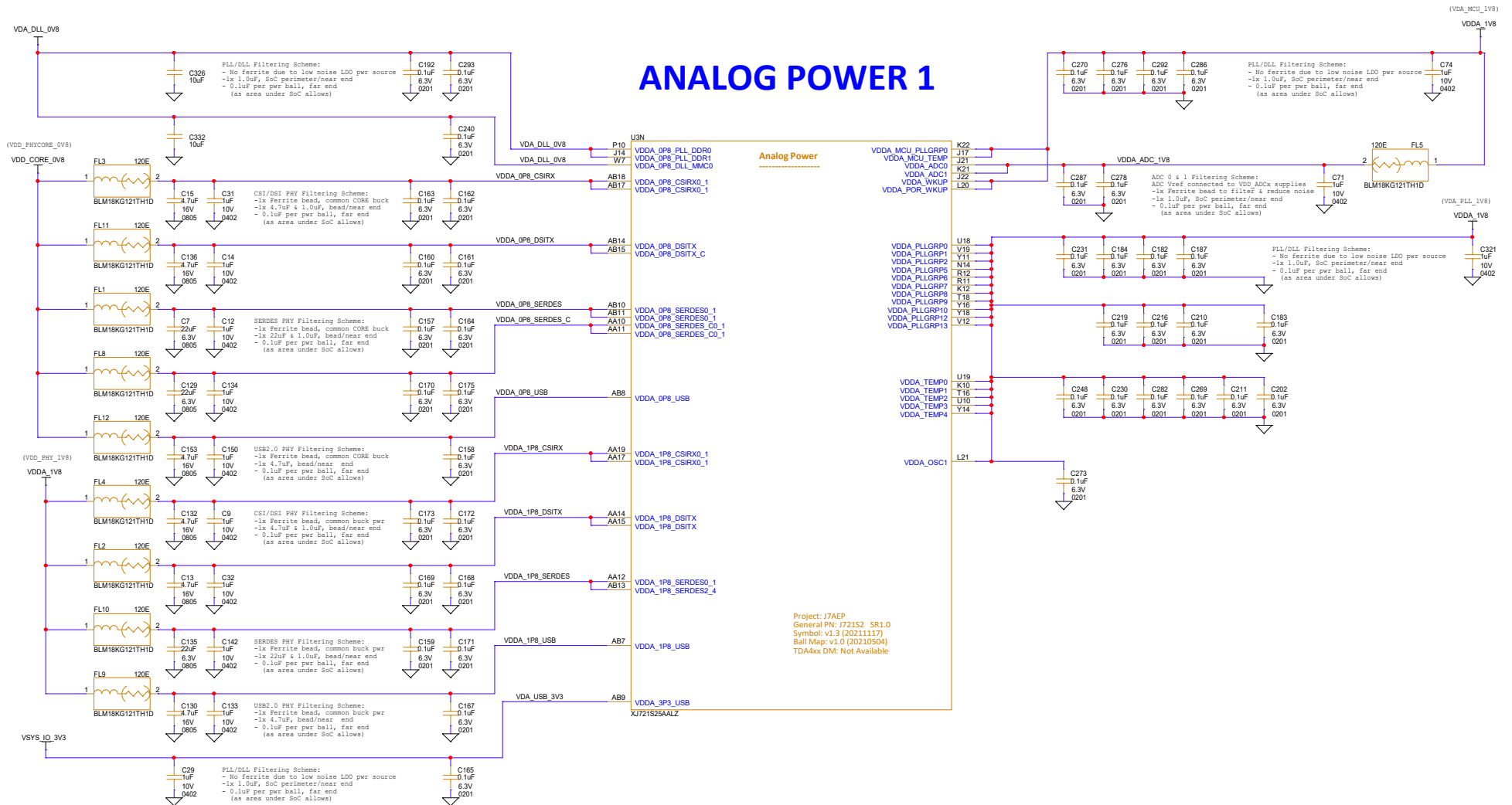


Project :  
J7 EVM



|                                  |            |
|----------------------------------|------------|
| Title<br>SOC_GENERAL_MCU_GENERAL |            |
| Size<br>C                        | Rev<br>E2A |
| Date: Thursday, August 07, 2025  |            |
| Sheet 13 of 21                   |            |

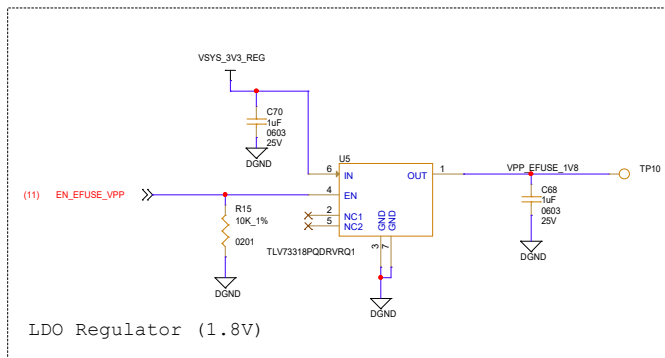
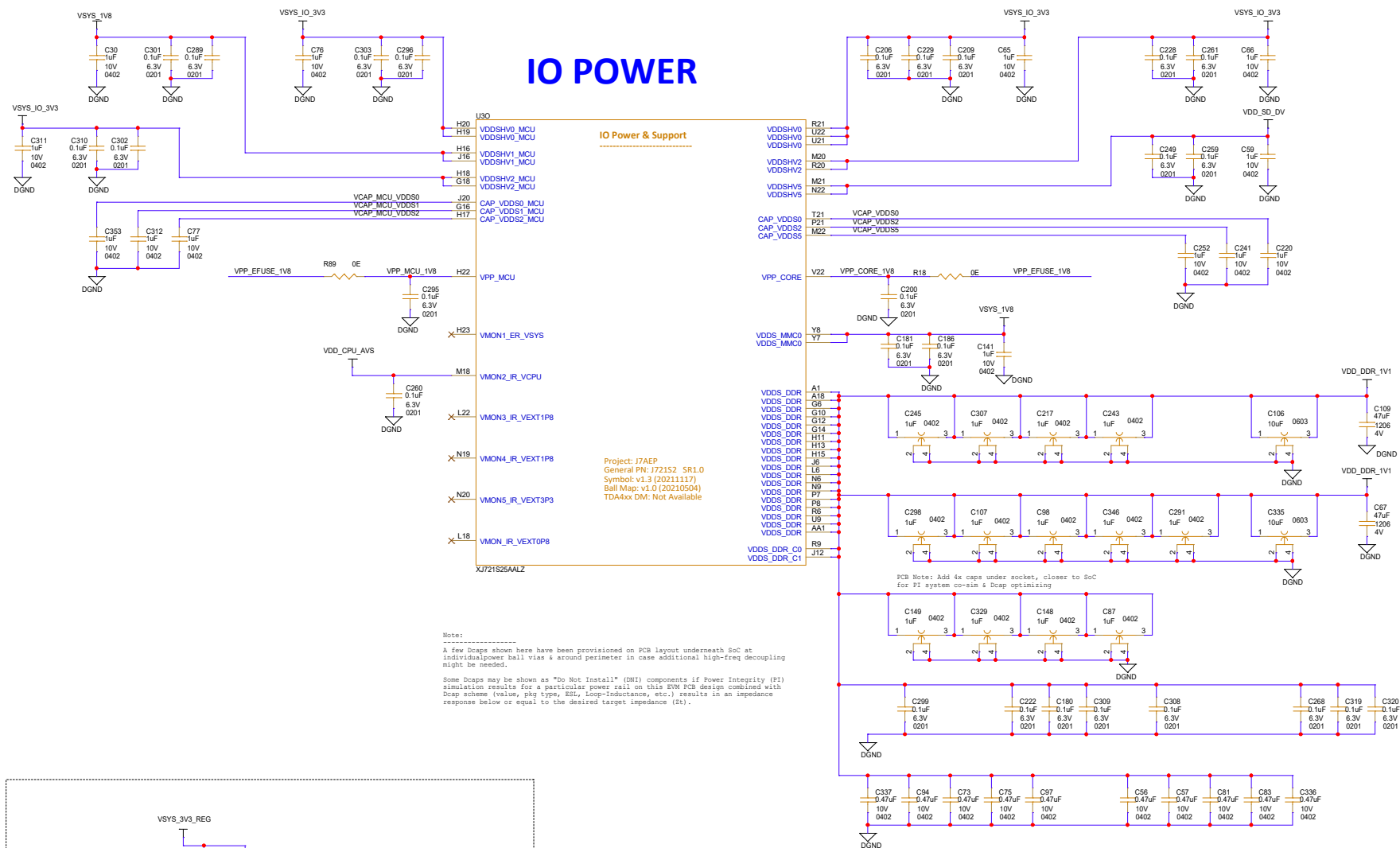
# ANALOG POWER 1



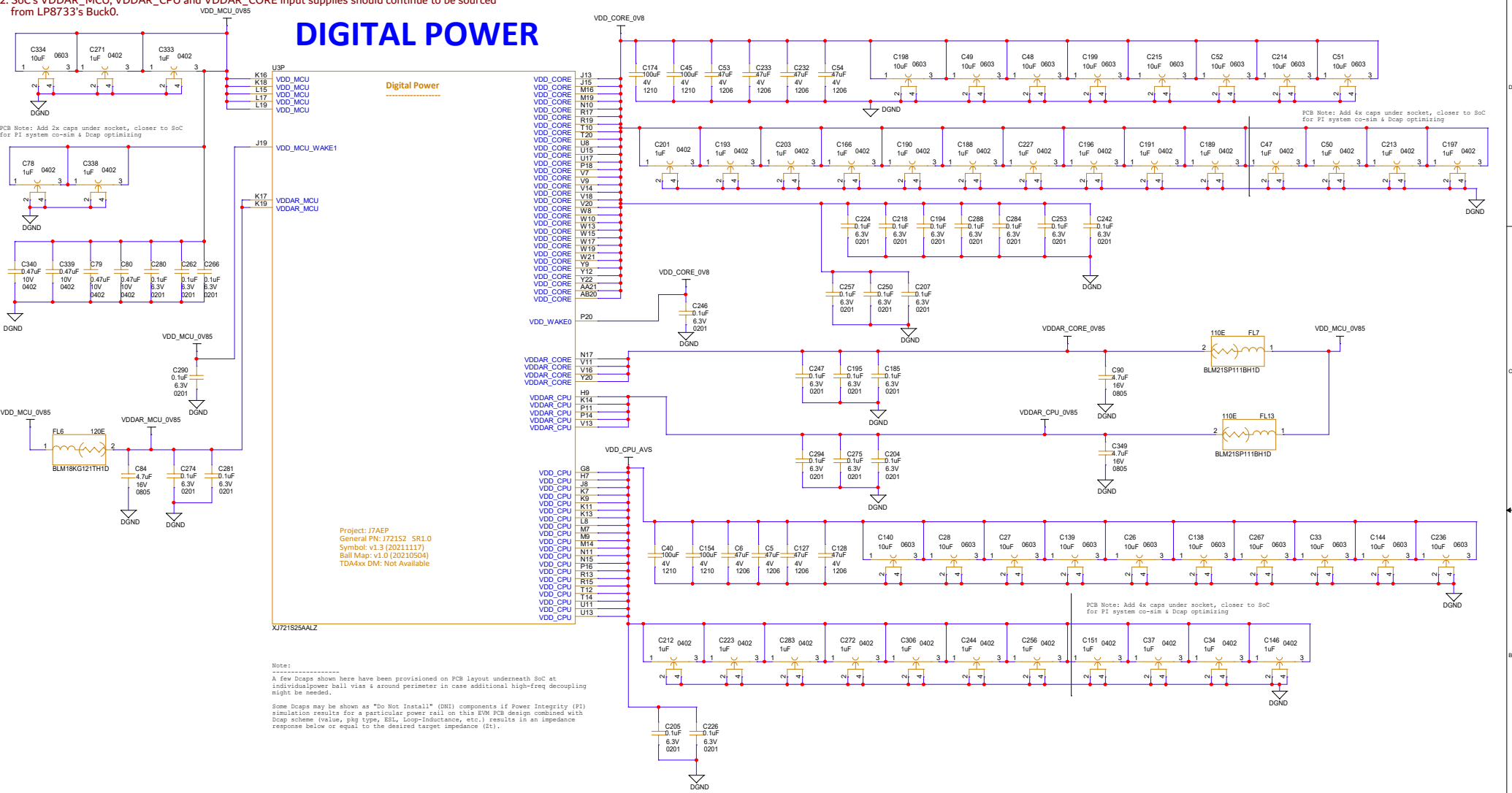
Project: J7AEP  
General PN: J721S2 SR1.0  
Symbol: v1.3 (20211117)  
Ball Map: v1.0 (20210504)  
TDA4xx DM: Not Available

|                                 |  |               |  |                             |  |
|---------------------------------|--|---------------|--|-----------------------------|--|
| Project :<br><br>J7 EVM         |  |               |  | Title<br>SOC ANALOG POWER 1 |  |
| Size<br>C                       |  | <Core Design> |  | Rev<br>E2A                  |  |
| Date: Thursday, August 07, 2025 |  | Sheet 14 of   |  | 21                          |  |

## IO POWER

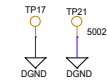
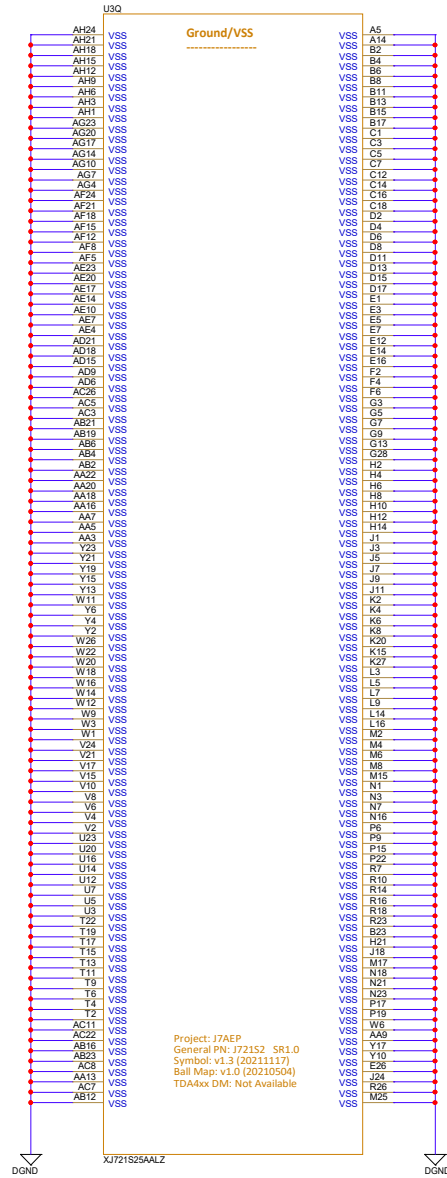


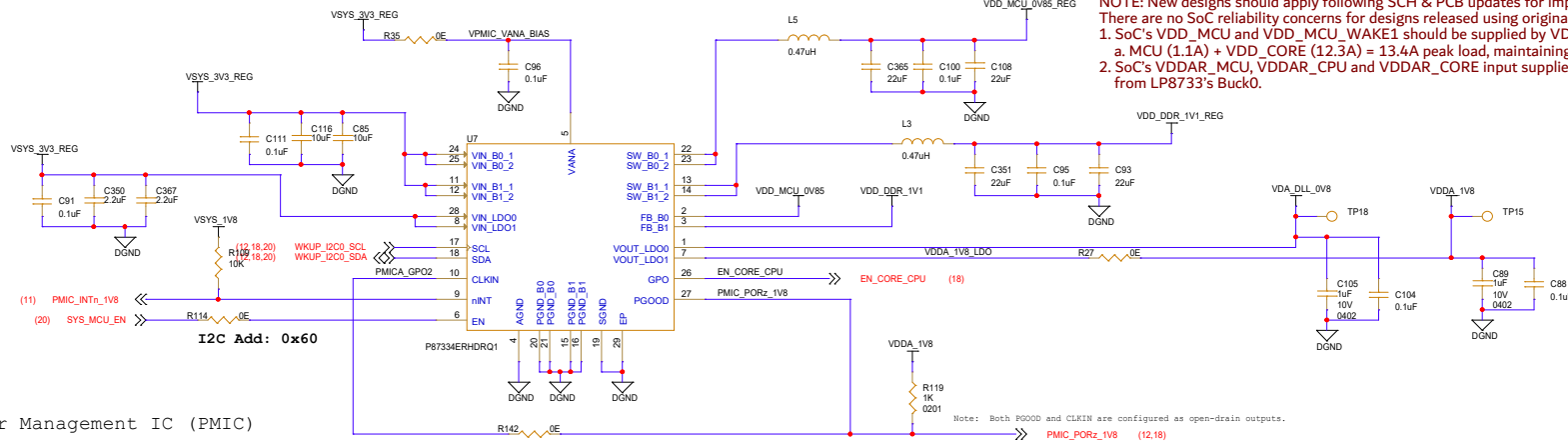
NOTE: New designs should apply following S&C & PCB updates for improved power sequencing.  
There are no SoC reliability concerns for designs released using original PDN power mapping.  
1. SoC's VDD\_MCU and VDD\_MCU\_WAKE1 should be supplied by VDD\_CORE\_OV8 power rail.  
a. MCU (1.1A) + VDD\_CORE (12.3A) = 13.4A peak load, maintaining +10.5 margin on power rail.  
2. SoC's VDDAR\_MCU, VDDAR\_CPU and VDDAR\_CORE input supplies should continue to be sourced from LP8733's Buck0.



|                         |  |                                                                                       |                              |            |
|-------------------------|--|---------------------------------------------------------------------------------------|------------------------------|------------|
| Project :<br><br>J7 EVM |  |  | Title<br>SOC DIGITAL POWER 3 |            |
| Size<br>C               |  |                                                                                       | <Core Design>                |            |
| Date:                   |  |                                                                                       | Thursday, August 07, 2025    |            |
|                         |  |                                                                                       | Sheet 16 of 21               |            |
|                         |  |                                                                                       |                              | Rev<br>E2A |

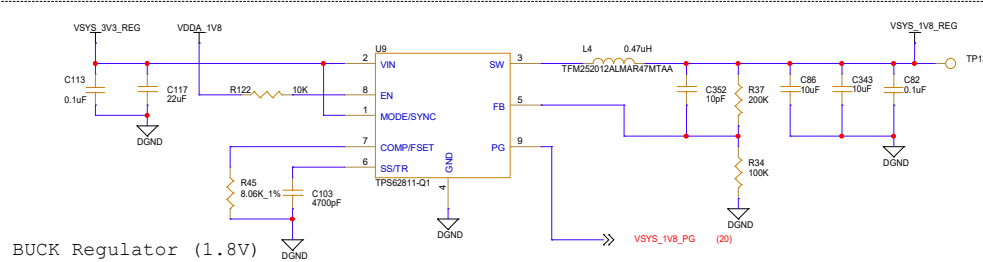
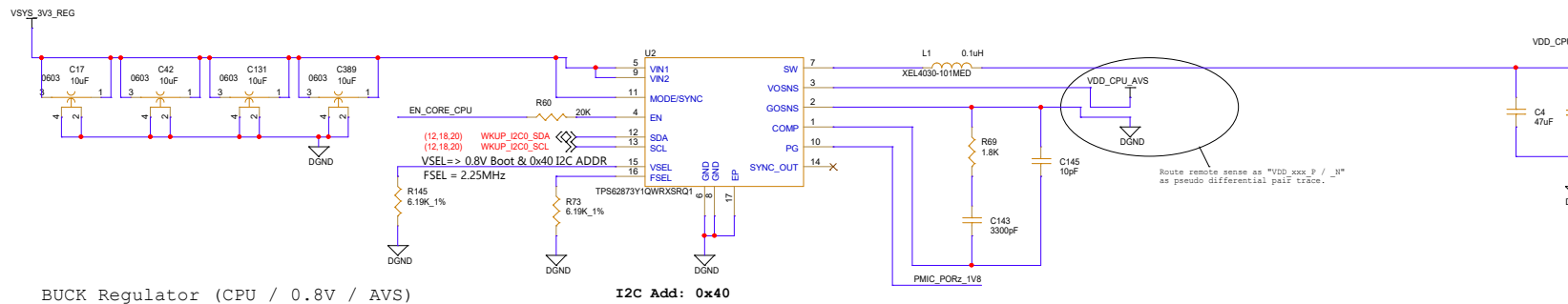
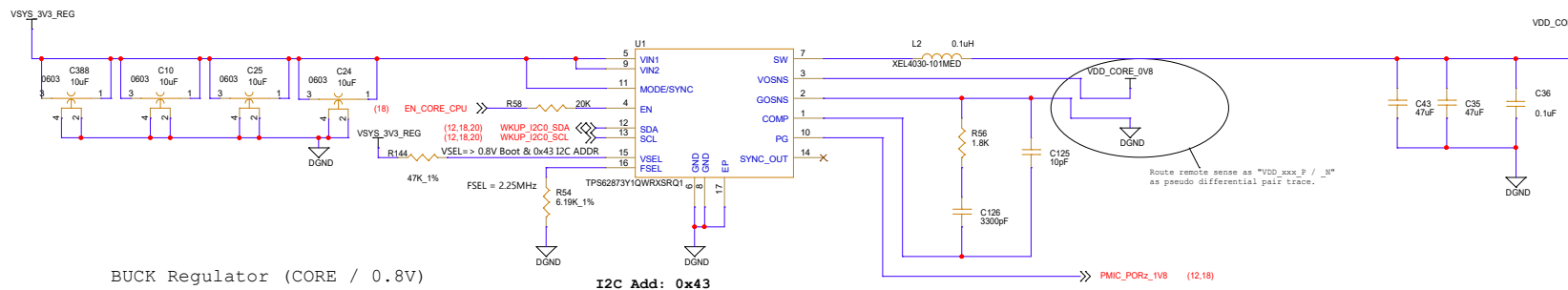
# SOC GROUND





**NOTE:** New designs should apply following SCH & PCB updates for improved power sequencing. There are no SoC reliability concerns for designs released using original PDN power mapping.

- SoC's VDD\_MCU and VDD\_MCU\_WAKE1 should be supplied by VDD\_CORE\_OV8 power rail.
  - MCU (1.1A) + VDD\_CORE (12.3A) = 13.4A peak load, maintaining +10.5 margin on power rail.
- SoC's VDDAR\_MCU, VDDAR\_CPU and VDDAR\_CORE input supplies should continue to be sourced from LP8733's Buck0.

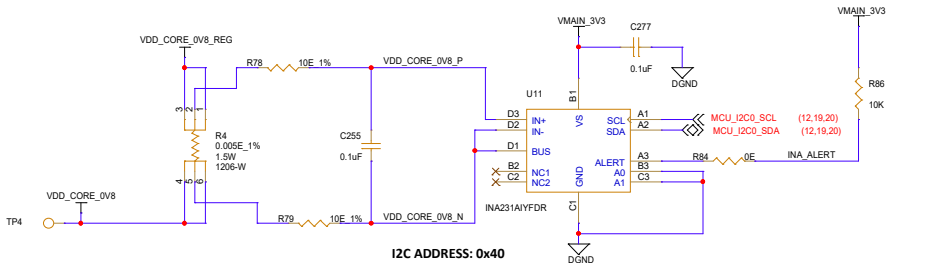


# POWER SUPPLY

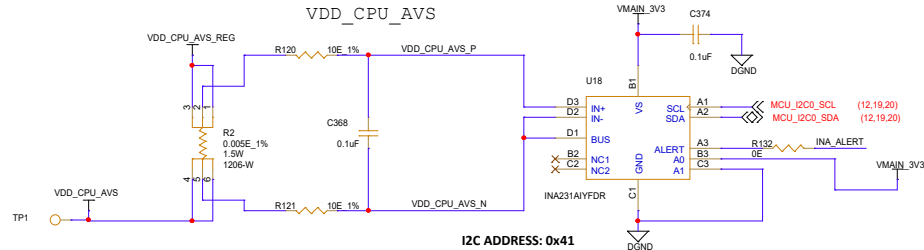
|                                  |  |                               |  |
|----------------------------------|--|-------------------------------|--|
| Project : J7 EVM                 |  | Title : PMIC and Power Supply |  |
| Size : <Core Design>             |  | Rev : E2A                     |  |
| Date : Thursday, August 07, 2025 |  | Sheet : 18 of 21              |  |

# CURRENT MONITOR

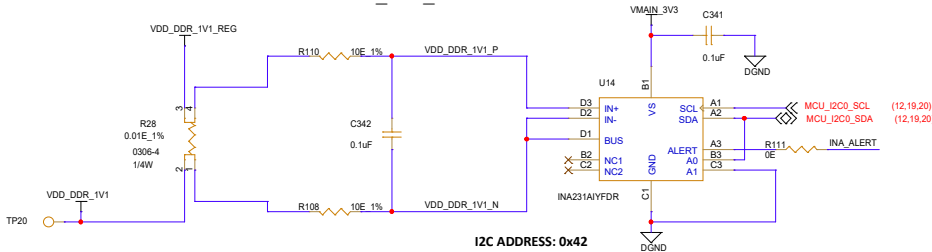
VDD\_CORE\_0V8



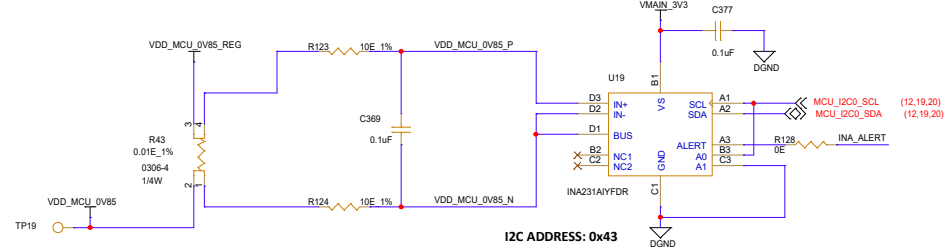
VDD\_CPU\_AV5



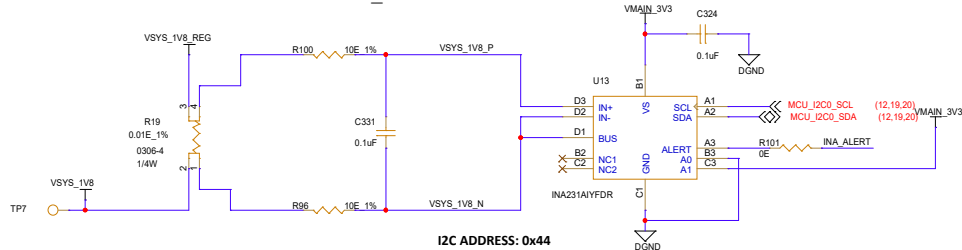
VDD\_DDR\_1V1



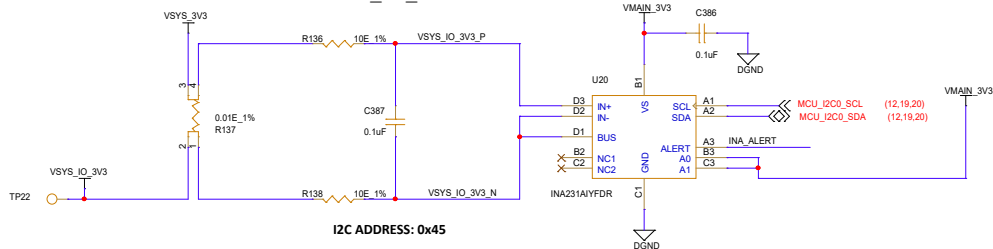
VDD\_MCU\_0V85



VSYS\_1V8



VSYS\_IO\_3V3



Project :

J7 EVM



Title  
Current sense

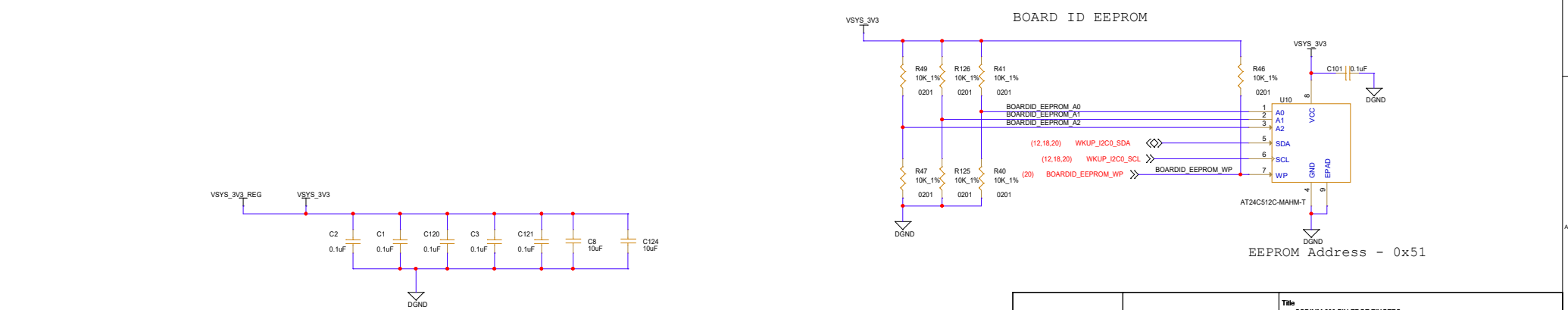
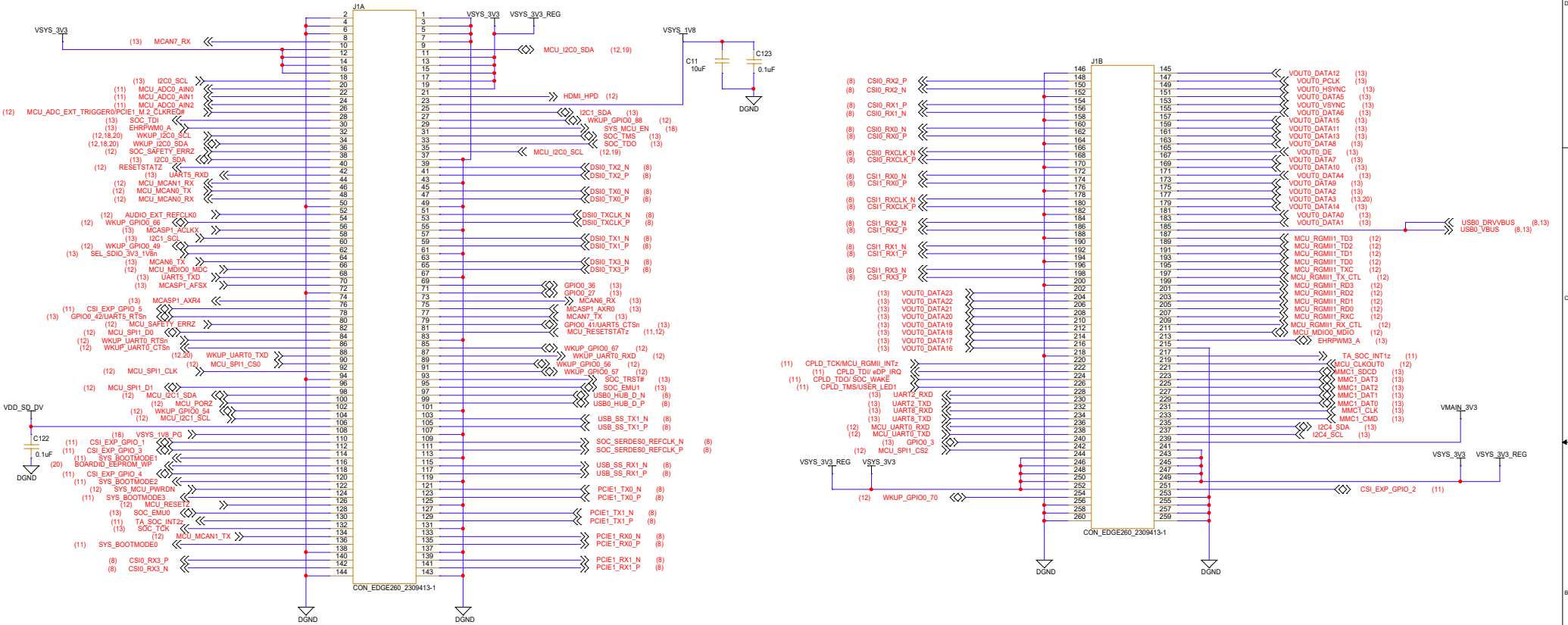
Size  
<Core Design>

Date: Thursday, August 07, 2025

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Rev  
E2A

260 PIN SODIMM CONNECTOR

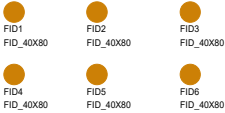


NOTES, HW & LABELS

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

FIDUCIALS



BARE PCB



AM68 SK ASSEMBLED  
BASEBOARD



LABELS

Board Serial No.



AM6-COMPROCEVM

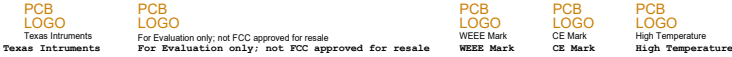
Assembly Revision.



AM6-COMPROCEVM

OPN: SK - AM68

LOGOs



STANDOFF,SCREW & WASHER FOR SOM



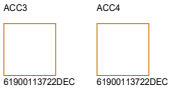
HEATSINK



FAN



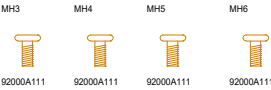
CRIMP PIN



CONN HOUSING



SCREW FOR FAN ASSEMBLY



Project :

J7 EVM



Title  
Hardware Schematic:

Size  
<Core Design>

C

Date: Thursday, August 07, 2025

Sheet 21 of 21

Rev  
E2A