



## REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	18 NOV 2021	Initial Draft	Mistral Design Team		
0.02	8 DEC 2021	C88 (1uF) is made DNI on VDDA_1V8 rail C48, C49 and C57 decap values changed from 4.7uF to 1uF	Mistral Design Team		
0.03	22 DEC 2021	Power Block Diagram updated	Mistral Design Team		
0.04	21 APRIL 2022	Updated all the changes of PROC114E3	Mistral Design Team		
0.05	22 APRIL 2022	Changed the I2C slave address of U23 and U25	Mistral Design Team		
0.06	2 MAY 2022	Added 0E RES option to short VDD_CORE and VDDR_CORE rails when both are generated from the same source	Mistral Design Team		
0.07	4 MAY 2022	Removed R641(0E) Resistor	Mistral Design Team		
0.08	6 MAY 2022	C502 Decap on VSYS pin of PMIC changed to 2.2uF.	Mistral Design Team		

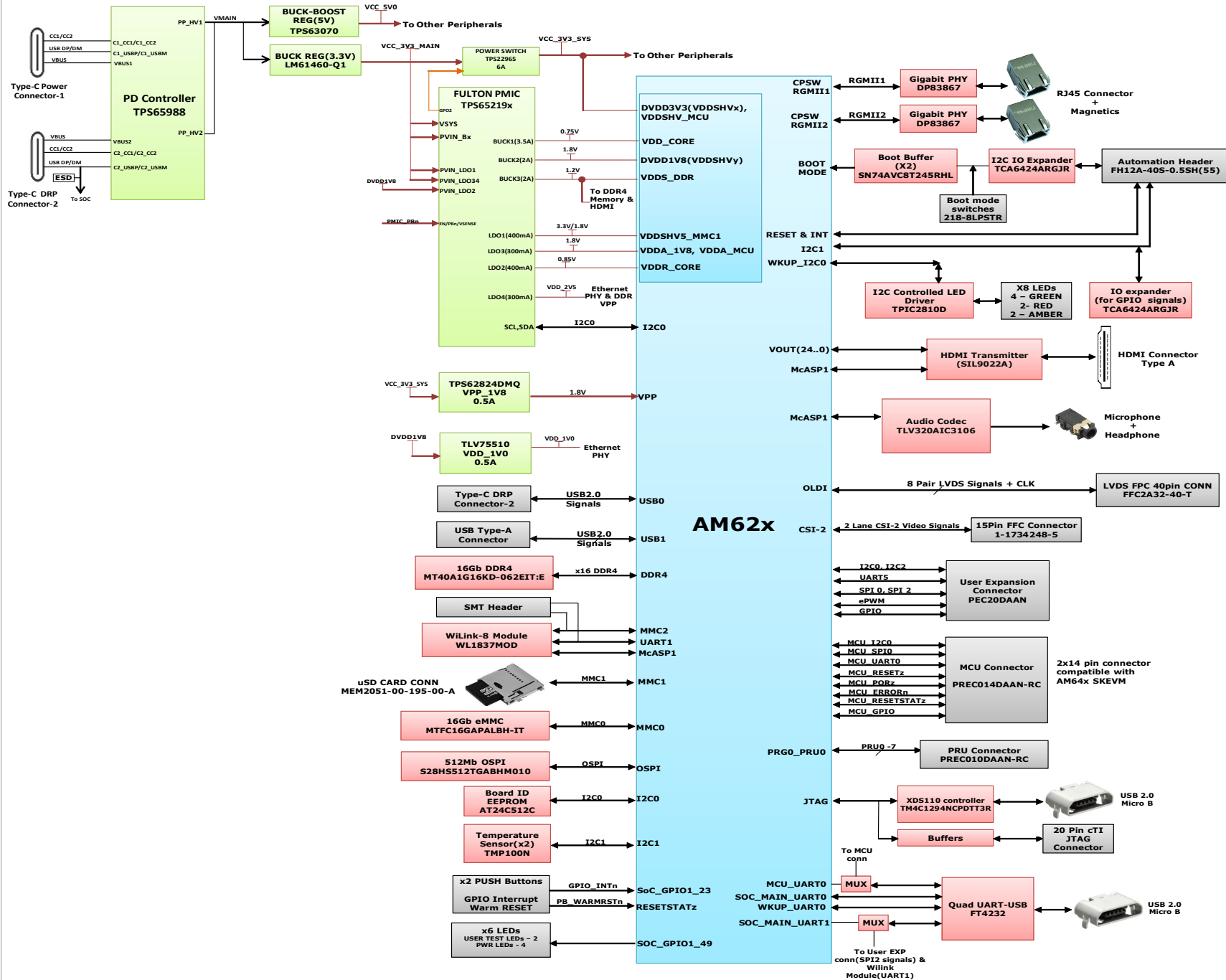
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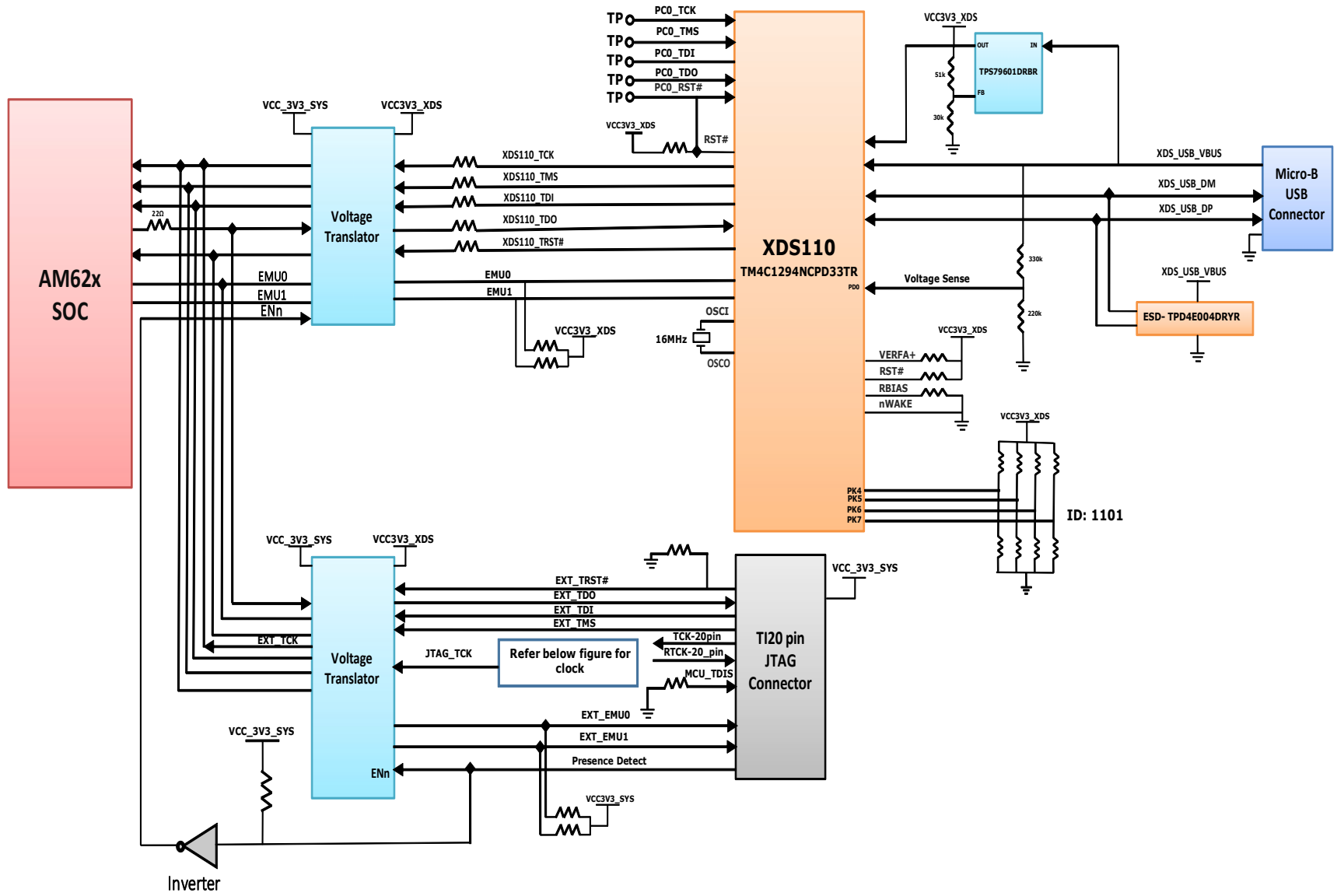
Title REVISION HISTORY

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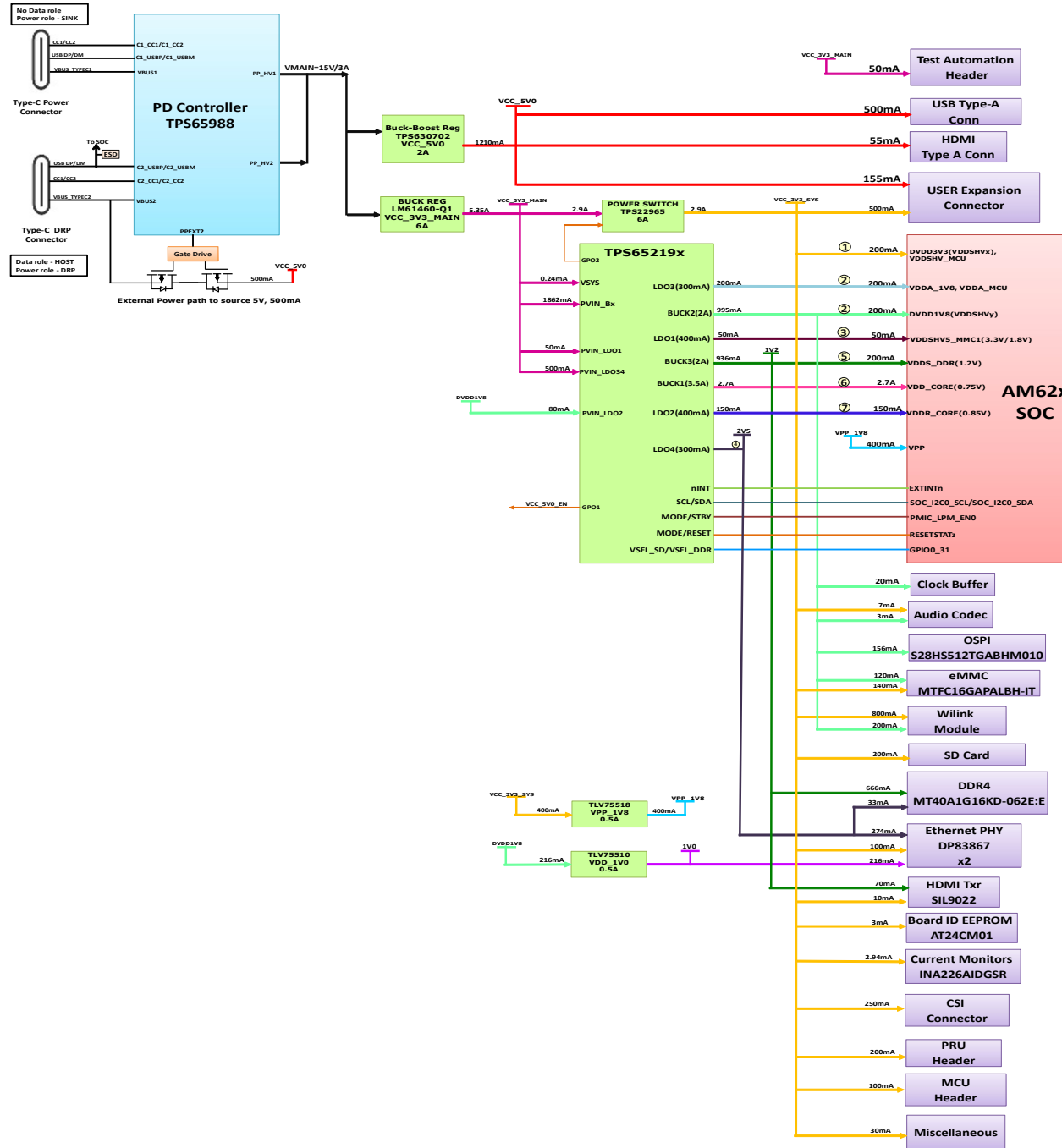
# BLOCK DIAGRAM



# BLOCK DIAGRAM\_XDS110



# POWER BLOCK DIAGRAM



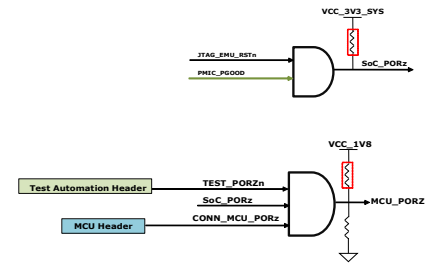
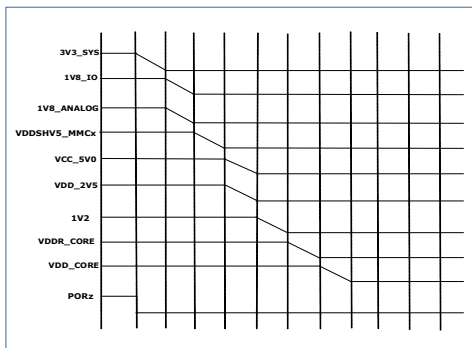
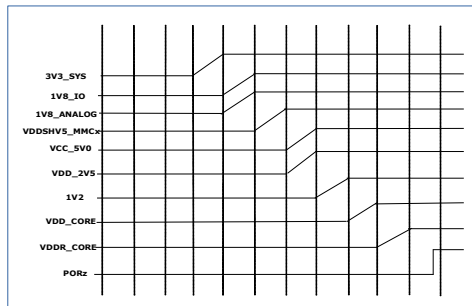
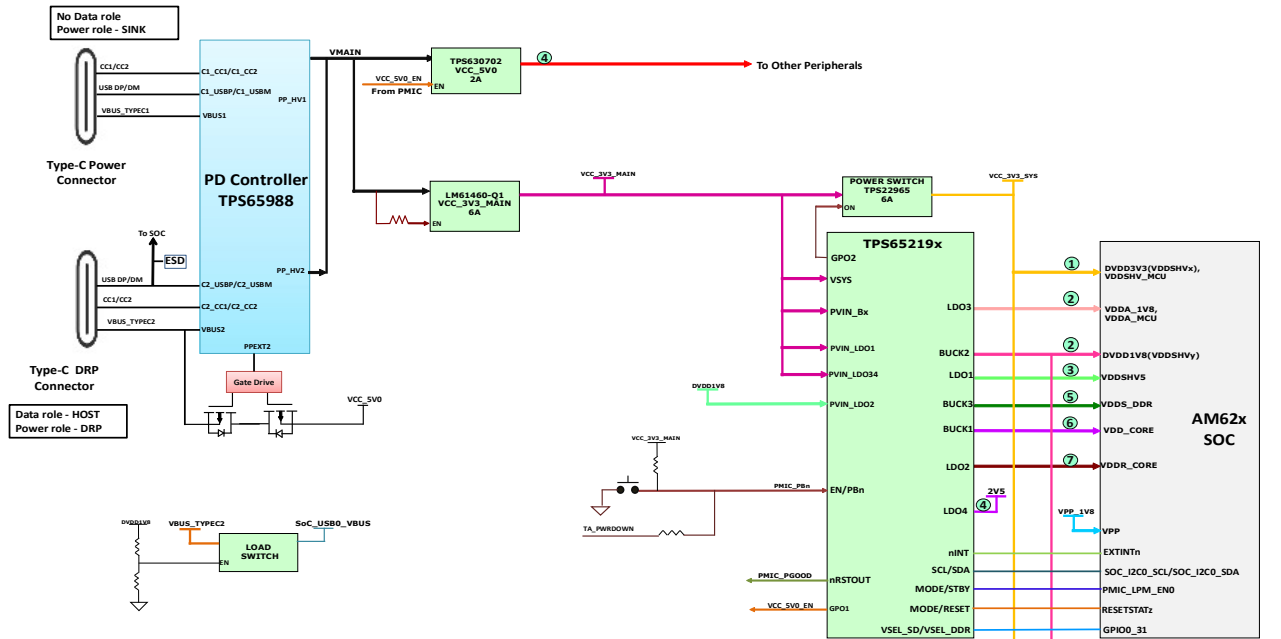
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Title: POWER BLOCK DIAGRAM

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# POWER SEQUENCE

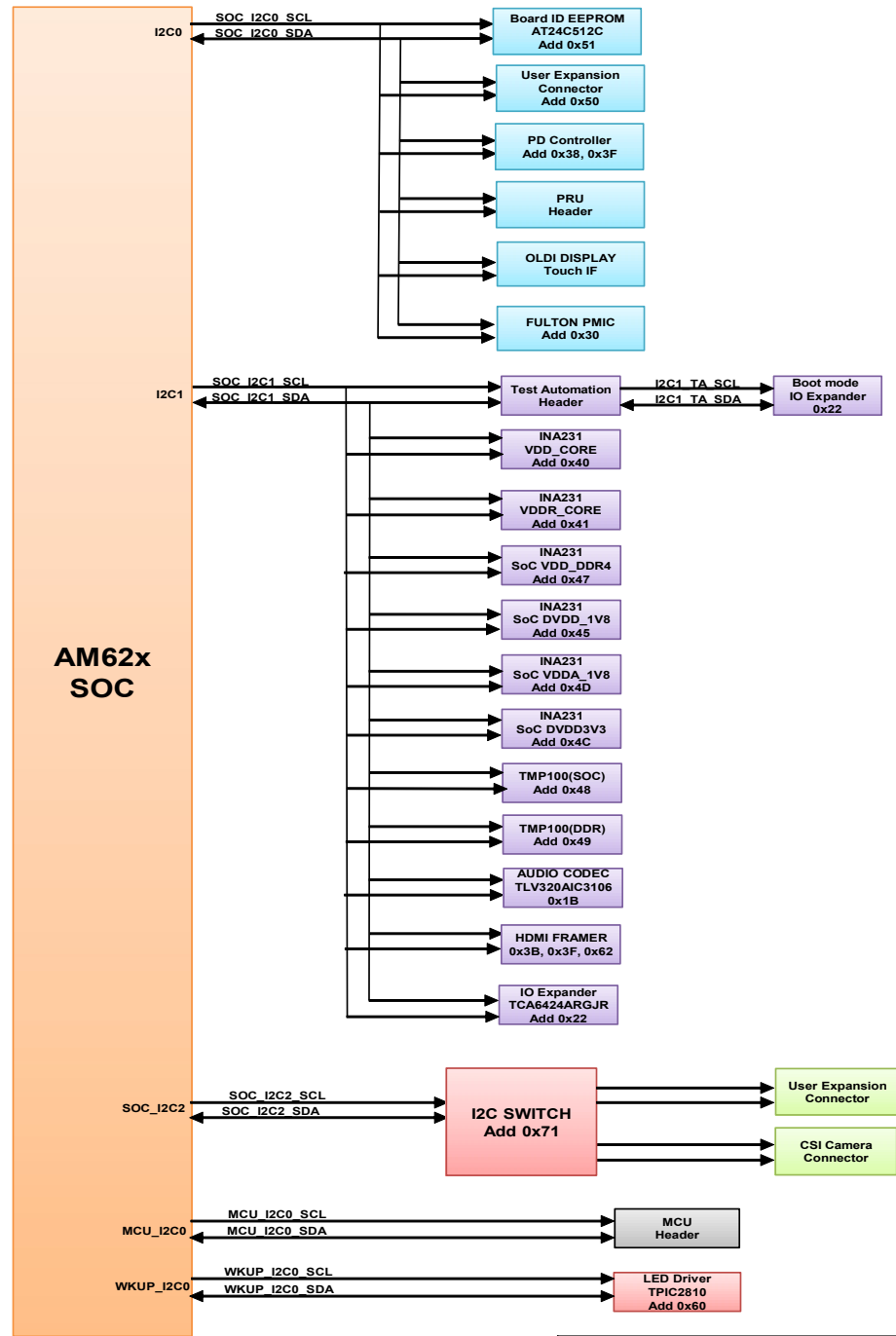


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# I2C TREE



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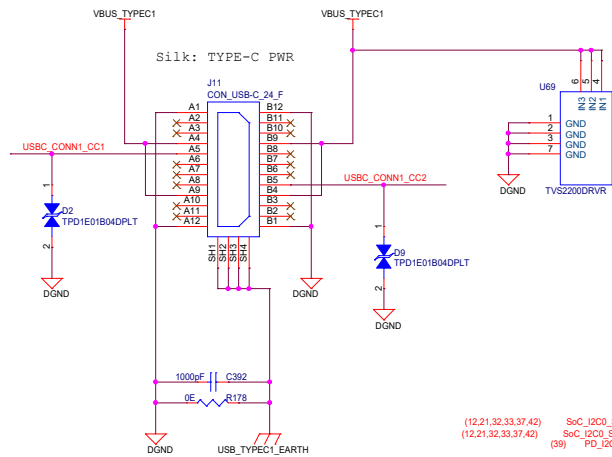
## GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_1	MCU_SPI0_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
	PRU Connector Interrupt									
	PMIC_INTn									
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMD0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	SoC_GPIO1_23	UART0_RTSM	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	User Interrupt Push Button/ TEST GPIO1 from Test Automation Connector									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
<b>IO EXPANDER - 01</b>										
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P00		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER - P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER - P10		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER - P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	UART1 FET Switch and Buffer Enable signal	UART1_FET_BUF_EN	ENABLE	IO EXPANDER - P12		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	PD Controller Interrupt	PD_I2C_IRQ	INTERRUPT	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP1 FET Switch Enable	MCASP1_FET_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20	MCASP1 Level Translator buffer for BT Enable	MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER - P23		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
21	MCASP1 FET Switch select pin status	MCASP1_FET_SEL	GPIO	IO EXPANDER - P24		INPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
22	SOC UART1 FET Switch Select	UART1_FET_SEL	SELECT	IO EXPANDER - P25		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INT#	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3

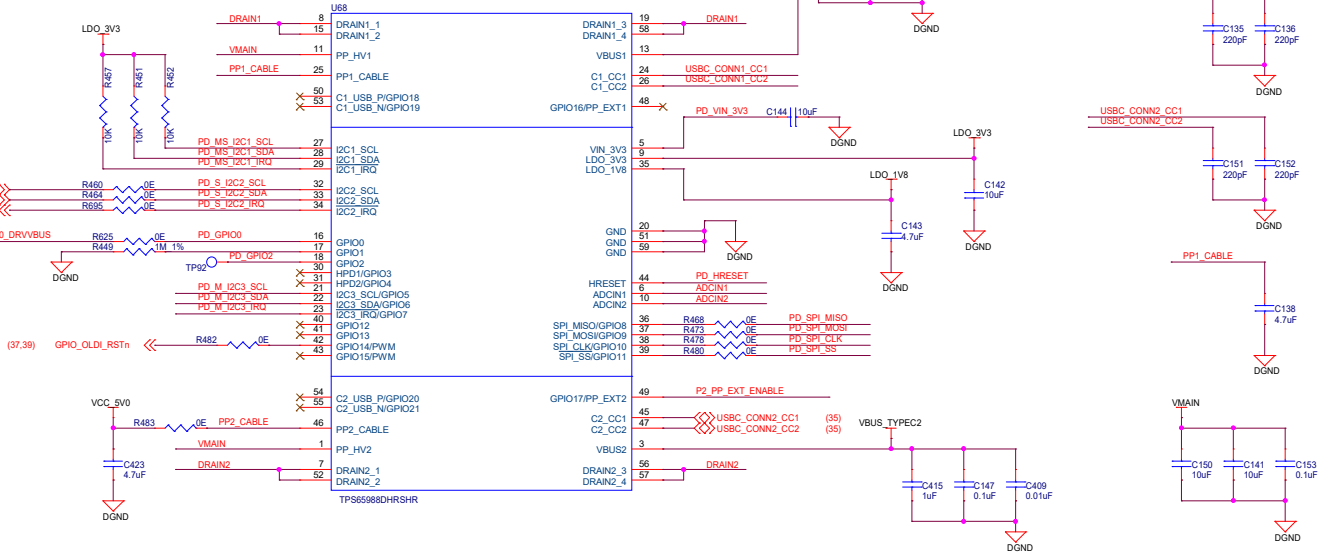
Designed for TI by Mistral Solutions Pvt Ltd		Title: GPIO MAPPING TABLE	
 <b>TEXAS INSTRUMENTS</b>	 <b>MISTRAL</b>	Size: PROC142E1	Rev: E1
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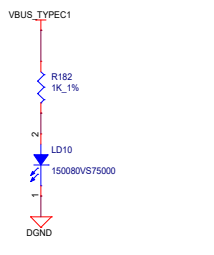
# USB TYPE-C POWER



## TYPE-C DUAL PD CONTROLLER

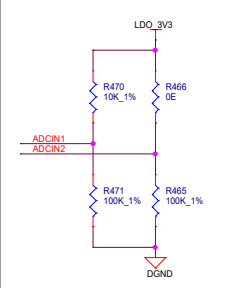


### POWER INDICATION LED: VBUS\_TYPEC1

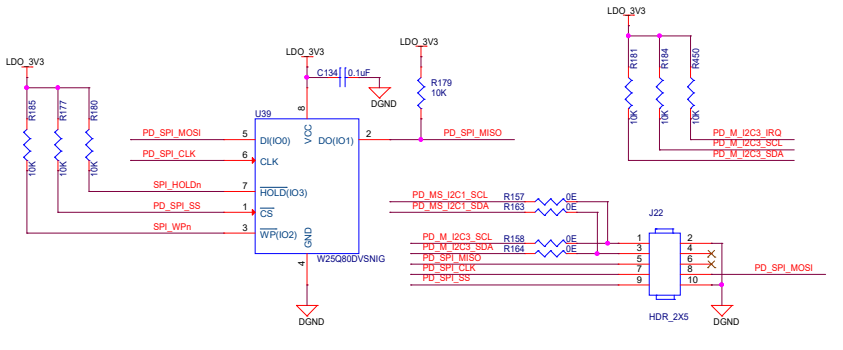


I2C Slave Address	Port1	Port2
I2C2 (Default)	0x38	0x3F
I2C1	0x20	0x24

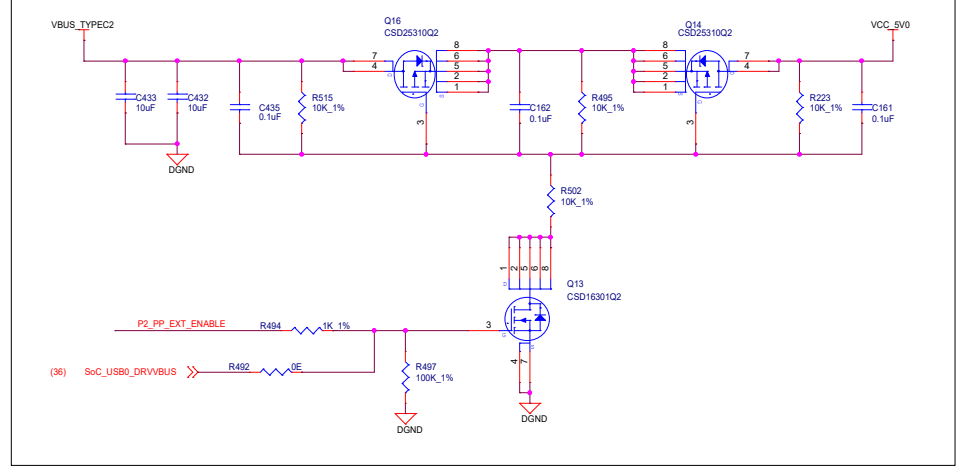
### BP NoWait Safe Configuration



### SPI EEPROM & PROGRAMMING HEADER



### EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A

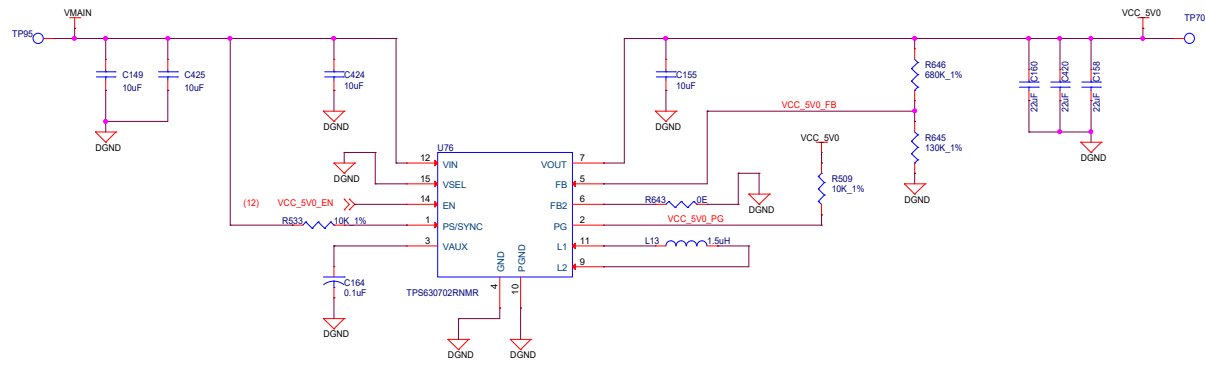


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# PERIPHERAL POWER SUPPLY-1



## GROUND TEST POINTS



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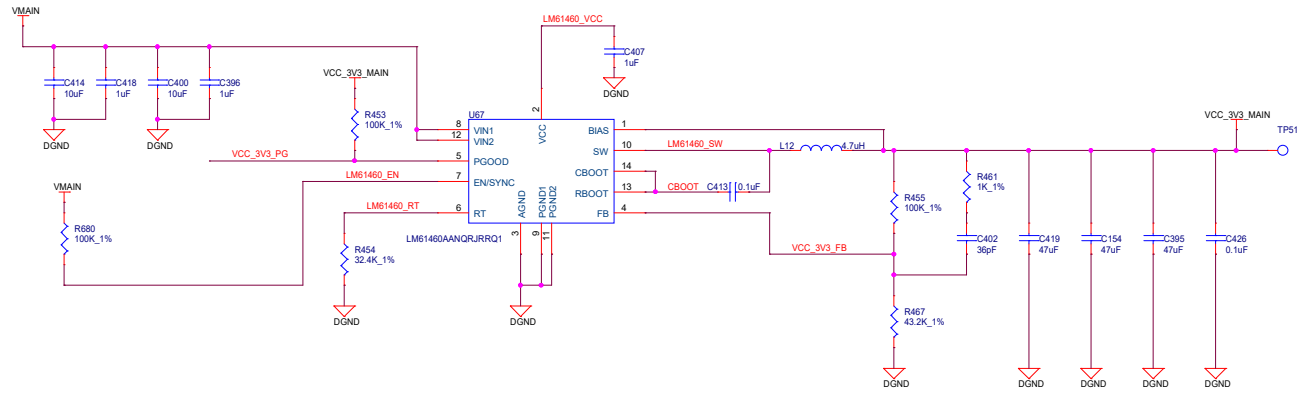
Title PERIPHERAL POWER SUPPLY -1

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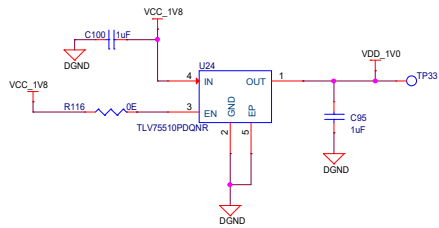
# PERIPHERAL POWER SUPPLY-2

VinMin = 4.5V  
 VinMax = 24V  
 Vout = 3.3V @ 6A

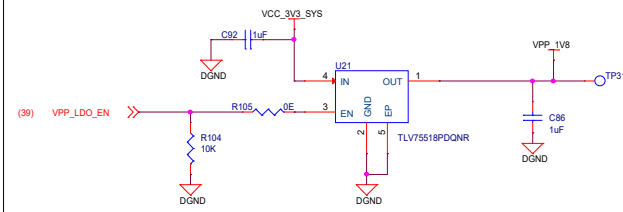
## 3.3V, 6.0AMPS SUPPLY



## 1.0V, 0.5AMPS SUPPLY (ETHERNET)



## 1.8V VPP, 0.5AMPS SUPPLY



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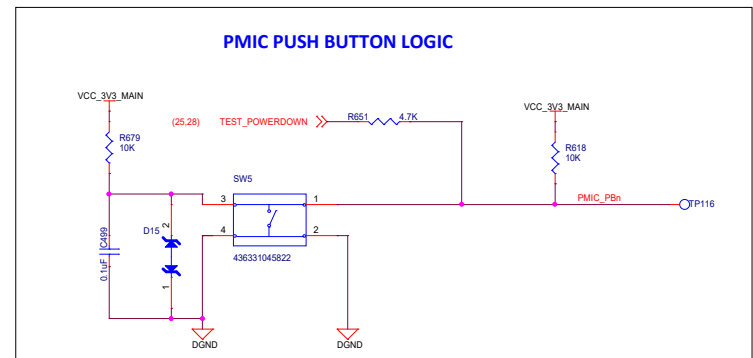
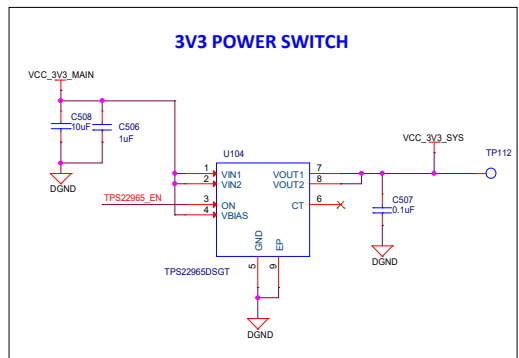
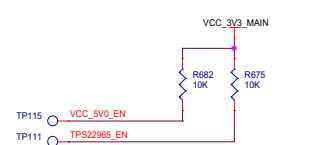
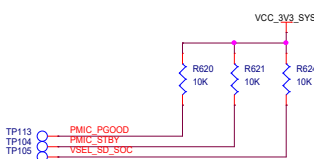
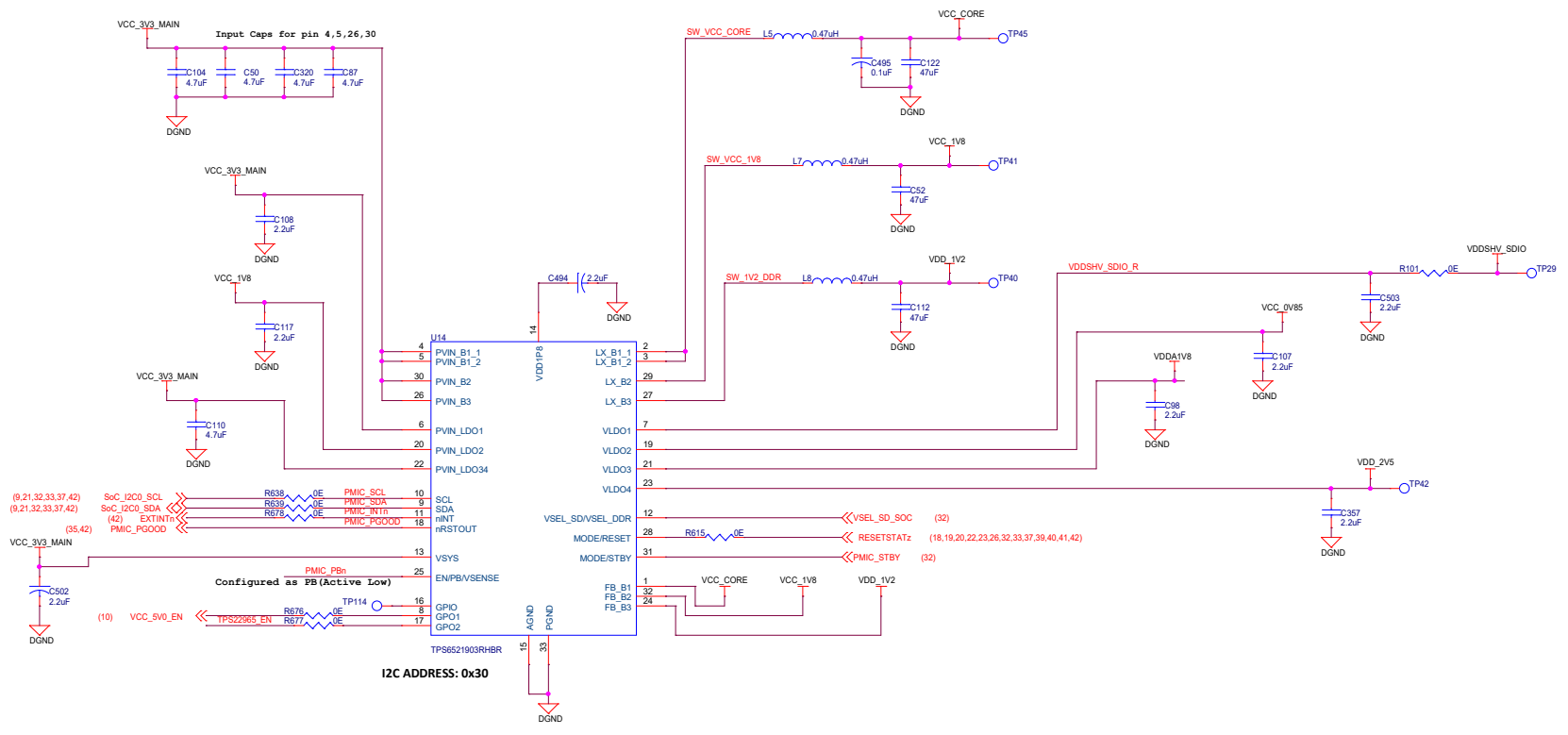


Title PERIPHERAL POWER SUPPLY-2

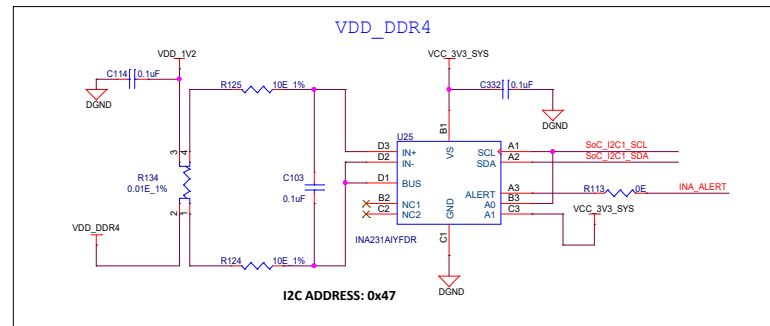
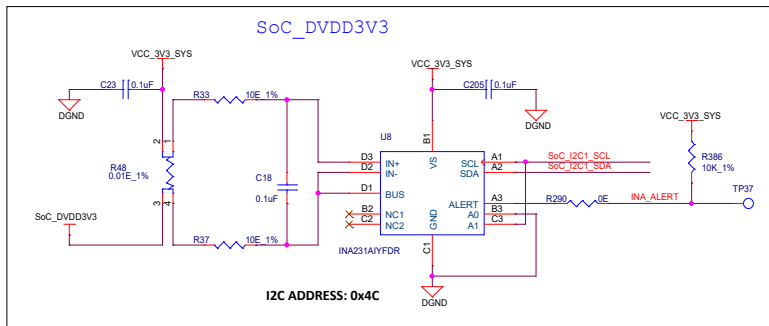
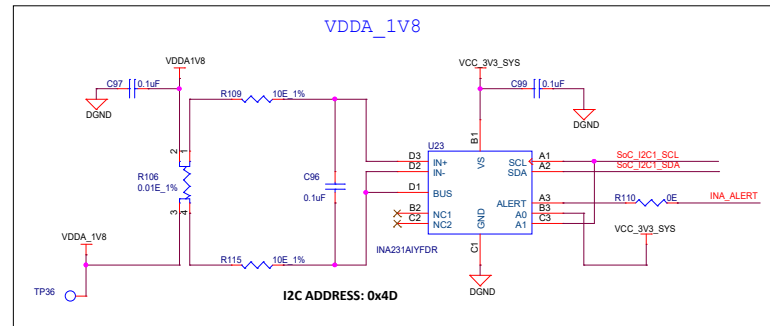
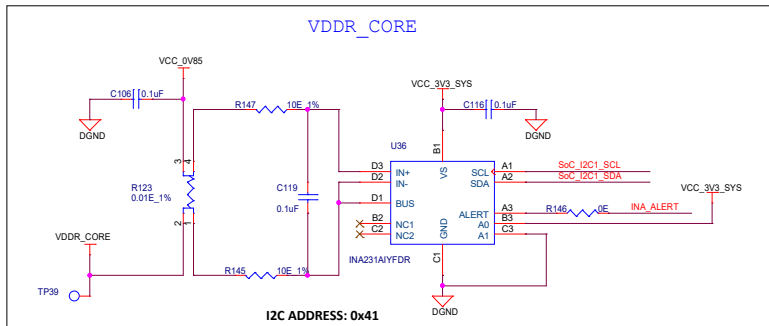
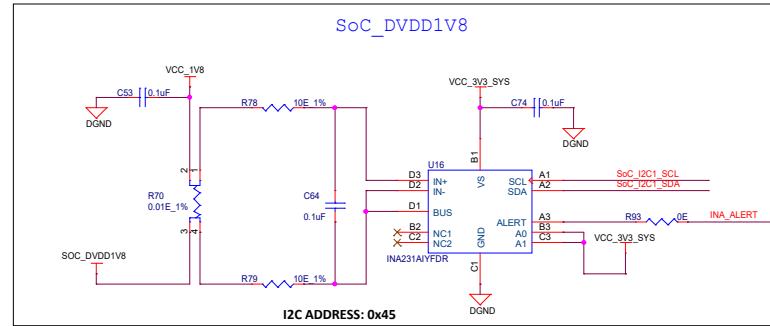
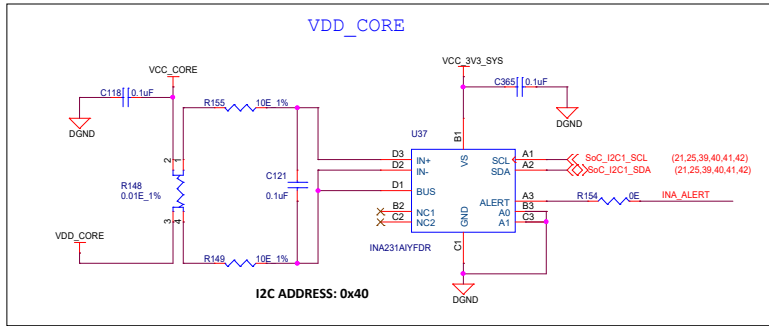
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# FULTON PMIC

PMIC REGULATORS	VOLTAGE RAIL	CURRENT (mA)
BUCK 1	VCC_CORE (0.75V)	2700
BUCK 2	VCC_1V8	995
BUCK 3	VDD_1V2	936
LDO 1	VDDSHV_SDIO	50
LDO 2	VDDR_CORE	150
LDO 3	VDDA_1V8	200
LDO 4	VDD_2V5	300



# CURRENT MONITORING DEVICES



RES Option to short VDD\_CORE and VDDR\_CORE rails when both are 0.85V (Both should be generated from the same source)



CORE SUPPLY	ARRAY CORE SUPPLY	Assembly
0.75 VDD_CORE	0.85 VDDR_CORE	DNI R699 and Mount R123
0.85 VDD_CORE	0.85 VDDR_CORE	DNI R123 and Mount R699

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_DV85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V2_DDR	VDD_DDR4	47

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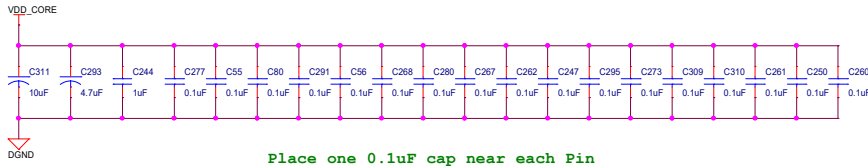
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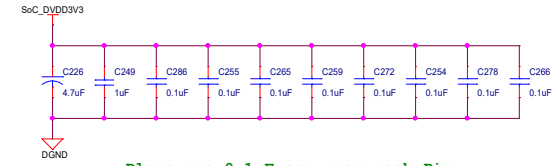
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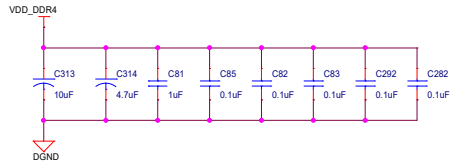
# SOC POWER DECAPS



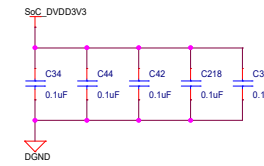
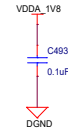
Place one 0.1uF cap near each Pin



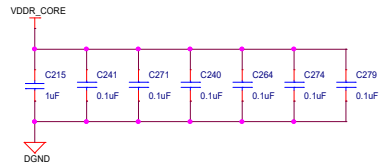
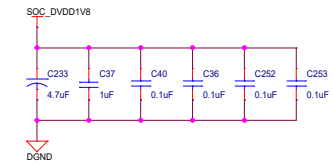
Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin



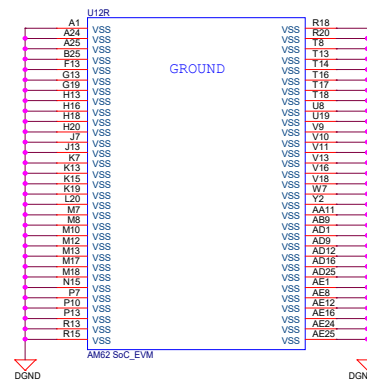
Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin



# SOC VSS



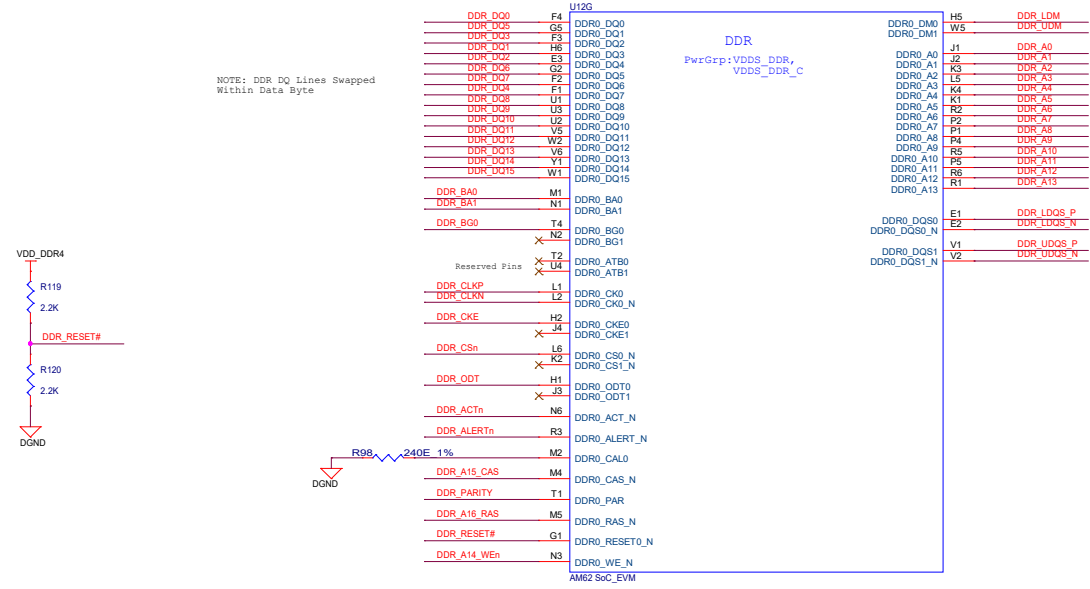
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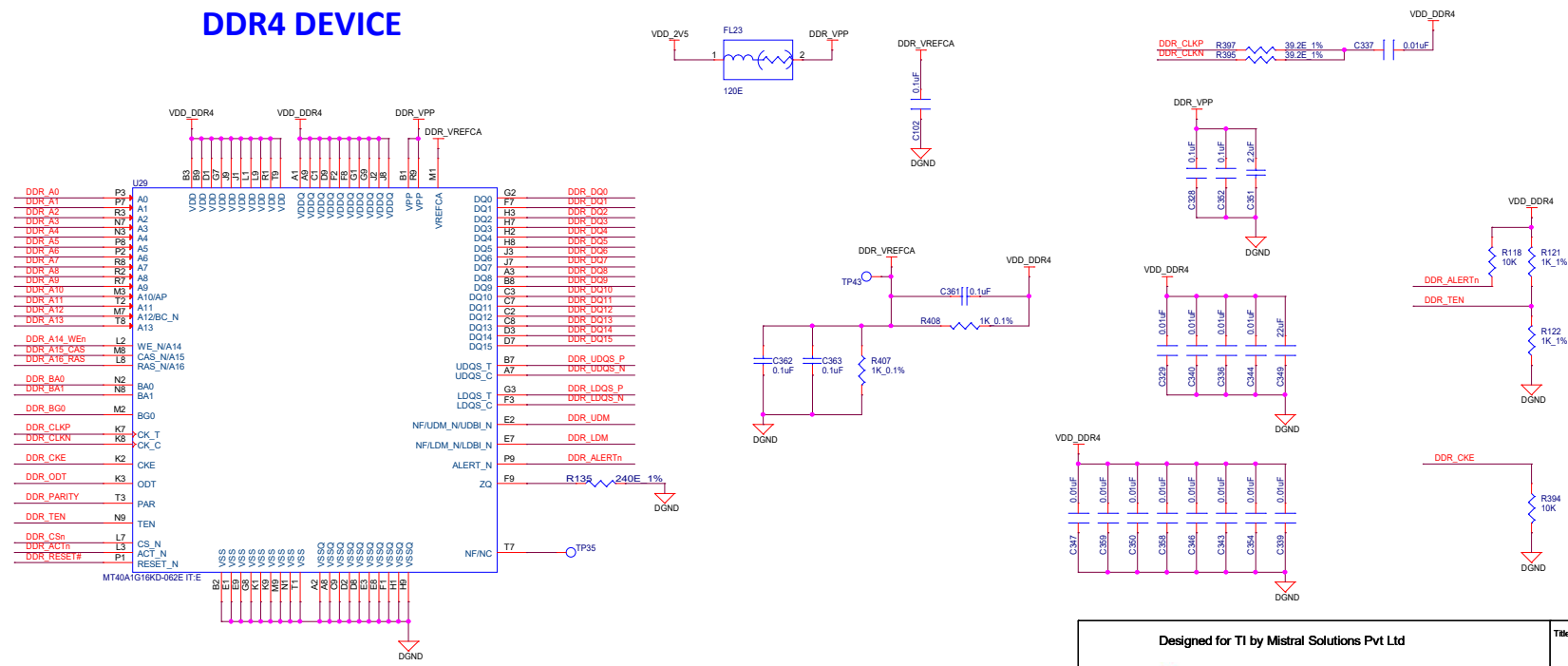
Title: SOC POWER CAPS & SOC VSS

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# SOC DDR INTERFACE

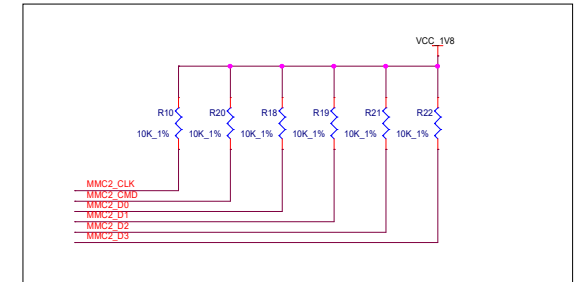
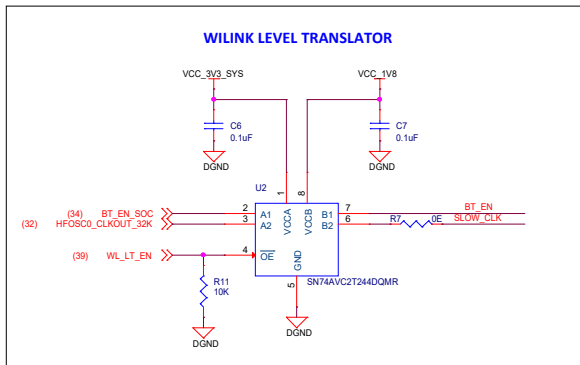
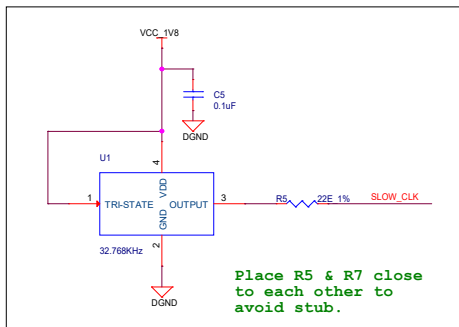
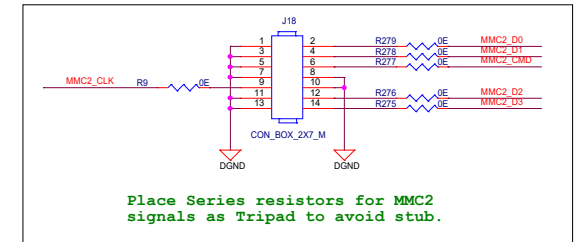
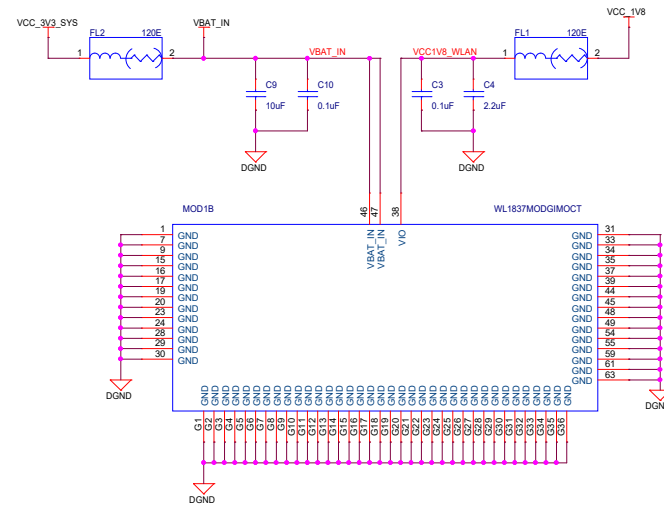
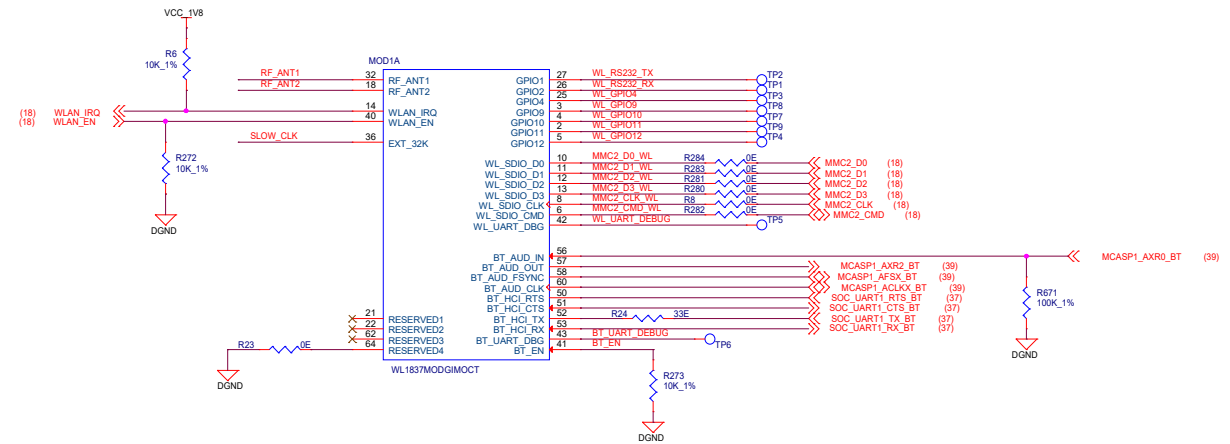
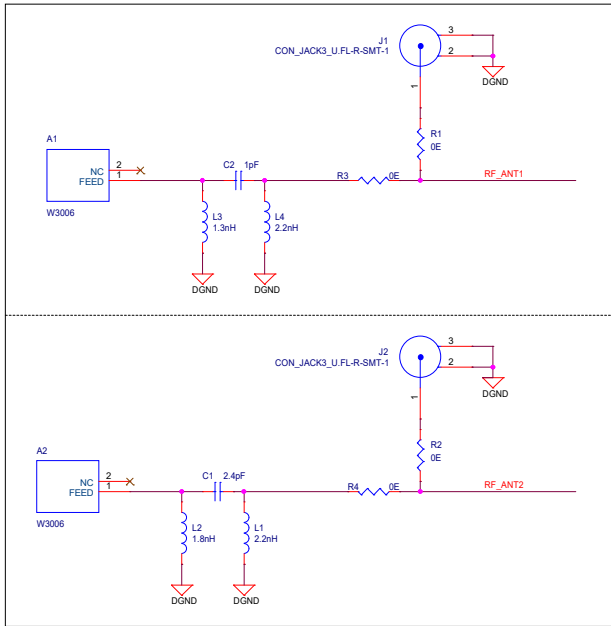


# DDR4 DEVICE

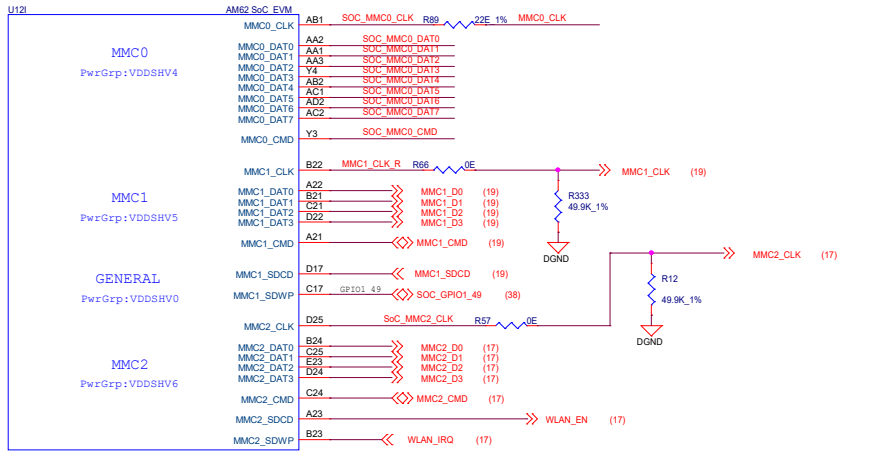




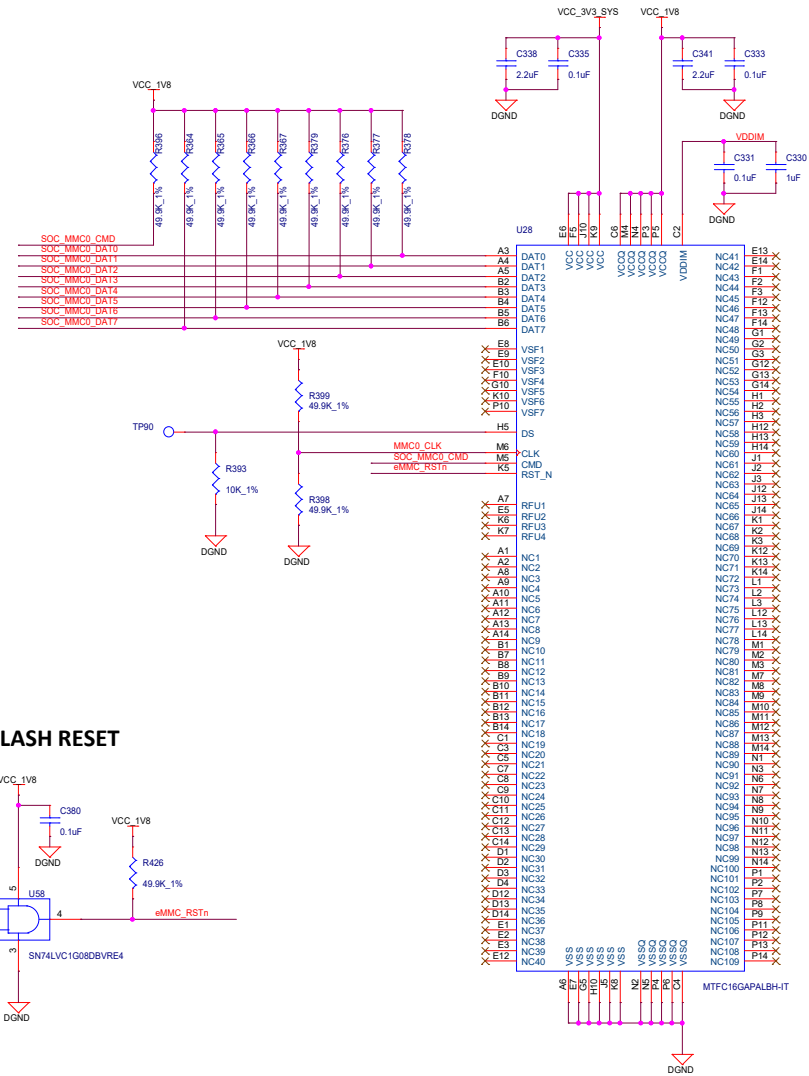
# WL1837 MODULE



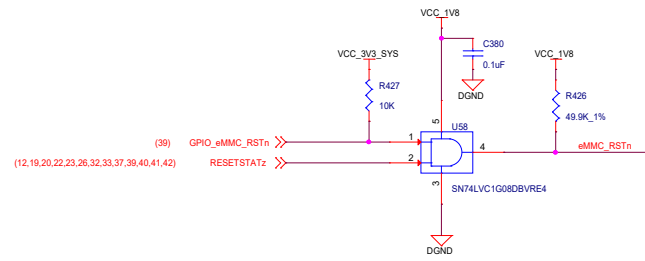
## SOC - MMC Interface



## eMMC FLASH



## eMMC FLASH RESET



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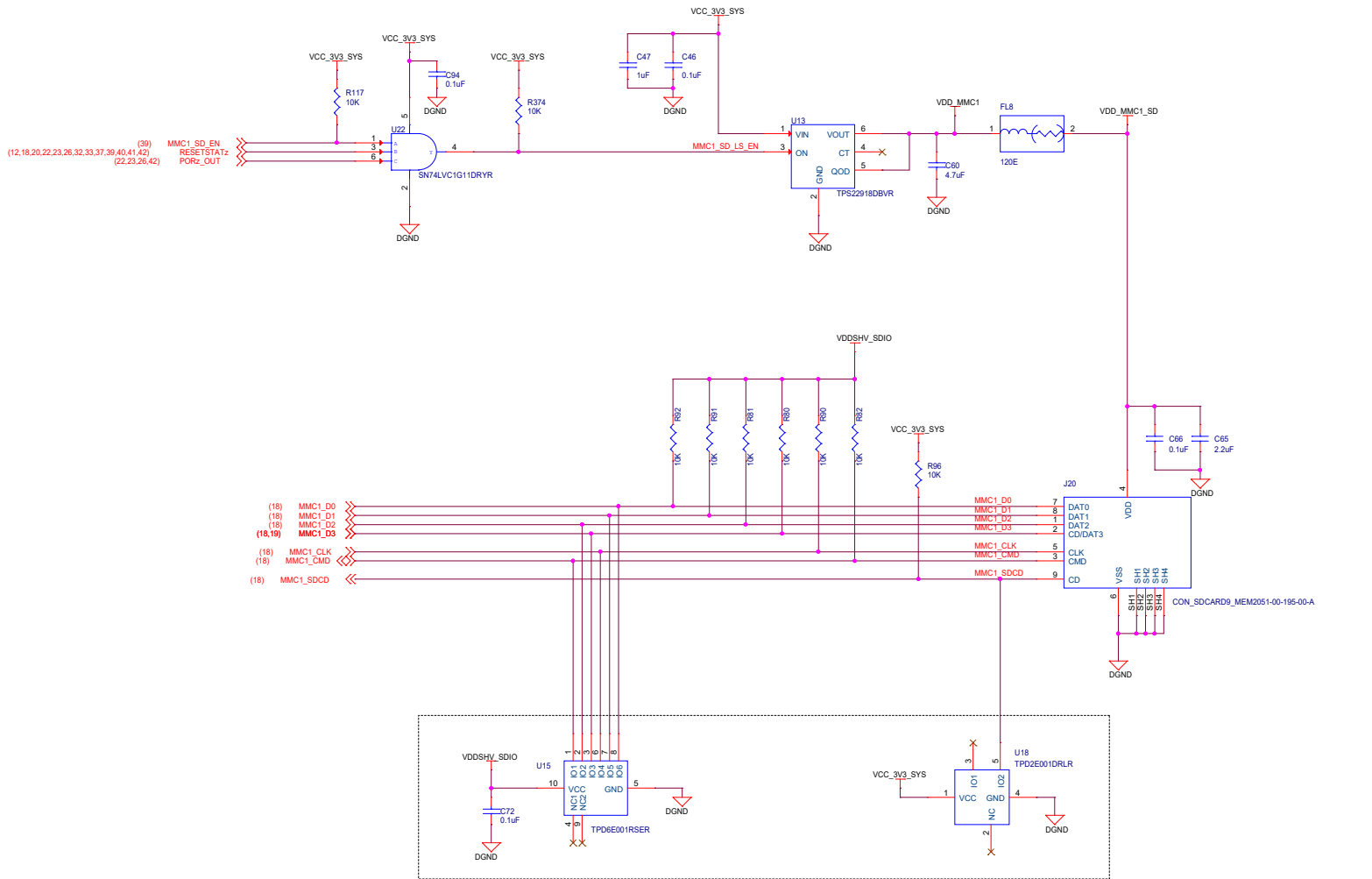
Title: eMMC FLASH INTERFACE

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# SD CARD INTERFACE

## SD CARD RESET

## LOAD SWITCH



Place near SD Card Connector

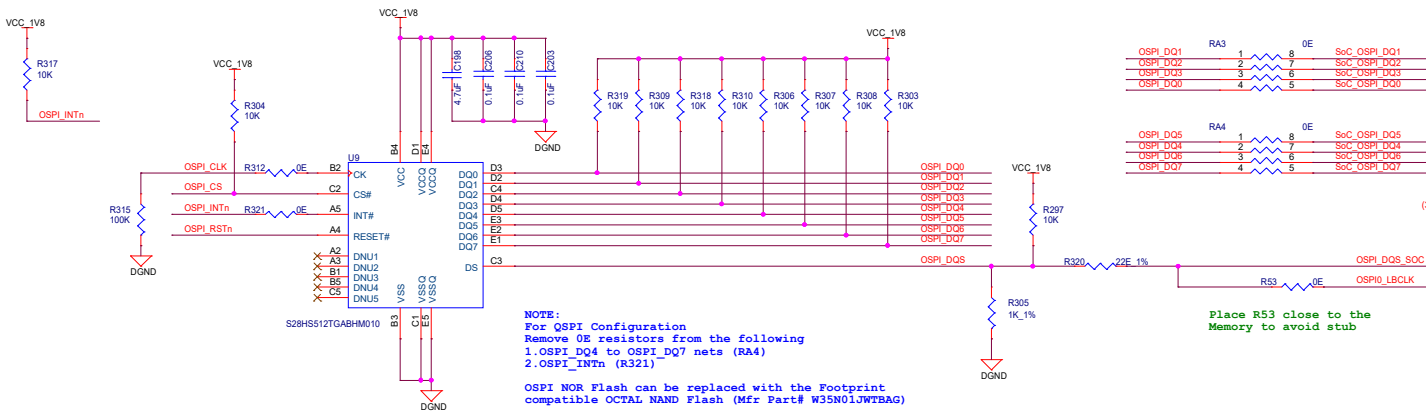
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Title SD CARD INTERFACE

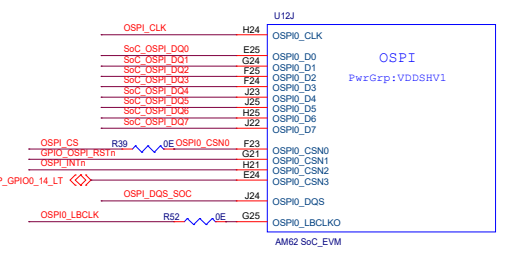
Size	PROC142E1	Rev	E1
Date:	Friday, September 16, 2022	Sheet	19 of 44

# OSPI FLASH



**NOTE:**  
 For QSPI Configuration  
 Remove OE resistors from the following  
 1. OSPI\_DQ4 to OSPI\_DQ7 nets (RA4)  
 2. OSPI\_INTn (R321)  
 OSPI NOR Flash can be replaced with the Footprint compatible OCTAL NAND Flash (Mfr Part# W35N01JWTDAG)

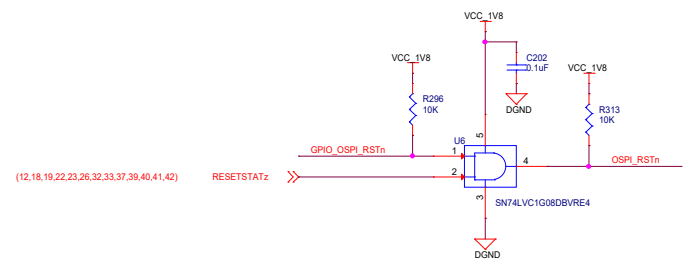
# SOC OSPI INTERFACE



Place R52 close to the SOC Ball with as little trace as possible

Place R53 close to the Memory to avoid stub

# OSPI FLASH RESET

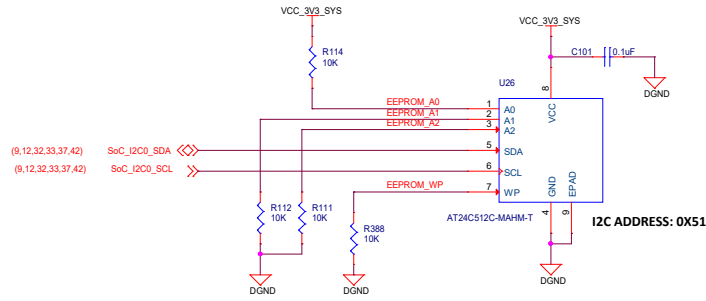


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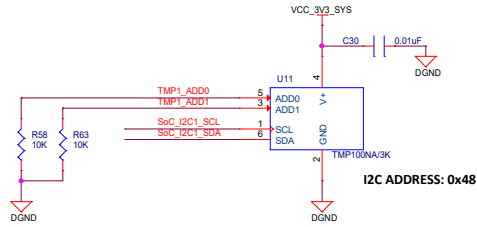


Title		OSPI INTERFACE	
Size	PROC142E1	Rev	E1
Date:	Friday, September 16, 2022	Sheet	20 of 44

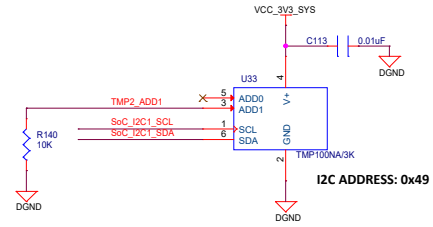
# BOARD ID EEPROM



# TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR U11 CLOSE TO SoC



CAD NOTE: PLACE TEMP SENSOR U33 CLOSE TO DDR4



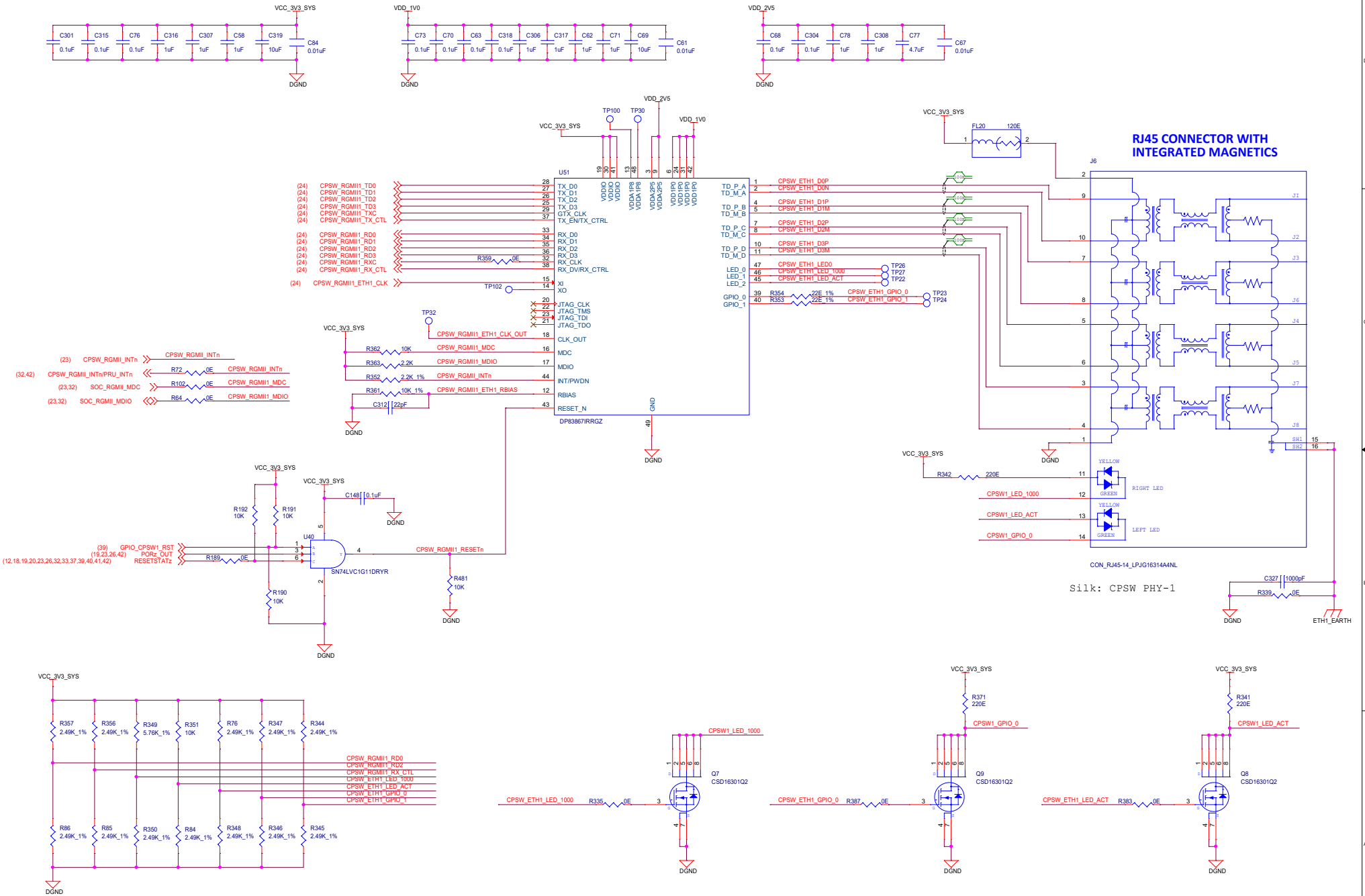
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Title: BOARD ID EEPROM & TEMPERATURE SENSORS

Size	PROC142E1	Rev	E1
Date:	Friday, September 16, 2022	Sheet	21 of 44

# CPSW RGMII 1 - PHY



- (23) CPSW\_RGMII\_INTn >> CPSW\_RGMII\_INTn
- (32,42) CPSW\_RGMII\_INTnPRU\_INTn << R72 0E CPSW\_RGMII\_INTn
- (23,32) SOC\_RGMII\_MDC << R102 0E CPSW\_RGMII\_MDC
- (23,32) SOC\_RGMII\_MDIO << R64 0E CPSW\_RGMII\_MDIO

- (39) GPIO\_CPSW1\_RST (19,23,26,42) PORz\_OUT RESETSTATz

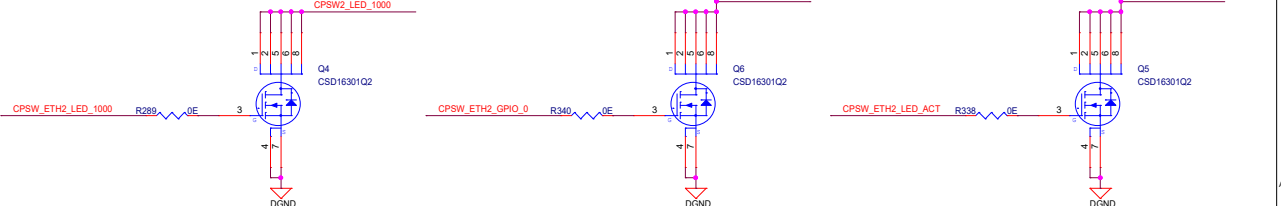
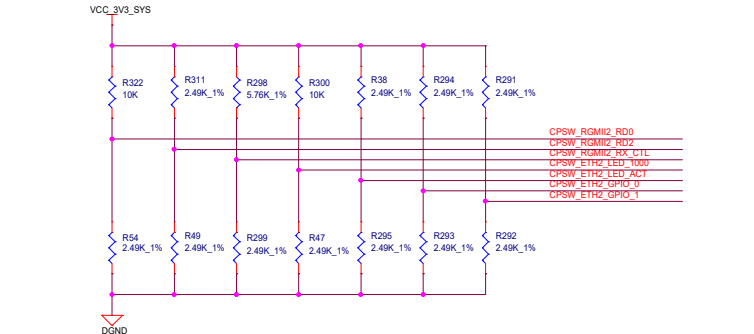
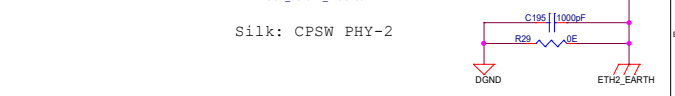
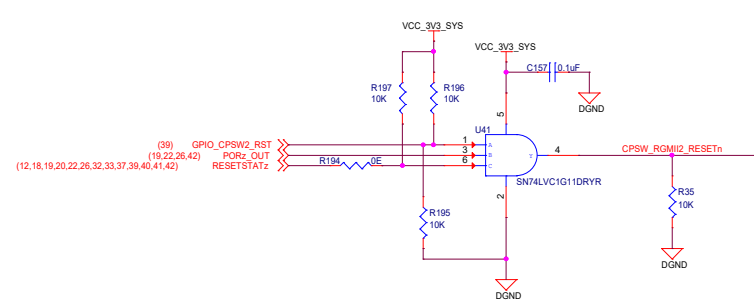
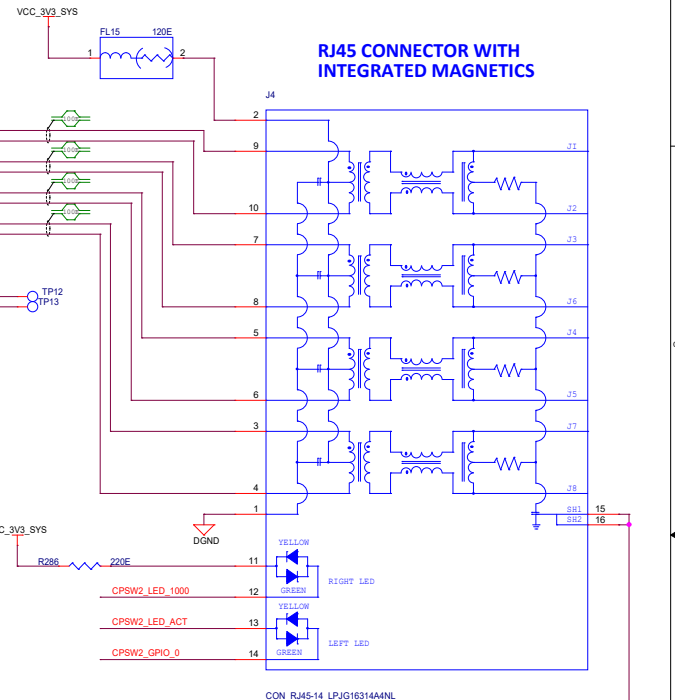
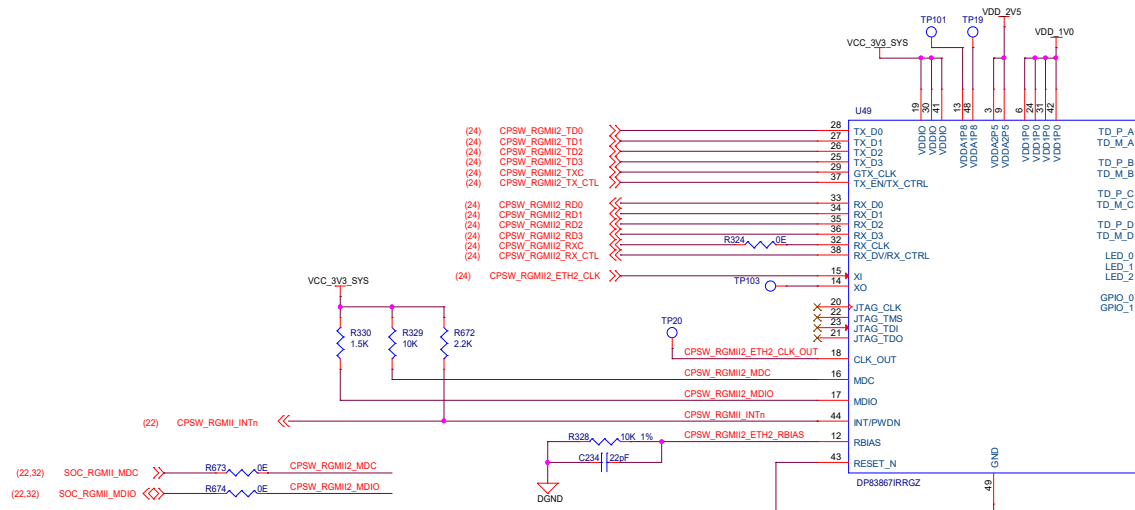
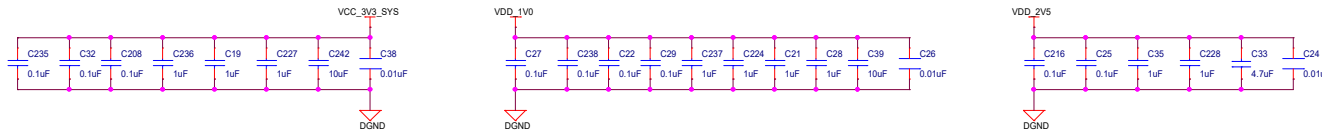
PHY ADDRESS = 00000  
 Auto-negotiation Enabled  
 10/100/1000 advertised, Auto-MDI-X  
 Tx Clock Skew = 0ns  
 Rx Clock Skew = 2ns

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**TEXAS INSTRUMENTS** **MISTRAL**

Title: CPSW RGMII_1 ETHERNET PHY	
Size: C	Rev: E1
Date: Friday, September 16, 2022	Sheet 22 of 44

# CPSW RGMII 2 - PHY



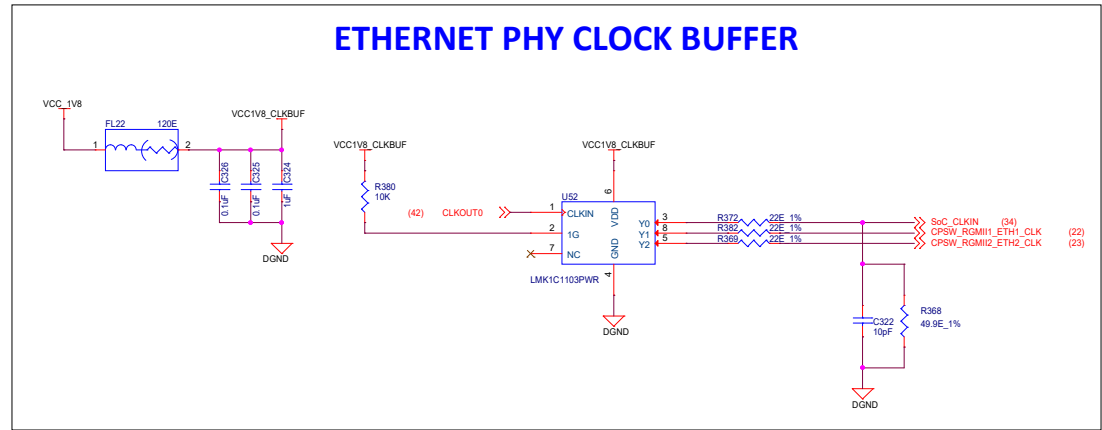
PHY ADDRESS = 00001  
 Auto-negotiation Enabled  
 10/100/1000 advertised, Auto-MDI-X  
 Tx Clock Skew = 0ns  
 Rx Clock Skew = 2ns

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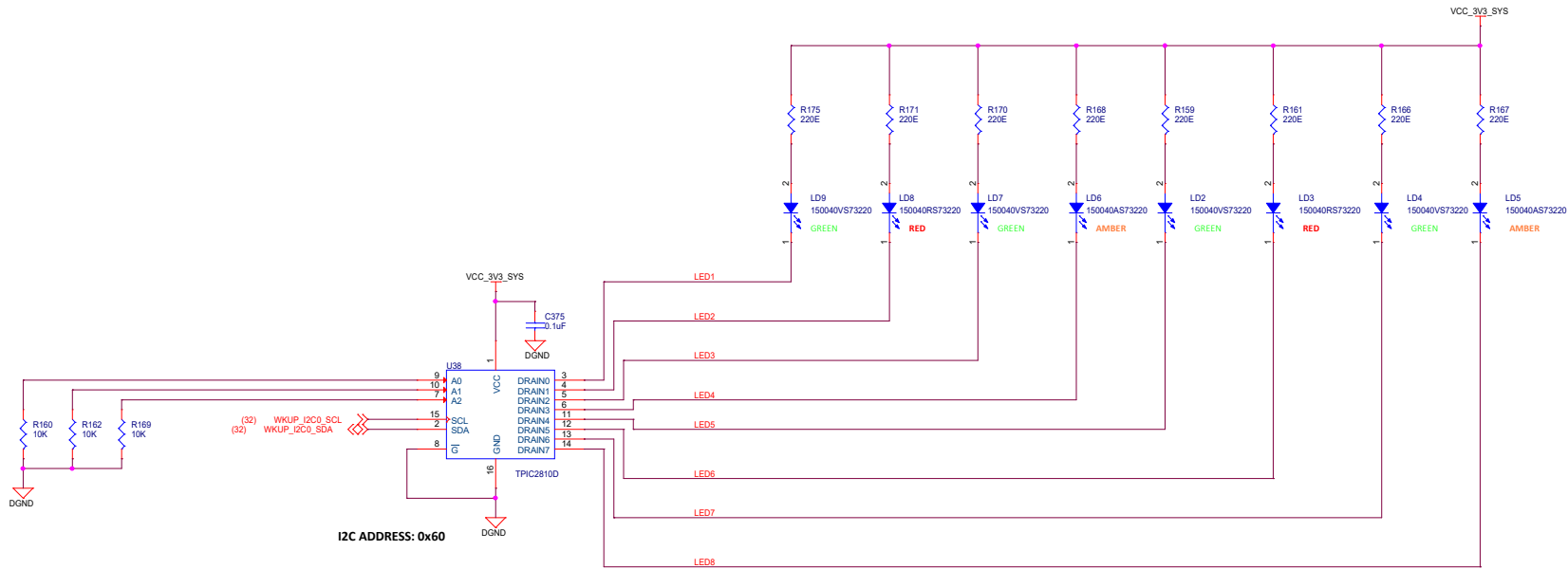
Title		CPSW RGMII 2 ETHERNET PHY	
Size	PROC142E1	Rev	E1
C		Date:	Friday, September 16, 2022
Sheet	23	of	44



## ETHERNET PHY CLOCK BUFFER



## LED DRIVER



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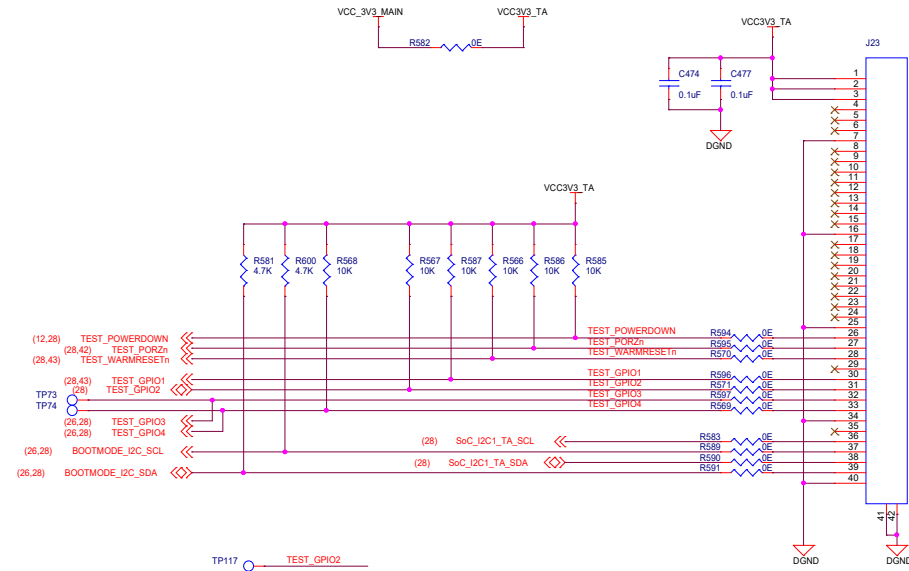
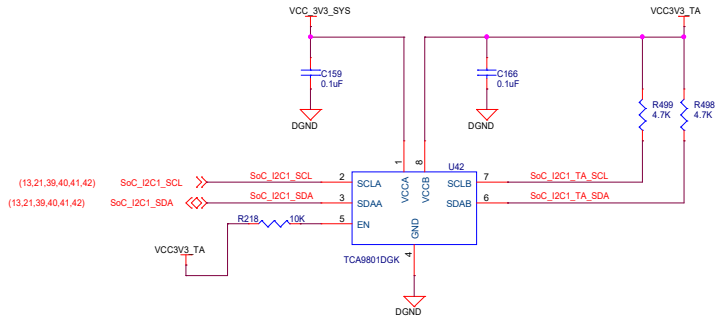
Title: ETHERNET PHY CLOCK BUFFER & LED DRIVER

Size	PROC142E1	Rev	E1
Date:	Friday, September 16, 2022	Sheet	24 of 44



# 40-PIN TEST AUTOMATION HEADER

## I2C BUS BUFFER



CON\_FLEX\_40X1\_FH12A-40S-0.5SH

Silk: AUTOMATION HDR

## TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETr	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on MCU_GPIO0_15 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to a Testpoint	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

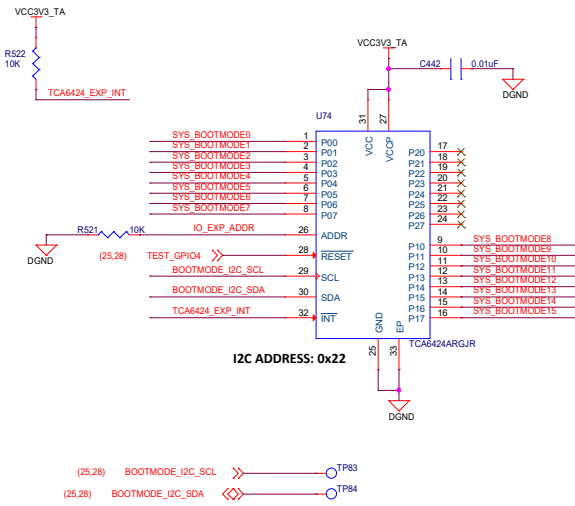
Designed for TI by Mistral Solutions Pvt Ltd



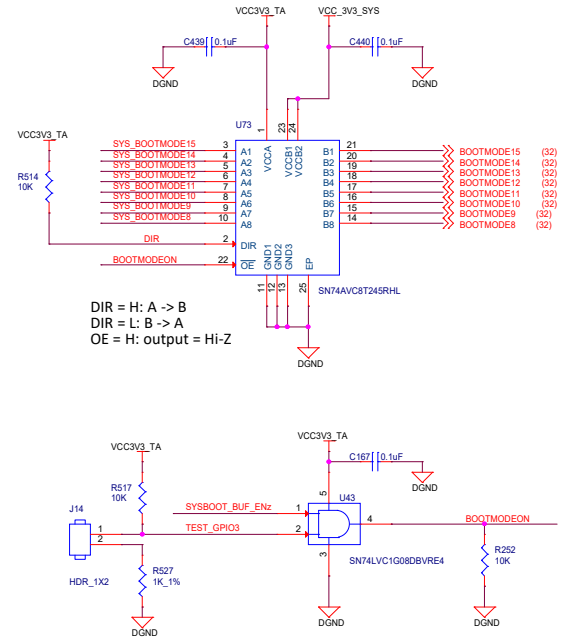
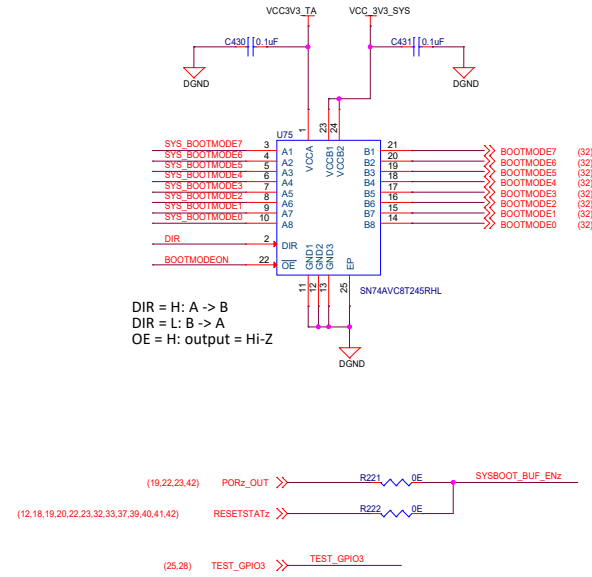
Title: TEST AUTOMATION

Size	PROC142E1	Rev	E1
Date:	Friday, September 16, 2022	Sheet	25 of 44

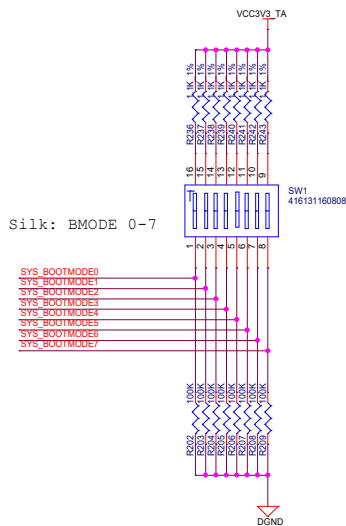
## BOOTMODE IO EXPANDER



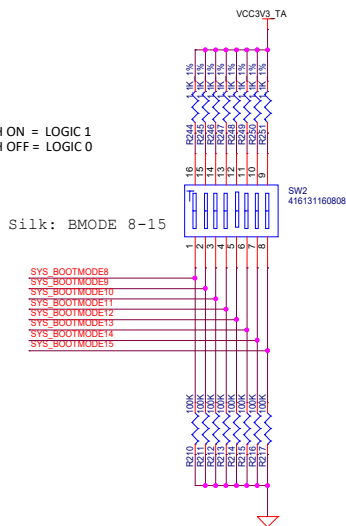
## BOOT MODE BUFFERS



## BOOT MODE SWITCHES



SWITCH ON = LOGIC 1  
SWITCH OFF = LOGIC 0



### BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. BACKUP BOOT OPTION

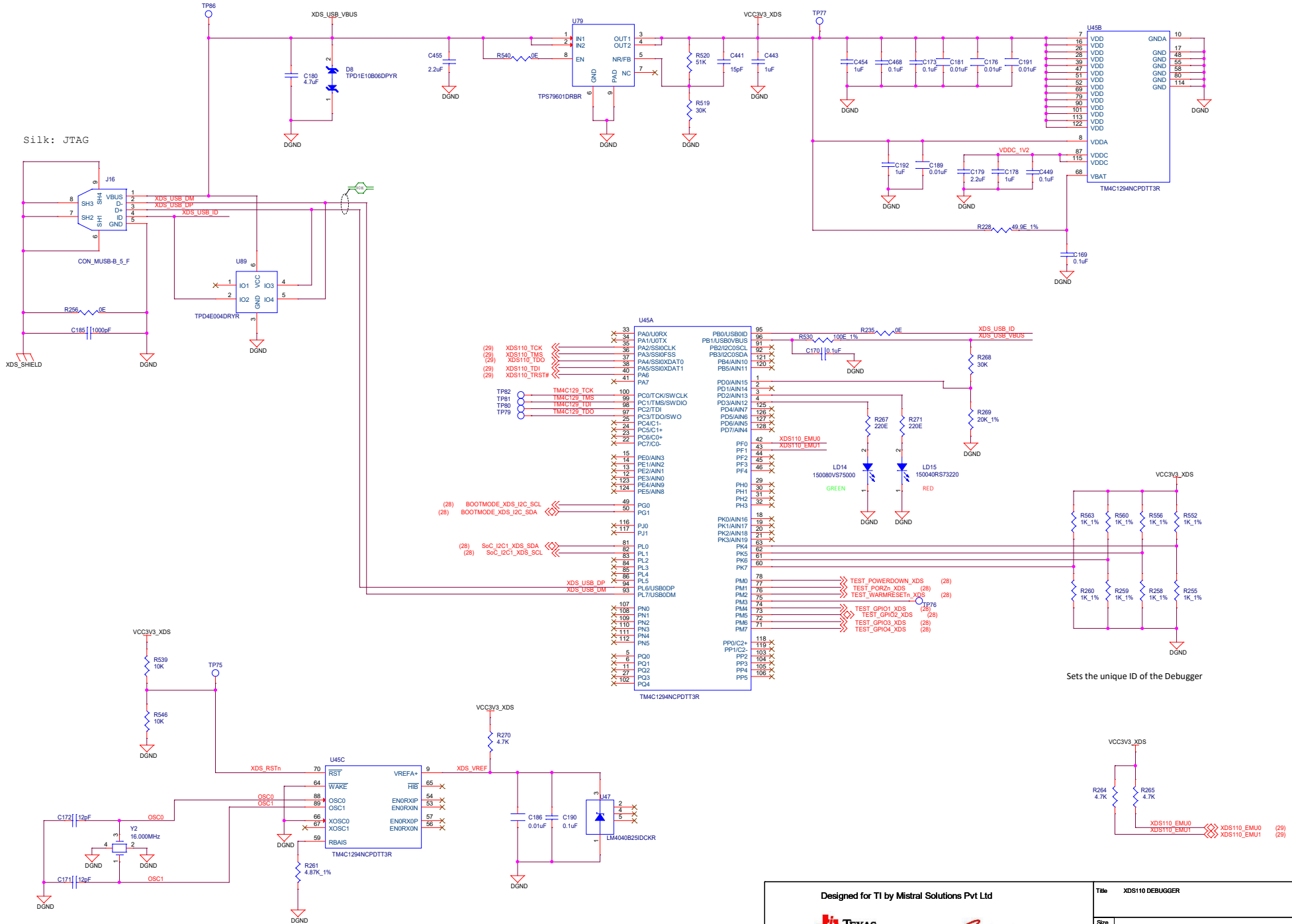
Designed for TI by Mistral Solutions Pvt Ltd



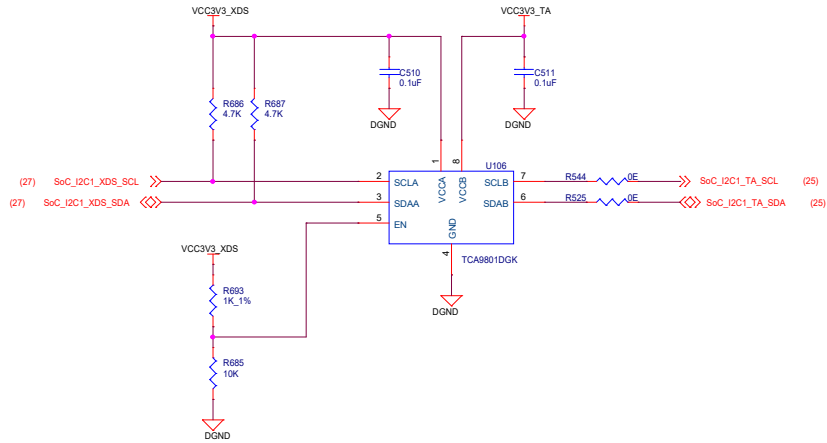
Title: BOOT MODE BUFFER & SWITCHES

Size: PROC142E1  
C: Rev: E1  
Date: Friday, September 16, 2022  
Sheet: 26 of 44

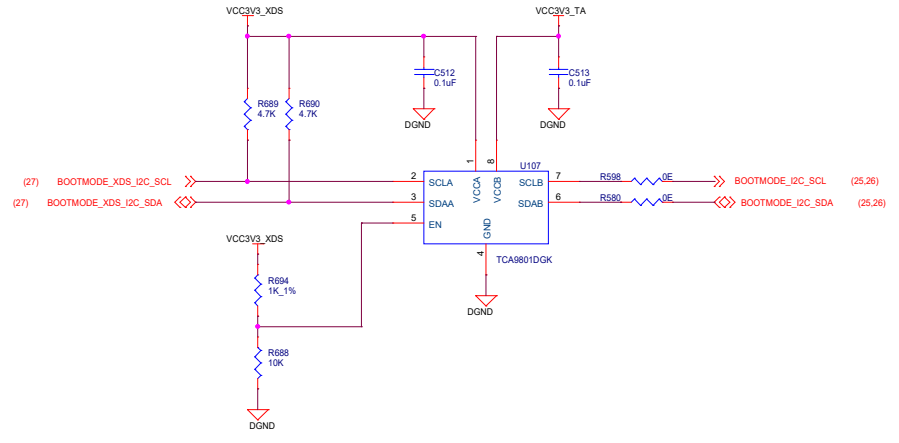
# XDS110 DEBUGGER



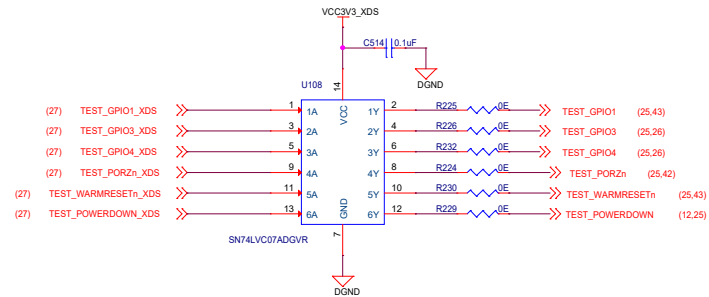
## I2C\_TA BUS BUFFER



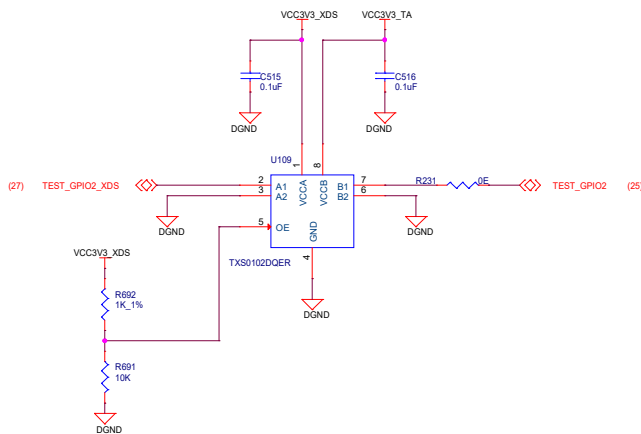
## BOOTMODE\_I2C\_TA BUFFER



## ISOLATION BUFFERS FOR TA SIGNALS



Pull ups (R567, R587, R517, R568, R585, R586 & R566) to VCC3V3\_TA are present



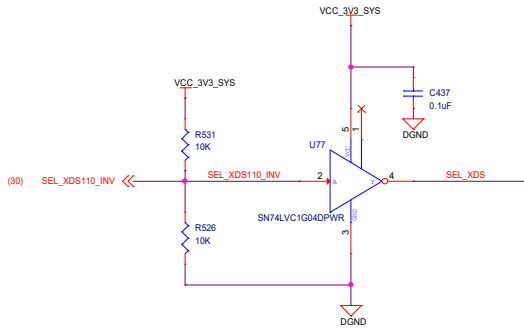
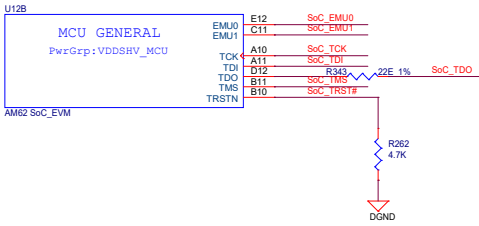
Designed for TI by Mistral Solutions Pvt Ltd



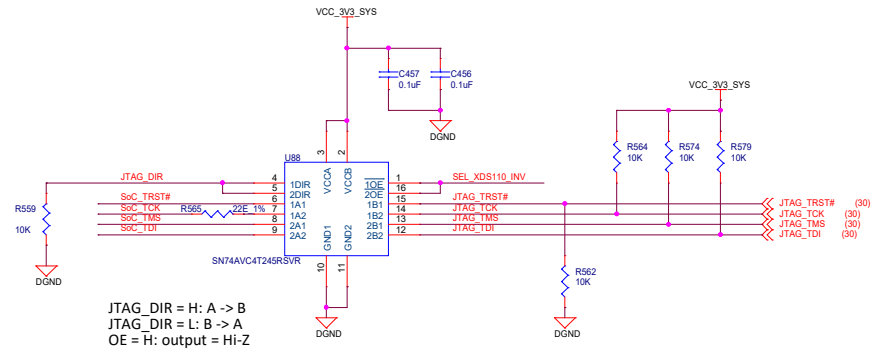
Title AUTOMATION SIGNALS BUFFER

Size	PROC114E3	Rev	E3
Date:	Friday, September 16, 2022	Sheet	28 of 44

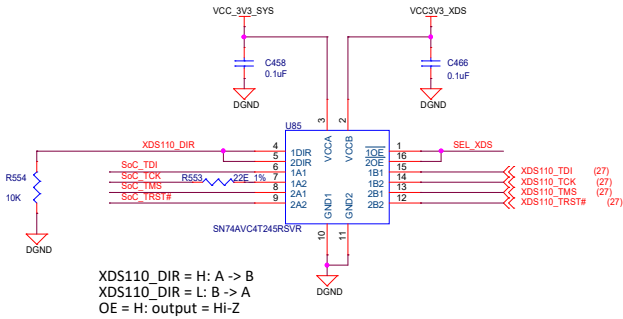
# JTAG SOC SECTION



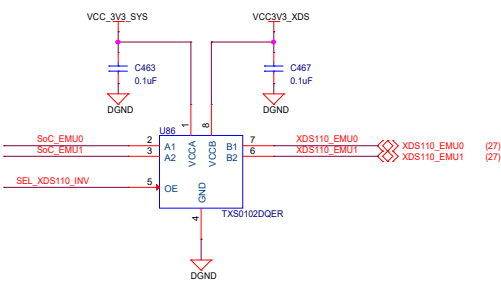
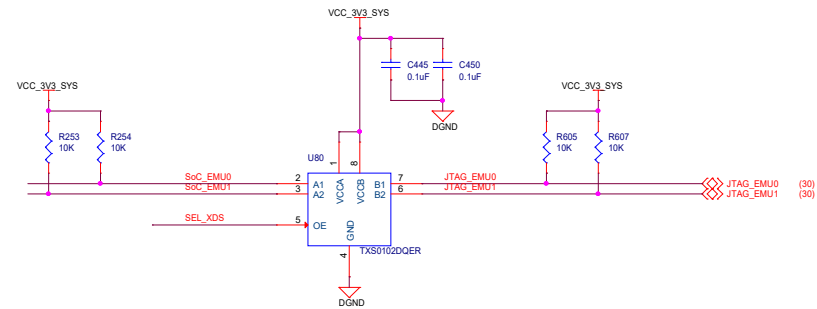
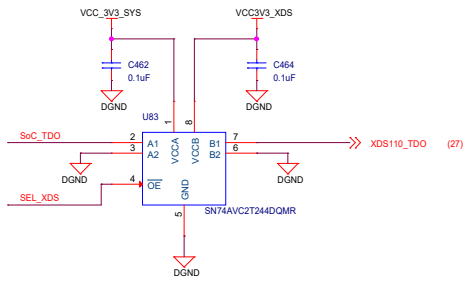
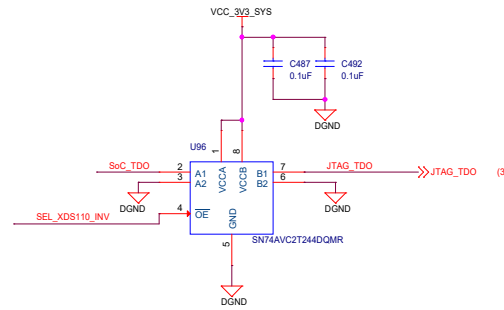
# cTI20 JTAG BUFFERS



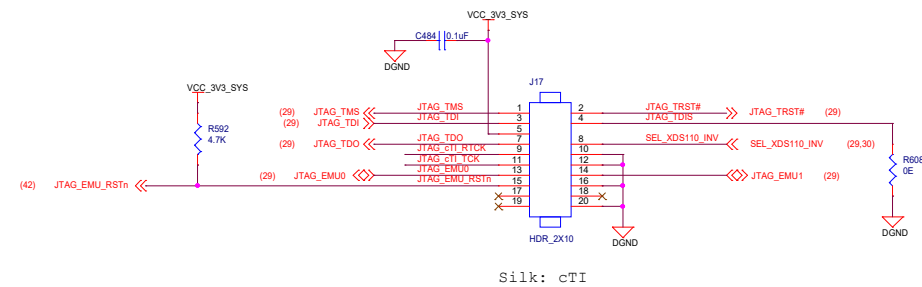
# BUFFER XDS110



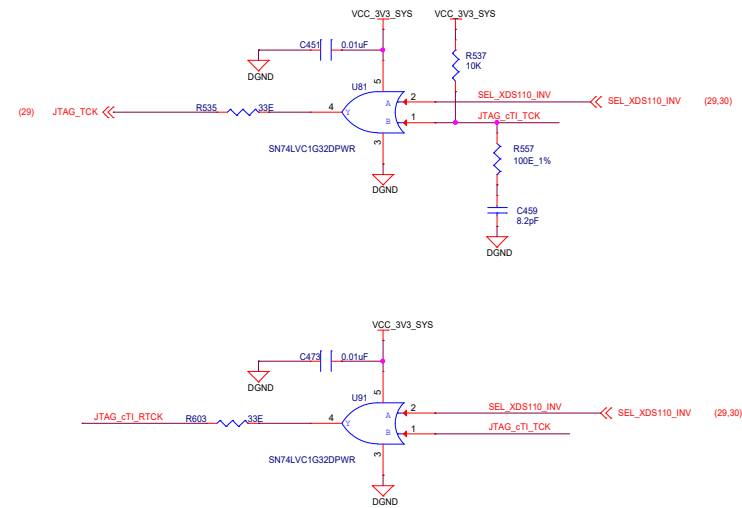
CAD NOTE: Buffers U88 and U96 need to be placed closer to the cTI-20pin connector J17 to reduce Stub length of the JTAG signals.



# JTAG 20 PIN cTI CONNECTOR



# JTAG CLOCK BUFFER

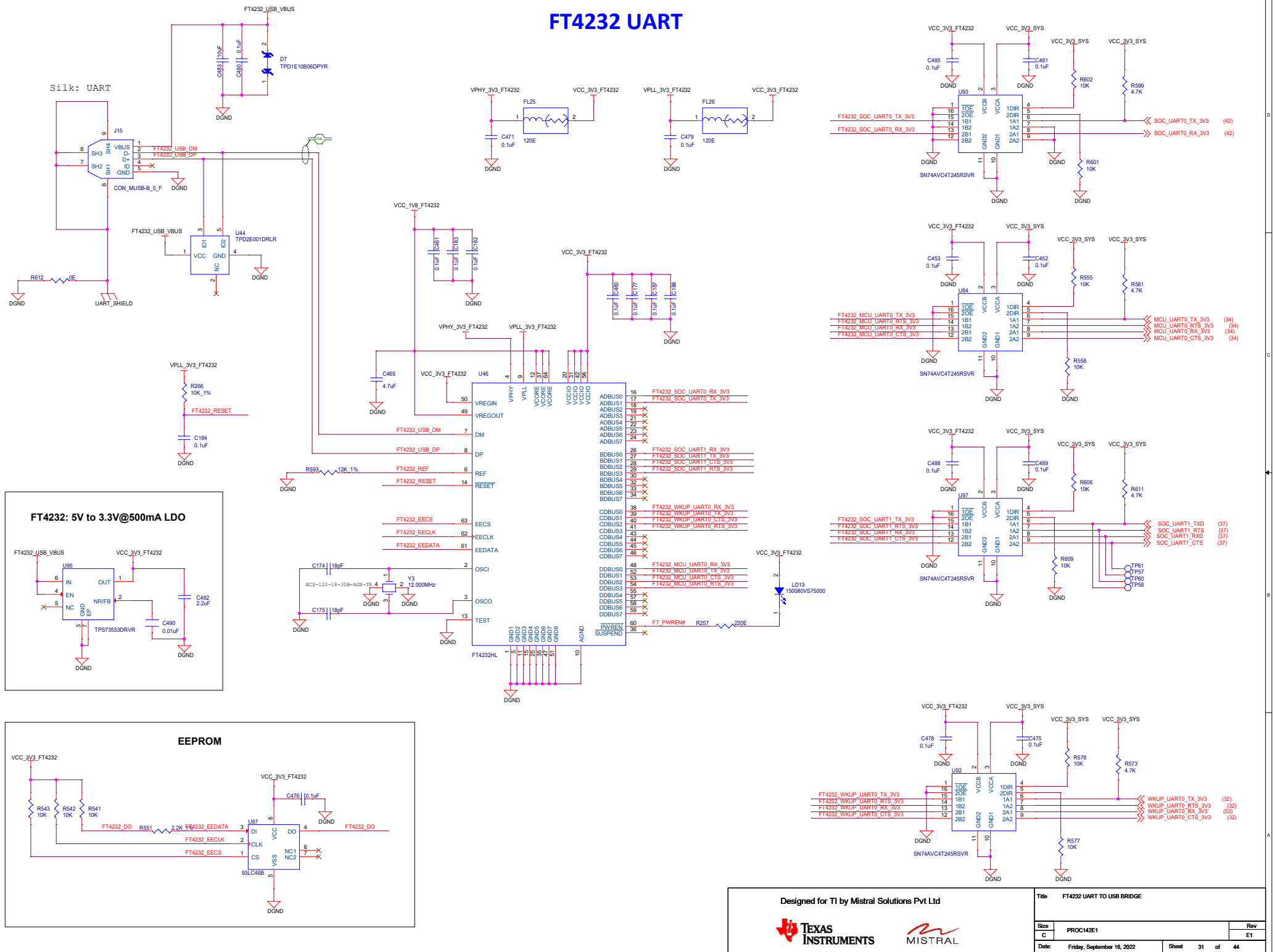


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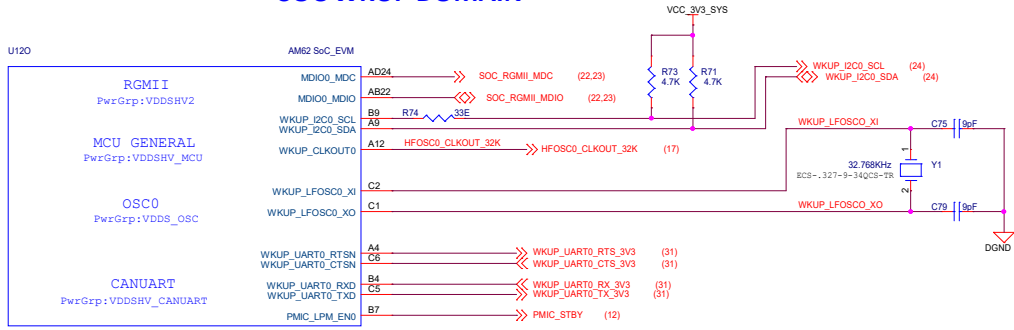
Title		JTAG 20 PIN cTI CONNECTOR	
Size	PROC142E1	Rev	E1
Date:	Friday, September 16, 2022	Sheet	30 of 44

# FT4232 UART

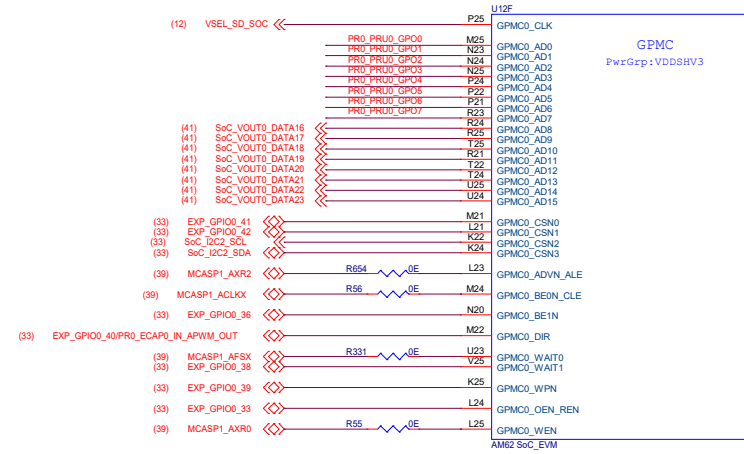


Designed for TI by Mistral Solutions Pvt Ltd		Title FT4232 UART to USB BRIDGE	
		Size	PROC142E1
		Rev	E1
Date:	Friday, September 16, 2022	Sheet	31 of 44

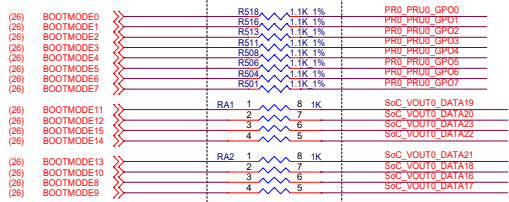
## SOC WKUP DOMAIN



## SOC GPMC

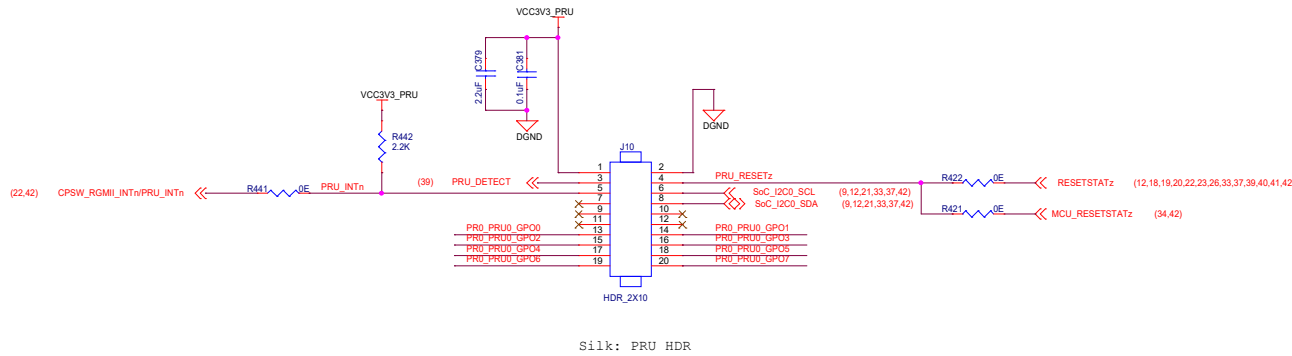


## BOOTMODE PINS



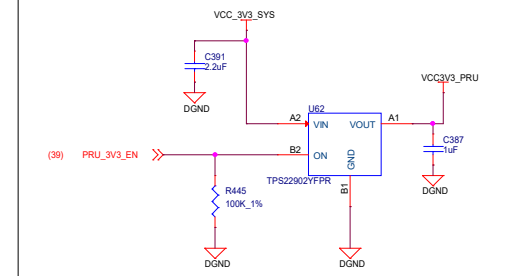
NOTE: Resistors are used to isolate the BOOTMODE control logic after the value is latched

## PRU HEADER



NOTE: PRU Header I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

## POWER SWITCH FOR PRU HEADER



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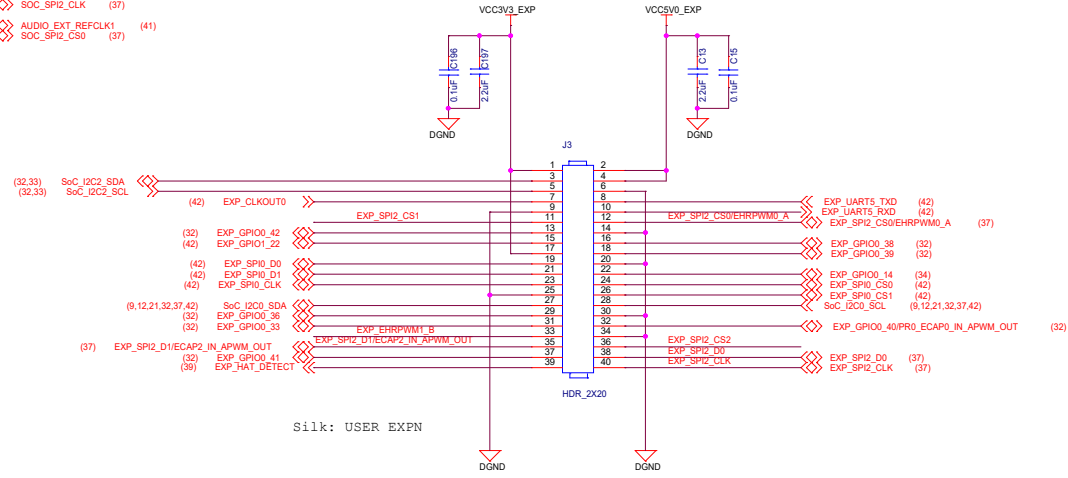
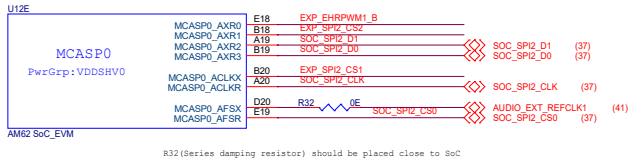
Title PRU HEADER

Size PROC142E1  
C  
Date: Friday, September 16, 2022  
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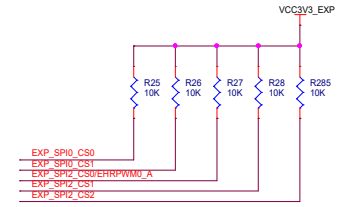
Rev E1



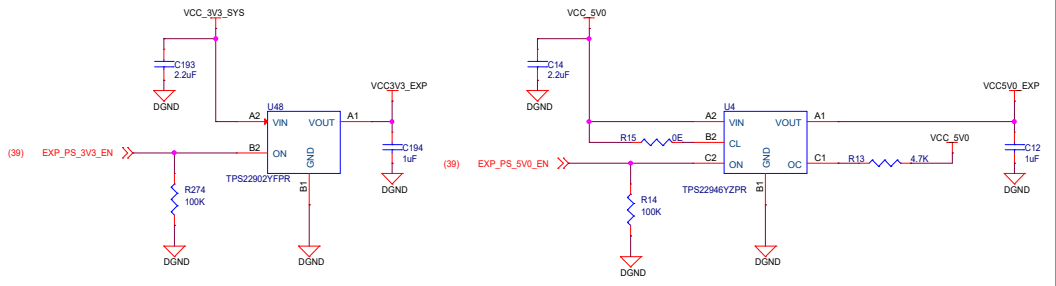
# USER EXPANSION CONNECTOR



Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)

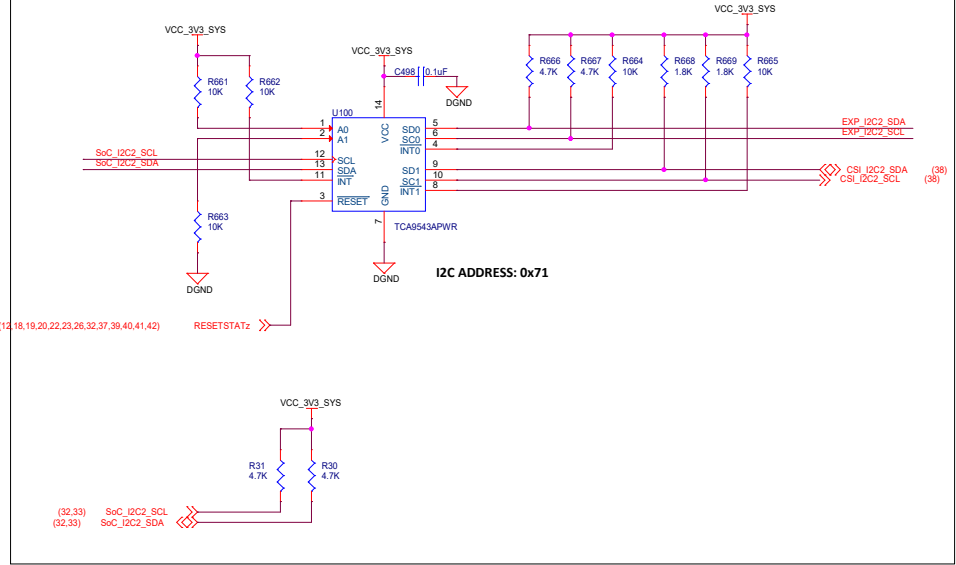


## POWER SWITCHES FOR USER EXPANSION CONNECTOR



**NOTE:**  
AM62x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.  
User Expansion Connector I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.  
5V supply of User Expansion Connector is limited to sourcing 155mA max.  
3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

## I2C SWITCH FOR SoC\_I2C2

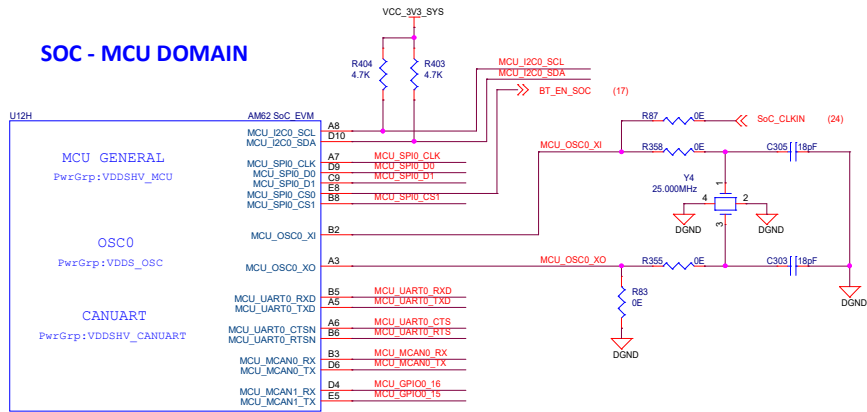


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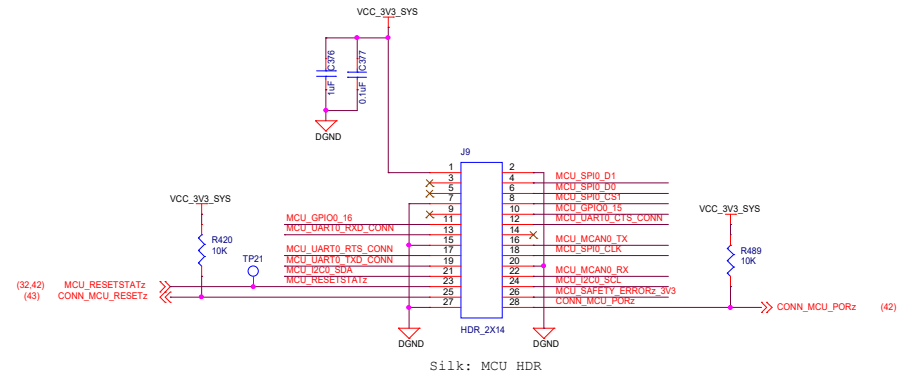


Title		USER EXPANSION CONNECTOR	
Size	PROC142E1	Rev	E1
C		Date:	Friday, September 16, 2022
Sheet		33 of 44	

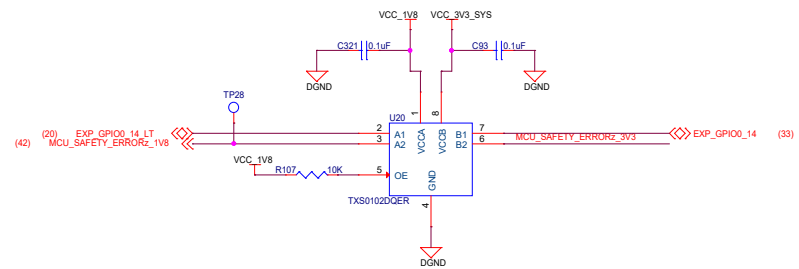
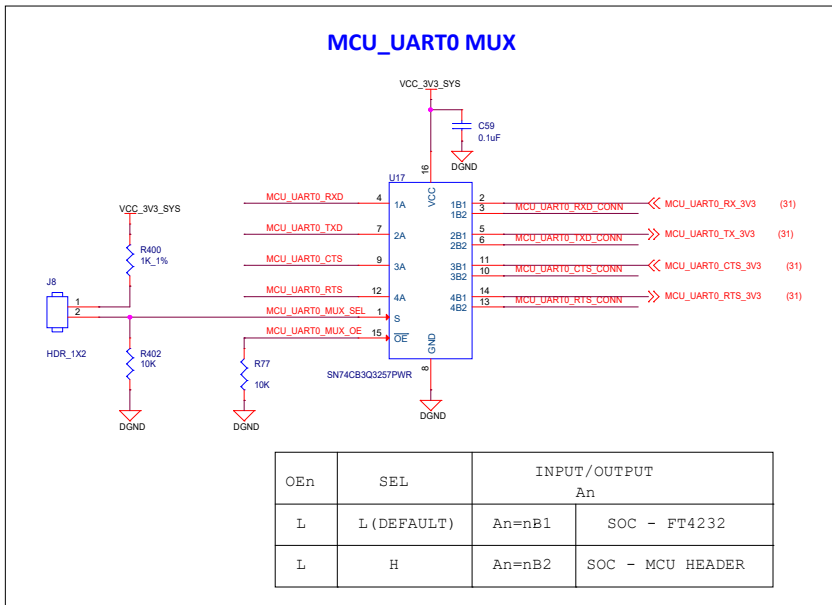
# SOC - MCU DOMAIN



# MCU HEADER



# MCU\_UART0 MUX



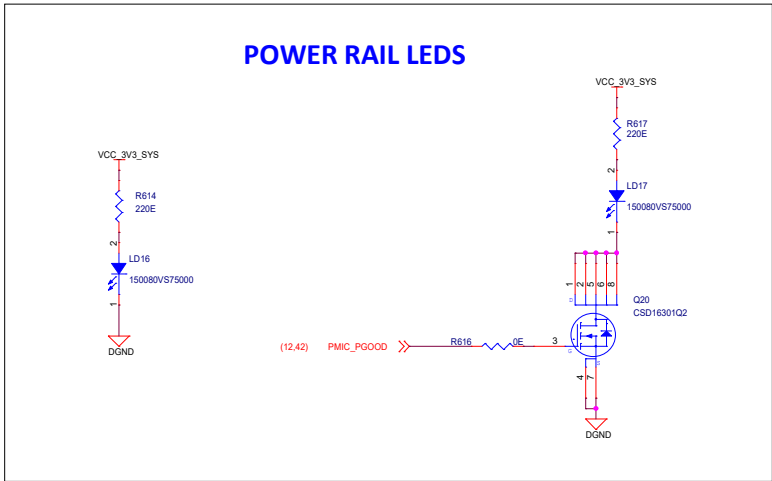
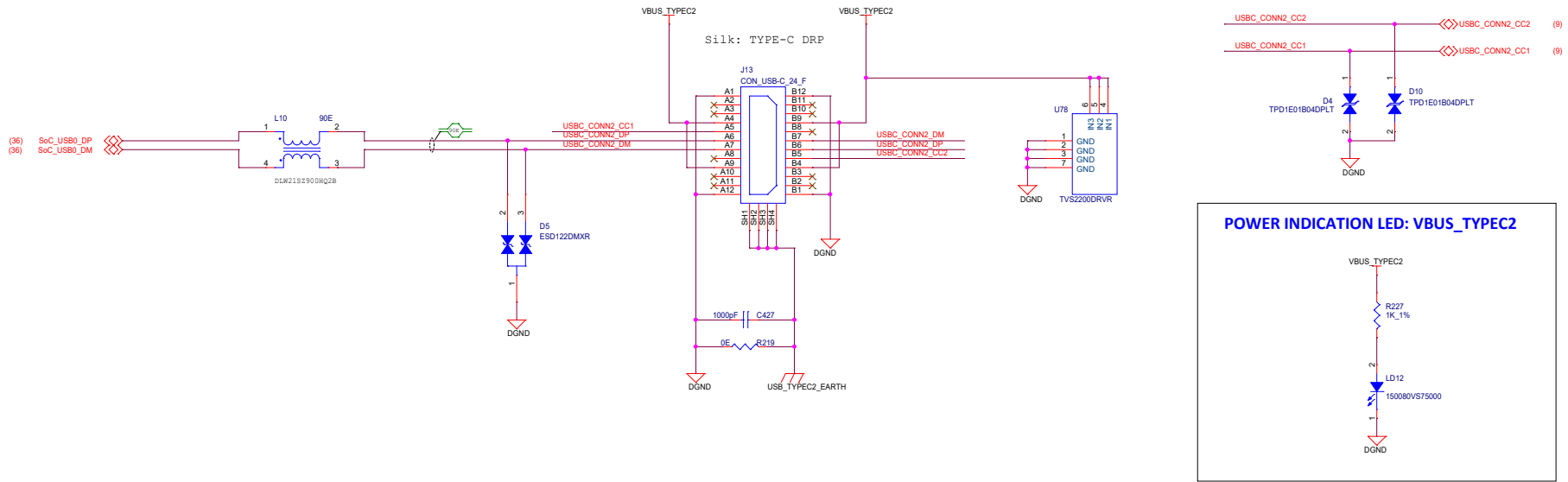
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Title: MCU HEADER

Size	PROC142E1	Rev	E1
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# USB0 TYPE-C DRP



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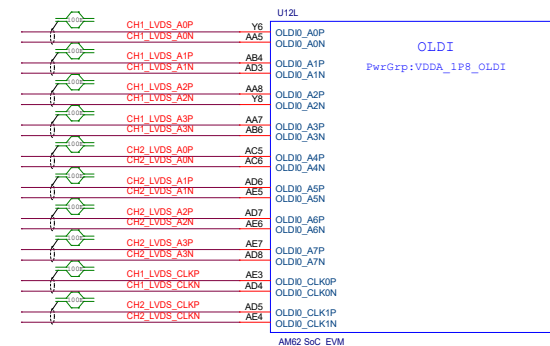
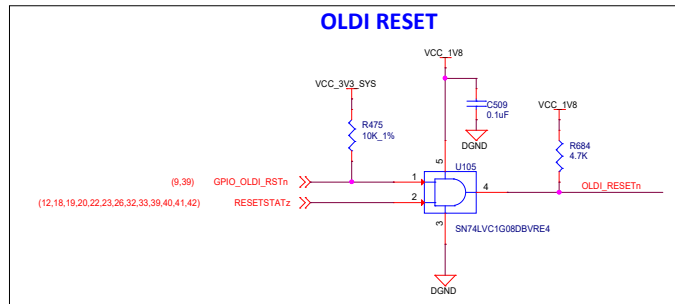
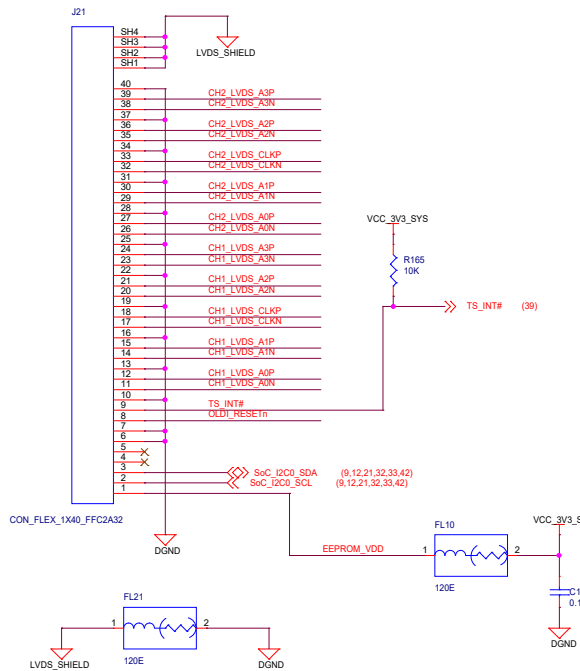


Title: USB0 TYPE-C DRP

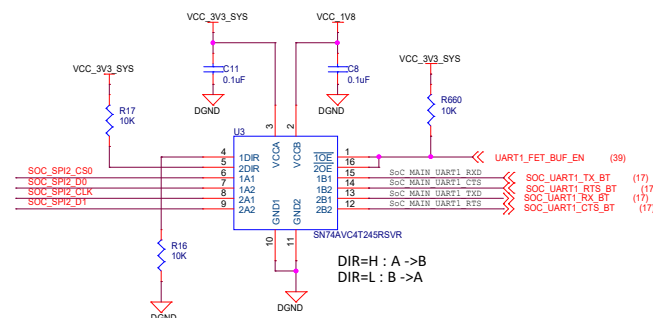
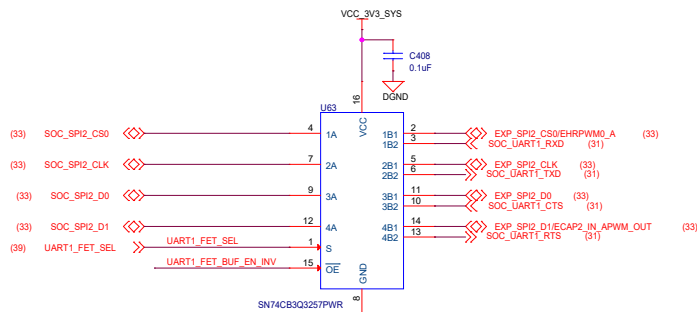
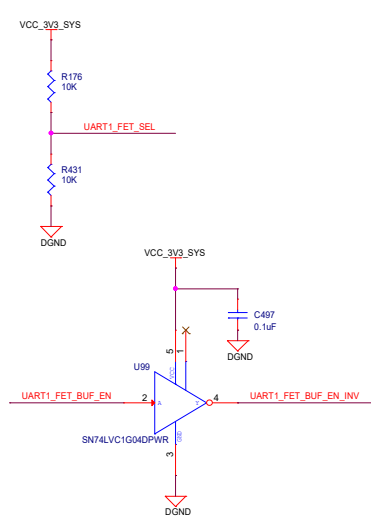
Size	PROC142E1	Rev	E1
Date:	Friday, September 16, 2022	Sheet	35 of 44



# OLDI DISPLAY INTERFACE



# SoC UART1 FET SWITCH & BUFFER



OE <sub>n</sub>	SEL	INPUT/OUTPUT An	
L	H (DEFAULT)	An=nB2	FT4232
L	L	An=nB1	EXP CONN

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Title: OLDI DISPLAY INTERFACE

Size: PROC142E1

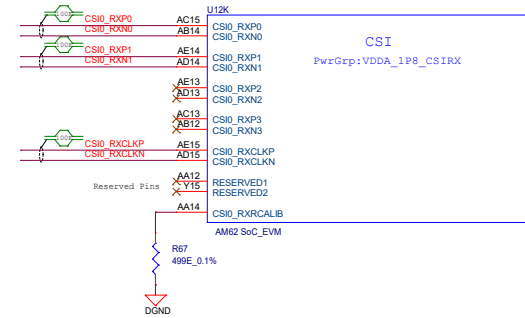
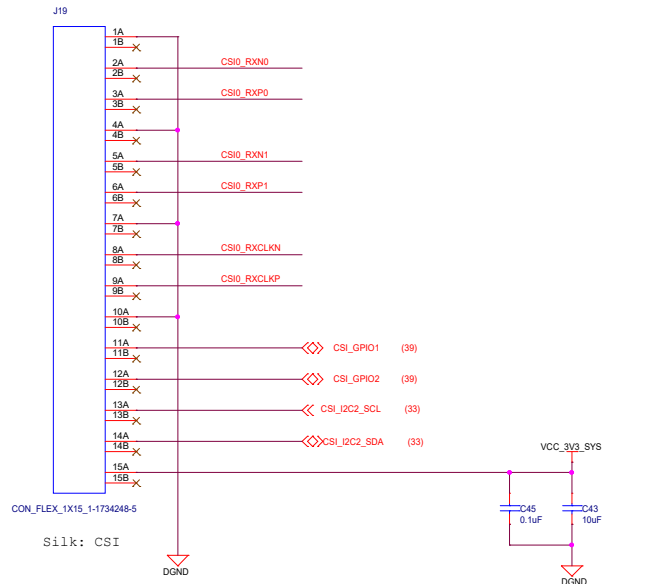
Date: Friday, September 16, 2022

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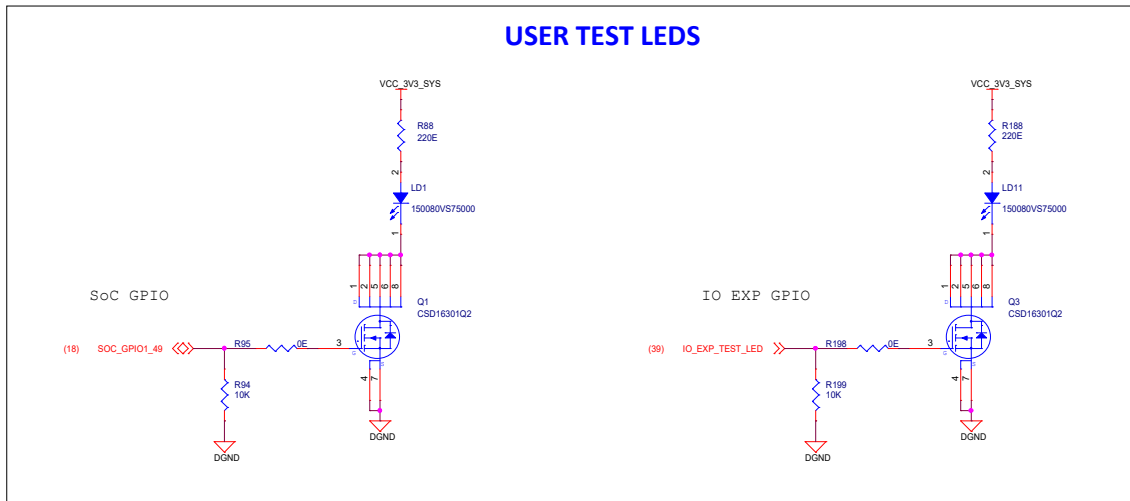
Rev: E1

# CSI INTERFACE

## CSI CAMERA HEADER



## USER TEST LEDS



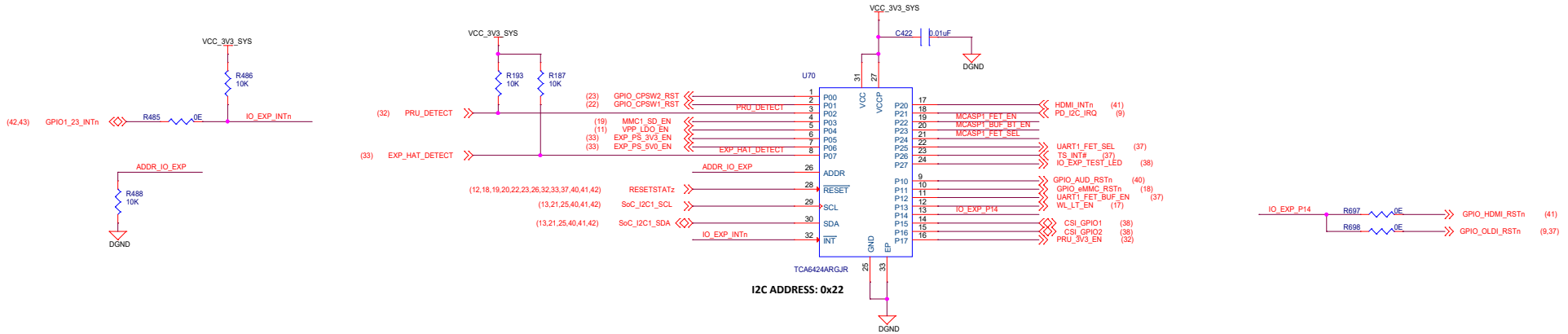
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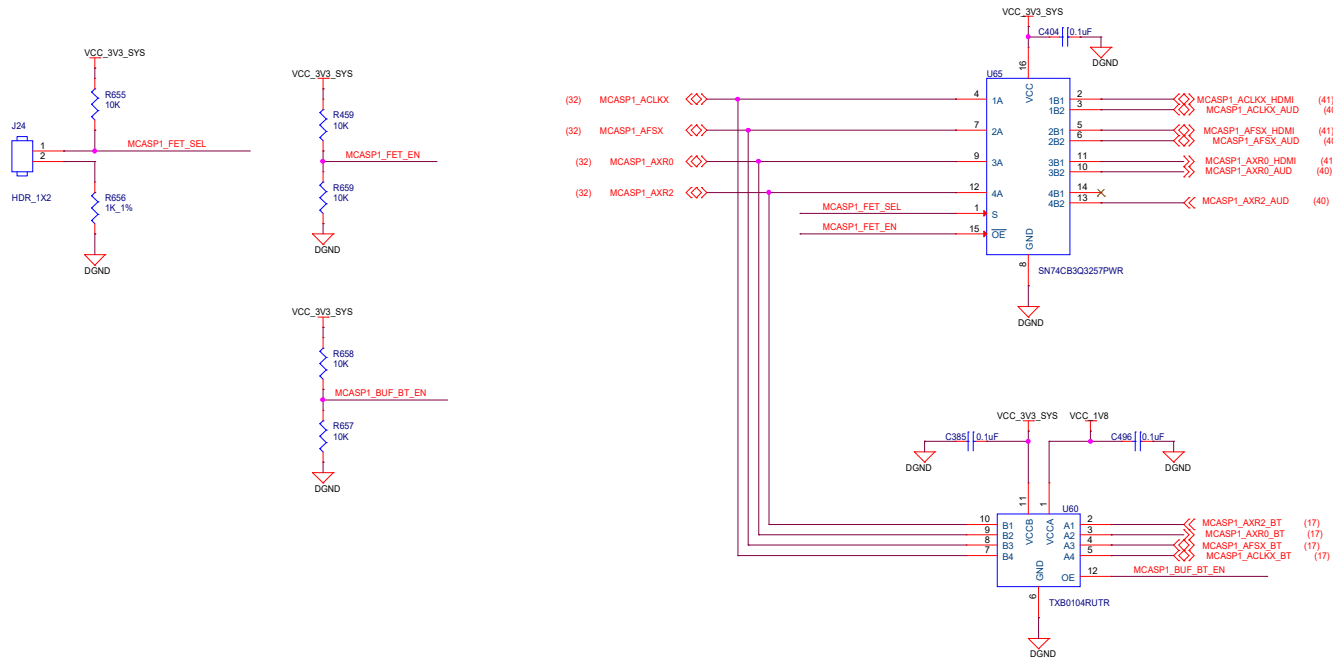
Title: CSI INTERFACE & USER TEST LEDS

Size	PROC142E1	Rev	E1
Date:	Friday, September 16, 2022	Sheet	38 of 44

# IO EXPANDER



# MCASP1 FET SWITCH & BUFFER



OEn	SEL	INPUT/OUTPUT An=nBn	
L	H (DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

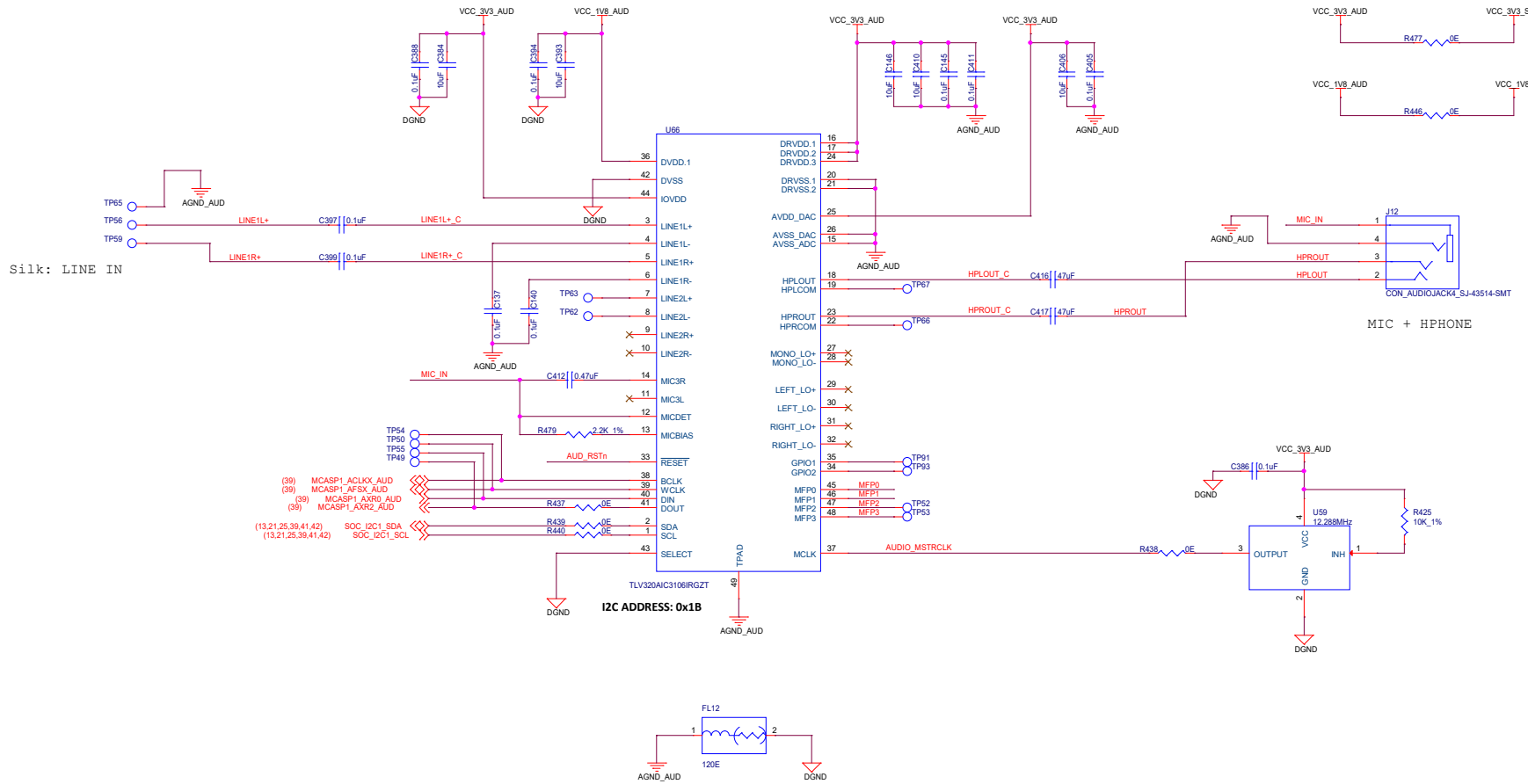
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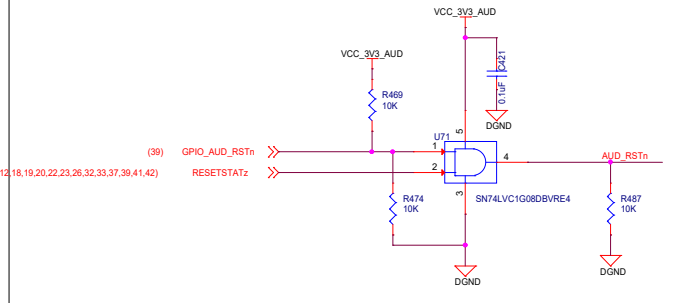
Title: IO EXPANDER

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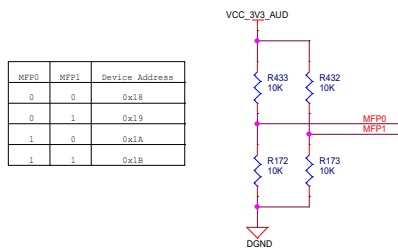
# AUDIO CODEC



## AUDIO CODEC RESET



## CODEC I2C ADDRESS SELECTION



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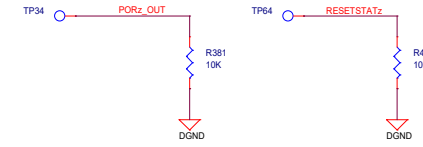
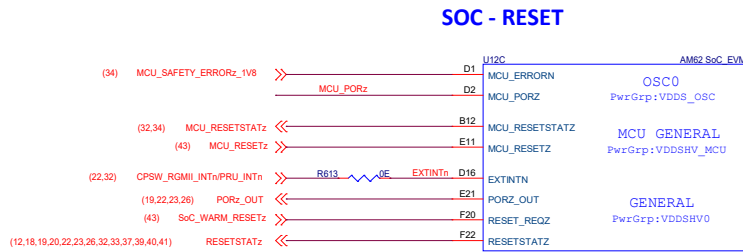
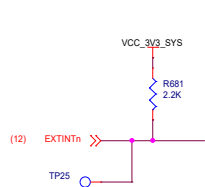
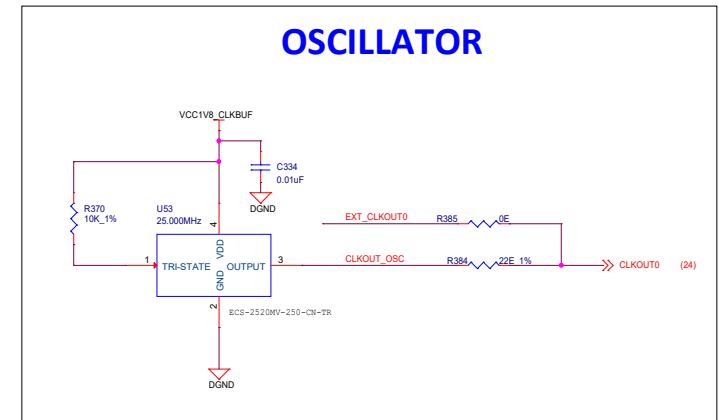
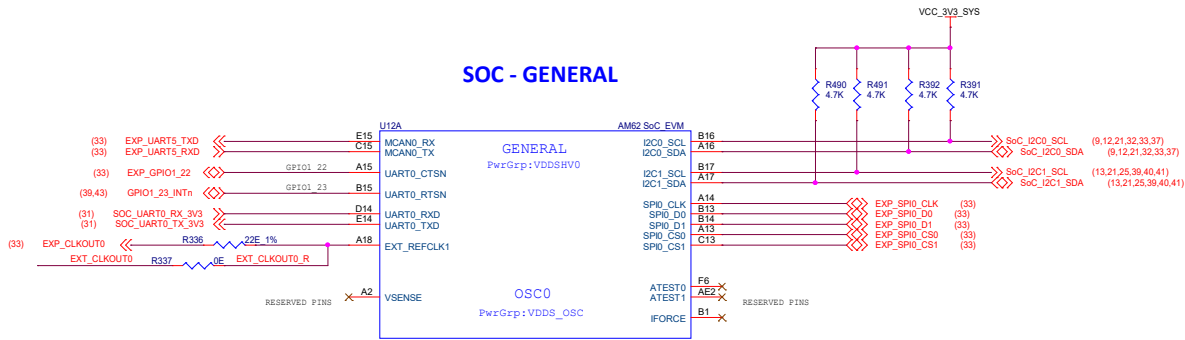


Title: AUDIO CODEC

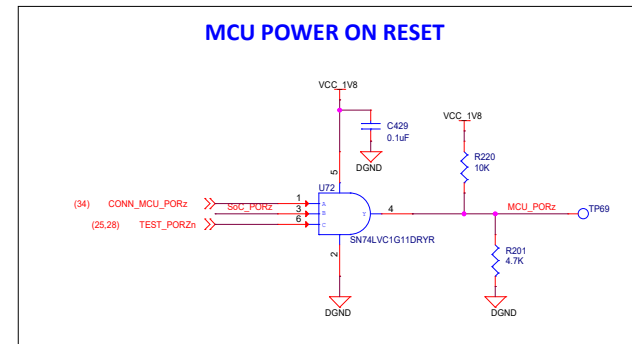
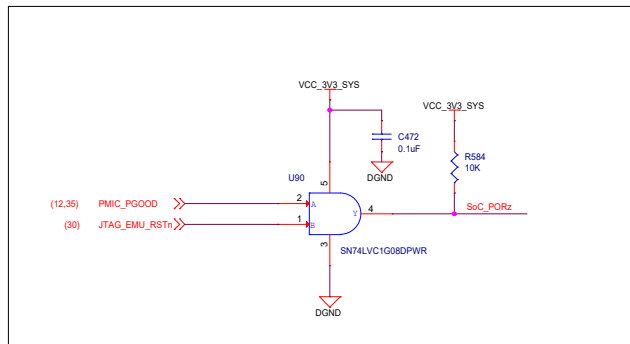
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Full-down resistor on PORz\_OUT is provided to keep the signal low until the processor is released from reset during the power-up sequence



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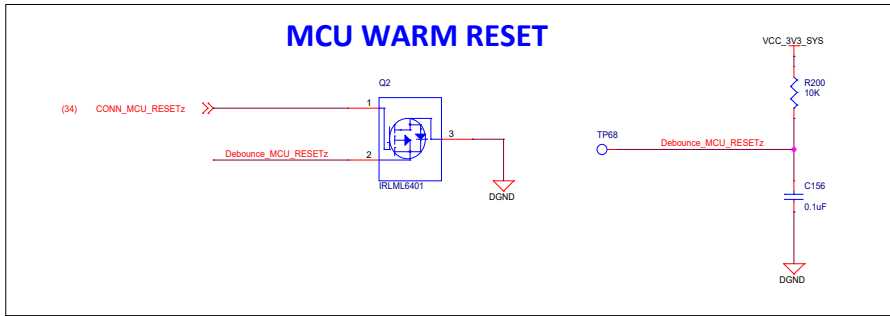


Title: OSCILLATOR

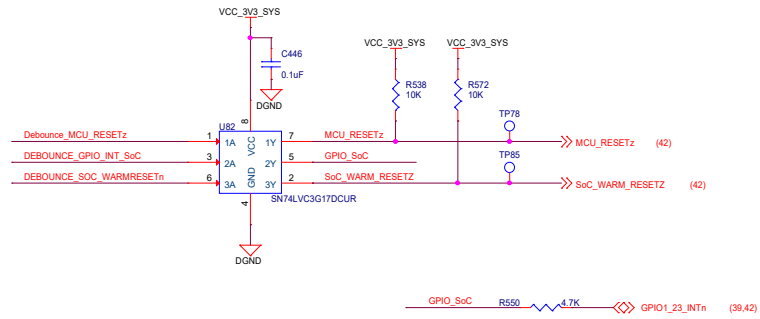
Size	PROC142E1	Rev	E1
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# RESET

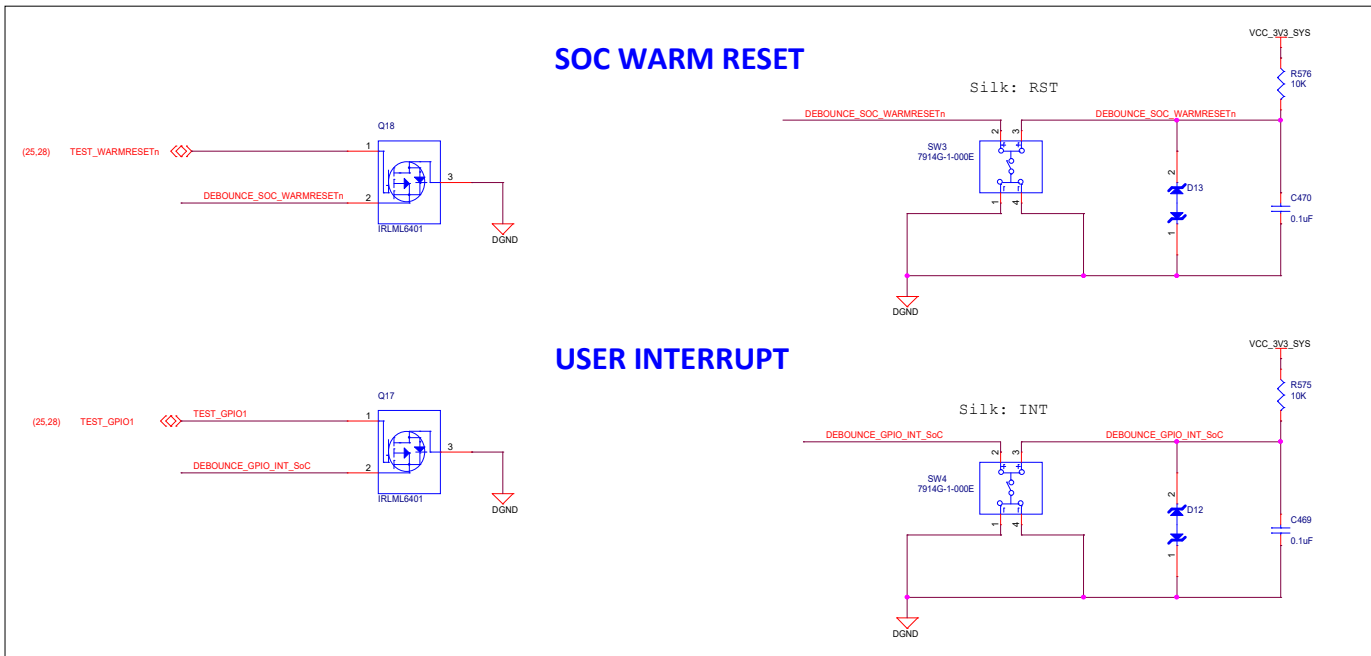
## MCU WARM RESET



## DEBOUNCE CIRCUIT



## SOC WARM RESET



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Title		RESET
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# HARDWARE SCHEMATICS

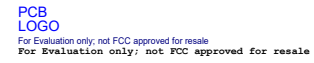
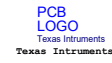
## ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

## BARE PCB



## LOGOs



## LABELS

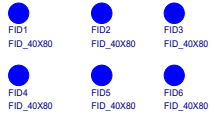
### Board Serial No.



### Assembly Revision



## FIDUCIALS



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Title: HARDWARE SCHEMATICS

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