AM625 SIP STARTER KIT EVM

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Revision Number

REV	E1
VER	0.04

D-Note:-

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

R-Note:-

* Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of board design before board assembly.
* A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor.
* Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details)

KEY LINKS TO COLLATERALS

Hardware Design Guide : https://www.ti.com/lit/an/sprad05b/sprad05b.pdf
Schematic Design and Review Checklist : https://www.ti.com/lit/an/sprad21d/sprad21d.pdf
PMIC Power Solutions application note : https://www.ti.com/lit/an/slvafp8/slvafp8.pdf
EVM/SKs (Starter Kits) for reference : SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP

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REVISION HISTORY

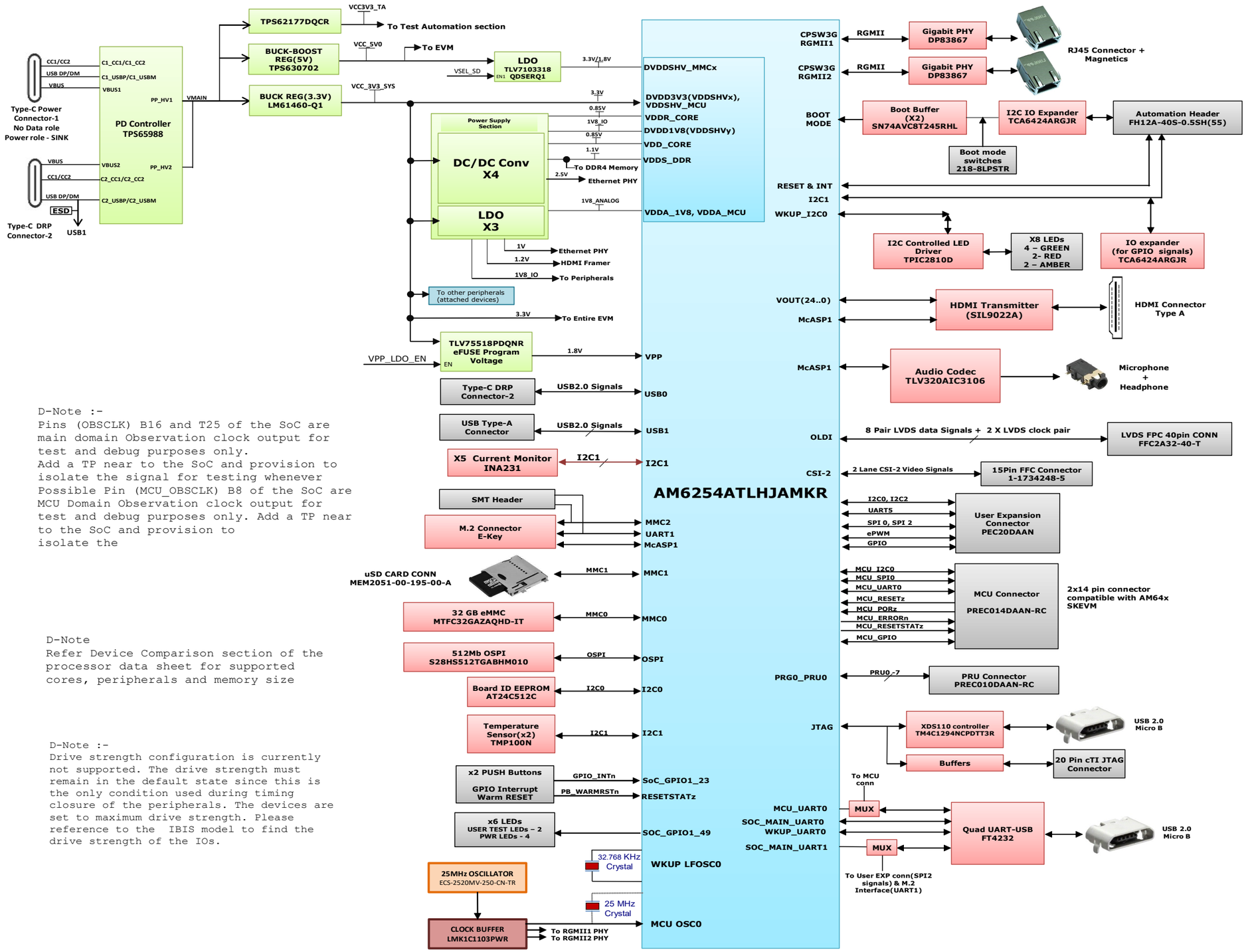
VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	20 APR 2023	Changed the HDMI external swing resistance to 7.5K. Added Standoff,Screw & Washer for M.2 connector. DNI'd R650 on SoC_USB1_DRVVBUS	Mistral Design Team		
0.02	16 MAY 2023	Test Automation Board power section populated and DNI'd the R738 resistor.	Mistral Design Team		
0.03	24 June 2024	SoC Symbol part# XAM6254ATLHJAMK Structured and rotated R148 sense resistor for footprint compatibility	Mistral Design Team		
0.04	28 June 2024	Updated SoC Part Number, Enabled Voltage ratings for all the capacitors and added Design Review notes Moved to DNI : C5,Y4,C303,C305. Moved to Mount : R319,R309,R318,R310,R306,R307,R308,R303,R538,R572. C86 - 1uF changed to 2.2uF ; C60 - 4.7uF changed to 1uF ; C46 - 0.1uF changed to 4.7uF ; C47 - 1uF changed to 0.1uF ; C75,C79 - 9pF changed to 18pF ; C391,C193,C14 - 2.2uF changed to 1uF ; C387,C194,C12 - 1uF changed to 0.1uF. Bootmode DIP switch Pulldown Resistors - 100K_1% changed to Std 100K; R12,R333,R398 - 49.9K_1% changed to Std 10K; R393 - 10K_1% changed to Std 10K; R89,R353,R354,R301,R302 - 22E_1% changed to 0E; R56 - 0E changed to Std 22E; R152,R649 - 3.4K_1% changed to 3.48K_1%; R723 - 2.2K changed to Std 10K.	Mistral Design Team		

LINKS TO KEY FAQs

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1297185/faq-am625sip-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-am62px-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1347063/faq-am625sip---custom-board-hardware-design---design-and-review-notes-for-reuse-of-sk-am62-sip-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1280721/faq-am625-am623-am625sip-am625-q1-am620-q1-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit

BLOCK DIAGRAM AM62 SIP_SKEVM

Main Block Diagram



D-Note :-
Pins (OBSCLK) B16 and T25 of the SoC are main domain Observation clock output for test and debug purposes only.
Add a TP near to the SoC and provision to isolate the signal for testing whenever Possible Pin (MCU_OBSCLK) B8 of the SoC are MCU Domain Observation clock output for test and debug purposes only. Add a TP near to the SoC and provision to isolate the

D-Note
Refer Device Comparison section of the processor data sheet for supported cores, peripherals and memory size

D-Note :-
Drive strength configuration is currently not supported. The drive strength must remain in the default state since this is the only condition used during timing closure of the peripherals. The devices are set to maximum drive strength. Please reference to the IBIS model to find the drive strength of the IOs.

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Title	BLOCK DIAGRAM AM62x SKEVM		
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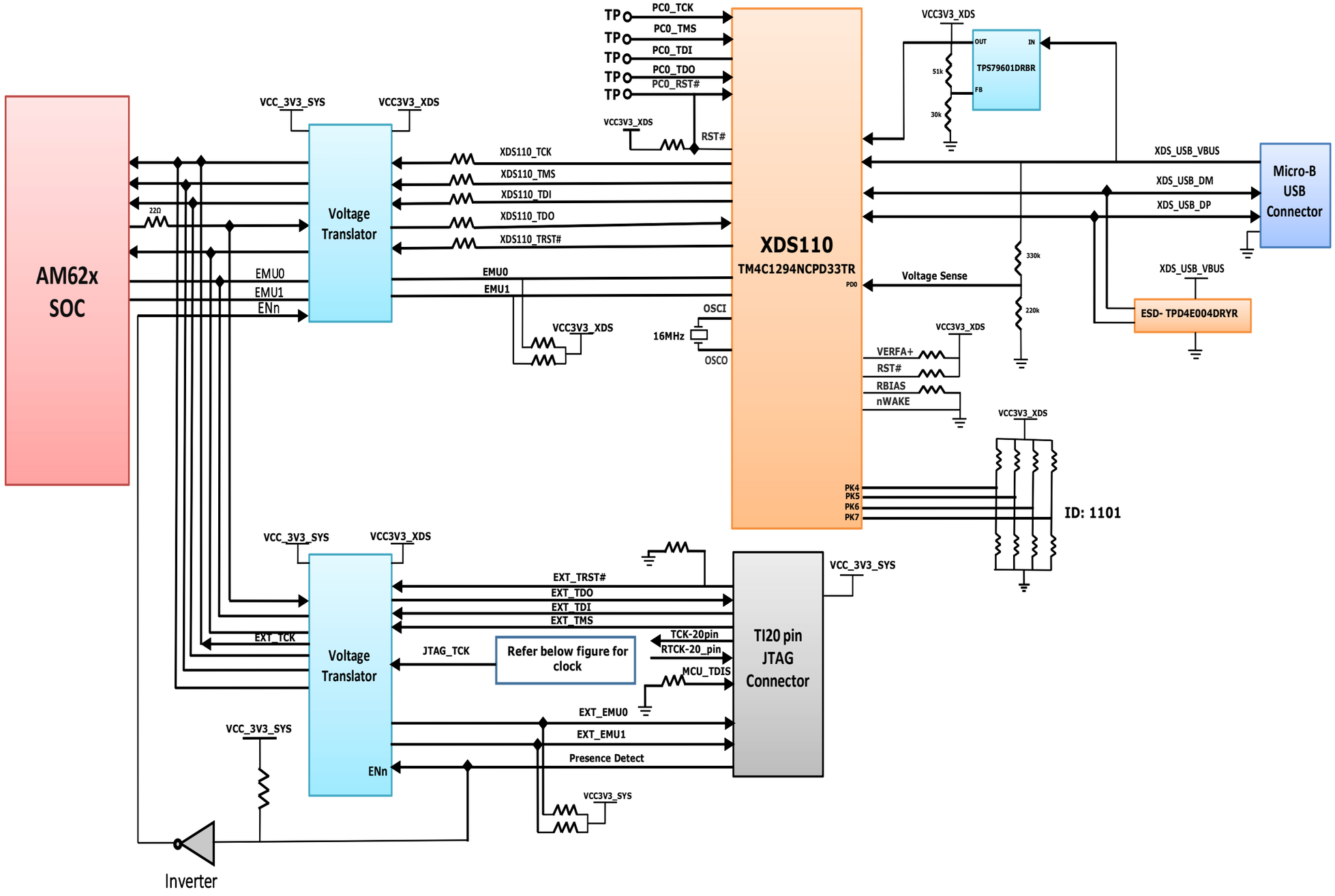
BLOCK DIAGRAM_XDS110

D-Note :-
Reference the latest XDS SK diagram as a note



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Title	BLOCK DIAGRAM_XDS110		
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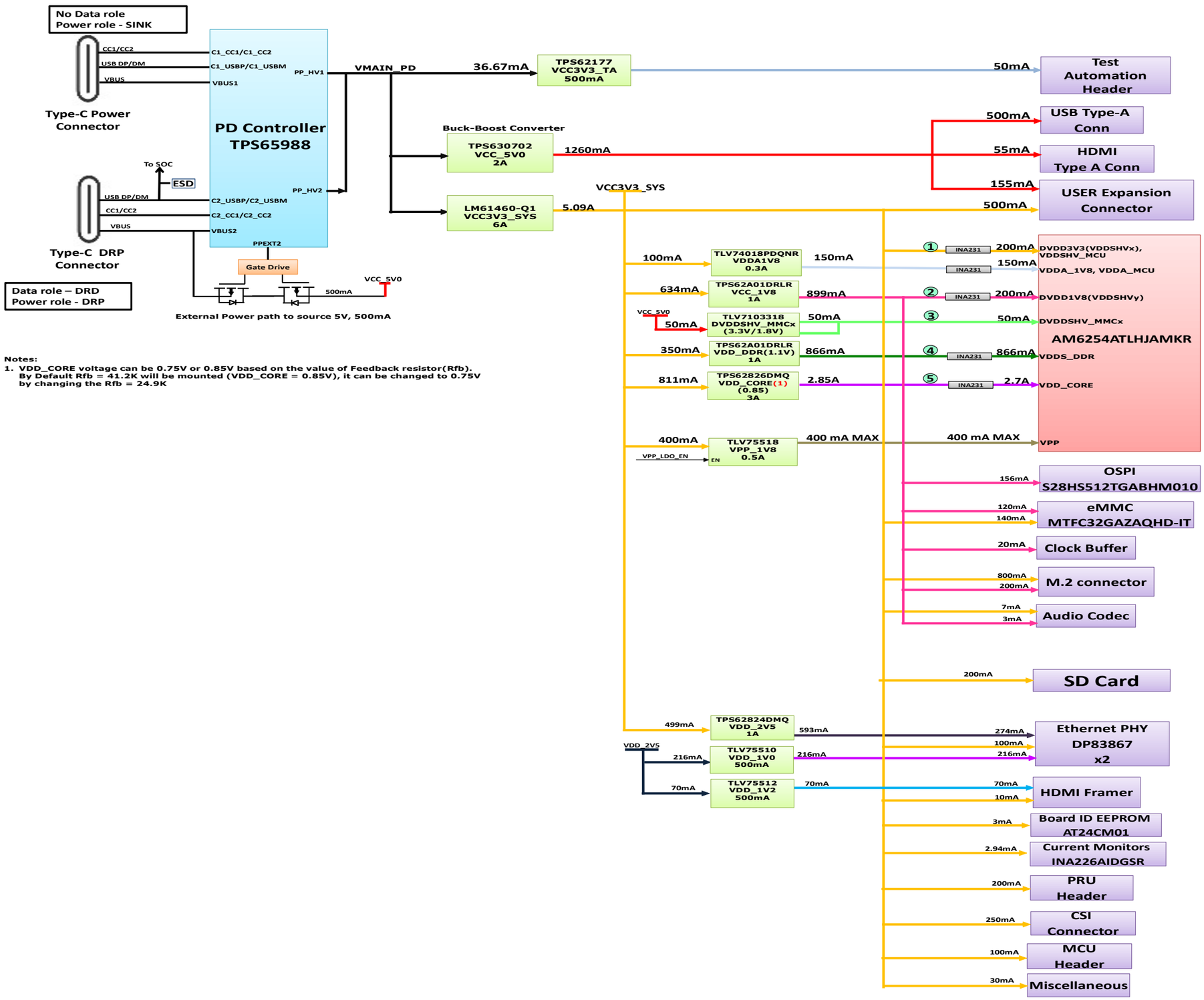
POWER ARCHITECTURE BLOCK DIAGRAM



Notes:

1. VDD_CORE voltage can be 0.75V or 0.85V based on the value of Feedback resistor(Rfb). By Default Rfb = 41.2K will be mounted (VDD_CORE = 0.85V), it can be changed to 0.75V by changing the Rfb = 24.9K

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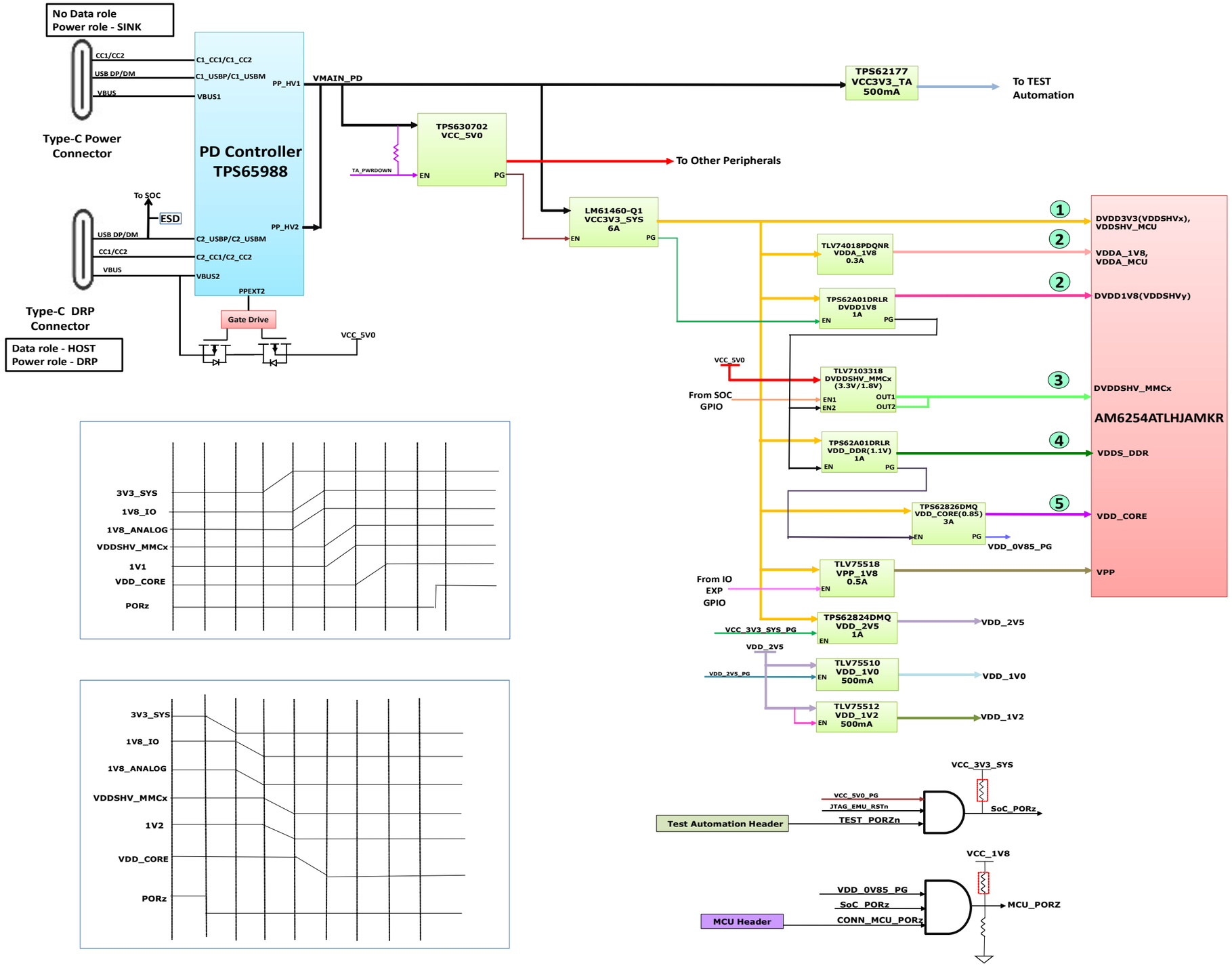
POWER SEQUENCE



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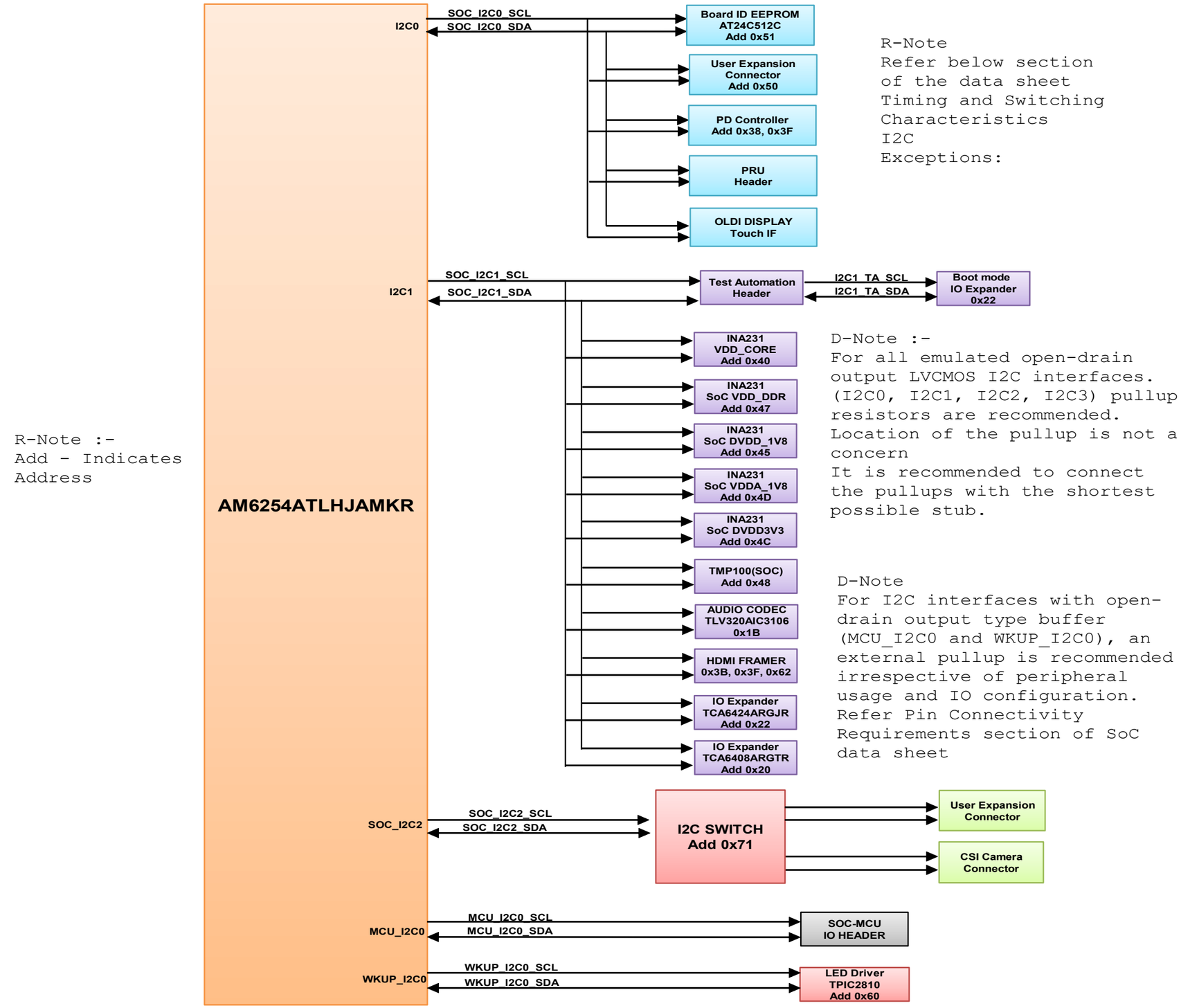
I2C TREE



R-Note :-
Add - Indicates Address

R-Note
Refer below section of the data sheet
Timing and Switching Characteristics
I2C
Exceptions:

D-Note :-
For all emulated open-drain output LVCMOS I2C interfaces. (I2C0, I2C1, I2C2, I2C3) pullup resistors are recommended.
Location of the pullup is not a concern
It is recommended to connect the pullups with the shortest possible stub.

D-Note
For I2C interfaces with open-drain output type buffer (MCU_I2C0 and WKUP_I2C0), an external pullup is recommended irrespective of peripheral usage and IO configuration.
Refer Pin Connectivity Requirements section of SoC data sheet

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Title	I2C TREE		
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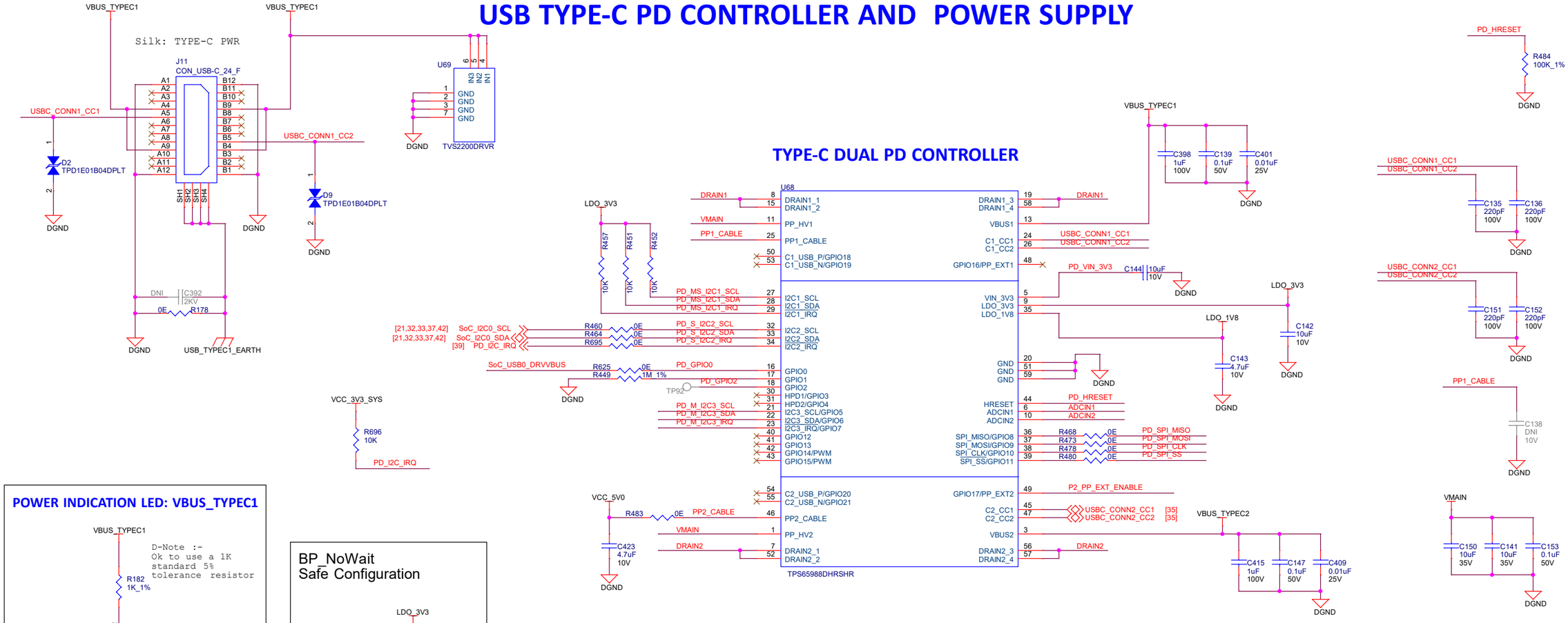
GPIO MAPPING TABLE

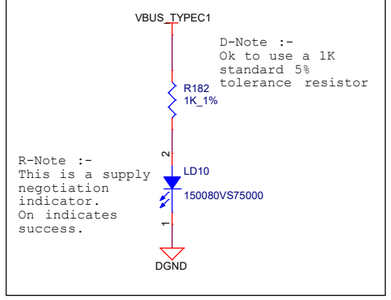
SL NO.	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	SoC_WLAN_EN_1V8	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	SoC_WLAN_IRQ_1V8	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC_3V3	ENABLE	MCU_GPIO0_1	MCU_SPI0_CS0	OUTPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt PRU Connector Interrupt PMIC_INTn	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
9	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER -P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	M.2 Connector Alert	WLAN_ALERT_3V3	ALERT	IO EXPANDER – P10		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	M.2 Connector WAKEUP	BT_UART_WAKE_SOC_3V3	WAKEUP	IO EXPANDER – P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	SOC UART1 Mux Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INT#	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 02										
1	M.2 Connector SDIO Reset Control GPIO	WLAN_SDIO_RST_3V3	RESET	IO EXPANDER – P0		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	OLDI Display Reset control	GPIO_TS_RSTn	RESET	IO EXPANDER – P1		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER – P2		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER – P3		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3

USB TYPE-C PD CONTROLLER AND POWER SUPPLY

TYPE-C DUAL PD CONTROLLER

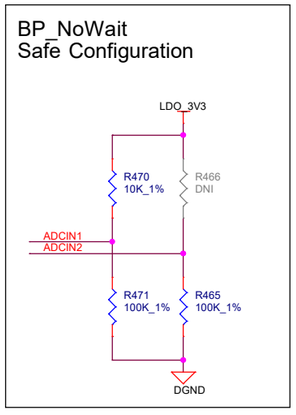


POWER INDICATION LED: VBUS_TYPEC1

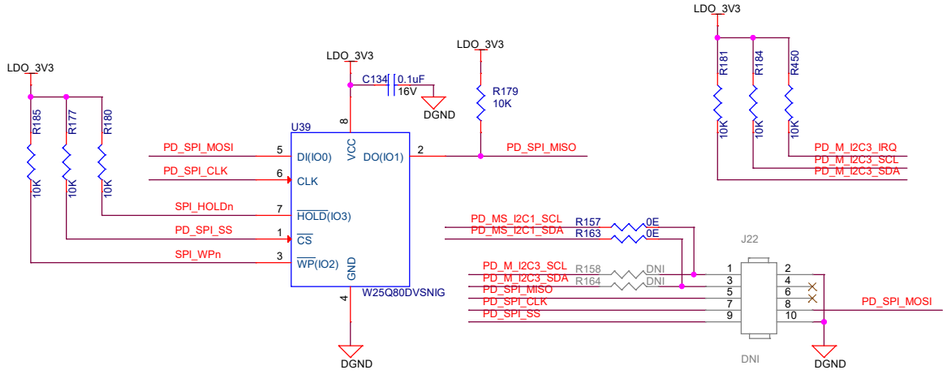


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

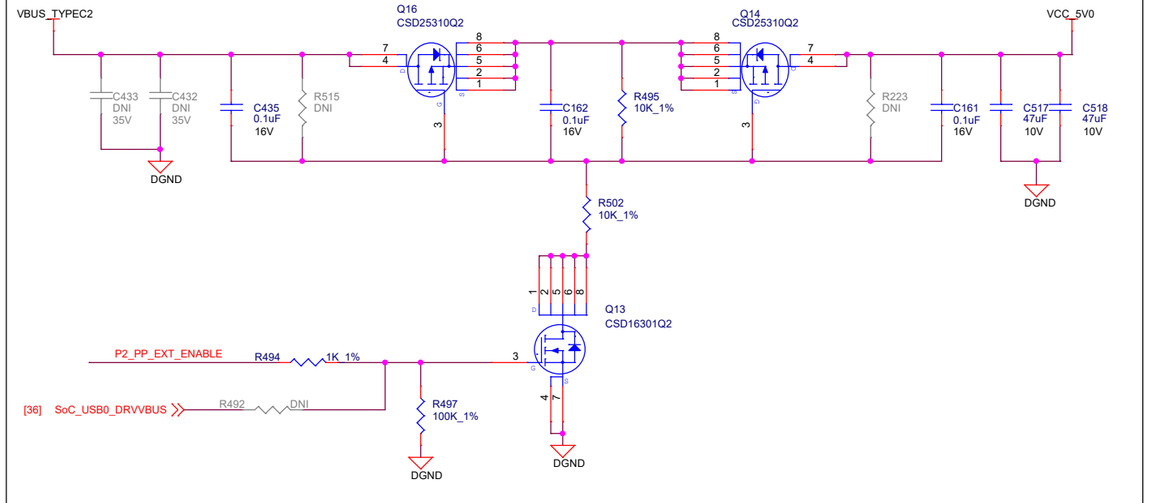
BP_NoWait Safe Configuration



SPI EEPROM & PROGRAMMING HEADER



EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



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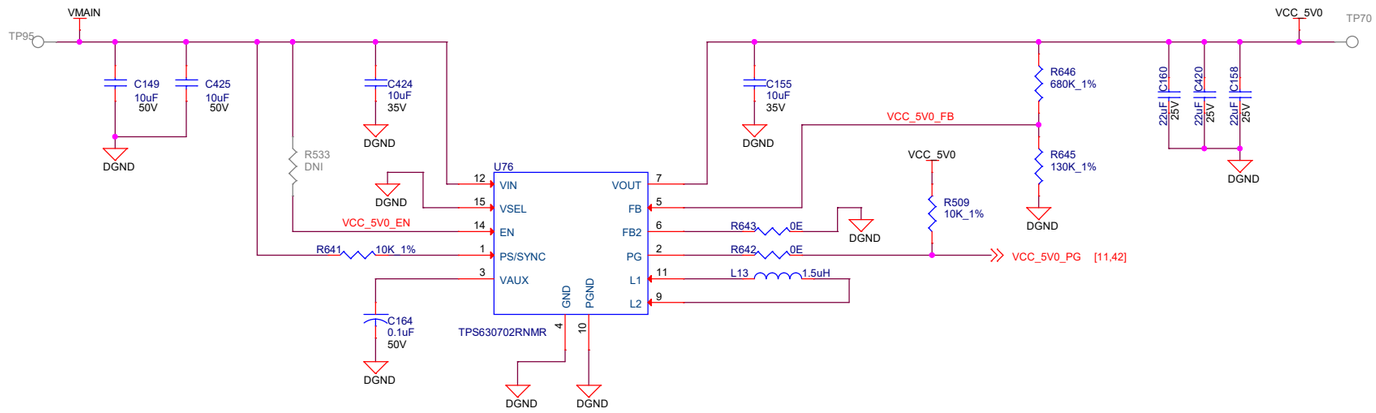
PERIPHERAL POWER SUPPLIES - 1



Power Cycle control from Test Automation

GROUND TEST POINTS

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Title	PERIPHERAL POWER SUPPLY -1	
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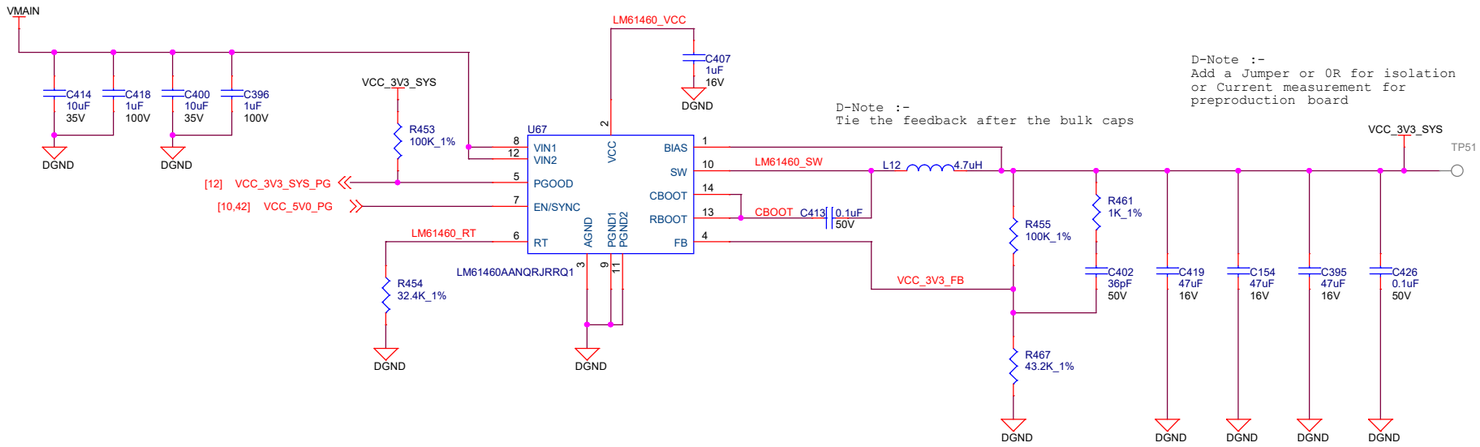
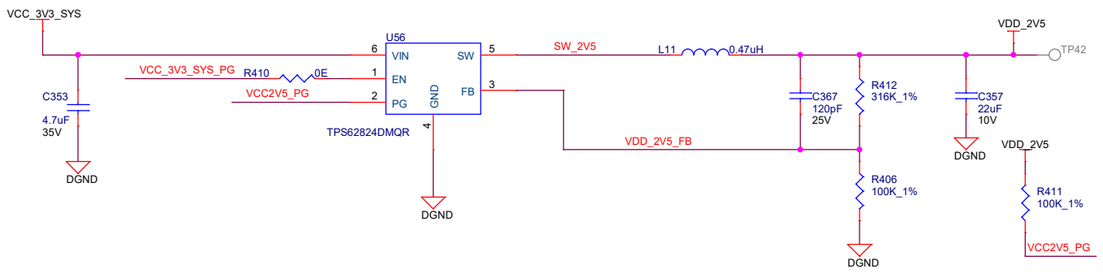
PERIPHERAL POWER SUPPLIES - 2

3.3V, 6.0 AMPS SUPPLY

VinMin = 4.5V
VinMax = 24V
Vout = 3.3V @ 6A



2.5V, 1.0 AMPS SUPPLY



1.8V VPP, 0.5 AMPS SUPPLY

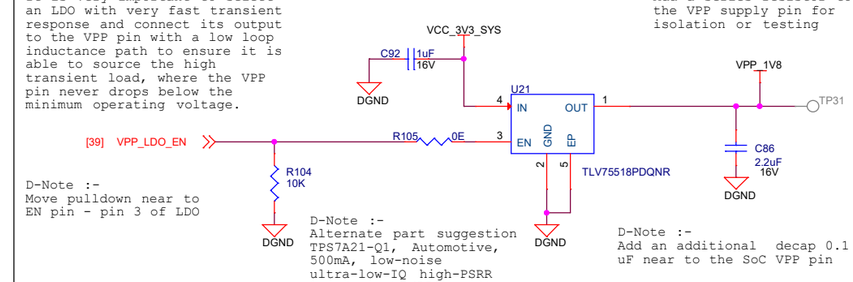
D-Note :-
It is very important to select an LDO with very fast transient response and connect its output to the VPP pin with a low loop inductance path to ensure it is able to source the high transient load, where the VPP pin never drops below the minimum operating voltage.

D-Note :-
Move pulldown near to EN pin - pin 3 of LDO

D-Note :-
Add a series resistor to the VPP supply pin for isolation or testing

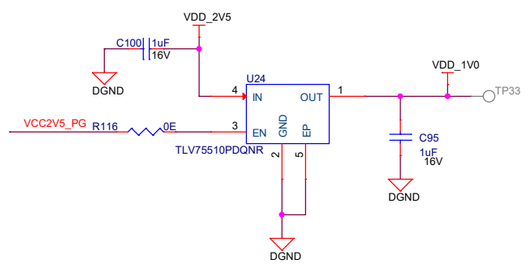
D-Note :-
Alternate part suggestion TPS7A21-Q1, Automotive, 500mA, low-noise ultra-low-IQ high-PSRR low-dropout (LDO) voltage regulator

D-Note :-
Add an additional decap 0.1 uF near to the SoC VPP pin

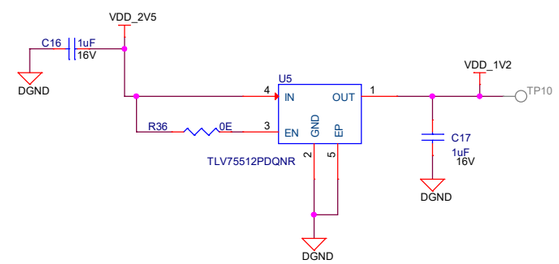


PERIPHERAL SUPPLY - ETHERNET PHY

1.0V, 0.5 AMP SUPPLY



1.2V, 0.5 AMP SUPPLY



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Title	PERIPHERAL POWER SUPPLY-2		
Size C	PROC162E1		Rev E1
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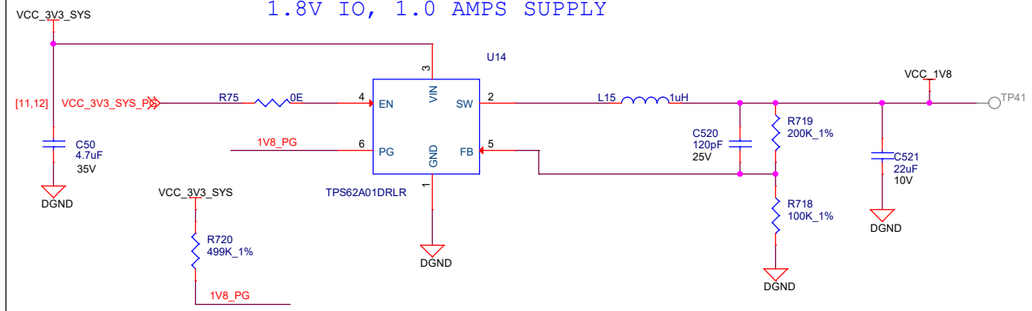
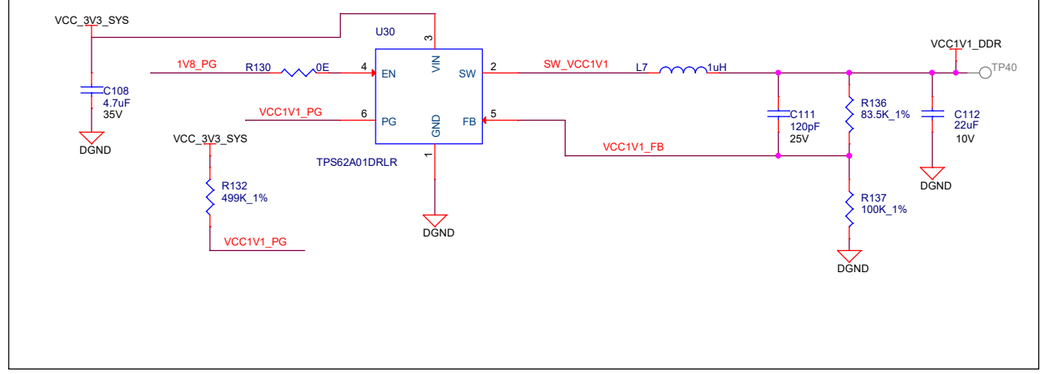
SOC POWER SUPPLY

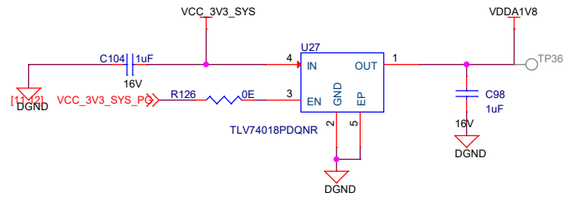
1.8V IO, 1.0 AMPS SUPPLY



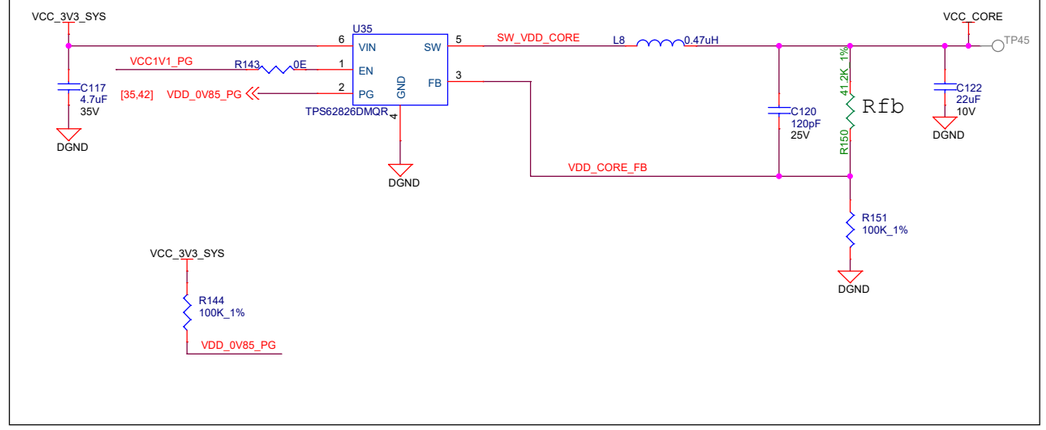
1.1V , 1.0 AMPS SUPPLY



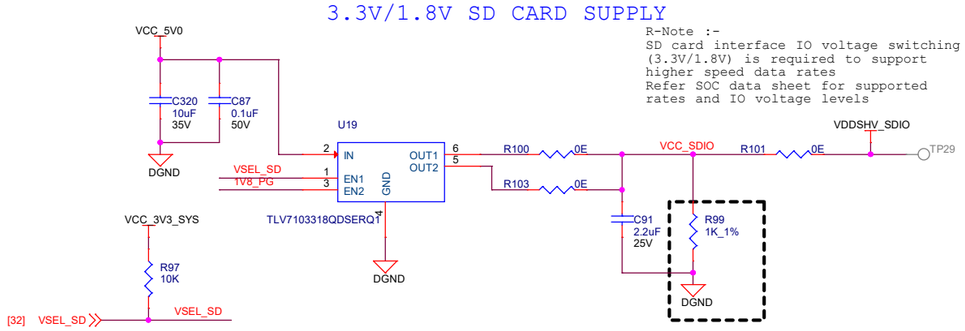
1.8V ANALOG , 0.3 AMPS SUPPLY



0.85V , 3.0 AMPS SUPPLY



3.3V/1.8V SD CARD SUPPLY



R-Note :-
SD card interface IO voltage switching (3.3V/1.8V) is required to support higher speed data rates
Refer SOC data sheet for supported rates and IO voltage levels

Note: Resistor is to 'bleed' off voltage.

VSEL_SD	SD VOLTAGE
HIGH(DEFAULT)	3.3V
LOW	1.8V

Designed for TI by Mistral Solutions Pvt Ltd

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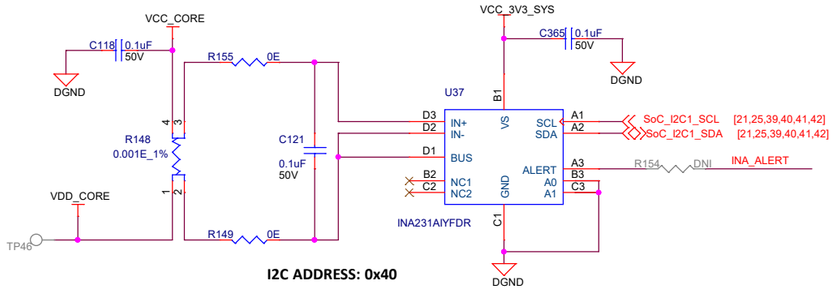
CURRENT MONITORING DEVICES

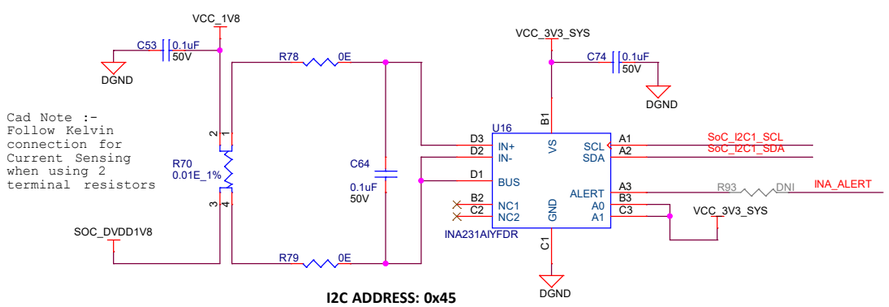
D-Note :-
Note the supply rail name change across
the shunt when optimizing the design
(Deleting the current sense resistor)

VDD_CORE



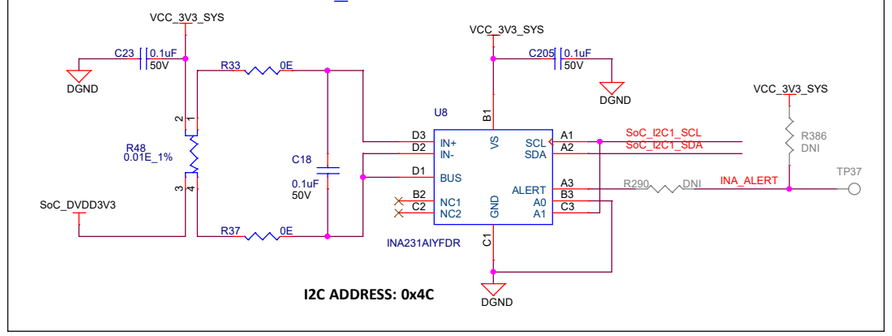
I2C ADDRESS: 0x40

SoC_DVDD1V8



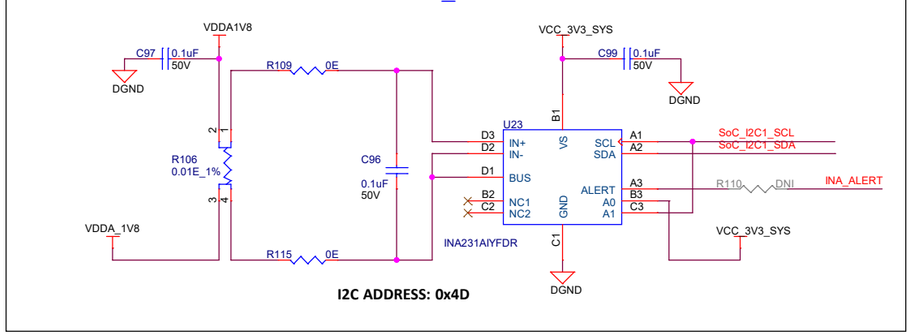
I2C ADDRESS: 0x45

SoC_DVDD3V3



I2C ADDRESS: 0x4C

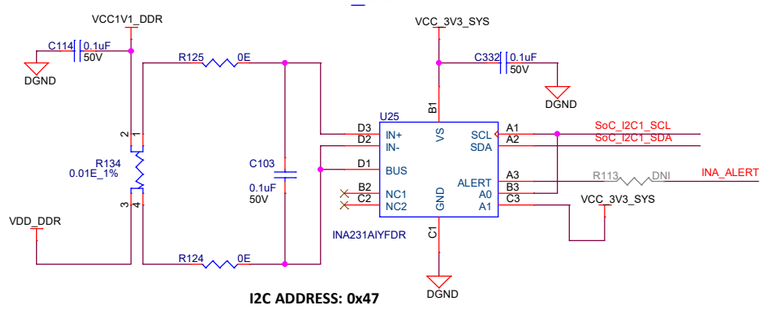
VDDA_1V8



I2C ADDRESS: 0x4D

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1_DDR	VDD_DDR	47

VDD_DDR



I2C ADDRESS: 0x47

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Title	CURRENT MONITORING DEVICES	
Size C	PROC162E1	Rev E1
Date: Friday, June 28, 2024	Sheet 13 of 44	

SOC POWER

D-Note :-
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure
It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts.
The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid false trigger
Refer System Power Supply Monitor Design Guidelines section of the data sheet

VCC_5V0
R375 100K_1%
VDDA_SYS_MON
C519 22pF 25V
R108 11K_1%
DGND

D-Note :-
VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V

D-Note :-
Changing the core voltage is not allowed after the device has been released from reset.
If you turn off the core supply, we expect you to turn off all power rails and ramp them down per the power-down sequence and wait until all supply rails decay below 300mv before turning on power again.

D-Note :-
Connecting 1.8V supply source directly to VPP continuously is not allowed

D-Note :-
Update the symbol
RSVD pins - Do not connect

D-Note :-
Note the Operating junction temperature range in the Recommended Operating Conditions section of the data sheet
https://www.ti.com/lit/ds/symlink/am625sip.pdf

U12K
ANALOG AND DIGITAL
AM6254ATLHJAMKR

VDD_CORE: H8, J11, J14, K17, L12, L15, M16, N8, N11, N13, P17, R11, R14, U12, V8, V15, V17
VDDR_CORE: J12, K16, N12, N14, P16, R12, T10, U14
VDD_DDR: K9, L8, M9, P9, R8
VDDA_1V8: G7
VDD_CORE: F8
SoC_DVDD1V8: G10
SoC_DVDD3V3: K10
VPP_1V8: H10
VDDA_SYS_MON: J8
TP105
TEMP_DIODE_P: E7

VDDSHV0: F15, G14 — SoC_DVDD3V3, SoC_DVDD1V8
VDDSHV1: L18, M19
VDDSHV2: W16, W19 — SoC_DVDD3V3
VDDSHV3: N18, P18, T19, U18 — SoC_DVDD1V8
VDDSHV4: T7 — VDDSHV_SDIO
VDDSHV5: G17 — SoC_DVDD1V8
VDDSHV6: J18 — SoC_DVDD3V3
VDDSHV_MCU: F11, G12
VDDSHV_CANUART: H9
VDDA_TEMP0: T9 — VDDA_1V8
VDDA_TEMP1: G16 — VDDA_1V8
VDDA_PLL0: U11 — VDDA_1V8
VDDA_PLL1: U15 — VDDA_1V8
VDDA_PLL2: L14 — VDDA_1V8
VDDA_MCU: L11 — VDDA_1V8
VDDA_1P8_OLDI0: W9
VDDA_1P8_OLDI0: W10 — VDDA_1V8
VDDA_CORE_USB: W12 — VDD_CORE
VDDA_CORE_CSIRX0: W13 — VDD_CORE
VDDA_1P8_CSIRX0: W14 — VDDA_1V8
VDDA_1P8_USB: Y11 — VDDA_1V8
VDDA_3P3_USB: Y13 — SoC_DVDD3V3

U12M
CAP
AM6254ATLHJAMKR

CAP_VDDS0 H15, CAP_VDDS1 K18, CAP_VDDS2 W17, CAP_VDDS3 P19, CAP_VDDS4 U7, CAP_VDDS5 H17, CAP_VDDS6 J19
CAP_VDDS_MCU H11
CAP_VDDS_CANUART G9

C256 1uF 16V, C251 1uF 16V, C302 1uF 16V, C258 1uF 16V, C239 1uF 16V, C276 1uF 16V, C294 1uF 16V, C269 1uF 16V, C257 1uF 16V
DGND

D-Note :-
Select cap with less the 1 ohm ESR
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package
Refer SoC Data sheet

D-Note :-
Refer SK-AM62B to add ferrites for sensitive analog and clock supply rails

D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the CSI analog and core supplies when CSI is not used
Ferrites and Bulk caps are optional when CSI is not used and boundary scan is used

D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

1.8V Analog SUPPLY

VDDA_1V8: C243 0.1uF 16V, C270 0.01uF 25V
VDDA_1V8: C245 0.1uF 16V, C288 0.01uF 25V
VDDA_1V8: C88 1uF 16V
VDDA_1V8: C298 0.1uF 16V, C287 0.01uF 25V
VDDA_1V8: C221 0.1uF 16V, C220 0.01uF 25V
VDDA_1V8: C89 0.1uF 16V, C90 0.01uF 25V
VDDA_1V8: C300 0.1uF 16V, C296 0.01uF 25V
VDDA_1V8: C284 0.1uF 16V, C290 0.01uF 25V
DGND

CORE SUPPLY

VDD_CORE: C283 0.1uF 16V, C289 0.01uF 25V
VDD_CORE: C49 4.7uF 10V
VDD_CORE: C275 0.1uF 16V, C281 0.01uF 25V
VDD_CORE: C54 0.1uF 16V, C51 0.01uF 25V
DGND

3.3V/1.8V MMC1 SUPPLY

VDDSHV_SDIO: C263 0.1uF 16V
DGND

D-Note :-
Common SOC LVCMOS IO interface guidelines
1. Mosy of the SOC IOs are not fail-safe. Mo input should be applied before supply ramps
2. SOC LVCOMOS IOs have slew rate requirements specified
3. SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IO
4. Any SOC IO that has a trace connected needs a parallel pull. When adding pull is not feasible, ensure the traces are paced away from noisy signals

D-Note :-
A Trace connected to SOC is effectively an antenna that will pick up noise. A potential will be generated on the signal when noise couples into the antenna. This potential will be largest on the highest impedance end of the signal. By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC POWER	
Size	PROC162E1	Rev E1
C		
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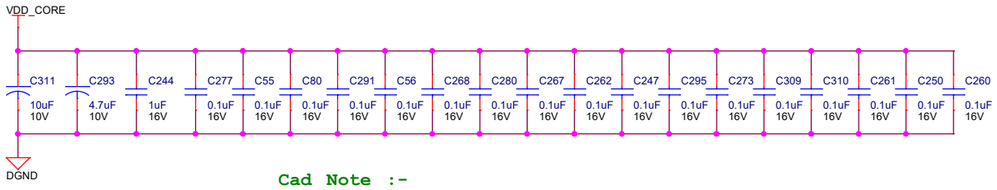
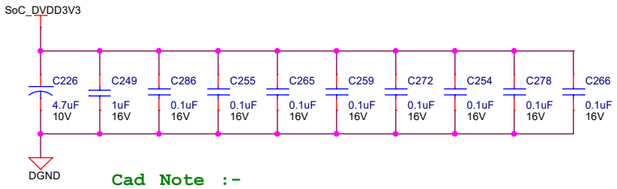
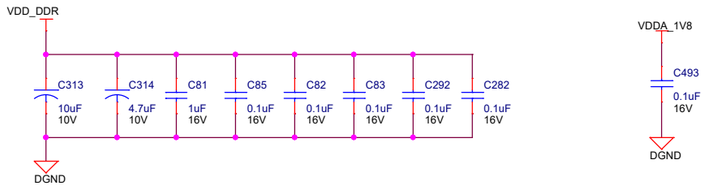
SOC POWER DECAPS



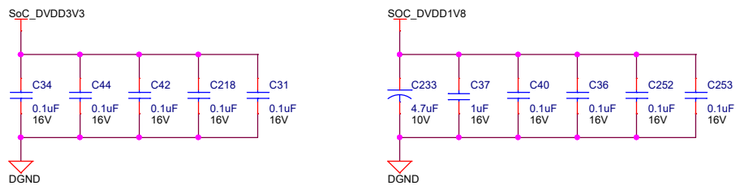
Cad Note :-
Place 0.1 uF caps near to SoC pins



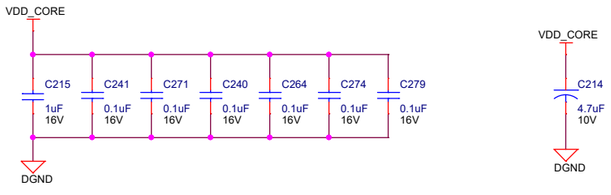
Cad Note :-
Place 0.1 uF caps near to SoC pins



Cad Note :-
Place 0.1 uF caps near to SoC pins

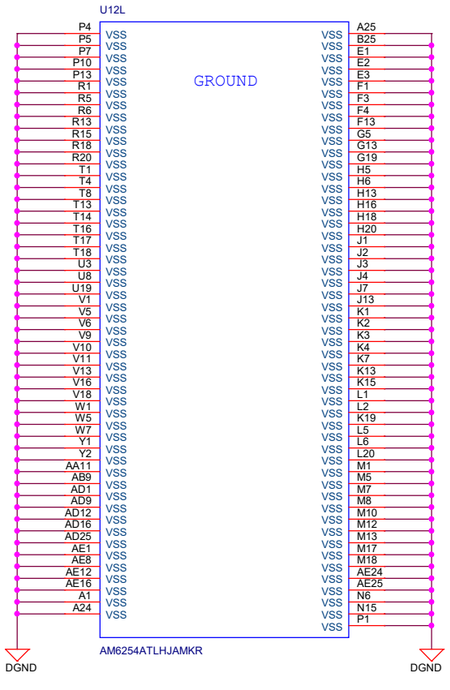


Cad Note :-
Place 0.1 uF caps near to SoC pins



Cad Note :-
Place 0.1 uF caps near to SoC pins

SOC VSS



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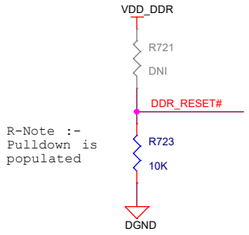
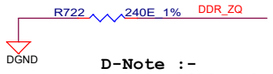
Title	SOC POWER CAPS & SOC VSS		
Size	C	PROC162E1	Rev
Date:	Friday, June 28, 2024	Sheet 15 of 44	

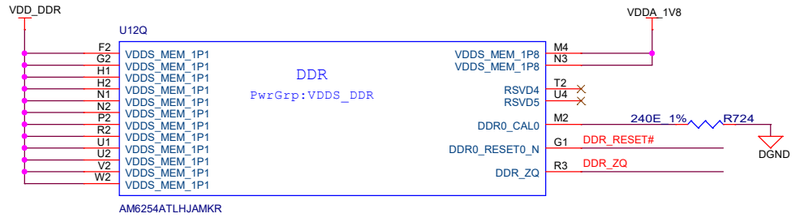
SOC LPDDR4 POWER SUPPLY



R-Note :-
Pulldown is
populated

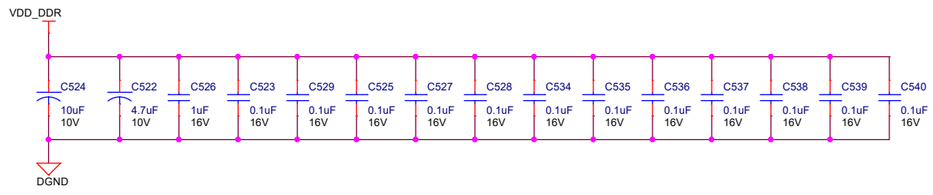


D-Note :-
Delete DGND net
Connect DDR_Zq to VDD_DDR

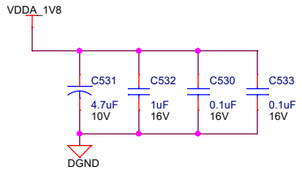


D-Note :-
The current version of PCB file has Zq connected to ground
and the SKs have been modified to connect to 1.1V.
This update is required to be taken care during board design
when reusing SK PCB files.

SOC INTERNAL LPDDR4 SUPPLY DECAPS



Place one 0.1uF cap near each Pin

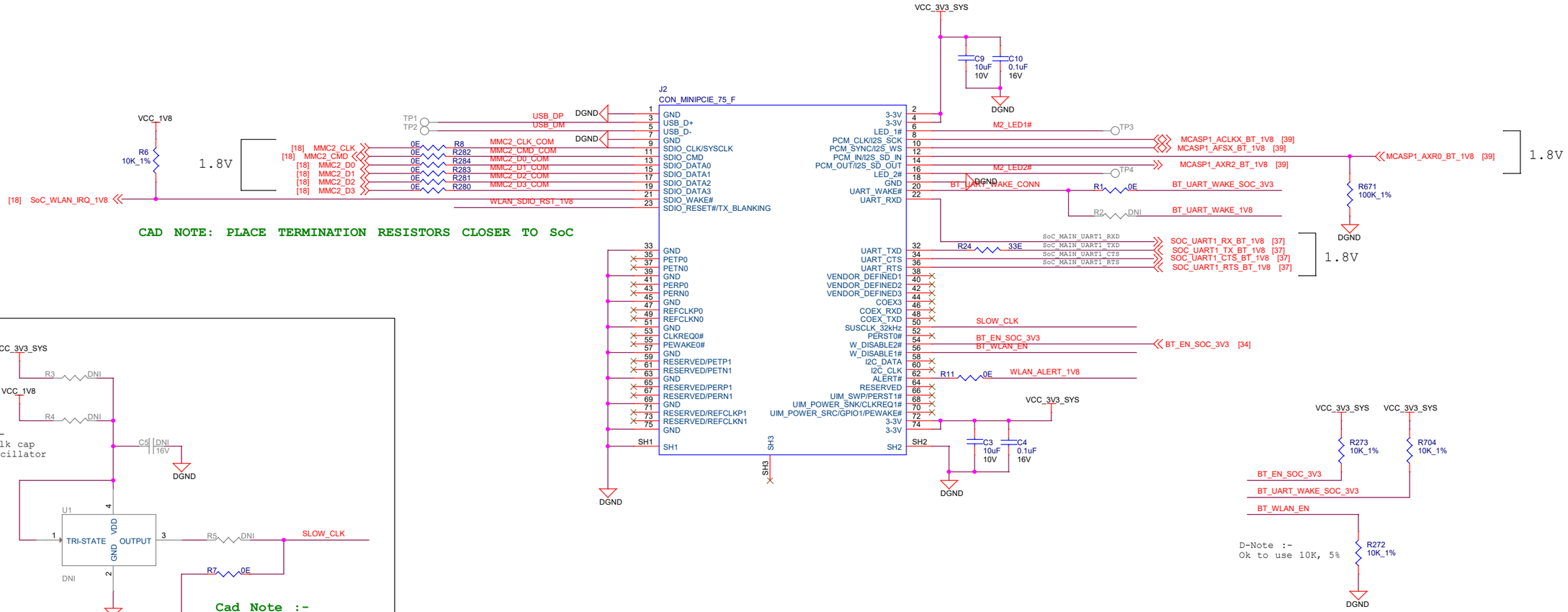


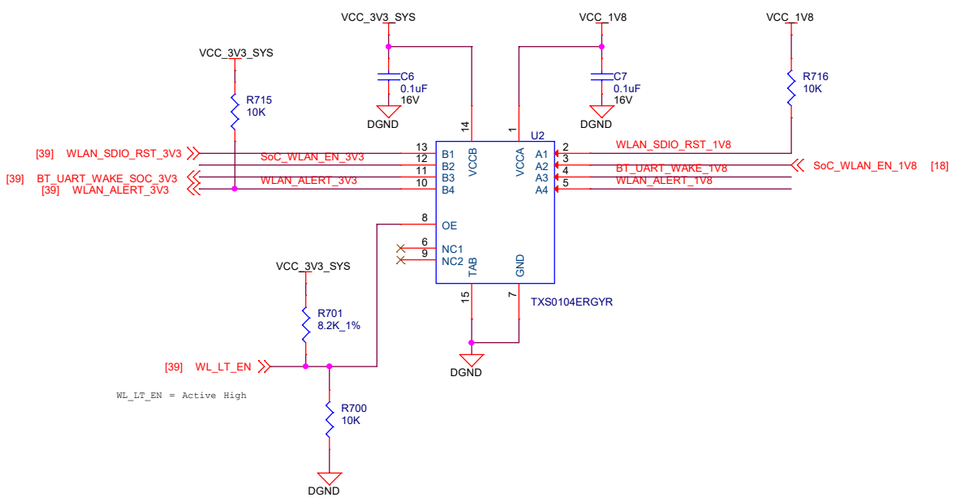
Place one 0.1uF cap near each Pin

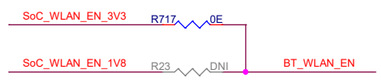
Designed for TI by Mistral Solutions Pvt Ltd

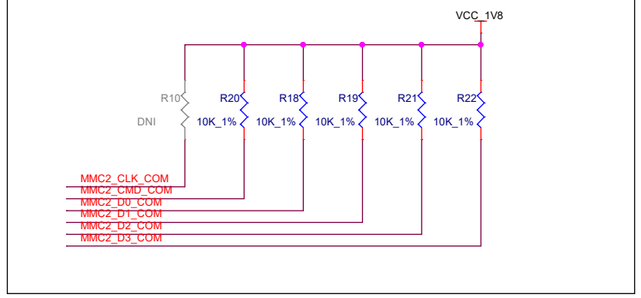
Title	DDR POWER		
Size	PROC162E1		Rev
C			E1
Date:	Friday, June 28, 2024	Sheet 16 of 44	

M.2 INTERFACE





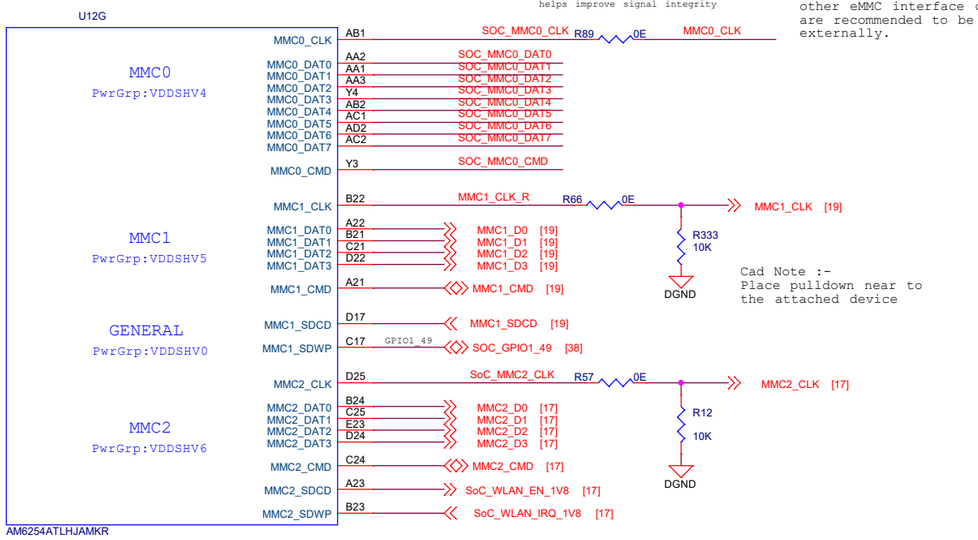




Designed for TI by Mistral Solutions Pvt Ltd

Title	WL1837 MODULE	
Size C	PROC162E1	Rev E1
Date: Friday, June 28, 2024	Sheet 17 of 44	

SOC - MMC Interface



AM6254ATLHJAMKR

D-Note :-
Series resistor provision
helps improve signal integrity

D-Note :-
This family of processor implements a soft PHY for eMMC interface.
The pull required for D0, Clock and other eMMC interface control signals are recommended to be implemented externally.

Cad Note :-
Place pulldown near to the attached device

D-Note :-
MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)

R-Note :-
What is the reason we selected pulldown instead of pullup for EMMC, SD card or other peripherals?
Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

D-Note :-
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or OLDI0 or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

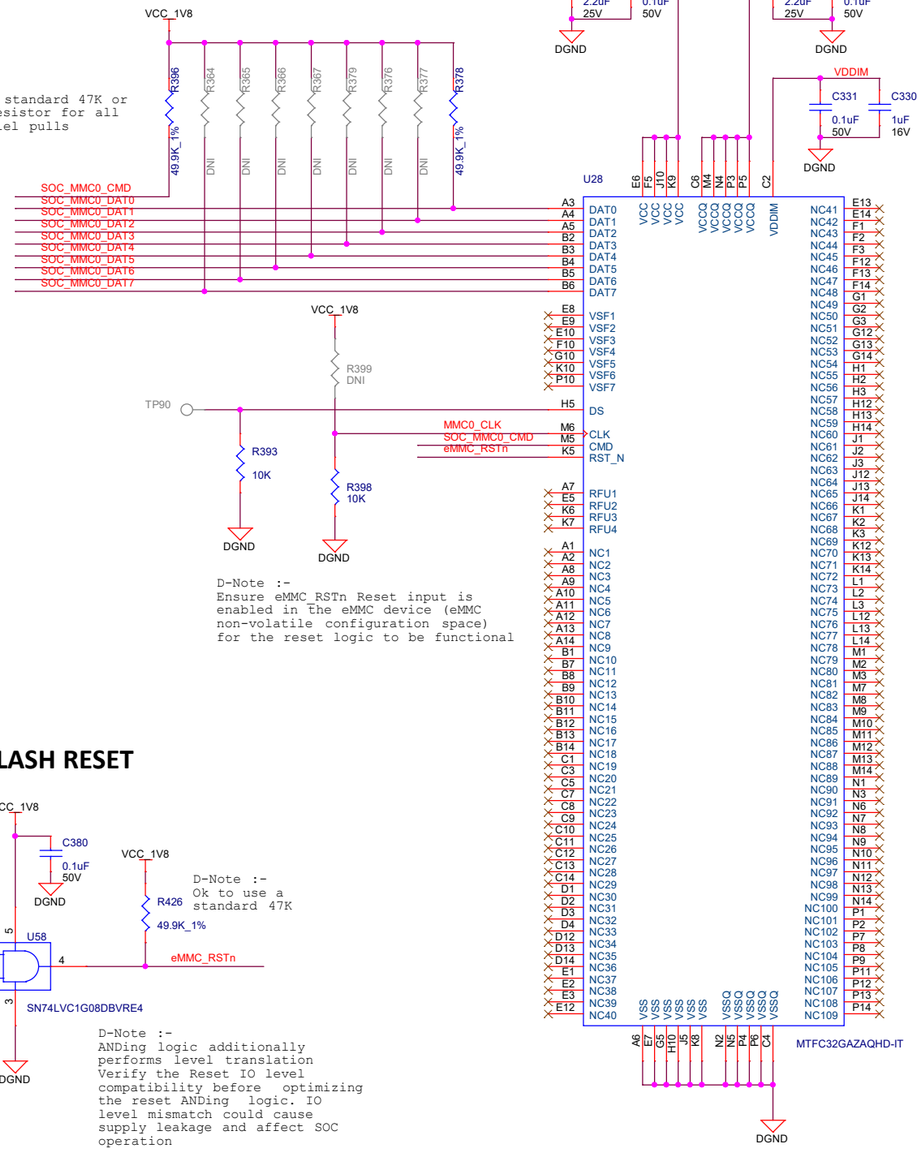
D-Note :-
You could eliminate the GPIO option and only use the reset output (Warm or cold), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.

eMMC FLASH

D-Note :-
For D7..D1 eMMC device is expected to have the pullups enabled by default. The eMMC host/phy disables the eMMC device pullups and enables SOC internal pullups. Provision for external pullups is optional or the pullups can be deleted

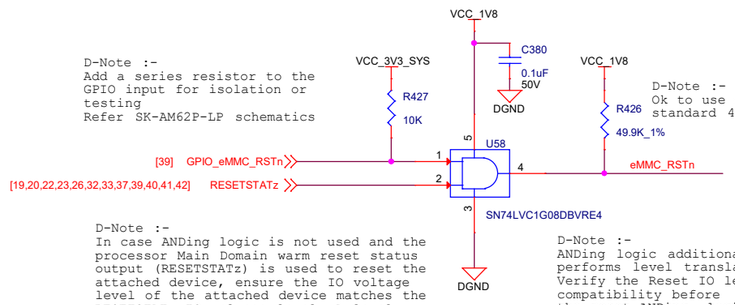
D-Note :-
Add additional decaps as required
Refer SK-AM62P-LP schematics

D-Note :-
Ok to use standard 47K or similar resistor for all the parallel pulls



D-Note :-
Ensure eMMC_RSTn Reset input is enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional

eMMC FLASH RESET



D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

D-Note :-
Ok to use a standard 47K

D-Note :-
In case ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level.
A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is selected. If too high the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If too low it will cause the AM62x to source too much steady-state current during normal operation.

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch could cause supply leakage and affect SOC operation

Designed for TI by Mistral Solutions Pvt Ltd

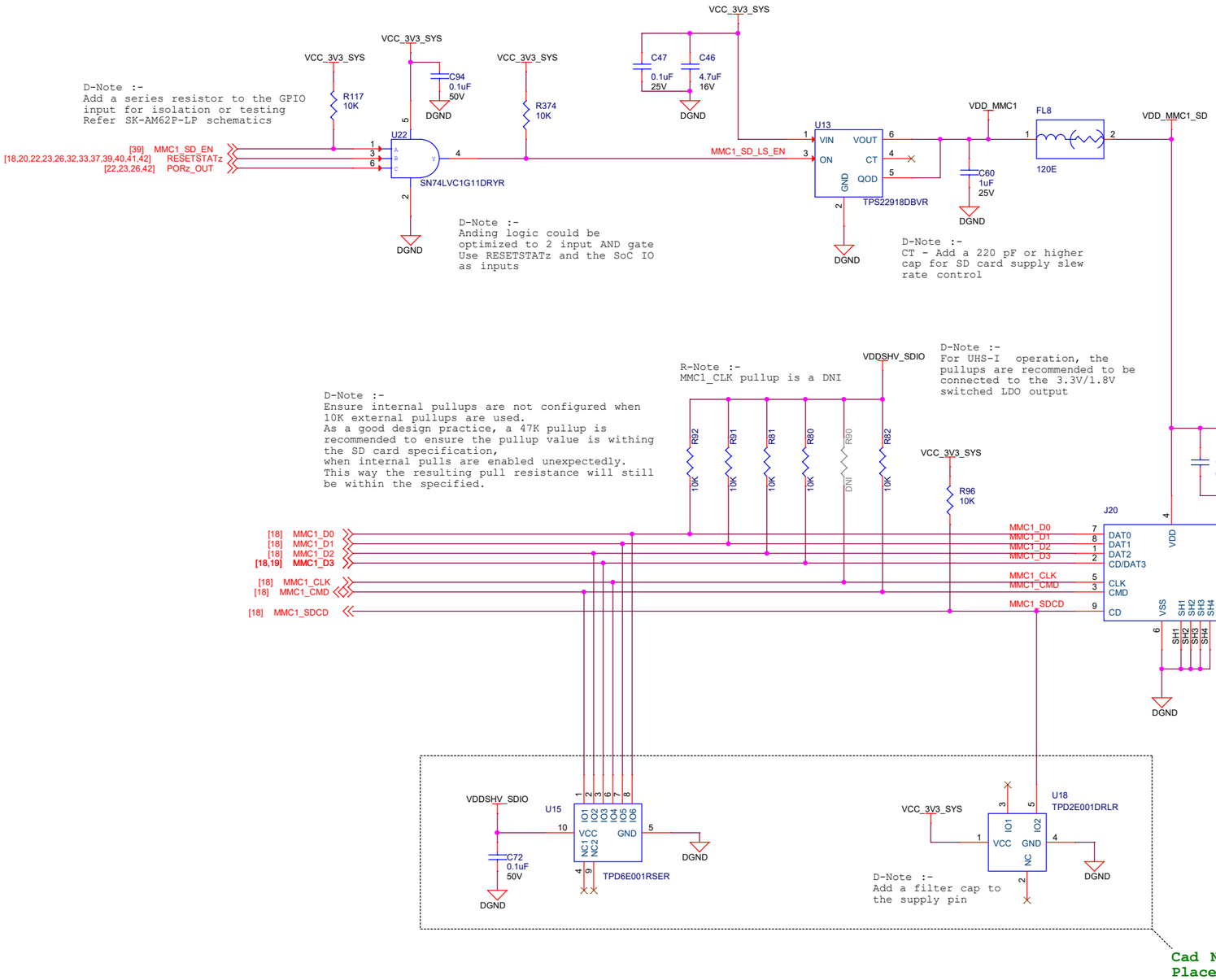
Title	eMMC FLASH INTERFACE	
Size C	PROC162E1	Rev E1
Date: Friday, June 28, 2024	Sheet 18 of 44	

SD CARD INTERFACE

D-Note :-
This power switch, along with the reset logic, and the host IO power supply circuit is required to support UHS-I SD Cards which begins communications using 3.3V signal levels and later change to 1.8V signal levels when changing to one of the faster data transfer speeds.
Cycling power to the SD Card is the only way to put it back into 3.3V mode since SD Cards do not have a reset pin.
The host IO power supply must power off/on and change voltage at the same time as the SD Card. These circuits and the software driver operating the signals sourcing these circuits ensure both devices are off, or on and operating at the same IO voltage at the same time.

SD CARD LOAD SWITCH RESET LOGIC

LOAD SWITCH

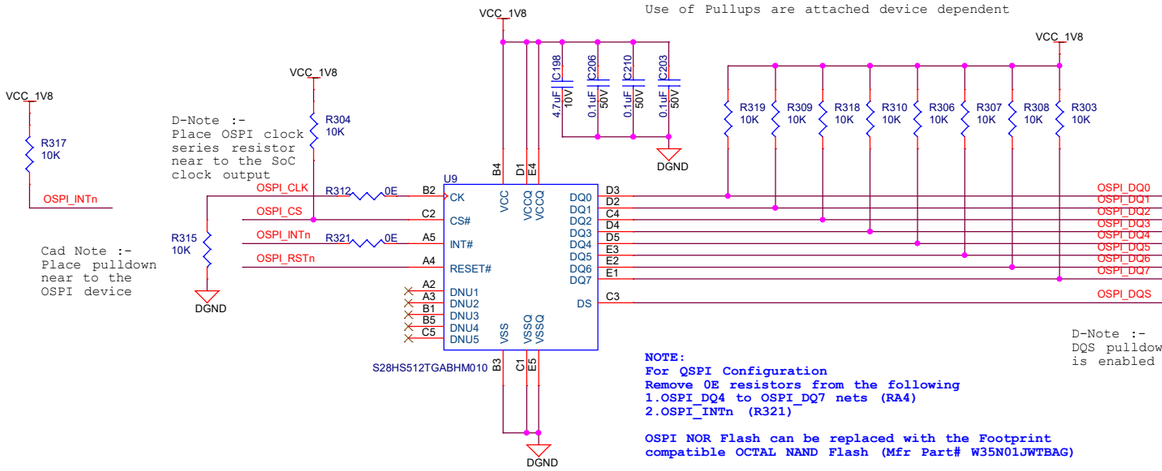


Designed for TI by Mistral Solutions Pvt Ltd

Title	SD CARD INTERFACE	
Size C	PROC162E1	Rev E1
Date: Friday, June 28, 2024	Sheet 19 of 44	

OSPI FLASH

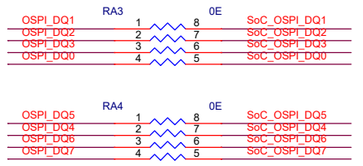
R-Note :-
SOC IO buffers are off during power-up. A pullup is recommended near to the attached device, to hold the attached device IOs in a known state.
Use of Pullups are attached device dependent



NOTE:
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (RA4)
2.OSPI_INTn (R321)

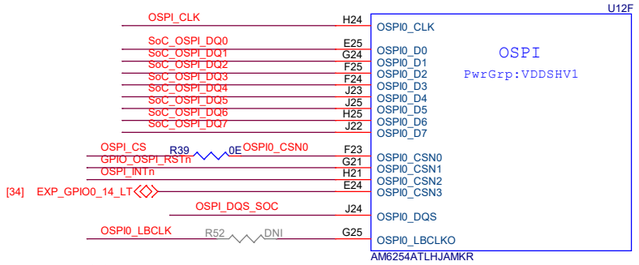
OSPI NOR Flash can be replaced with the Footprint compatible OCTAL NAND Flash (Mfr Part# W35N01JWTBAG)

D-Note :-
These 0R resistors are used for configuring QSPI and OSPI
This is optional during custom board design



D-Note :-
Connecting OSPI interface to multiple devices is not recommended or supported

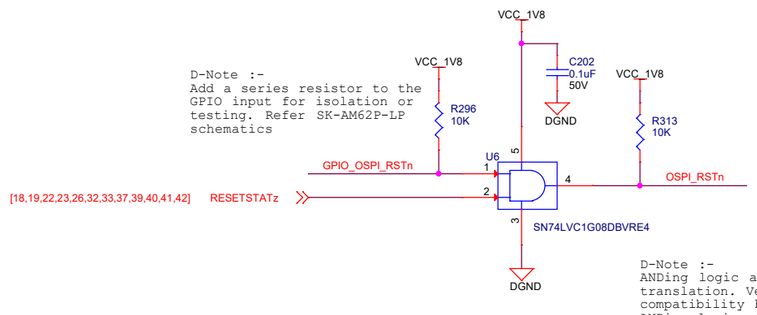
SOC OSPI INTERFACE



R-Note :-
External loopback clock series resistors are DNI when DQS is connected

Cad Note :-
Place R52 close to the SOC Ball with as little trace as possible

OSPI FLASH RESET

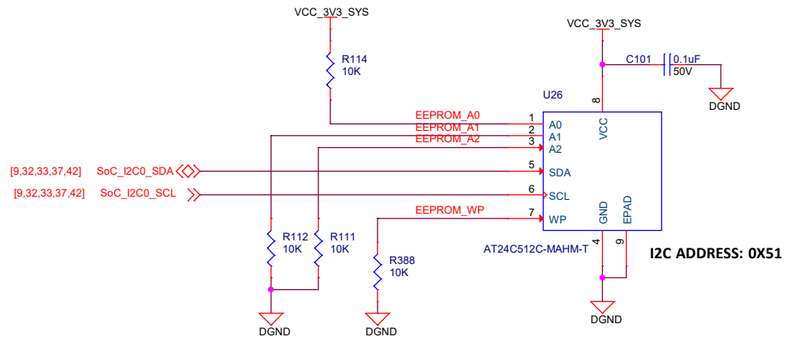


D-Note :-
ANDing logic additionally performs level translation. Verify the Reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch could cause supply leakage and affect SOC operation

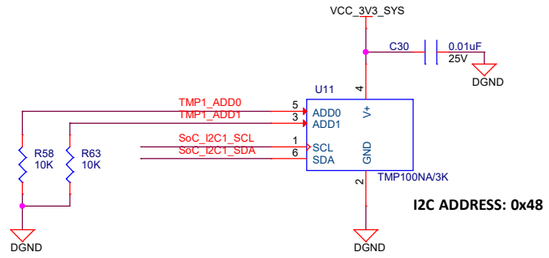
Designed for TI by Mistral Solutions Pvt Ltd

Title	OSPI INTERFACE		
Size C	PROC162E1		Rev E1
Date: Friday, June 28, 2024		Sheet 20 of 44	

BOARD ID EEPROM



DIGITAL TEMPERATURE SENSOR



CAD NOTE: PLACE TEMP SENSOR CLOSE TO SoC

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOARD ID EEPROM & TEMPERATURE SENSORS	
Size: C	PROC162E1	Rev: E1
Date: Friday, June 28, 2024	Sheet 21 of 44	

CPSW3G RGMII 1 - ETHERNET PHY

D-Note :-
The caps and values used are as per the EPHY data sheet recommendations.

VCC_3V3_SYS: C301 0.1uF 16V, C315 0.1uF 16V, C76 0.1uF 16V, C316 1uF 16V, C307 1uF 16V, C58 1uF 16V, C319 10uF 10V, C84 0.01uF 25V → DGND

VDD_1V0: C73 0.1uF 16V, C70 0.1uF 16V, C63 0.1uF 16V, C318 0.1uF 16V, C306 1uF 16V, C317 1uF 16V, C62 1uF 16V, C71 1uF 16V, C69 10uF 10V, C61 0.01uF 25V → DGND

VDD_2V5: C68 0.1uF 16V, C304 0.1uF 16V, C78 1uF 16V, C308 1uF 16V, C77 10uF 10V, C67 0.01uF 25V → DGND

D-Note :-
Refer to DP83867ERGZ-R-EVM when using LAN Discrete Transformer Module and RJ45 connector

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

R-Note :-
Ferrite is DNI

VCC_3V3_SYS, TP100, TP30, VDD_2V5, VDD_1V0

U51 DP83867IRRGZ

[24] CPSW_RGMII1_TD0	28	TX_D0
[24] CPSW_RGMII1_TD1	27	TX_D1
[24] CPSW_RGMII1_TD2	26	TX_D2
[24] CPSW_RGMII1_TD3	25	TX_D3
[24] CPSW_RGMII1_TXC	29	GTX_CLK
[24] CPSW_RGMII1_TX_CTL	37	TX_EN/TX_CTRL
[24] CPSW_RGMII1_RD0	33	RX_D0
[24] CPSW_RGMII1_RD1	34	RX_D1
[24] CPSW_RGMII1_RD2	35	RX_D2
[24] CPSW_RGMII1_RD3	36	RX_D3
[24] CPSW_RGMII1_RXC	32	RX_CLK
[24] CPSW_RGMII1_RX_CTL	38	RX_DV/RX_CTRL
[24] CPSW_RGMII1_ETH1_CLK	15	XI
	14	XO
	20	JTAG_CLK
	22	JTAG_TMS
	23	JTAG_TDI
	21	JTAG_TDO
CPSW_RGMII1_ETH1_CLK_OUT	18	CLK_OUT
CPSW_RGMII1_MDC	16	MDC
CPSW_RGMII1_MDIO	17	MDIO
CPSW_RGMII_INTn	44	INT/PWDN
CPSW_RGMII1_ETH1_RBIAS	12	RBIAS
CPSW_RGMII1_RESETn	43	RESET_N
	49	GND

VDDIO, VDDIO, VDDIO; VDDA1P8, VDDA1P8; VDDA2P5, VDDA2P5; VDD1P0, VDD1P0, VDD1P0, VDD1P0

TD_P_A	1	CPSW_ETH1_D0P
TD_M_A	2	CPSW_ETH1_D0N
TD_P_B	4	CPSW_ETH1_D1P
TD_M_B	5	CPSW_ETH1_D1M
TD_P_C	7	CPSW_ETH1_D2P
TD_M_C	8	CPSW_ETH1_D2M
TD_P_D	10	CPSW_ETH1_D3P
TD_M_D	11	CPSW_ETH1_D3M
LED_0	47	CPSW_ETH1_LED0 → TP26
LED_1	46	CPSW_ETH1_LED_1000 → TP27
LED_2	45	CPSW_ETH1_LED_ACT → TP22
GPIO_0	39	R354 0E CPSW_ETH1_GPIO_0 → TP23
GPIO_1	40	R353 0E CPSW_ETH1_GPIO_1 → TP24

D-Note :-
Provide provision for Series resistor based on EPHY for RX signals near to EPHY

R359 0E

D-Note :-
XI clock Input amplitude allowed is 1.8V irrespective of the IO supply Use a CAP DIVIDER when the clock amplified is 3.3V

TP102

D-Note :-
Refer EPHY EVM for JTAG connection

TP32

VCC_3V3_SYS

R362 DNI CPSW_RGMII1_MDC
R363 DNI CPSW_RGMII1_MDIO
R352 2.2K 1% CPSW_RGMII_INTn
R361 10K 1% CPSW_RGMII1_ETH1_RBIAS
C312 22pF 25V → DGND

[23] CPSW_RGMII_INTn → CPSW_RGMII_INTn
[32,42] CPSW_RGMII_INTn/PRU_INTn → R72 0E → CPSW_RGMII_INTn
[23,24] SoC_RGMII_MDC → R102 0E → CPSW_RGMII1_MDC
[23,24] SoC_RGMII_MDIO → R64 0E → CPSW_RGMII1_MDIO

R-Note :-
Pullup is enabled for GPIO input RESETSTATz series resistor is DNI

D-Note :-
Add a isolation resistor to the GPIO input for isolation or testing Refer SK-AM62P-LP schematics

VCC_3V3_SYS
R192 10K, R191 10K
C148 0.1uF 16V → DGND

U40 SN74LVC1G11DRYR

[39] GPIO_CPSW1_RST
[19,23,26,42] PORz_OUT
[18,19,20,23,26,32,33,37,39,40,41,42] RESETSTATz
R189 DNI
R190 DNI
CPSW_RGMII1_RESETn
R481 10K → DGND

D-Note :-
ANDing logic could be optimized to 2 input AND gate Use RESETSTATz and the SoC IO as inputs

D-Note :-
ANDing logic additionally performs level translation. Verify the Reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch could cause supply leakage and affect SOC operation

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

VCC_3V3_SYS
FL20 DNI

J6

2	9	J1
10	7	J2
8	5	J3
6	3	J4
4	1	J5
		J7
		J8
SH1	15	
SH2	16	

VCC_3V3_SYS
R342 220E
CPSW1_LED_1000 → 12 YELLOW GREEN RIGHT LED
CPSW1_LED_ACT → 13 YELLOW GREEN LEFT LED
CPSW1_GPIO_0 → 14

CON_RJ45-14_LPJG16314A4NL

C327 DNI 2KV
R339 0E
DGND, ETH1_EARTH

Silk: CPSW PHY-1

VCC_3V3_SYS
R357 DNI, R356 DNI, R349 5.76K_1%, R351 10K, R76 DNI, R347 DNI, R344 DNI
CPSW_RGMII1_RD0
CPSW_RGMII1_RD2
CPSW_RGMII1_RX_CTL
CPSW_ETH1_LED_1000
CPSW_ETH1_LED_ACT
CPSW_ETH1_GPIO_0
CPSW_ETH1_GPIO_1
R86 DNI, R85 DNI, R350 2.49K_1%, R84 2.49K_1%, R348 DNI, R346 DNI, R345 DNI
→ DGND

CPSW1_LED_1000 → Q7 CSD16301Q2
CPSW_ETH1_LED_1000 R335 0E
→ DGND

VCC_3V3_SYS
R371 220E
CPSW1_GPIO_0 → Q9 CSD16301Q2
CPSW_ETH1_GPIO_0 R387 0E
→ DGND

VCC_3V3_SYS
R341 220E
CPSW1_LED_ACT → Q8 CSD16301Q2
CPSW_ETH1_LED_ACT R383 0E
→ DGND

PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 2ns
Rx Clock Skew = 2ns

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_1 ETHERNET PHY	
Size C	PROC162E1	Rev E1
Date: Friday, June 28, 2024	Sheet 22 of 44	

CPSW3G RGMII 2 - ETHERNET PHY

D-Note :-
The caps and values used are as per the EPHY data sheet recommendations.

VCC_3V3_SYS: C235 0.1uF 16V, C32 0.1uF 16V, C208 0.1uF 16V, C236 1uF 16V, C19 1uF 16V, C227 1uF 16V, C242 10uF 10V, C38 0.01uF 25V → DGND

VDD_1V0: C27 0.1uF 16V, C238 0.1uF 16V, C22 0.1uF 16V, C29 0.1uF 16V, C237 1uF 16V, C224 1uF 16V, C21 1uF 16V, C28 1uF 16V, C39 10uF 10V, C26 0.01uF 25V → DGND

VDD_2V5: C216 0.1uF 16V, C25 0.1uF 16V, C35 1uF 16V, C228 1uF 16V, C33 10uF 10V, C24 0.01uF 25V → DGND

D-Note :-
Refer to DP83867ERGZ-R-EVM when using LAN Discrete Transformer Module and RJ45 connector

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

R-Note :-
Ferrite is DNI

VCC_3V3_SYS, TP101, TP19, VDD_2V5, VDD_1V0

U49 DP83867IRRGZ

28	TX_D0	[24] CPSW_RGMII2_TD0
27	TX_D1	[24] CPSW_RGMII2_TD1
26	TX_D2	[24] CPSW_RGMII2_TD2
25	TX_D3	[24] CPSW_RGMII2_TD3
29	GTX_CLK	[24] CPSW_RGMII2_TXC
37	TX_EN/TX_CTRL	[24] CPSW_RGMII2_TX_CTL
33	RX_D0	[24] CPSW_RGMII2_RD0
34	RX_D1	[24] CPSW_RGMII2_RD1
35	RX_D2	[24] CPSW_RGMII2_RD2
36	RX_D3	[24] CPSW_RGMII2_RD3
32	RX_CLK	[24] CPSW_RGMII2_RXC
38	RX_DV/RX_CTRL	[24] CPSW_RGMII2_RX_CTL
15	XI	[24] CPSW_RGMII2_ETH2_CLK
14	XO	TP103
20	JTAG_CLK	
22	JTAG_TMS	
23	JTAG_TDI	
21	JTAG_TDO	
18	CLK_OUT	CPSW_RGMII2_ETH2_CLK_OUT
16	MDC	CPSW_RGMII2_MDC
17	MDIO	CPSW_RGMII2_MDIO
44	INT/PWDN	CPSW_RGMII_INTn
12	RBIAS	CPSW_RGMII2_ETH2_RBIAS
43	RESET_N	
49	GND	DGND
19, 30, 41	VDDIO	VCC_3V3_SYS
13, 48	VDDA1P8	VCC_3V3_SYS
3, 9	VDDA2P5	VDD_2V5
6, 24, 31, 42	VDD1P0	VDD_1V0

1	TD_P_A	CPSW_ETH2_D0P
2	TD_M_A	CPSW_ETH2_D0N
4	TD_P_B	CPSW_ETH2_D1P
5	TD_M_B	CPSW_ETH2_D1M
7	TD_P_C	CPSW_ETH2_D2P
8	TD_M_C	CPSW_ETH2_D2M
10	TD_P_D	CPSW_ETH2_D3P
11	TD_M_D	CPSW_ETH2_D3M
47	LED_0	CPSW_ETH2_LED0 → TP15
46	LED_1	CPSW_ETH2_LED_1000 → TP17
45	LED_2	CPSW_ETH2_LED_ACT → TP11
39	GPIO_0	R302 0E CPSW_ETH2_GPIO_0 → TP12
40	GPIO_1	R301 0E CPSW_ETH2_GPIO_1 → TP13

D-Note :-
Provision for Series resistor based on EPHY for RX signals near to EPHY

R324 0E

VCC_3V3_SYS: R330 1.5K, R329 DNI, R672 DNI

TP20

R328 10K 1%, C234 22pF 25V → DGND

[22] CPSW_RGMII_INTn

[22,24] SoC_RGMII_MDC — R673 0E — CPSW_RGMII2_MDC

[22,24] SoC_RGMII_MDIO — R674 0E — CPSW_RGMII2_MDIO

R-Note :-
Pullup is enabled for GPIO input RESETSTATz series resistor is DNI

D-Note :-
Add a isolation resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

VCC_3V3_SYS: R197 10K, R196 10K, C157 0.1uF 16V → DGND

[39] GPIO_CPSW2_RST
[19,22,26,42] PORz_OUT
[18,19,20,22,26,32,33,37,39,40,41,42] RESETSTATz
R194 DNI

U41 SN74LVC1G11DRYR

CPSW_RGMII2_RESETn

R195 DNI

R35 10K → DGND

D-Note :-
Anding logic could be optimized to 2 input AND gate. Use RESETSTATz and the SoC IO as inputs

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

VCC_3V3_SYS — FL15 DNI

J4

2	TD1+	J1
9	TD1-	J1
10	TD2+	J2
7	TD2-	J2
8	TD3+	J6
5	TD3-	J6
6	TD4+	J5
3	TD4-	J5
4	CT	J7
1	CT	J7
11	LED_A	J8
12	LED_B	J8
13	LED_C	J8
14	LED_D	J8
SH1 15, SH2 16	SHIELD	J8

YELLOW / GREEN — RIGHT LED

CPSW2_LED_1000 — 12
CPSW2_LED_ACT — 13
CPSW2_GPIO_0 — 14

YELLOW / GREEN — LEFT LED

R286 220E

CON_RJ45-14_LPJG16314A4NL

C195 DNI 2KV, R29 0E → DGND, ETH2_EARTH

Silk: CPSW PHY-2

VCC_3V3_SYS: R322 10K, R311 DNI, R298 5.76K_1%, R300 10K, R38 DNI, R294 DNI, R291 DNI

CPSW_RGMII2_RD0
CPSW_RGMII2_RD2
CPSW_RGMII2_RX_CTL
CPSW_ETH2_LED_1000
CPSW_ETH2_LED_ACT
CPSW_ETH2_GPIO_0
CPSW_ETH2_GPIO_1

R54 2.49K_1%, R49 DNI, R299 2.49K_1%, R47 2.49K_1%, R295 DNI, R293 DNI, R292 DNI → DGND

PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 2ns
Rx Clock Skew = 2ns

CPSW2_LED_1000 — Q4 CSD16301Q2 — CPSW_ETH2_LED_1000 — R289 0E → DGND

VCC_3V3_SYS — R334 220E — CPSW2_GPIO_0 — Q6 CSD16301Q2 — CPSW_ETH2_GPIO_0 — R340 0E → DGND

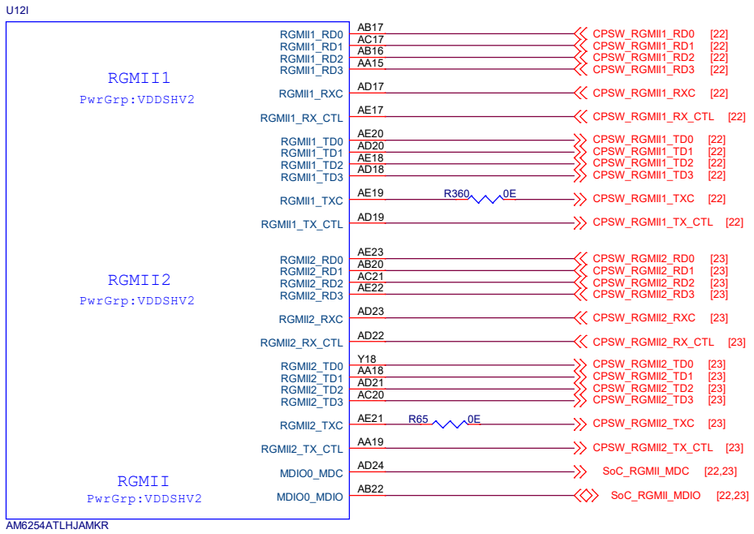
VCC_3V3_SYS — R288 220E — CPSW2_LED_ACT — Q5 CSD16301Q2 — CPSW_ETH2_LED_ACT — R338 0E → DGND

Designed for TI by Mistral Solutions Pvt Ltd

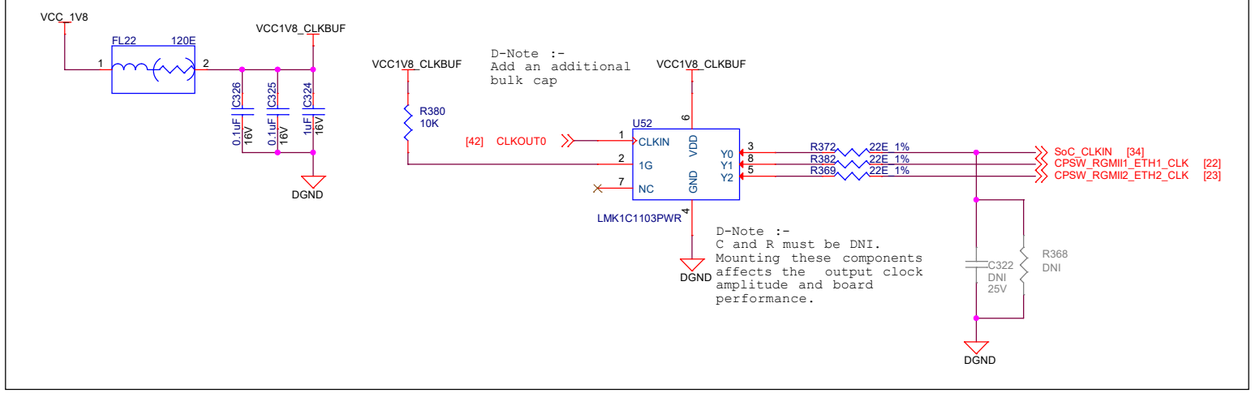
Title	CPSW RGMII_2 ETHERNET PHY		
Size	C	PROC162E1	Rev E1
Date:	Friday, June 28, 2024	Sheet 23 of 44	

SOC MAC INTERFACE

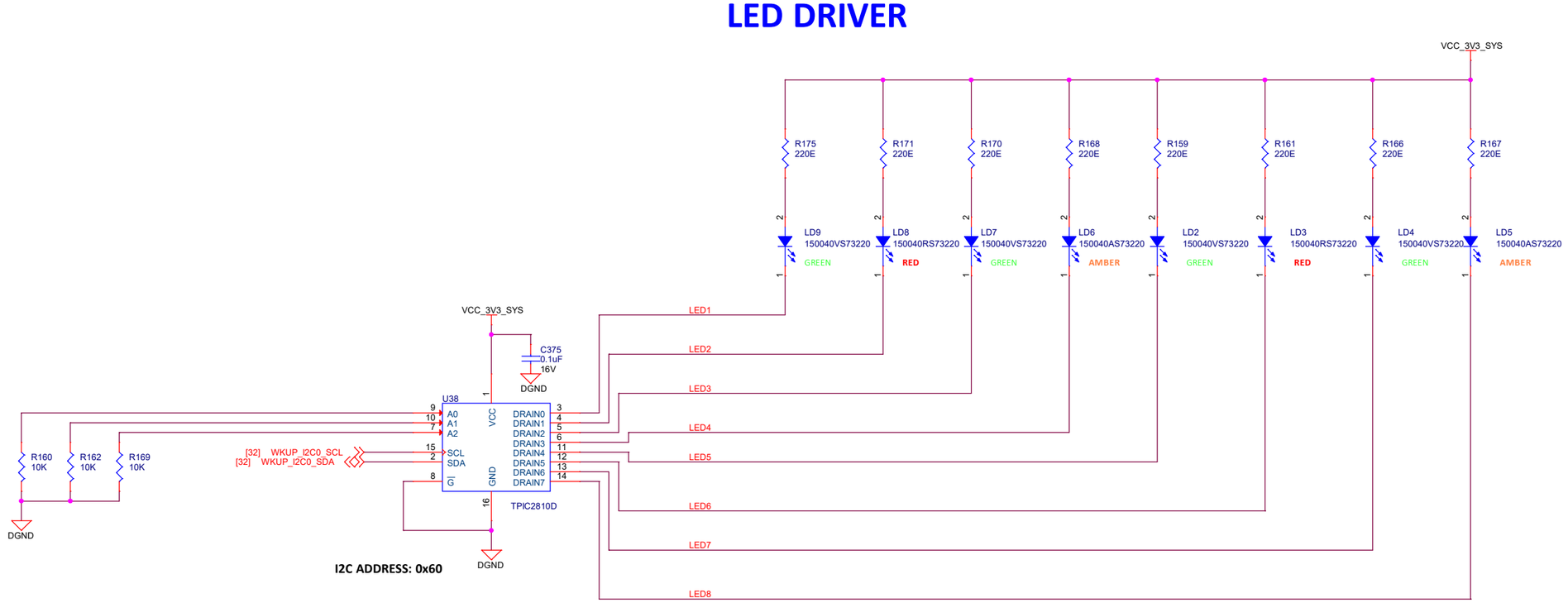
D-Note :-
Add series resistors 22 R on the Ethernet interface TX (TDx) signals near to the SoC



CLOCK BUFFER FOR SOC AND ETHERNET PHYs



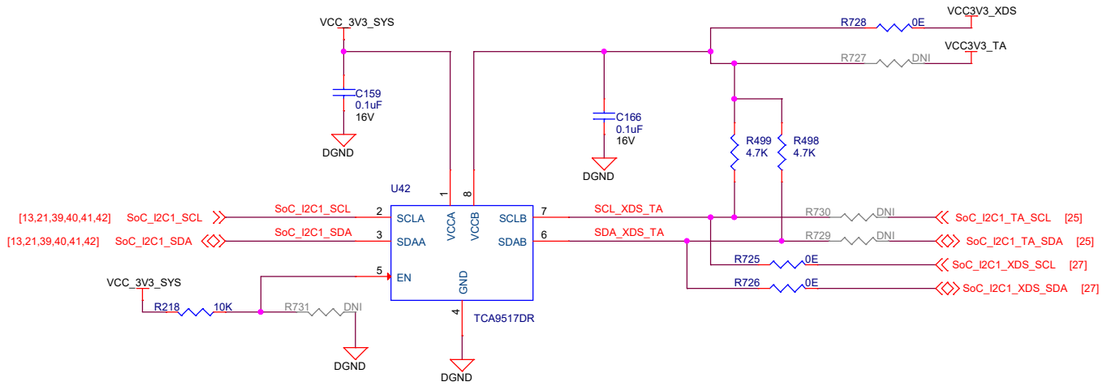
LED DRIVER



Designed for TI by Mistral Solutions Pvt Ltd

Title	ETHERNET PHY CLOCK BUFFER & LED DRIVER	
Size C	PROC162E1	Rev E1
Date: Friday, June 28, 2024	Sheet 24 of 44	

I2C BUS BUFFER

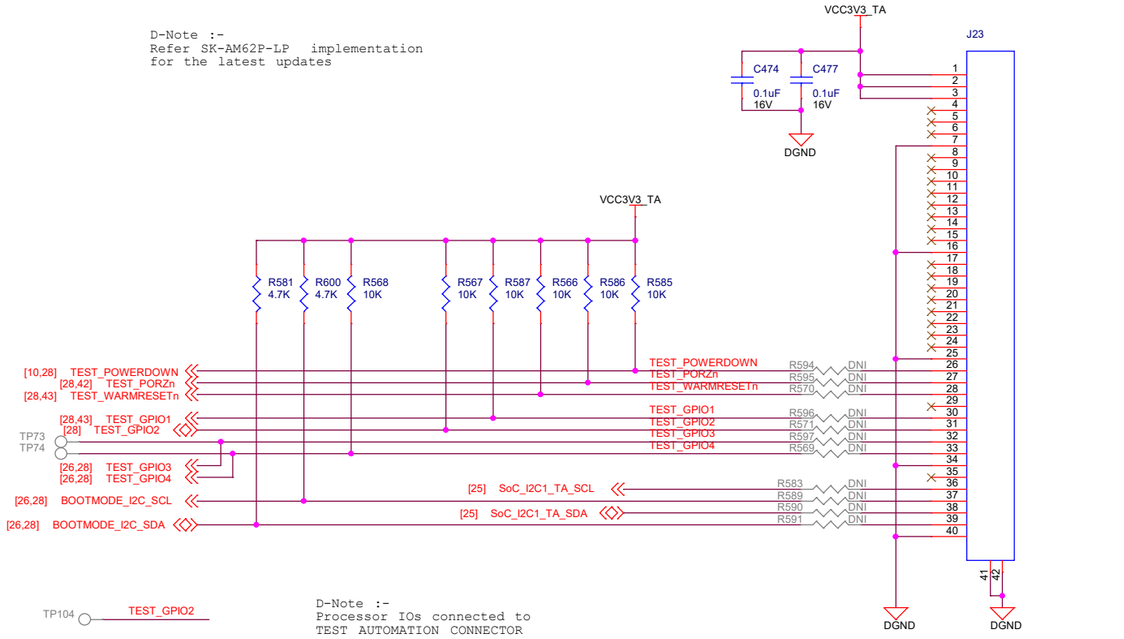


TA Configuration

Mount : R730, R729, R727
Demount : R725, R726, R728

40-PIN TEST AUTOMATION HEADER

D-Note :-
Refer SK-AM62P-LP implementation
for the latest updates



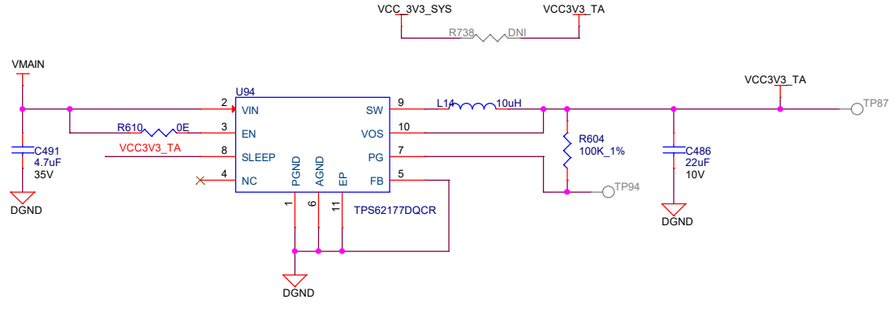
D-Note :-
Processor IOs connected to
TEST AUTOMATION CONNECTOR
are not fail-safe. No
external input shall be
applied when when Starter
Kit/EVM is not powered-up.

CON_FLEX_40X1_FH12A-40S-0.5SH

Silk: AUTOMATION HDR

TEST AUTOMATION BOARD POWER

VinMin = 4.75V
VinMax = 24V
Vout = 3.3V @ 0.5A



TEST AUTOMATION GPIO MAPPING

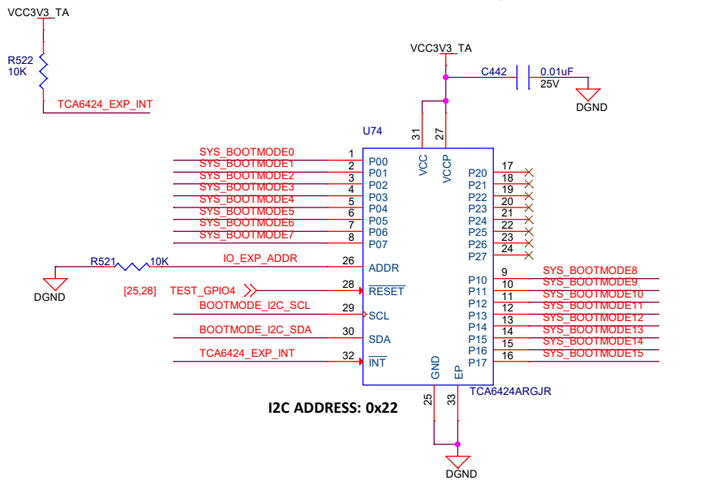
SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SoC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

Designed for TI by Mistral Solutions Pvt Ltd

Title	TEST AUTOMATION		
Size C	PROC162E1		Rev E1
Date:	Friday, June 28, 2024	Sheet 25 of 44	

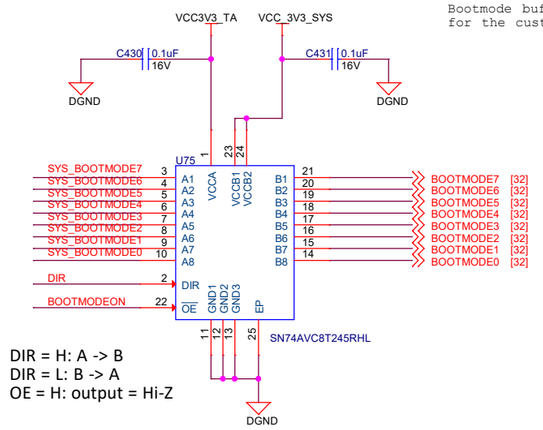
BOOTMODE IO EXPANDER

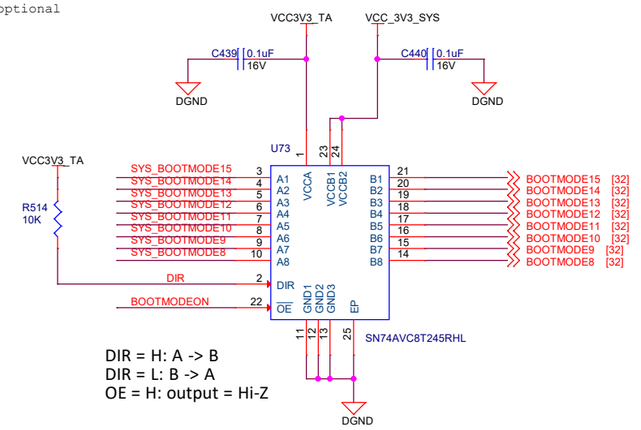
D-Note :-
Add additional decap
Verify and terminate unused IOs

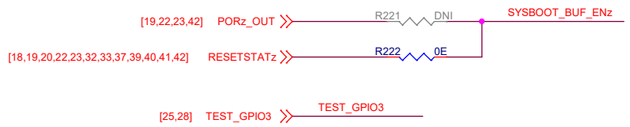


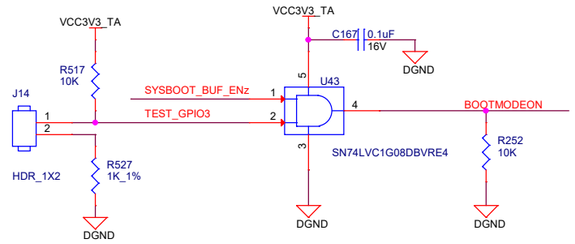
BOOT MODE BUFFERS

D-Note :-
Bootmode buffers are optional
for the custom board









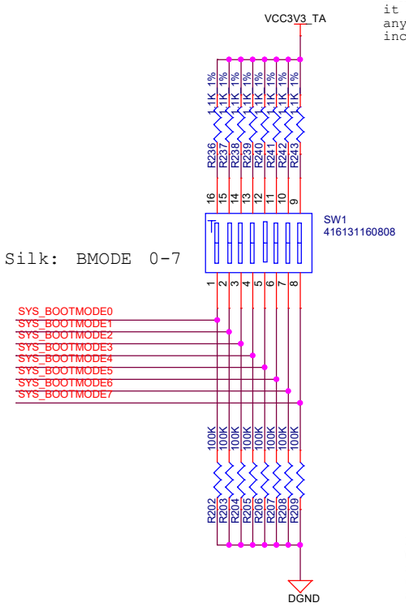
BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES

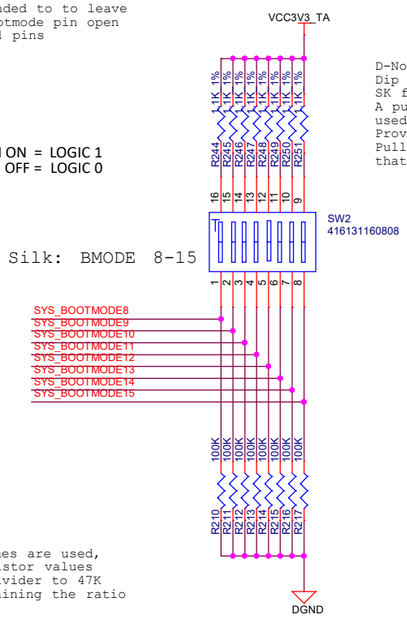
D-Note :-
VCC3V3_XDS_TA supply is used for
tes t automation. Connect
SoC_DVDD3V3 in the custom board
design when buffers are not used

D-Note :-
it is not recommended to leave
any of the the bootmode pin open
including reserved pins

SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

D-Note :-
Dip switch is optional and used on the
SK for ease of configuration
A pullup or pulldown resistor can be
used to set the BOOTMODE configuration
Provide provision for Pullup and
Pulldown resistors for the bootmode pins
that have configuration capability





D-Note :-
When DIP switches are used,
reduce the resistor values
used for the divider to 47K
and 470R maintaining the ratio

BOOT MODES SUPPORTED
1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. BACKUP BOOT OPTION

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOOT MODE BUFFER & SWITCHES	
Size C	PROC162E1	Rev E1
Date: Friday, June 28, 2024	Sheet 26 of 44	

XDS110 DEBUGGER

D-Note :-
Please follow SK-AM62P-LP EVM implementations
for latest updates on XDS110

Silk: JTAG

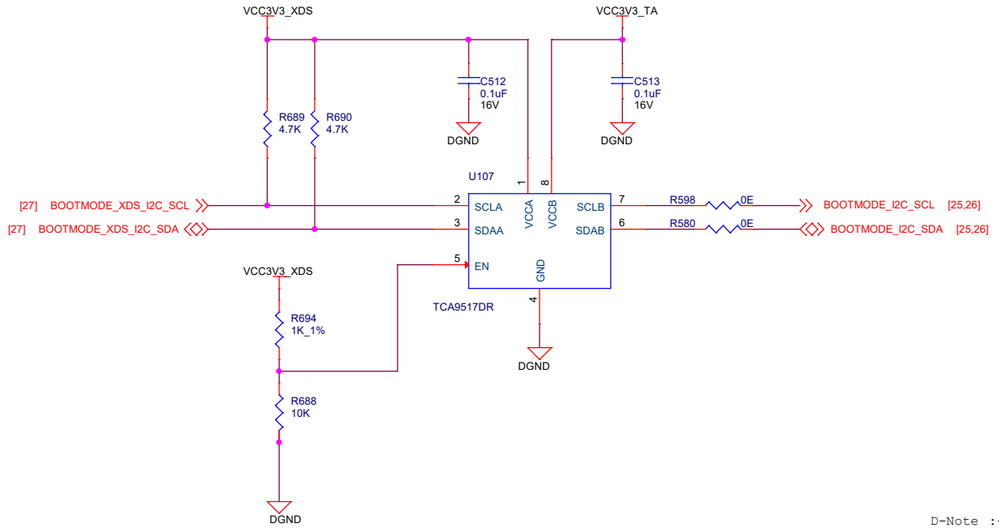
D-Note :-
Add a filter
cap (0.1uF)

Sets the unique ID of the Debugger

Designed for TI by Mistral Solutions Pvt Ltd

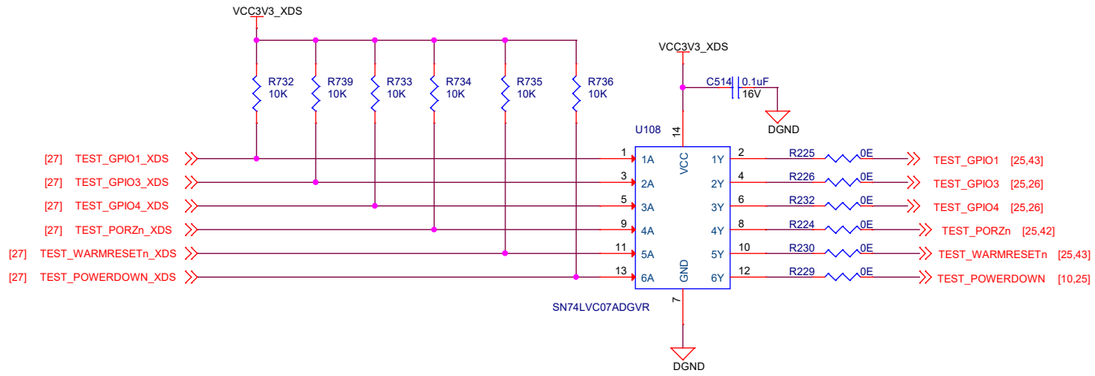
Title	XDS110 DEBUGGER	
Size: C	PROC162E1	Rev: E1
Date: Friday, June 28, 2024	Sheet 27 of 44	

BOOTMODE_I2C_TA BUFFER

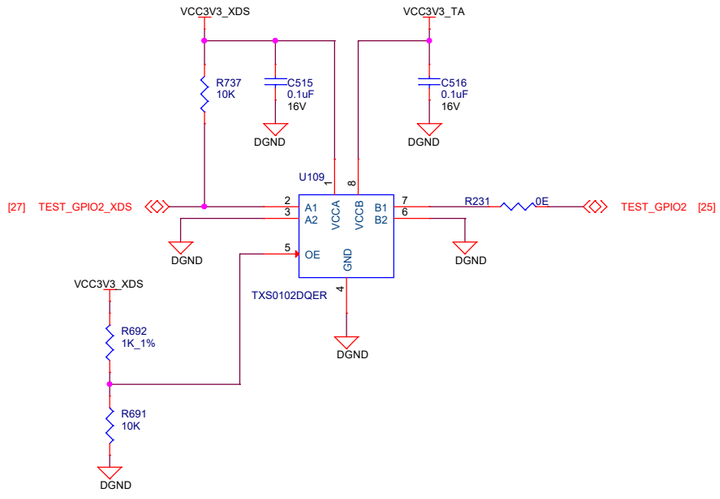


D-Note :-
Refer SK-AM62P-LP for the latest implementation

ISOLATION BUFFERS FOR TA SIGNALS



Pull ups(R567, R587, R517, R568, R585, R586 & R566) to VCC3V3_TA are present

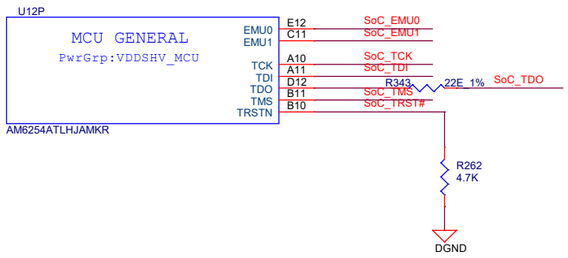


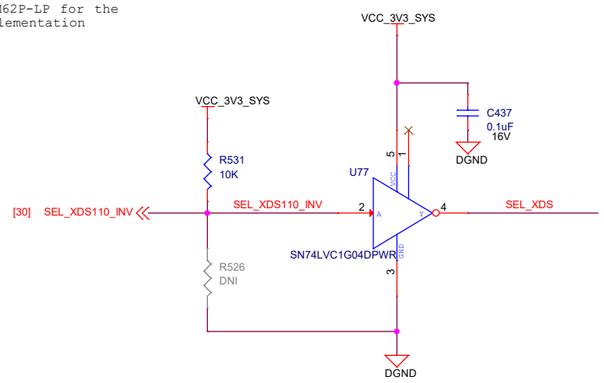
Designed for TI by Mistral Solutions Pvt Ltd

Title	AUTOMATION SIGNALS BUFFER		
Size C	PROC162E1		Rev E1
Date: Friday, June 28, 2024		Sheet 28 of 44	

D-Note :-
Refer SK-AM62P-LP for the latest implementation

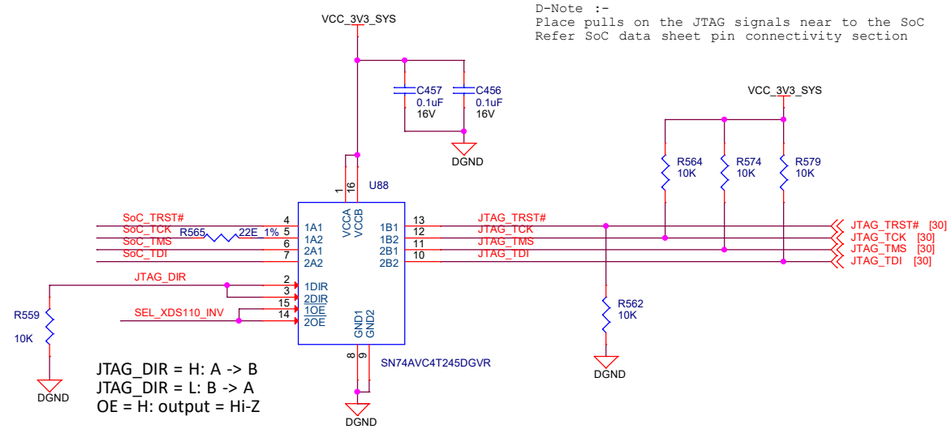
JTAG SOC SECTION



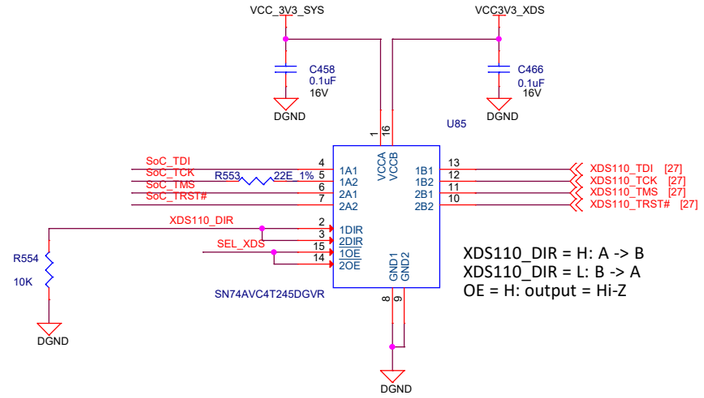


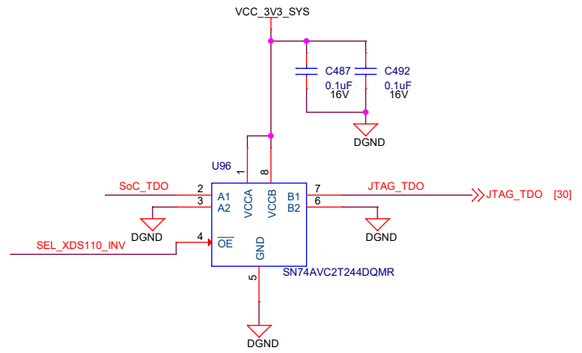
cTI20 JTAG BUFFERS

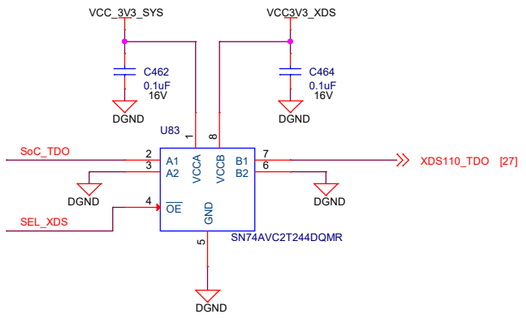
D-Note :-
Place pulls on the JTAG signals near to the SoC
Refer SoC data sheet pin connectivity section



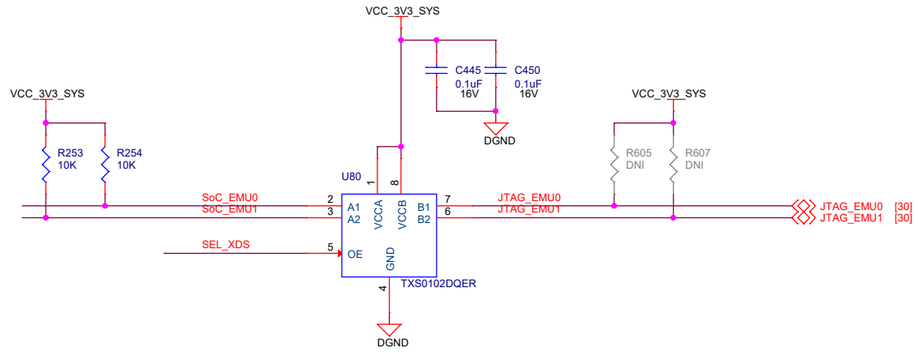
BUFFER XDS110

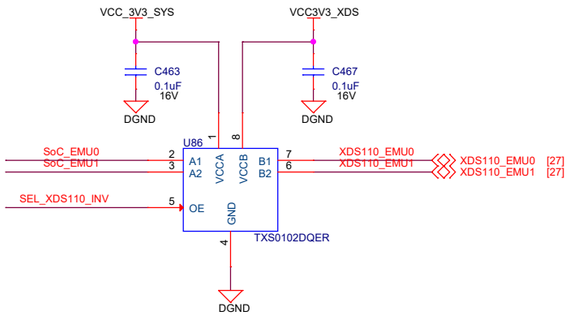






CAD NOTE: Buffers U88 and U96 need to be placed closer to the cTI-20pin connector J17 to reduce Stub length of the JTAG signals.



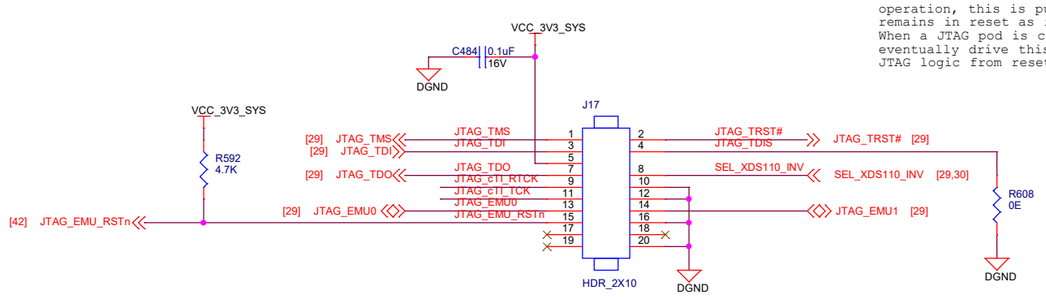


Designed for TI by Mistral Solutions Pvt Ltd

Title	JTAG BUFFER	
Size: C	PROC162E1	Rev: E1
Date: Friday, June 28, 2024	Sheet 29 of 44	

JTAG 20 PIN cTI CONNECTOR

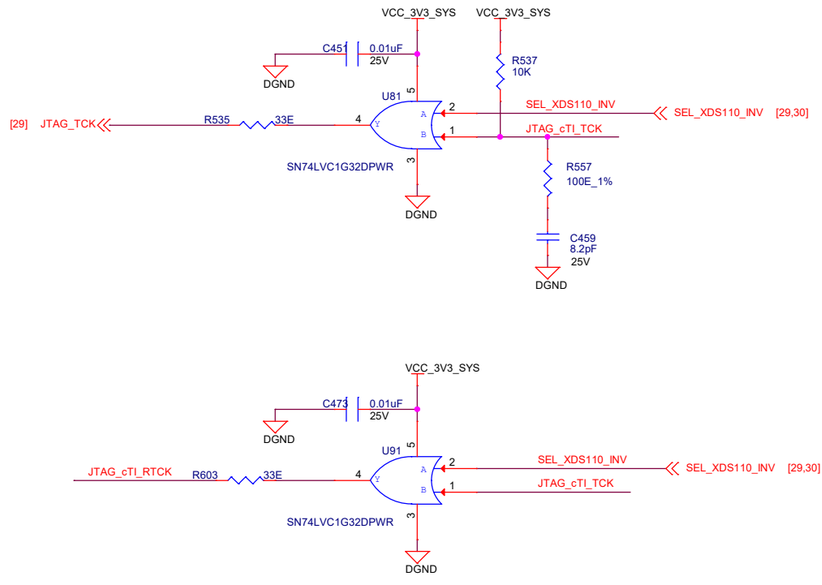
D-Note :-
TRSTn is the reset to the JTAG logic. For normal operation, this is pulled low, and thus the JTAG remains in reset as it is not being used.
When a JTAG pod is connected, the pod will eventually drive this signal high to release the JTAG logic from reset and enable a JTAG connection.



Silk: cTI

D-Note :-
Add an external ESD protection to provide system level ESD protection when external connector is used for debug. Add Test points and ESD protection when JATG connector is not used

JTAG CLOCK BUFFER



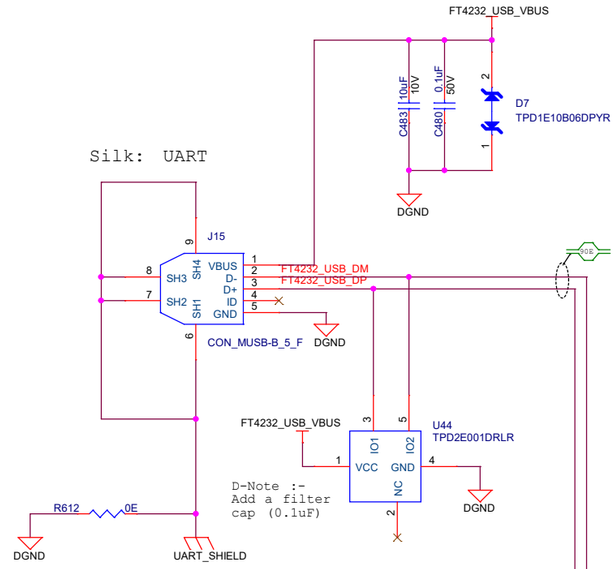
Designed for TI by Mistral Solutions Pvt Ltd

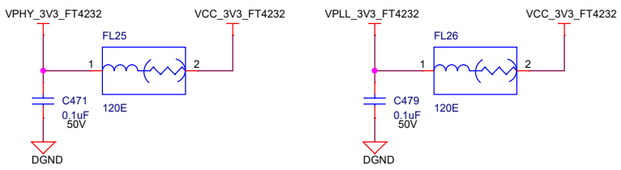
Title	JTAG 20 PIN cTI CONNECTOR	
Size C	PROC162E1	Rev E1
Date: Friday, June 28, 2024	Sheet 30 of 44	

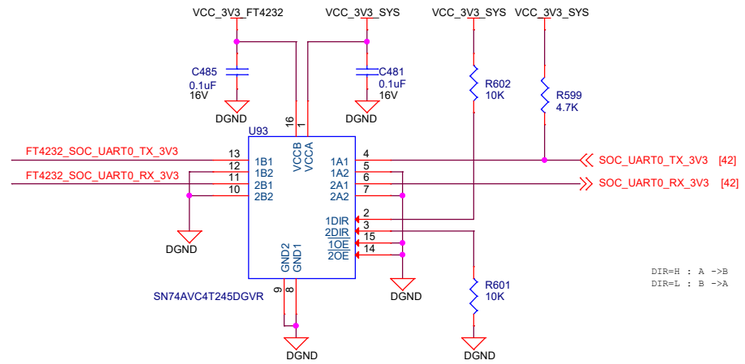
FT4232 UART

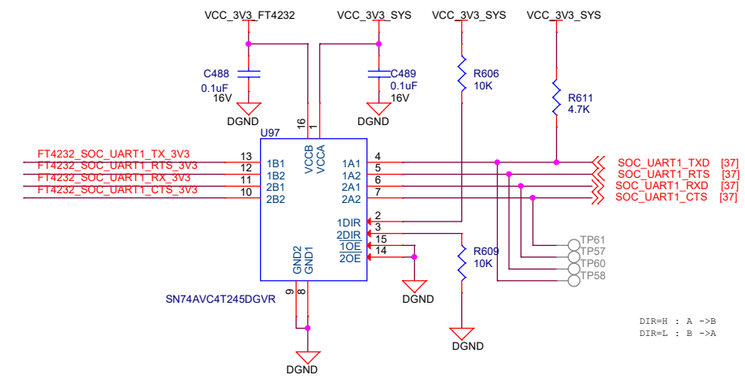
D-Note :-
Follow SK-AM62P-LP for latest FT4232 implementations

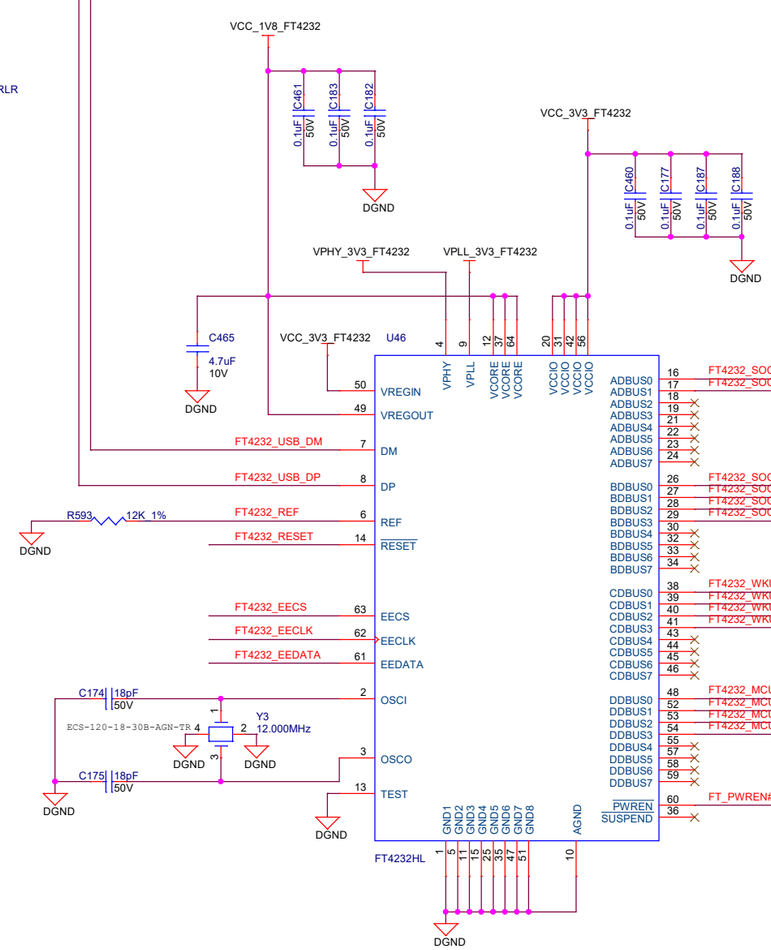
Silk: UART

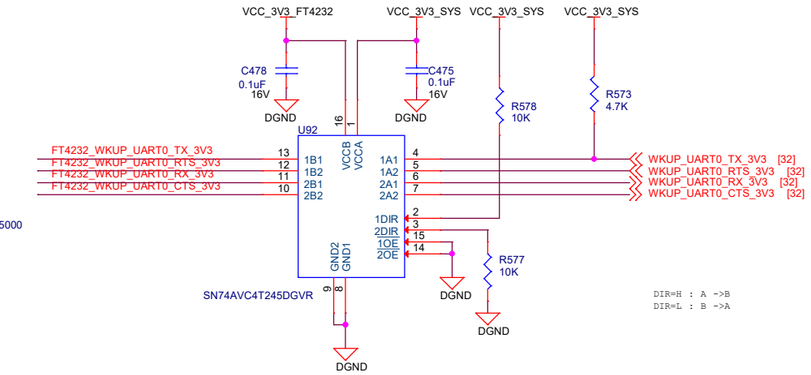


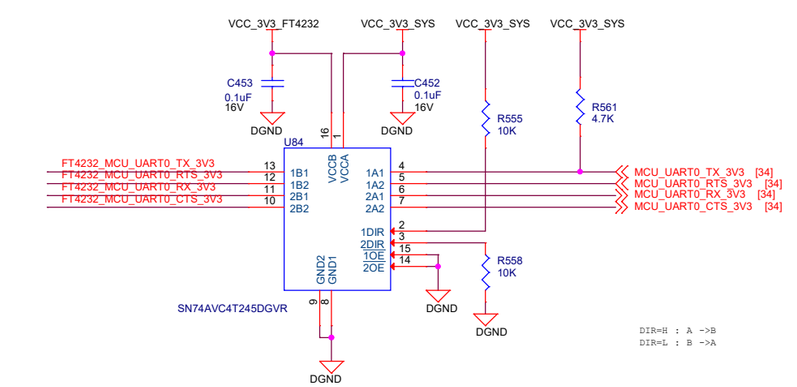




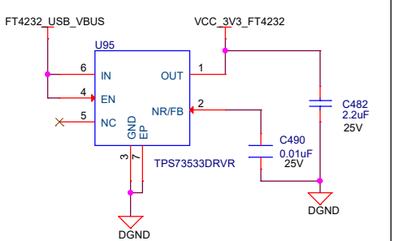




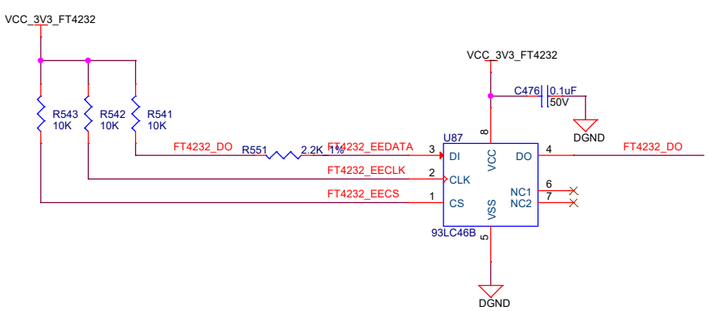




FT4232: 5V to 3.3V@500mA LDO



EEPROM



R-Note :-
Verify the implementation with the device manufacturer

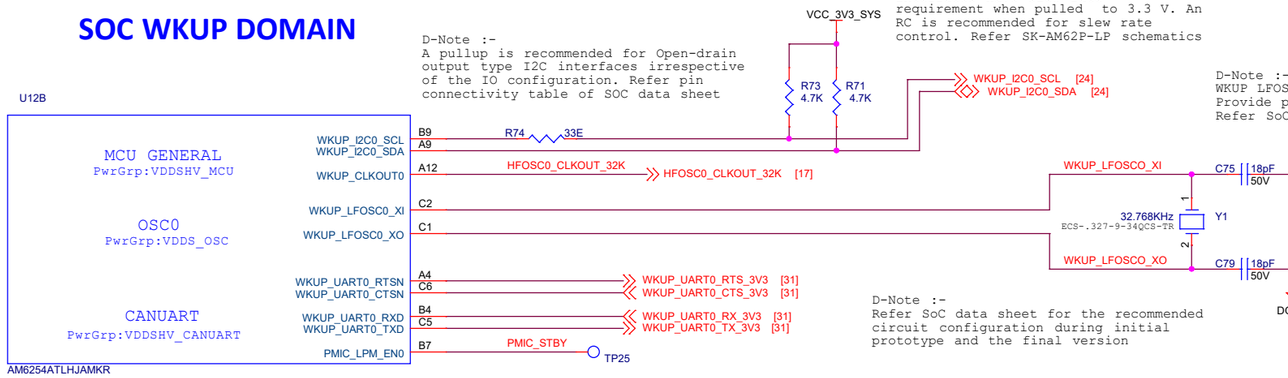
Designed for TI by Mistral Solutions Pvt Ltd

Title	FT4232 UART TO USB BRIDGE		
Size	PROC162E1		Rev
C			E1
Date:	Friday, June 28, 2024	Sheet 31 of 44	

SOC WKUP DOMAIN

D-Note :-
A pullup is recommended for Open-drain output type I2C interfaces irrespective of the IO configuration. Refer pin connectivity table of SOC data sheet

D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V. An RC is recommended for slew rate control. Refer SK-AM62P-LP schematics



D-Note :-
WKUP LFOSC0 has limited use case
Provide provision to ground Xi when not used
Refer SoC datasheet

D-Note :-
The only LFOSC0 register bits that should be changed by the customer are BP_C, PD_C, and CTRLMMR_WKUP_LFXOSC_TRIM[18:16], where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source.The CTRLMMR_WKUP_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the Load Capacitance Equation. The load capacitance range of the crystal will be half of the recommended capacitor value range. since there are connected in series with the crystals resonate circuit.

D-Note :-
Refer SoC data sheet for the recommended circuit configuration during initial prototype and the final version

D-Note :-
WKUP_CLKOUT0 is a buffered output of the high frequency oscillator (HFOSC0) available during power-up as default.

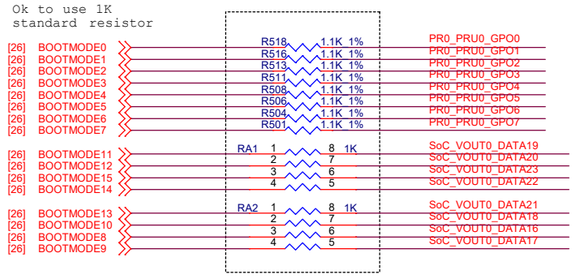
SOC GPMC INTERFACE

D-Note :-
Add a series resistor 0R when used as GPMC0_CLk

D-Note :-
Reduce the series resistor value when buffer is not used to 0R
These resistors are used to isolate the alternate function during testing

BOOTMODE PINS

D-Note :-
Ok to use 1K standard resistor

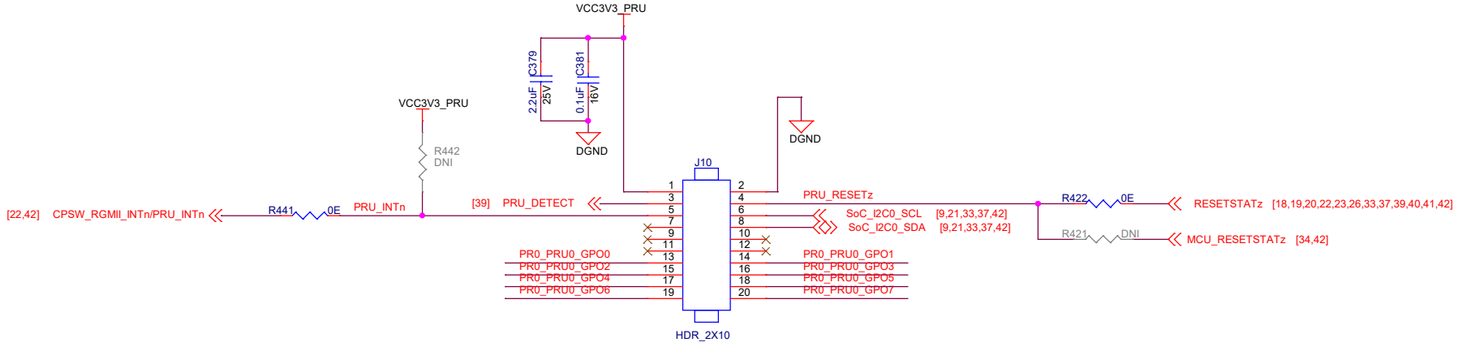


R-Note :-
Resistors are used to isolate the BOOTMODE control logic after the value is latched

D-Note :-
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot. Shorting the bootmode pins directly to VCC or ground directly is not recommended. Connect each of the bootmode pins through separate resistor. Choose the bootmode resistor value based on the use case (10K or similar)

D-Note :-
SOC IO buffers used for GPMC interface signals are disabled during reset. The required pulls for the interfaced signals are provided on the GPMC interface card

PRU HEADER

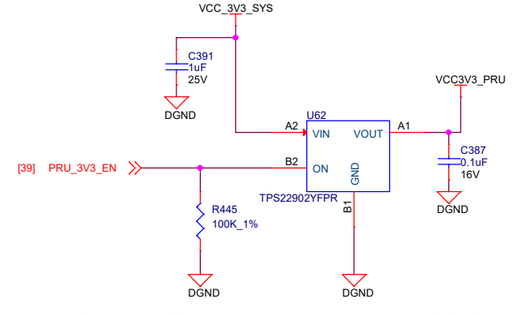


Silk: PRU HDR

D-Note :-
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull

D-Note :-
Processor IOs connected to PRU Header are not fail-safe.
No external input shall be driven when when Starter Kit is not powered-up.

LOAD SWITCH FOR PRU HEADER

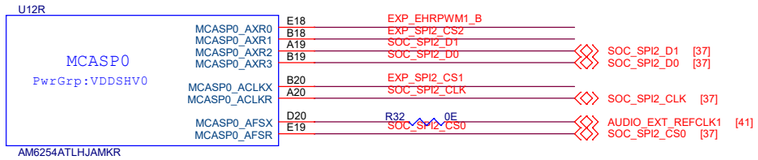


3V3 supply of PRU Header is limited to sourcing 500mA max.

Designed for TI by Mistral Solutions Pvt Ltd

Title	PRU HEADER		
Size	C	PROC162E1	Rev E1
Date:	Friday, June 28, 2024	Sheet 32 of 44	

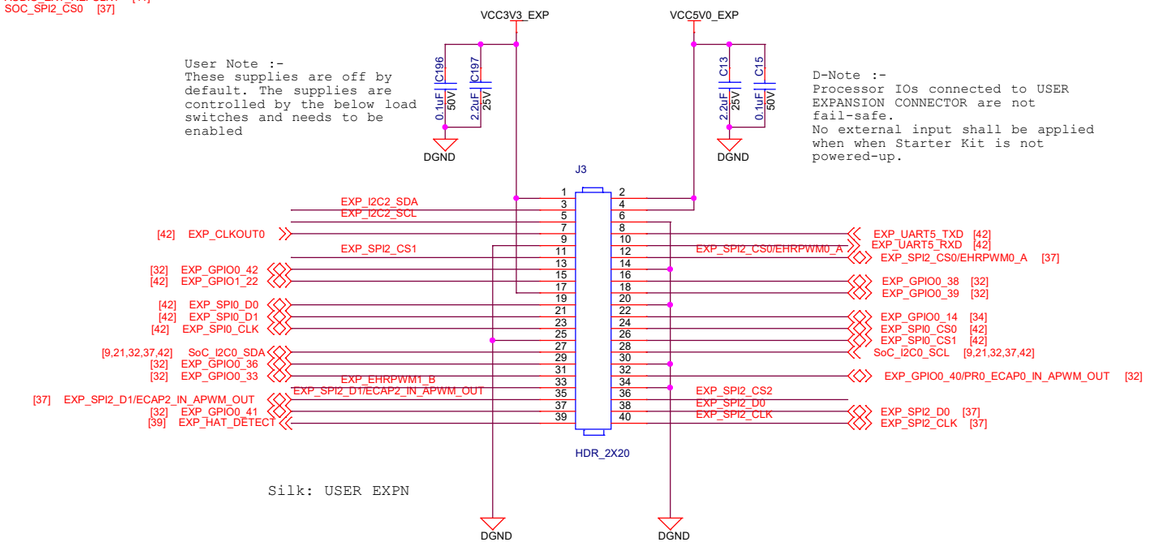
USER EXPANSION CONNECTOR



R32(Series damping resistor) should be placed close to SoC

D-Note :-
Add a series resistor 22R
on the SPI clock output
signal near to the SoC

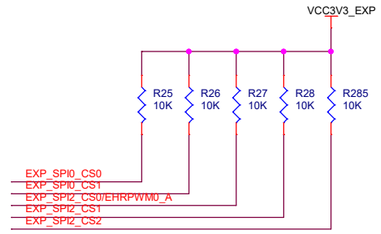
User Note :-
These supplies are off by
default. The supplies are
controlled by the below load
switches and needs to be
enabled



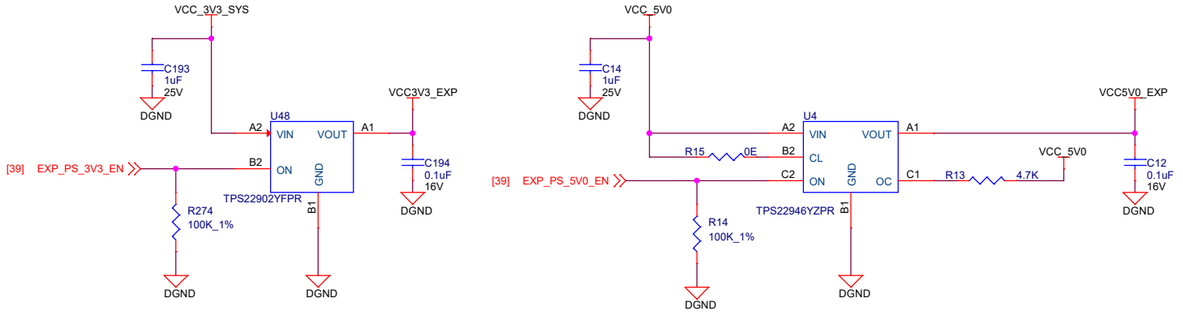
Silk: USER EXPN

D-Note :-
Processor IOs connected to USER
EXPANSION CONNECTOR are not
fail-safe.
No external input shall be applied
when when Starter Kit is not
powered-up.

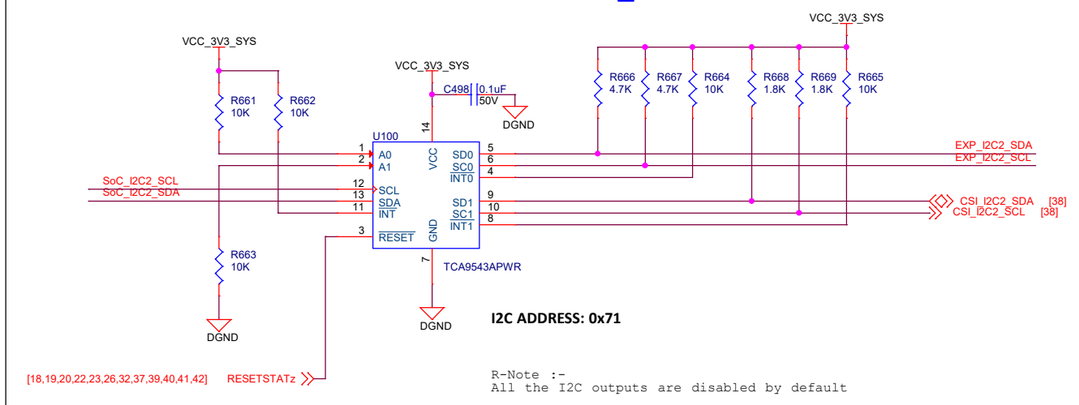
Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



LOAD SWITCHES FOR USER EXPANSION CONNECTOR



I2C SWITCH FOR SoC_I2C2



R-Note :-

AM62x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

Designed for TI by Mistral Solutions Pvt Ltd

Title	USER EXPANSION CONNECTOR		
Size C	PROC162E1		Rev E1
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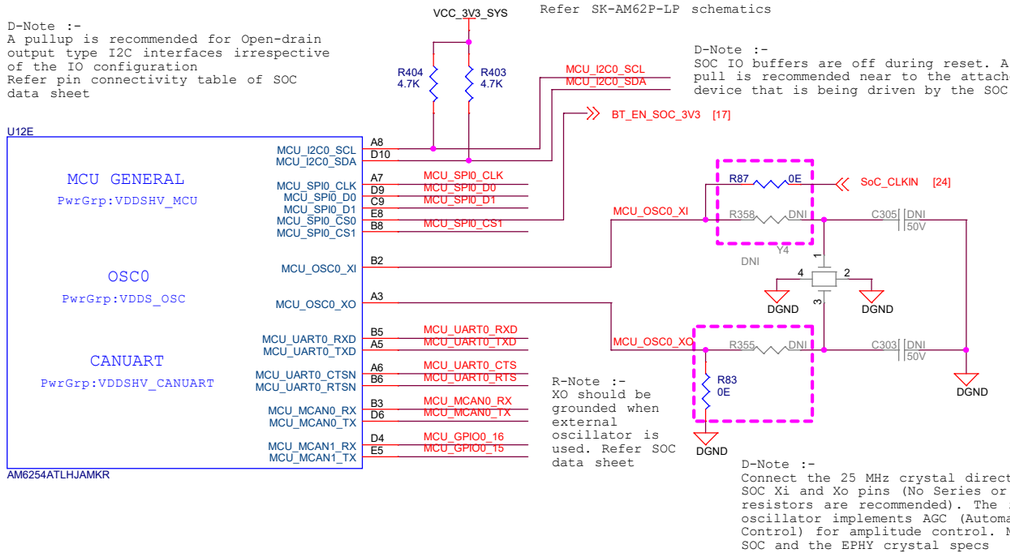
SOC - MCU DOMAIN

D-Note :-
A pullup is recommended for Open-drain output type I2C interfaces irrespective of the IO configuration
Refer pin connectivity table of SOC data sheet

D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V
An RC is recommended for slew rate control
Refer SK-AM62P-LP schematics

D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

D-Note :-
Add a series resistor 22R to the SPI0 clock output near to the SoC



R-Note :-
XO should be grounded when external oscillator is used. Refer SOC data sheet

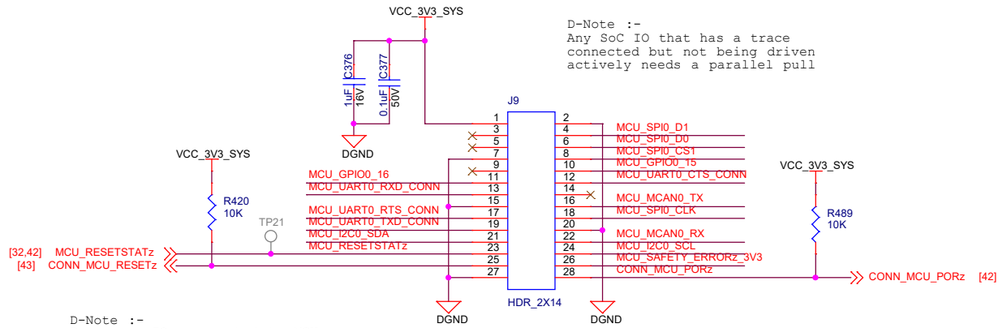
D-Note :-
Connect the 25 MHz crystal directly to the SOC Xi and Xo pins (No Series or parallel resistors are recommended). The internal oscillator implements AGC (Automatic Gain Control) for amplitude control. Match the SOC and the EPHY crystal specs

D-Note :-
No HFOSC0 registers are required to be changed. These registers should remain in their default state. Select the appropriate crystal circuit components that are compliant to the values defined in the MCU_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

D-Note :-
Refer Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:
Clock Routing Guidelines
Oscillator Routing

D-Note :-
MCU_OSC0 has been validated only with a 25 MHz clock source, so that is the only frequency supported. The datasheet shows MCU_OSC0 not starting until after the core voltage because there are some cases where the oscillator may not start until VDD_CORE is valid. In most cases it will start as early as VDDS_OSC0, but this may not always be the case. This diagram in the datasheet is showing the maximum start-up time, which must include the case where the delay is based on VDD_CORE being valid.

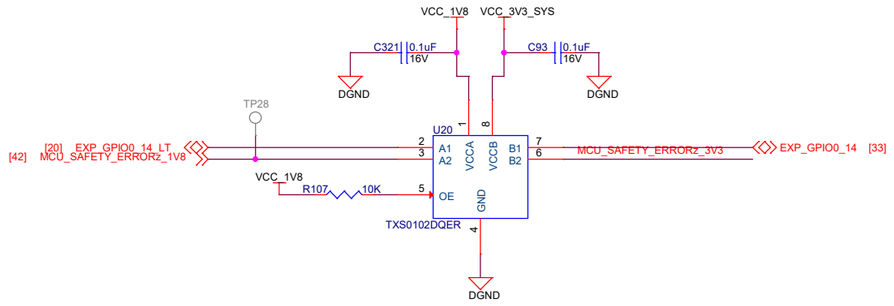
SOC-MCU HEADER



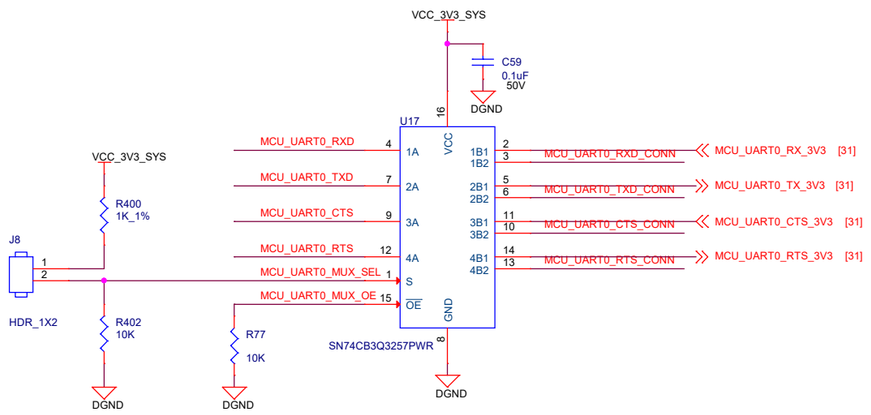
D-Note :-
Any SoC IO that has a trace connected but not being driven actively needs a parallel pull

D-Note :-
Processor IOs connected to MCU expansion CONNECTOR are not fail-safe. No external input shall be applied when when Starter Kit/EVM is not powered-up.

Silk: MCU HDR



SOC - MCU_UART0 MUX

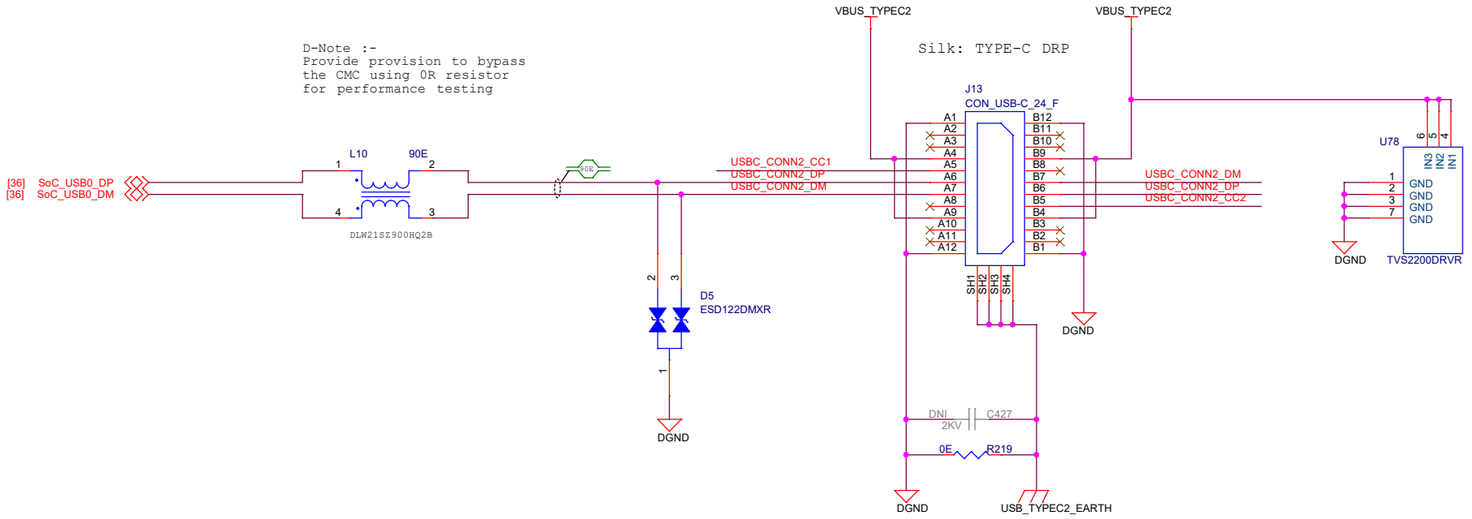


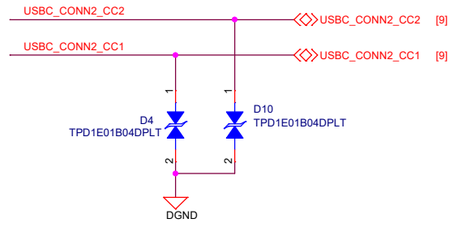
OEn	SEL	INPUT/OUTPUT An	
L	L(DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

Designed for TI by Mistral Solutions Pvt Ltd

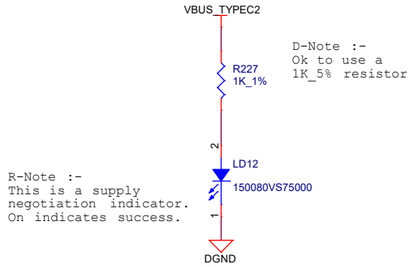
Title	MCU HEADER	
Size C	PROC162E1	Rev E1
Date: Friday, June 28, 2024	Sheet 34 of 44	

USB0 TYPE-C DRP

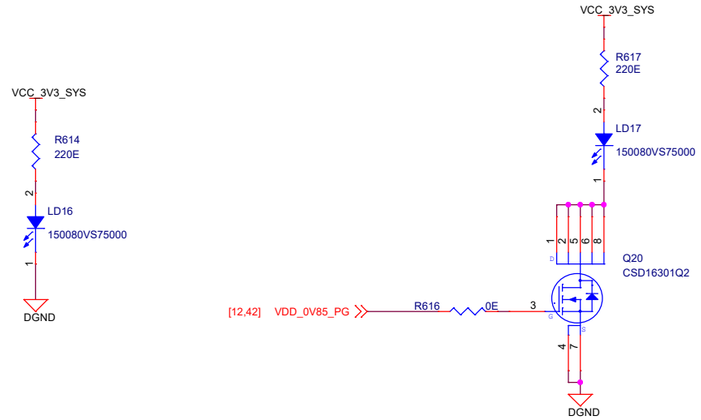




POWER INDICATION LED: VBUS_TYPEC2



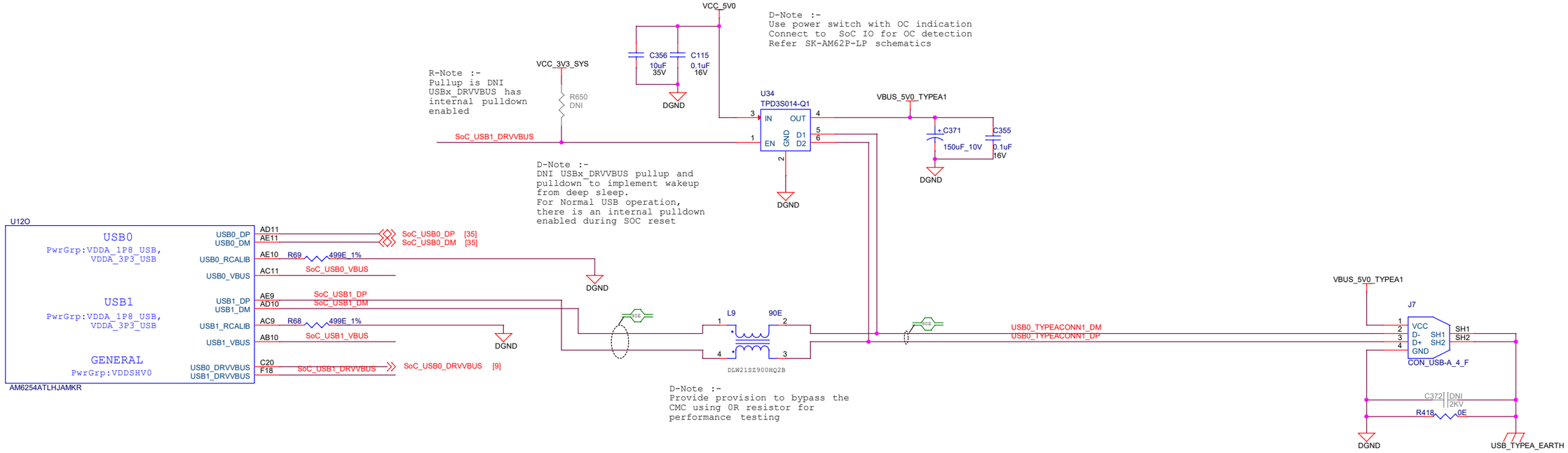
POWER RAIL LEDS



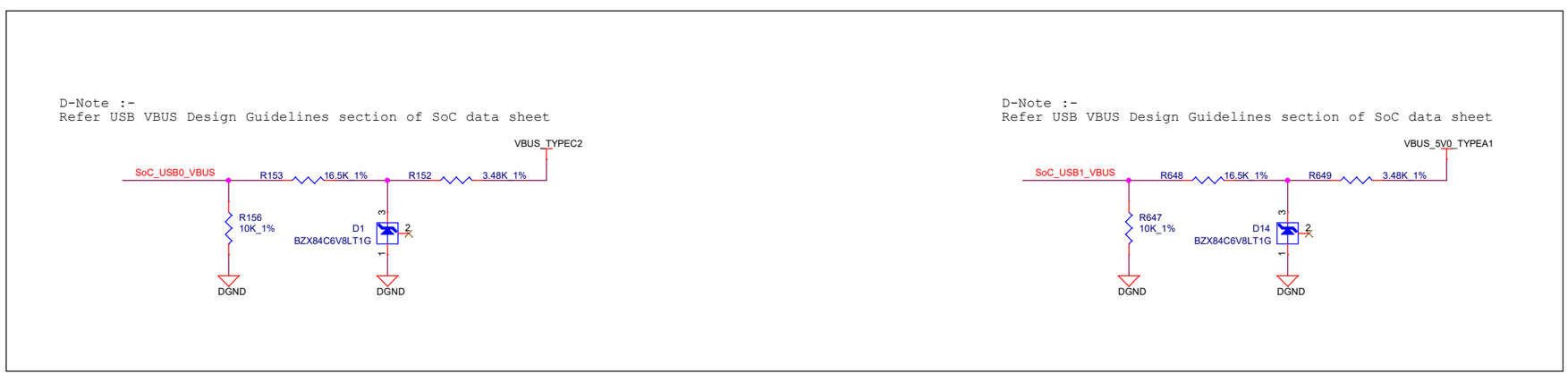
Designed for TI by Mistral Solutions Pvt Ltd

Title	USB0 TYPE-C DRP		
Size C	PROC162E1		Rev E1
Date:	Friday, June 28, 2024	Sheet 35 of 44	

USB1 TYPE-A



D-Note :-
VBUS connection is optional for Host configuration



Designed for TI by Mistral Solutions Pvt Ltd

Title	USB1 TYPE-A		
Size C	PROC162E1		Rev E1
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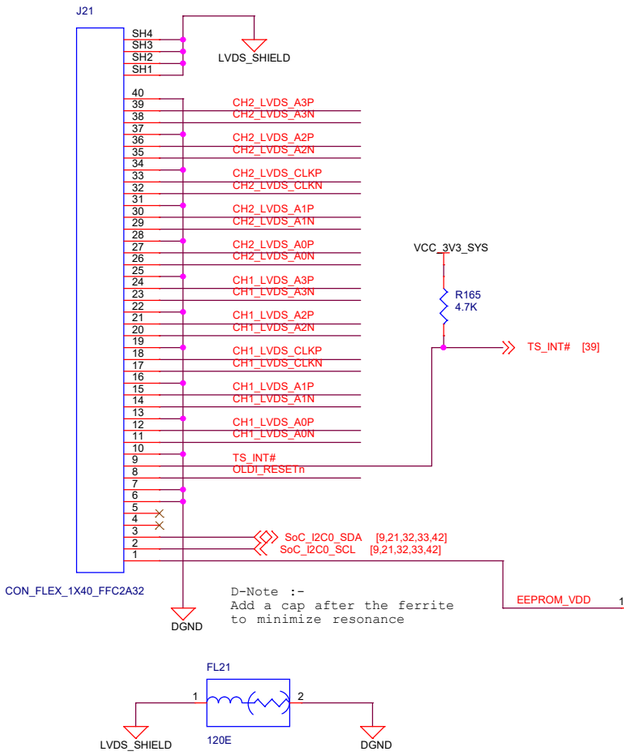
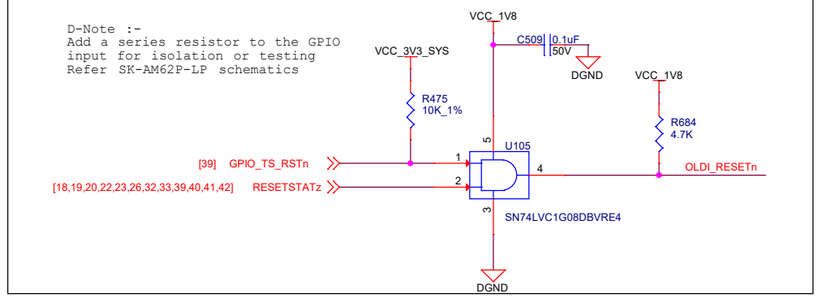
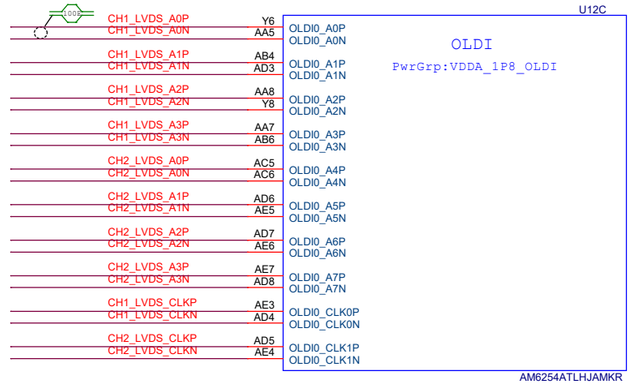
OLDI DISPLAY INTERFACE

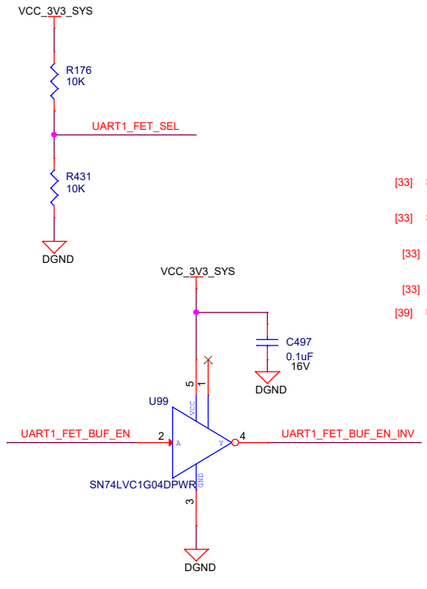


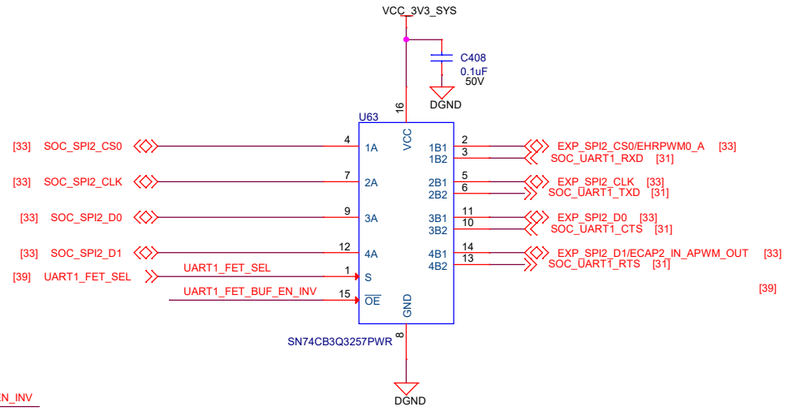
OLDI RESET

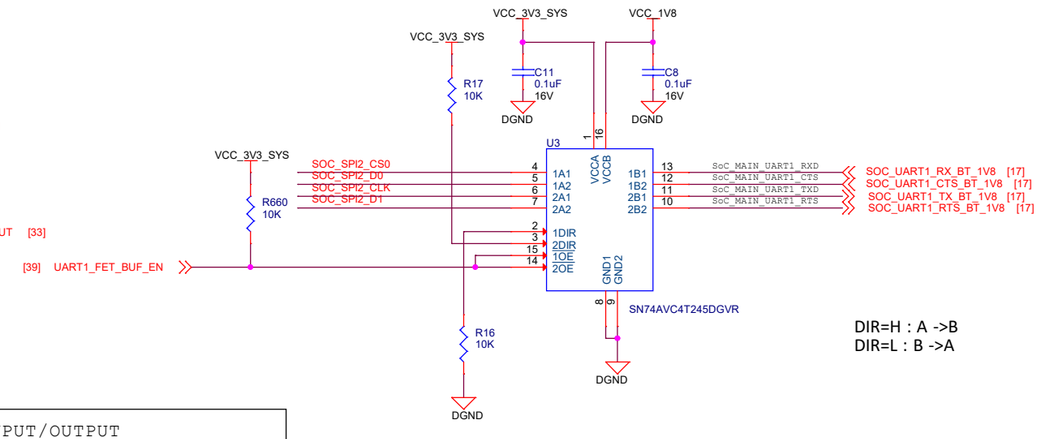




SoC UART1 FET SWITCH & BUFFER







OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	FT4232
L	L	An=nB1	USER EXPANSION CONNECTOR

Designed for TI by Mistral Solutions Pvt Ltd

Title	OLDI DISPLAY INTERFACE	
Size	PROC162E1	Rev
C		E1
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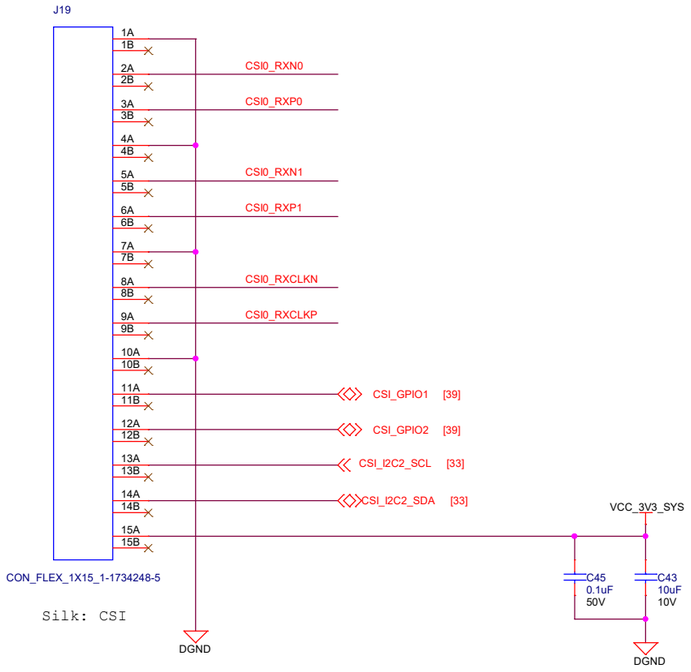
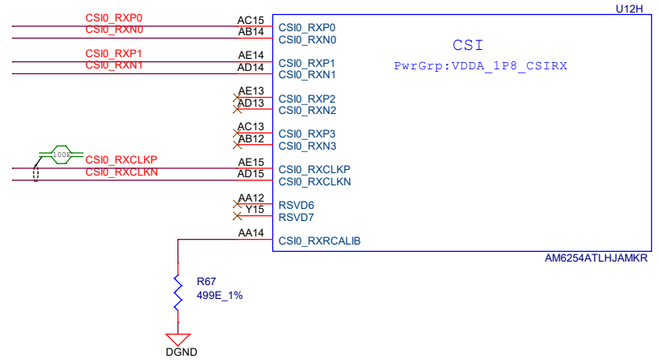
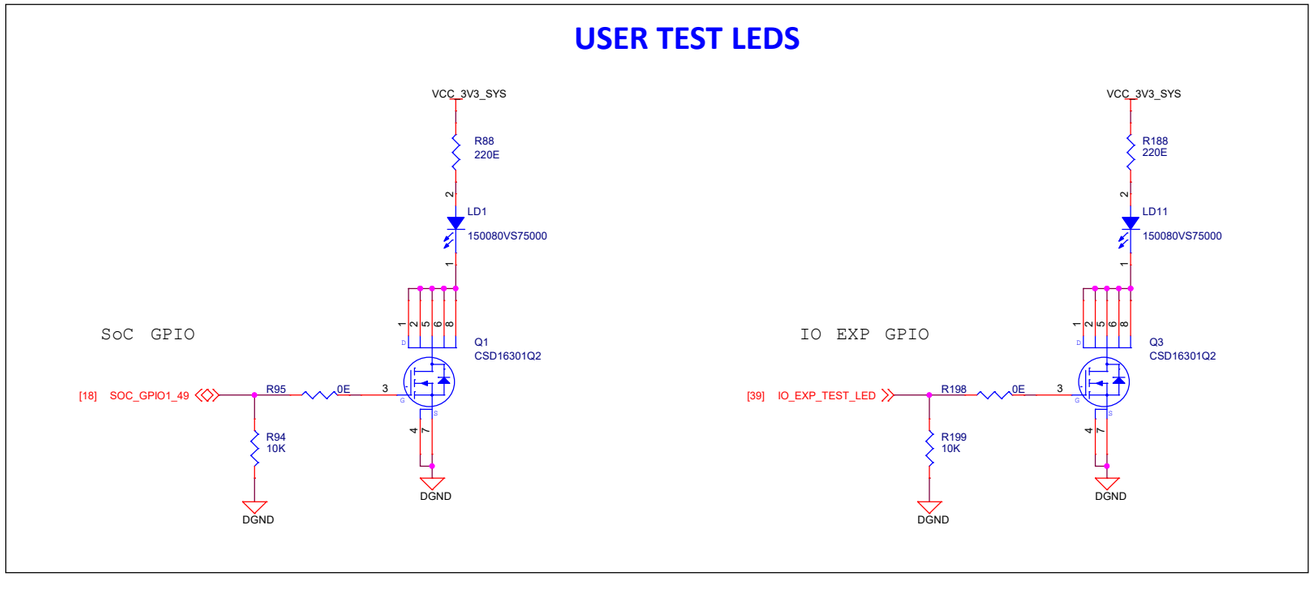
CSI INTERFACE

CSI CAMERA HEADER





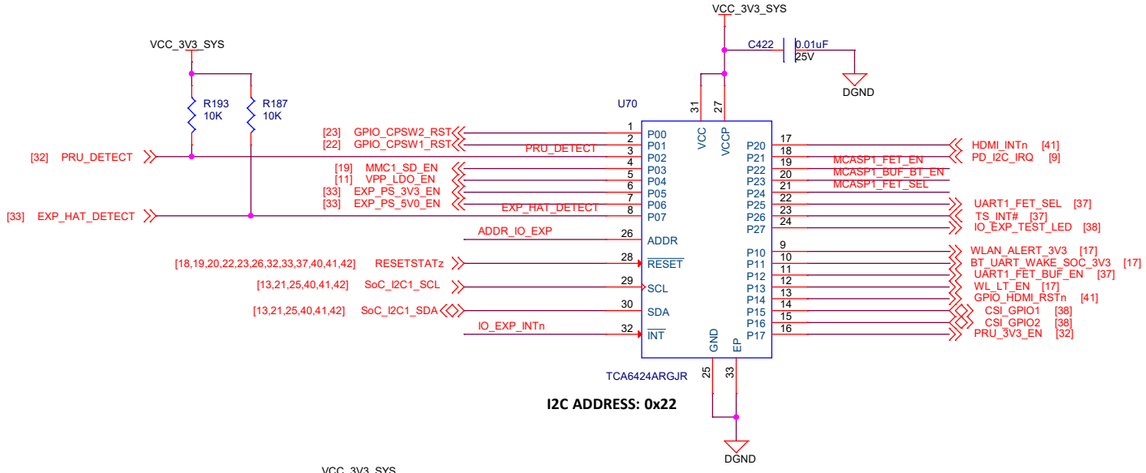
USER TEST LEDS

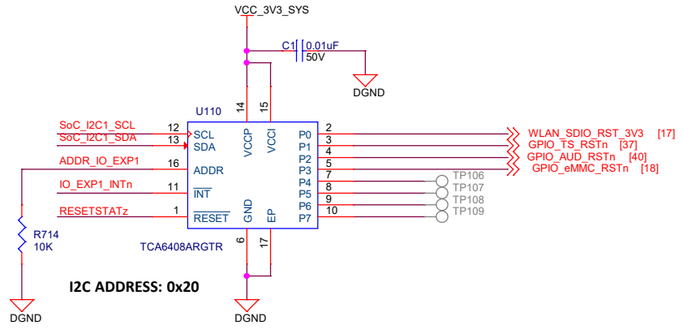


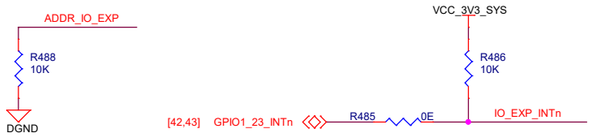
Designed for TI by Mistral Solutions Pvt Ltd

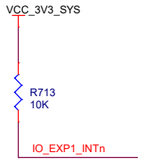
Title	CSI INTERFACE & USER TEST LEDS	
Size C	PROC162E1	Rev E1
Date: Friday, June 28, 2024	Sheet 38 of 44	

IO EXPANDER

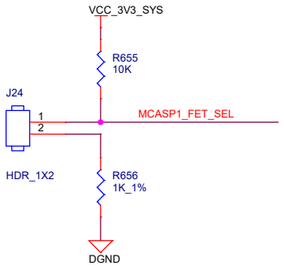


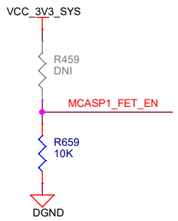


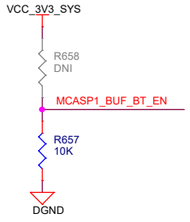


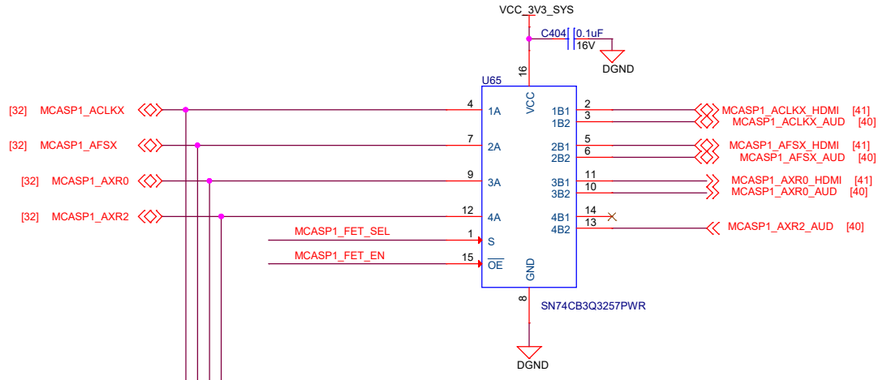


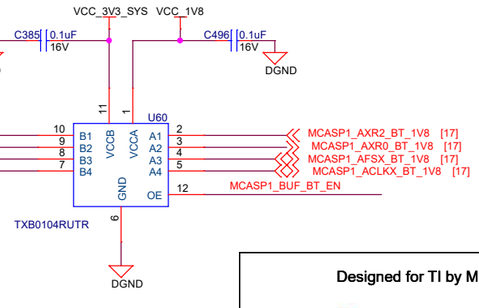
MCASP1 FET SWITCH & BUFFER









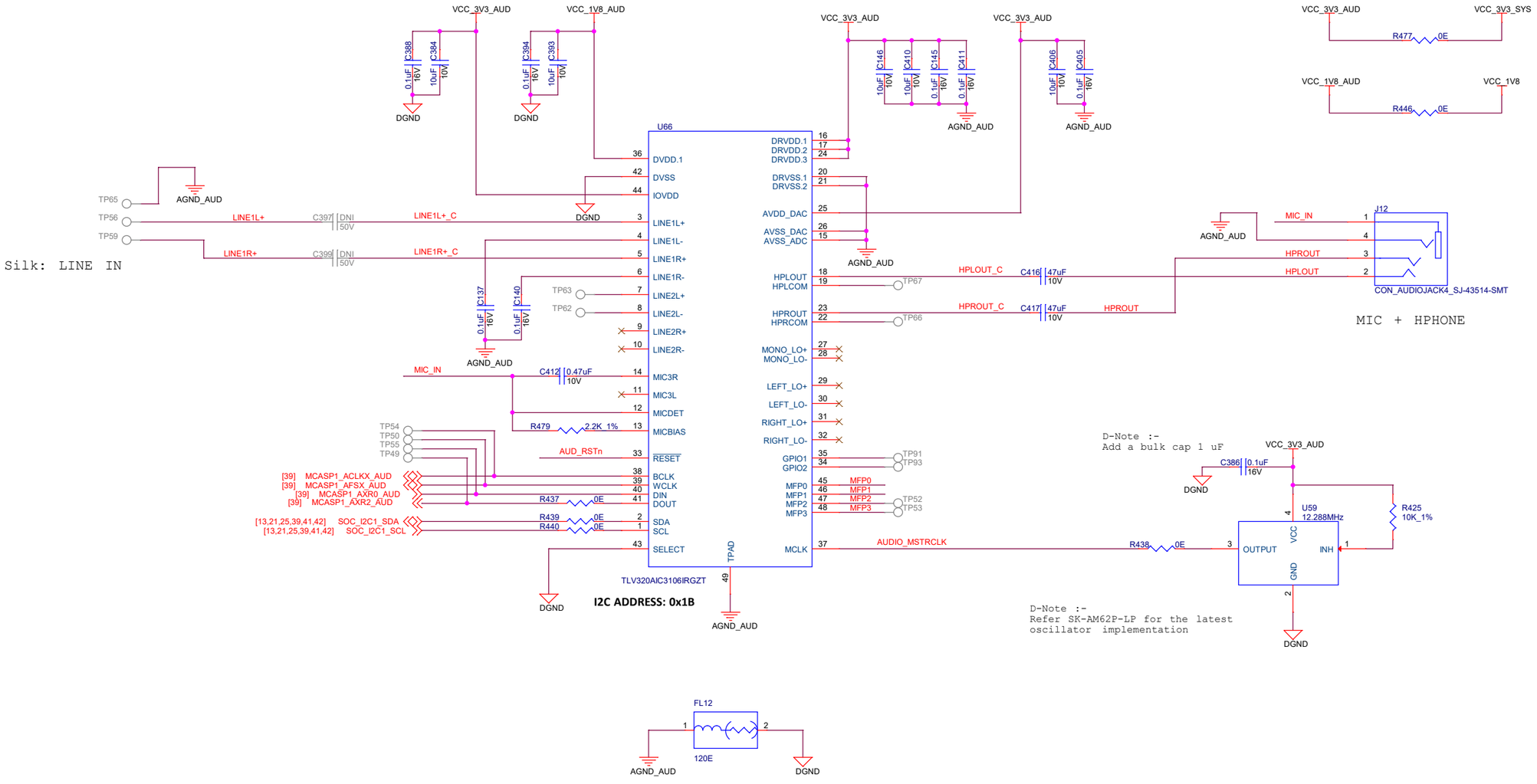


OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

Designed for TI by Mistral Solutions Pvt Ltd

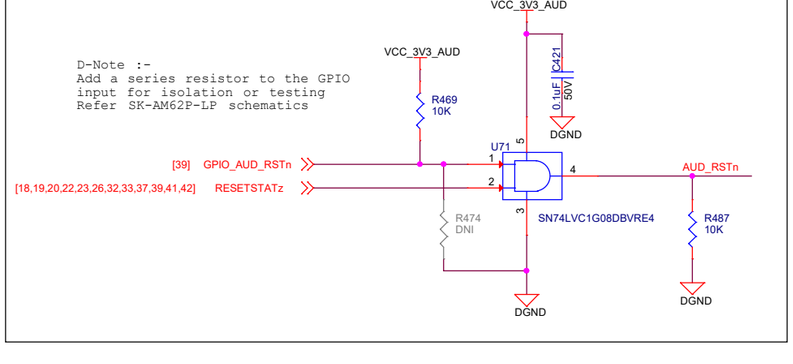
Title	IO EXPANDER		
Size	PROC162E1		Rev
C			E1
Date:	Friday, June 28, 2024	Sheet 39 of 44	

AUDIO CODEC



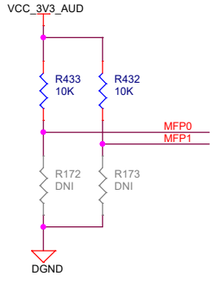
Silk: LINE IN

AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



Designed for TI by Mistral Solutions Pvt Ltd

Title	AUDIO CODEC		
Size	PROC162E1		Rev
C			E1
Date:	Friday, June 28, 2024	Sheet 40 of 44	

HDMI INTERFACE

U12J
VOUT0
PwrGrp:VDDSHV3
AM6254ATLHJAMKR

VOUT0_DATA0	U22	SoC_VOUT0_DATA0
VOUT0_DATA1	V24	SoC_VOUT0_DATA1
VOUT0_DATA2	W25	SoC_VOUT0_DATA2
VOUT0_DATA3	W24	SoC_VOUT0_DATA3
VOUT0_DATA4	Y25	SoC_VOUT0_DATA4
VOUT0_DATA5	Y24	SoC_VOUT0_DATA5
VOUT0_DATA6	Y23	SoC_VOUT0_DATA6
VOUT0_DATA7	AA25	SoC_VOUT0_DATA7
VOUT0_DATA8	V21	SoC_VOUT0_DATA8
VOUT0_DATA9	W21	SoC_VOUT0_DATA9
VOUT0_DATA10	V20	SoC_VOUT0_DATA10
VOUT0_DATA11	AA23	SoC_VOUT0_DATA11
VOUT0_DATA12	AB25	SoC_VOUT0_DATA12
VOUT0_DATA13	AA24	SoC_VOUT0_DATA13
VOUT0_DATA14	Y22	SoC_VOUT0_DATA14
VOUT0_DATA15	AA21	SoC_VOUT0_DATA15
VOUT0_PCLK	AC24	SoC_VOUT0_PCLK
VOUT0_DE	Y20	SoC_VOUT0_DE
VOUT0_VSYNC	AC25	SoC_VOUT0_VSYNC
VOUT0_HSYNC	AB24	SoC_VOUT0_HSYNC

SoC_VOUT0_PCLK — R60 0E — HDMI_PCLK

VDD_1V2 — FB3 300E — VHDMI_AVCC_1V2
C232 22uF 10V — DGND
C230 10uF 10V, C231 0.1uF 16V, C229 0.1uF 16V — DGND

VHDMI_CVCC_1V2 — FB2 300E — VDD_1V2
C213, C209, C200, C207, C225, C217: 0.1uF 16V — DGND
C201 10uF 10V — DGND

VHDMI_IOVCC_3V3 — FB1 300E — VCC_3V3_SYS
C223 0.1uF 16V, C212 0.1uF 16V, C199 10uF 10V — DGND
C204 10uF 10V — DGND

D-Note :-
Add an additional decap

D-Note :-
Add bulk caps

VHDMI_IOVCC_3V3
R61 4.7K
R316 DNI, R323 DNI, R325 10K

U10

[13,21,25,39,40,42] SoC_I2C1_SCL	1	CSCL	
[13,21,25,39,40,42] SoC_I2C1_SDA	2	CSDA	
	72	CI2CA	
HDMI_RSTn	51	RESET#	
HDMI_PCLK	22	IDCK	
	60, 66	AVCC12_1, AVCC12_2	
	5	CVCC12_1	
	12	CVCC12_2	
	26	CVCC12_3	
	42	CVCC12_4	
	47	CVCC12_5	
	53	CVCC12_6	
	3, 21, 46	IOVCC1, IOVCC2, IOVCC3	
	48	DSDA	HDMI_I2C_SDA
	49	DSCL	HDMI_I2C_SCL
	52	INT	HDMI_INTn [39]
	54	HPD	HDMI_HPD
	56	EXT_SWING	HDMI_EXTSWING
	59, 58	TXC+, TXC-	HDMI_CLK+, HDMI_CLK-
	62, 61	TX0+, TX0-	HDMI_TX0+, HDMI_TX0-
	65, 64	TX1+, TX1-	HDMI_TX1+, HDMI_TX1-
	68, 67	TX2+, TX2-	HDMI_TX2+, HDMI_TX2-
	71	CEC_A	HDMI_CEC
	50	CEC_D	HDMI_CEC_D — TP18
	55	RSVDL	
	69	IO_SEL	R62 0E — DGND
	70	VDDQ	
	41	SD0	MCASP1_AXR0_HDMI [39]
	40	SD1	HDMI_AUDD1 — TP16
	39	SD2	HDMI_AUDD2 — TP14
	37	SD3	HDMI_AUDD3 — TP88
SoC_VOUT0_DATA0	32	D0	
SoC_VOUT0_DATA1	31	D1	
SoC_VOUT0_DATA2	30	D2	
SoC_VOUT0_DATA3	29	D3	
SoC_VOUT0_DATA4	28	D4	
SoC_VOUT0_DATA5	27	D5	
SoC_VOUT0_DATA6	25	D6	
SoC_VOUT0_DATA7	24	D7	
SoC_VOUT0_DATA8	23	D8	
SoC_VOUT0_DATA9	20	D9	
SoC_VOUT0_DATA10	19	D10	
SoC_VOUT0_DATA11	18	D11	
SoC_VOUT0_DATA12	17	D12	
SoC_VOUT0_DATA13	16	D13	
SoC_VOUT0_DATA14	15	D14	
SoC_VOUT0_DATA15	14	D15	
[32] SoC_VOUT0_DATA16	13	D16	
[32] SoC_VOUT0_DATA17	11	D17	
[32] SoC_VOUT0_DATA18	10	D18	
[32] SoC_VOUT0_DATA19	9	D19	
[32] SoC_VOUT0_DATA20	8	D20	
[32] SoC_VOUT0_DATA21	7	D21	
[32] SoC_VOUT0_DATA22	6	D22	
[32] SoC_VOUT0_DATA23	4	D23	
SoC_VOUT0_HSYNC	34	HSYNC	
SoC_VOUT0_VSYNC	35	VSYNC	
SoC_VOUT0_DE	33	DE	
	36	SPDIF	
HDMI_MSTRCLK	38	MCLK	
[39] MCASP1_ACLKX_HDMI	45	SCK	
[39] MCASP1_AFSX_HDMI	44	WS	
	57, 43, 63, 73	IOGND, CGND, AGND, PAD	

R327 7.5K — DGND
R326 DNI — DGND

D-Note :-
REXT_SWING modified to 7.5K 5%, Value changed for internal testing (Radiated Emission). Refer device data sheet for the recommended value

D-Note :-
Refer SK-AM62P-LP for the latest oscillator implementation

VCC_3V3_SYS
C20 0.1uF 16V — DGND
R41 10K_1%
U7 — INH, VCC, OUTPUT, GND — 12.288MHz
R34 DNI
[33] AUDIO_EXT_REFCLK1

R-Note :-
M_CLK is not used

Cad Note :-
Move the net after the 0R and add a 0R to choose the required configuration

R287 0E — Sil9022ACNU

I2C ADDRESS: 0x3B, 0x3F, 0x62

HDMI ESD DEVICE

VCC_3V3_SYS — C248 10uF 10V — DGND
VCC_5V0 — C219 10uF 10V — DGND
VCC_3V3_SYS — R314 0E
VCC_5V0_HDMICONN — C211 10uF 10V — DGND

U50 — TPD12S016PWR

HDMI_TX0+	18	D0+	
HDMI_TX0-	17	D0-	
HDMI_TX1+	21	D1+	
HDMI_TX1-	20	D1-	
HDMI_TX2+	23	D2+	
HDMI_TX2-	22	D2-	
HDMI_CLK+	16	CLK+	
HDMI_CLK-	15	CLK-	
HDMI_CONN_I2CSCL	8	SCL_B	
HDMI_CONN_I2CSDA	9	SDA_B	
HDMICONN_HPD	10	HPD_B	
HDMI_CONNCEC	7	CEC_B	
	24	VCCA	
	11	VCC5V	
	13	5V_OUT	
	12	CT_HPD	
	5	LS_OE	
HDMI_I2C_SCL	2	SCL_A	
HDMI_I2C_SDA	3	SDA_A	
HDMI_HPD	4	HPD_A	
HDMI_CEC	1	CEC_A	
	6, 14, 19	GND1, GND2, GND3	

R-Note :-
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR

J5 — CON_HDMI_1X19_F

HDMI_TX2+	1	
HDMI_TX2-	2	
HDMI_TX1+	3	
HDMI_TX1-	4	
HDMI_TX0+	5	
HDMI_TX0-	6	
HDMI_CLK+	7	
HDMI_CLK-	8	
HDMI_CONNCEC	9	
HDMI_CONN_I2CSCL	10	
HDMI_CONN_I2CSDA	11	
VCC_5V0_HDMICONN	12	
HDMICONN_HPD	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20, 21, 22, 23	

FL17 — 120E — DGND, HDMI_EARTH

Silk: HDMI

HDMI RESET

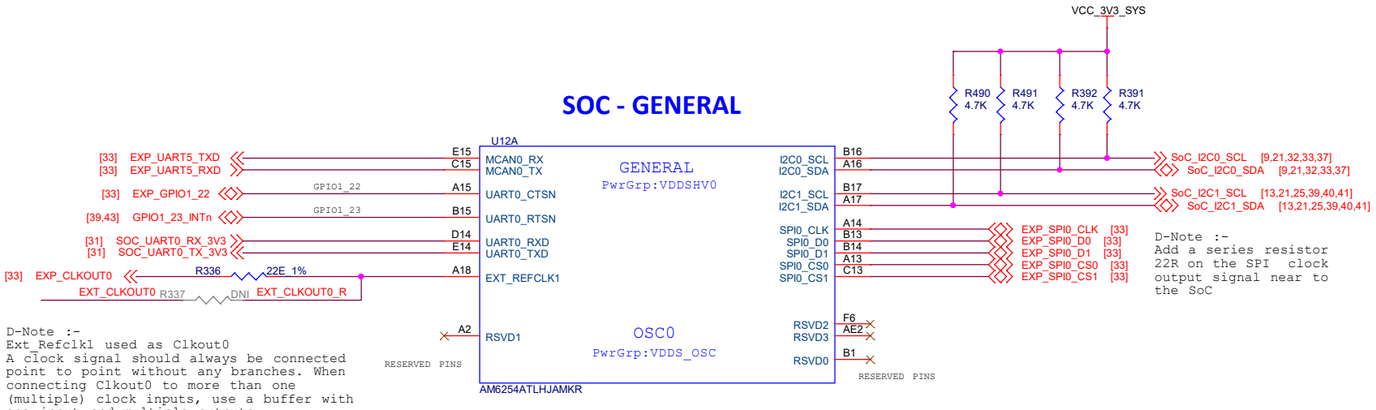
D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics

VCC_3V3_SYS — R389 10K
C323 0.1uF 50V — DGND
U54 — SN74LVC1G08DBVRE4
[39] GPIO_HDMI_RST
[18,19,20,22,23,26,32,33,37,39,40,42] RESETSTATz
HDMI_RSTn
R390 DNI
R373 10K — DGND

Designed for TI by Mistral Solutions Pvt Ltd

Title	HDMI INTERFACE		
Size	C	PROC162E1	Rev E1
Date:	Friday, June 28, 2024	Sheet 41 of 44	

SOC - GENERAL

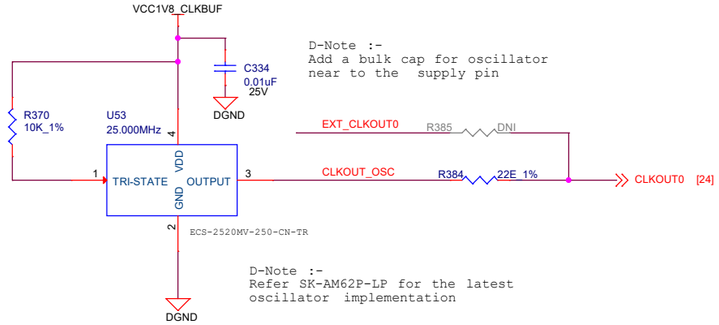


D-Note :-
Ext_Refclk1 used as Clkout0
A clock signal should always be connected point to point without any branches. When connecting Clkout0 to more than one (multiple) clock inputs, use a buffer with one input and multiple outputs.

D-Note :-
Add a series resistor 22R on the SPI clock output signal near to the SoC

OSCILLATOR

D-Note :-
Refer SoC data sheet for oscillator specs

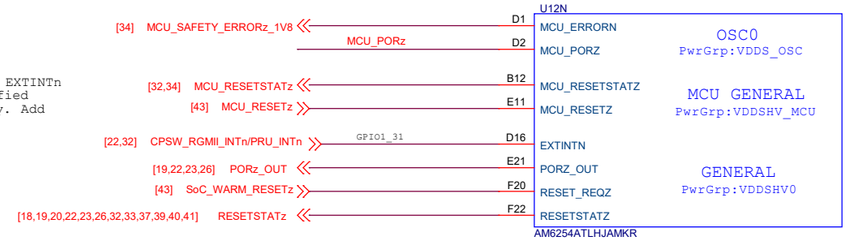


D-Note :-
Add a bulk cap for oscillator near to the supply pin

D-Note :-
Refer SK-AM62P-LP for the latest oscillator implementation

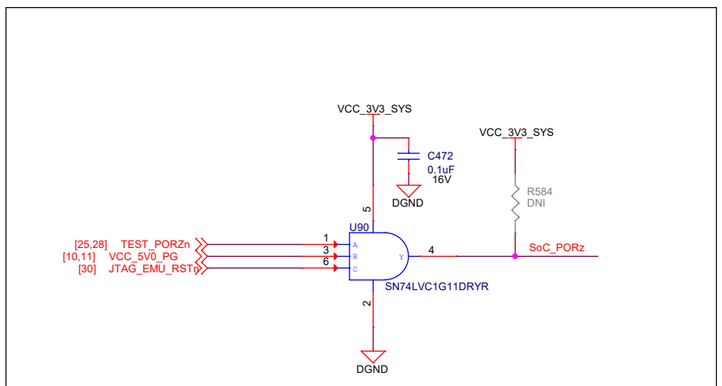
SOC - RESET

D-Note :-
Provision for a pulldow. Populate when attached device is connected. Refer SOC data sheet pin connectivity requirements

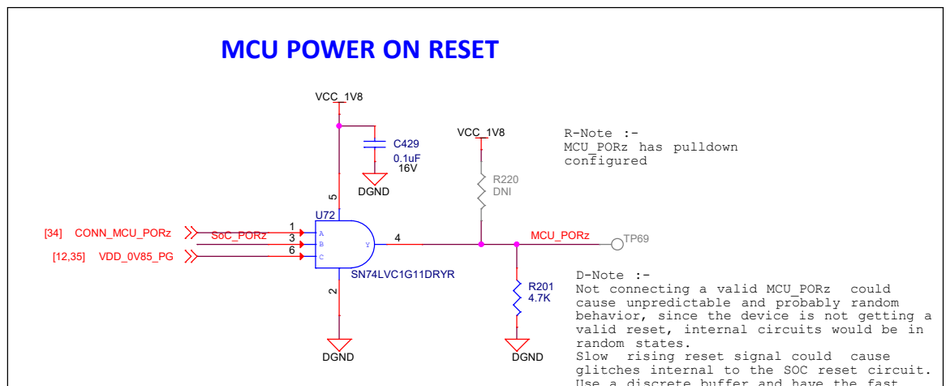


D-Note :-
Open drain output type IO EXTINTn has slew rate limit specified when pulled to 3.3V supply. Add an RC at the input. Refer TMDS64EVM.

D-Note :-
Pull-down resistor on PORz_OUT and RESETSTATz is provided to hold the attached device in reset condition during SOC reset and power-up



MCU POWER ON RESET



R-Note :-
MCU_PORz has pulldown configured

D-Note :-
Not connecting a valid MCU_PORz could cause unpredictable and probably random behavior, since the device is not getting a valid reset, internal circuits would be in random states.
Slow rising reset signal could cause glitches internal to the SOC reset circuit. Use a discrete buffer and have the fast rising output of the buffer drive the MCU_PORz is recommended

D-Note :-
A delay circuit recommended in the below section of the data sheet may be required when crystal is used as clock source
MCU_PORz Timing Requirements

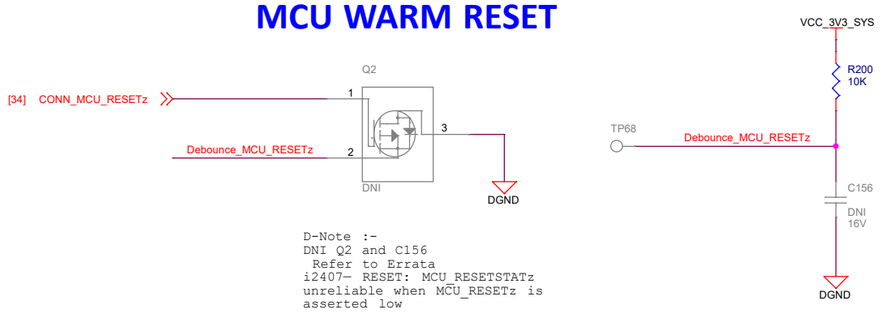
D-Note :-
It is recommended to connect the output from logic gate or discrete buffer (with fast rise time) as MCU_PORz input rather than slow rising open drain output (could glitch internally).

Designed for TI by Mistral Solutions Pvt Ltd

Title	OSCILLATOR		
Size	PROC162E1		Rev
C			E1
Date:	Friday, June 28, 2024	Sheet 42 of 44	

EXTERNAL RESET INPUT AND SCHMITT TRIGGER DEBOUNCE LOGIC

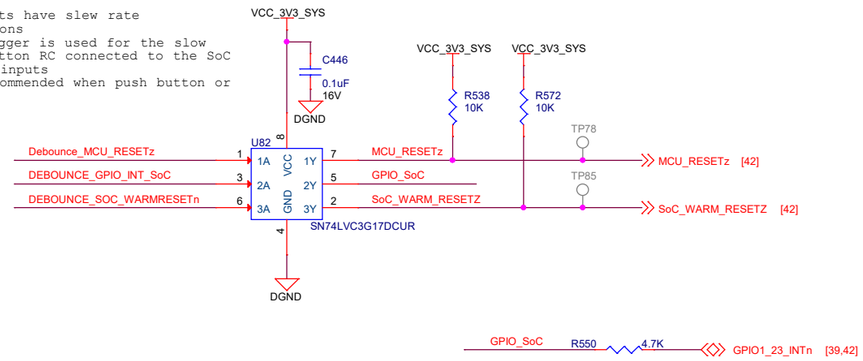
MCU WARM RESET



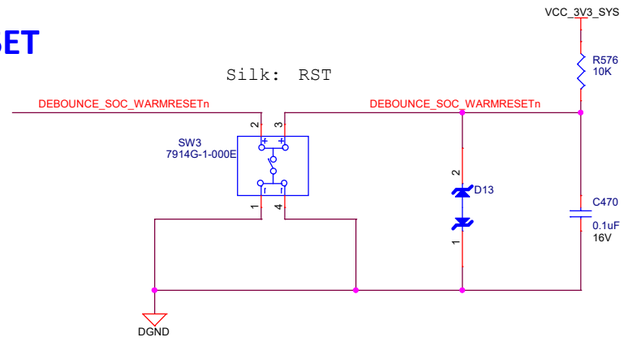
D-Note :-
DNI Q2 and C156
Refer to Errata
i2407– RESET: MCU_RESETSTATz unreliable when MCU_RESETz is asserted low

DEBOUNCE CIRCUIT

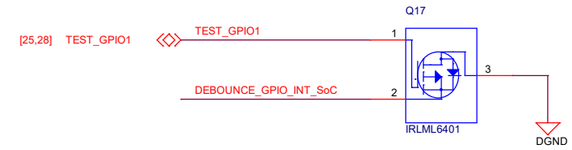
D-Note :-
LVCMOS inputs have slew rate specifications
Schmitt trigger is used for the slow ramp pushbutton RC connected to the SoC warm reset inputs
This is recommended when push button or RC is used.

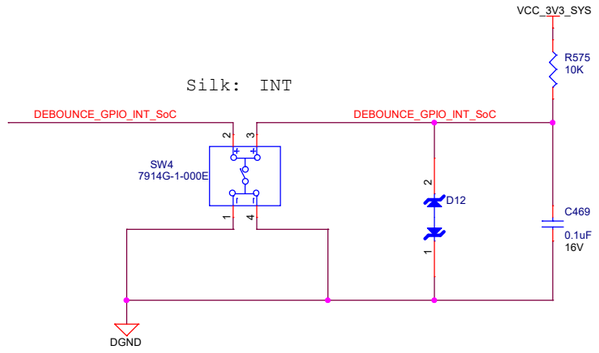


SOC WARM RESET



USER INTERRUPT





Designed for TI by Mistral Solutions Pvt Ltd

Title	RESET	
Size	PROC162E1	Rev
C		E1
Date: Friday, June 28, 2024	Sheet 43 of 44	

MOUNTING HARDWARE

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and
packed securely before shipment.

BARE PCB

PROC114

PROC114E1

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

LABELS

Board Serial No.

LBL1
PCB LABEL
DNI

Assembly Revision

LBL2
PCB LABEL
DNI

STANDOFF,SCREW & WASHER FOR PCIe M.2

ACC1
9774015243R

MH1
FLAT WASHER_M2
3356

MH2
PAN HEAD_M2 X 5
MPMS 002 0005 PH

FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

R-Note :-
Refer STRAP CONFIGURATION OF ETHERNET
PHYS page from SK-AM64B schematics

Designed for TI by Mistral Solutions Pvt Ltd

TEXAS INSTRUMENTS

MISTRAL

Title	HARDWARE SCHEMATICS	
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