AM62P STARTER KIT EVM

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BOARD REVISION	E1-1
SCHEMATIC VERSION	2.0

Note:
Verify the DNI components configuration with respect to the SK schematics (Use PDF) after completion of design before board assembly

Link to Design Collaterals : https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review

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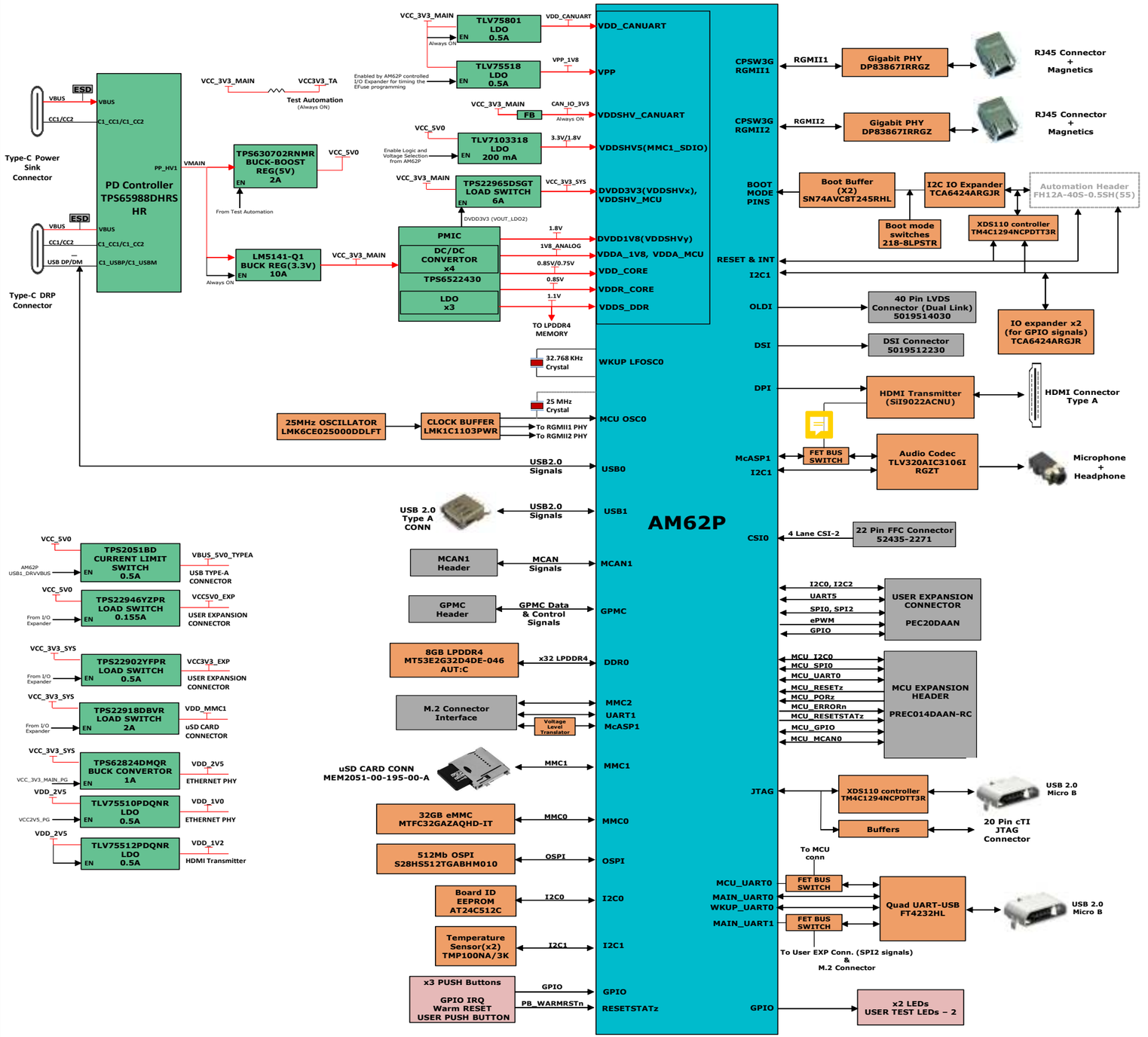
REVISION HISTORY

	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	0.01	20 FEB 2023	Initial Draft derived from AM62A SK - PROC135E3 schematics	Mistral Design Team		
	0.02	23 FEB 2023	Updated power section & PMIC part as per PDN	Mistral Design Team		
	0.03	24 FEB 2023	1. Added pullups on XDS110 side for Test Automation signals 2. Added 5V0 sourcing caps to meet USB Specifications	Mistral Design Team	Nishant	
	0.04	27 FEB 2023	Replaced parts : LPDDR4 (8 GB), eMMC (32 GB with HS400 support), OSPI (512 Mb NOR Flash)	Mistral Design Team		
	0.06	01 MAR 2023	Replaced parts : LPDDR4 (8 GB), eMMC (32 GB with HS400 support), OSPI (512 Mb NOR Flash) Added DSI, OLDI, GPMC (x8) connectors & updated respective net connections	Mistral Design Team	Nishant	
	0.07	03 MAR 2023	Updated PMIC local caps, GPIO connections & assembly variants	Mistral Design Team		
	0.08	08 MAR 2023	1. Updated INA section to include INA228 as default with footprint support for INA231 2. INA Kelvin sense resisitors moved to PMIC sheet as per modular design requirement	Mistral Design Team	Nishant	
	0.09	15 MAR 2023	1. Updated TI review comments 2. Updated PMIC connections as per PDN v1.5	Mistral Design Team	Nishant	
	0.10	16 MAR 2023	Added separate dual LDO for VDDSHV_SDIO, 5V0 headers for OLDI & DSI daughter cards	Mistral Design Team		
	0.11	20 MAR 2023	1. Updated PMIC Enable & GPIO connections 2. Modified RC shield connections for RGMII1, RGMII2 & USB Type A connectors	Mistral Design Team		
	0.12	22 MAR 2023	1. Updated TI review comments on PD Controller 2. Replaced HDMI EXT_SWING resistor with 7.5K_5% ohms	Mistral Design Team	Nishant	
	0.13	28 MAR 2023	Added extra local caps to PMIC Switching outputs as recommended in datasheet	Mistral Design Team		
	0.14	04 APR 2023	Modified SoC decaps & added RC circuit for I2C	Mistral Design Team		
	0.15	07 APR 2023	1. Added series resistors for RGMII TX signals 2. Swapped DDR DQ & DMI bits	Mistral Design Team		
	0.16	13 APR 2023	Implemented review comments from TI	Mistral Design Team	Nishant	Ajit
	0.17	18 APR 2023	1. Updated Internal and review comments from TI 2. Replaced Oscillator with new LMK6CE series (BAW), OLDI and DSI Connector.	Mistral Design Team	Nishant	Ajit
	0.18	03 MAY 2023	Modified the 3T decaps as 4 pin IC's and updated a few review comments from TI	Mistral Design Team	Nishant	
	0.19	10 MAY 2023	Modified the 2T current sense resistor parts to 4T sense similar to AM62A SK	Mistral Design Team	Nishant	
	0.20	16 MAY 2023	1. Replaced USB Type A load switch (with OC) & ESD protection device 2. Added capacitor to CT pin of VCC_3V3_SYS & VDD_MMC1 load switches	Mistral Design Team	Nishant	Ajit
	0.21	24 MAY 2023	1. VMON connection modified for PMIC to meet threshold of 3.3V 2. Part References Back annotated from PCB file	Mistral Design Team		
	0.22	16 JUNE 2023	1. Updated OPN's for SoC and PMIC 2. Removed dip switch for VDD_CORE voltage configuration. 3. Replaced HDMI connector part	Mistral Design Team	Nishant	
	0.23	21 JUNE 2023	1. Removed shorting jumper for VCC_CORE rail 2. Added dip switch control for EMU0 & EMU1 signals	Mistral Design Team	Nishant	
	0.24	23 JUNE 2023	1.Modified decaps for VDD_CORE 2.Replaced 3T SoC decaps with correct symbol & footprints	Mistral Design Team	Nishant	
	0.25	21 AUG 2023	1. Corrected power architecture & sequencing diagrams 2. Baselined	Mistral Design Team	Nishant	Ajit
E1-1	1.1	03 OCT 2023	1. Modified WD_DISABLE pull to VCC_3V3_MAIN 2. Modified PMIC_RSTOUT pull to VCC_3V3_SYS 3. Changed Assembly instruction for R280 to Mount 4. Changed the PMIC VSENSE voltage from VMAIN to VBUS_TYPEC1 and VBUS_TYPEC2 (dual input) and implemented ORing diode.	Mistral Design Team	Nishant	Ajit MB
	1.2	05 OCT 2023	Few circuits marked DNI as captured in change list document	Mistral Design Team	Nishant	Ajit MB
	2.0	21 NOV 2023	Baselined	Mistral Design Team	Nishant	Ajit MB

BLOCK DIAGRAM - AM62P SKEVM



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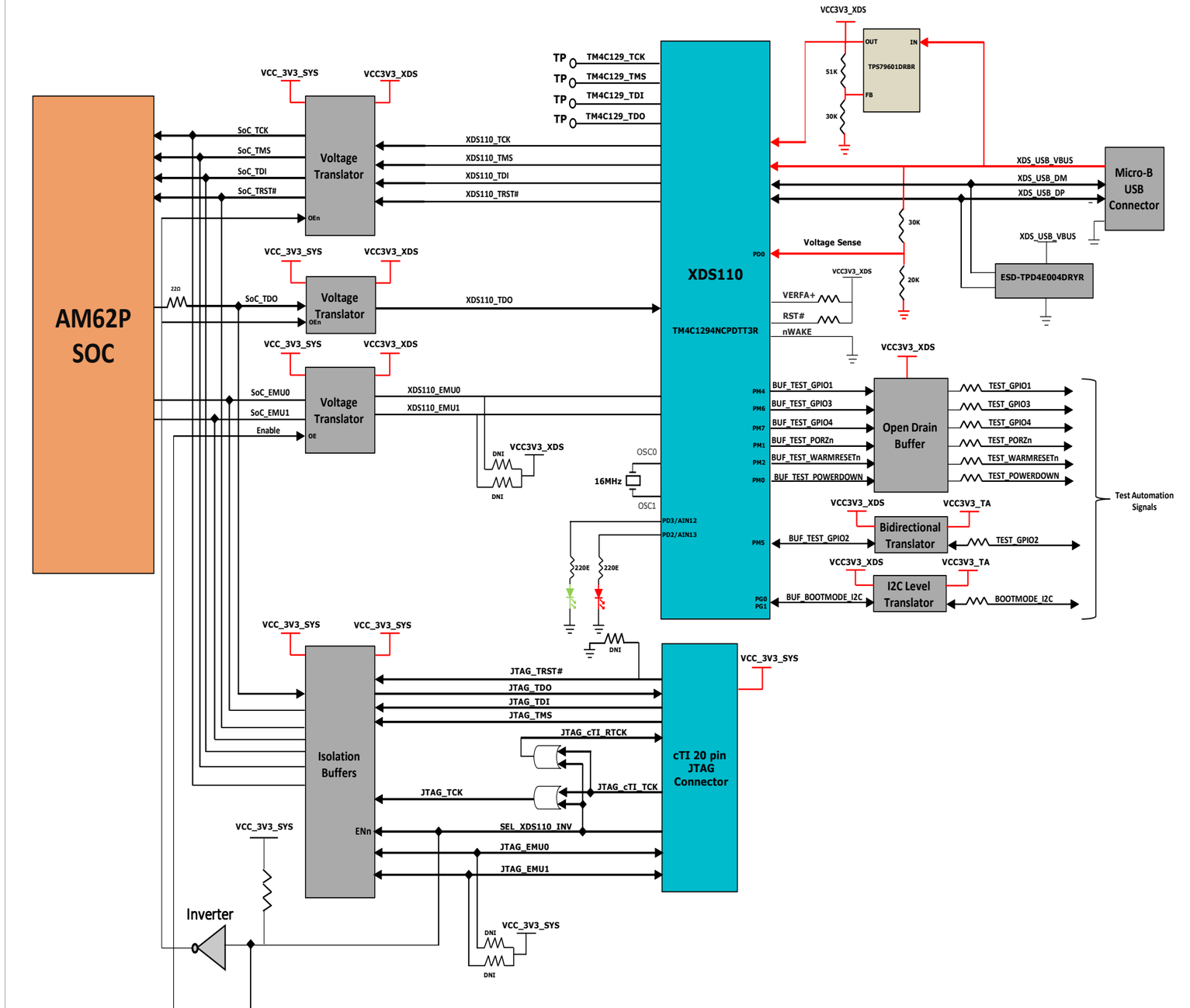
BLOCK DIAGRAM - XDS110



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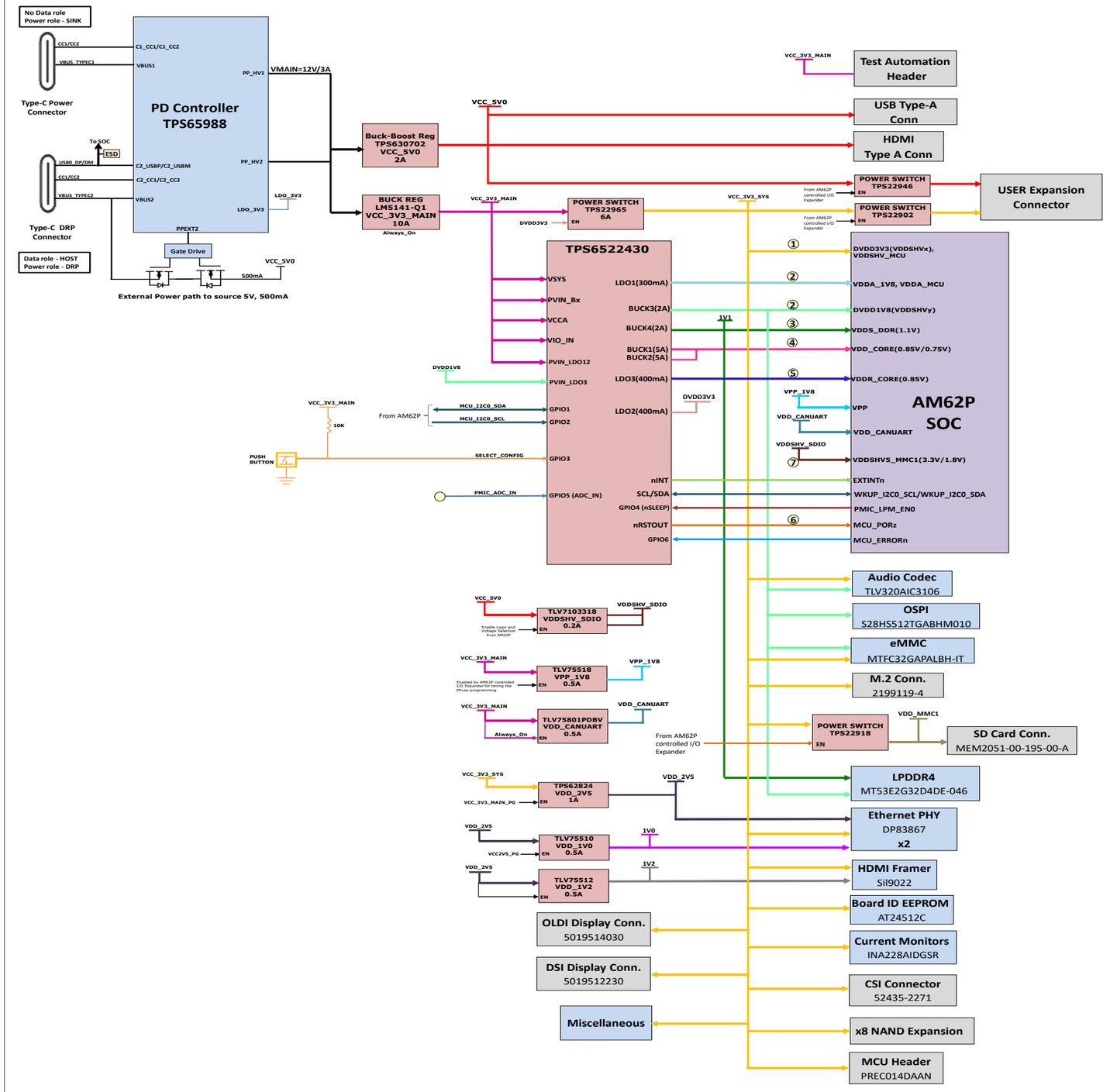
POWER ARCHITECTURE BLOCK DIAGRAM



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Title	POWER BLOCK DGM		
Size	PROC164E1-1		Rev
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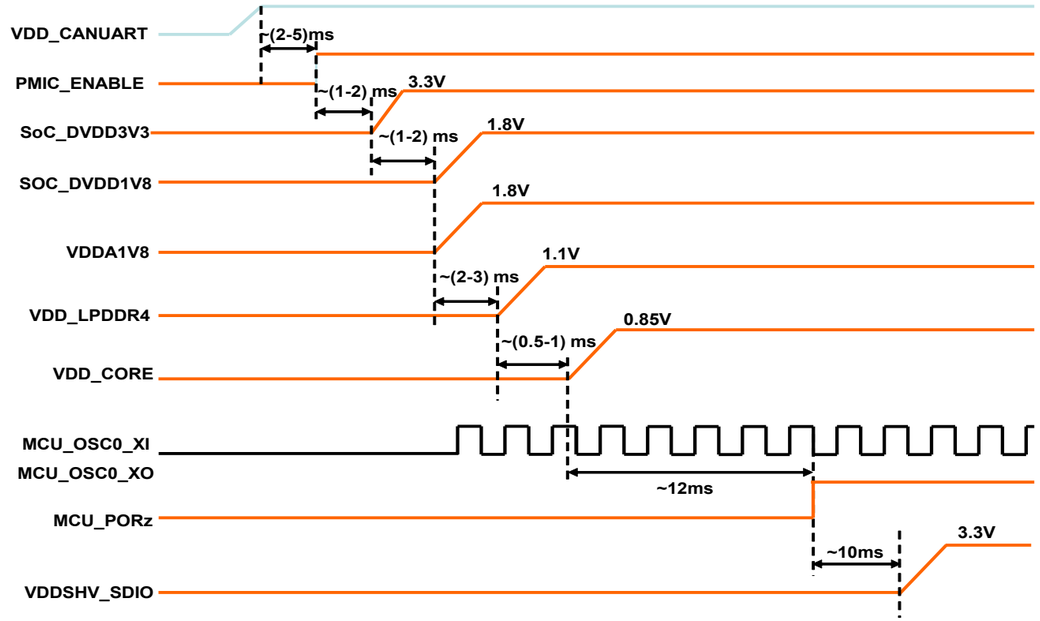
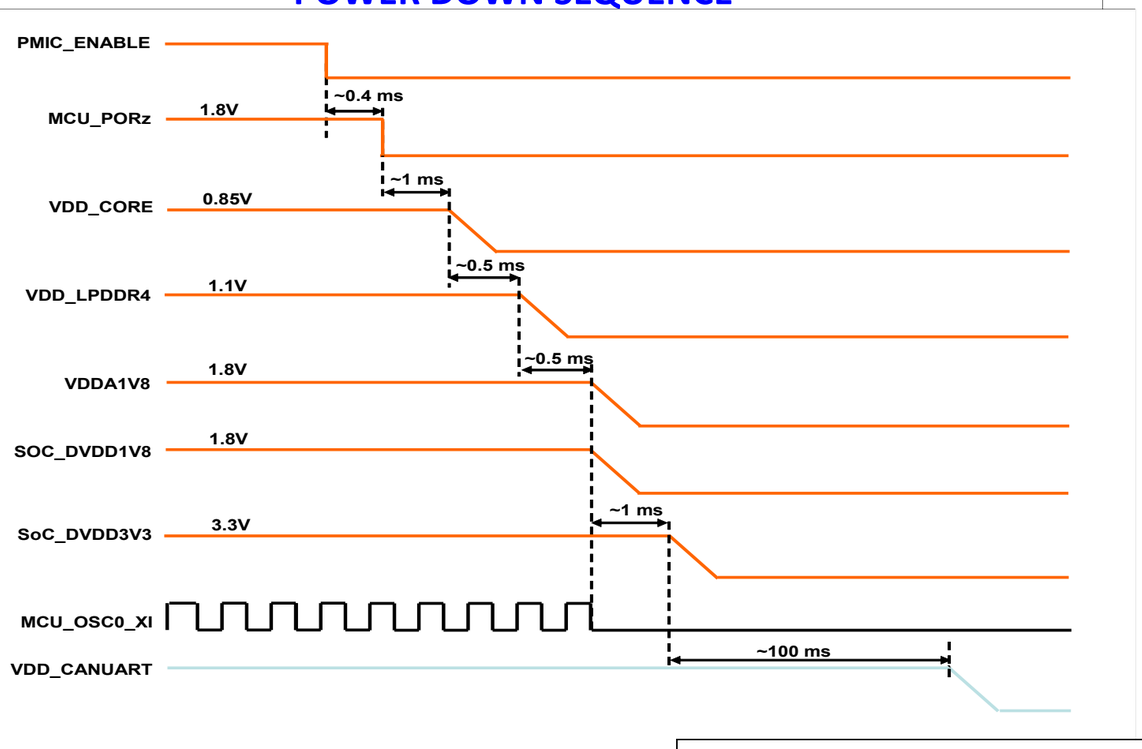
POWER UP SEQUENCE



POWER DOWN SEQUENCE



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MISTRAL

Title	POWER SEQUENCE	
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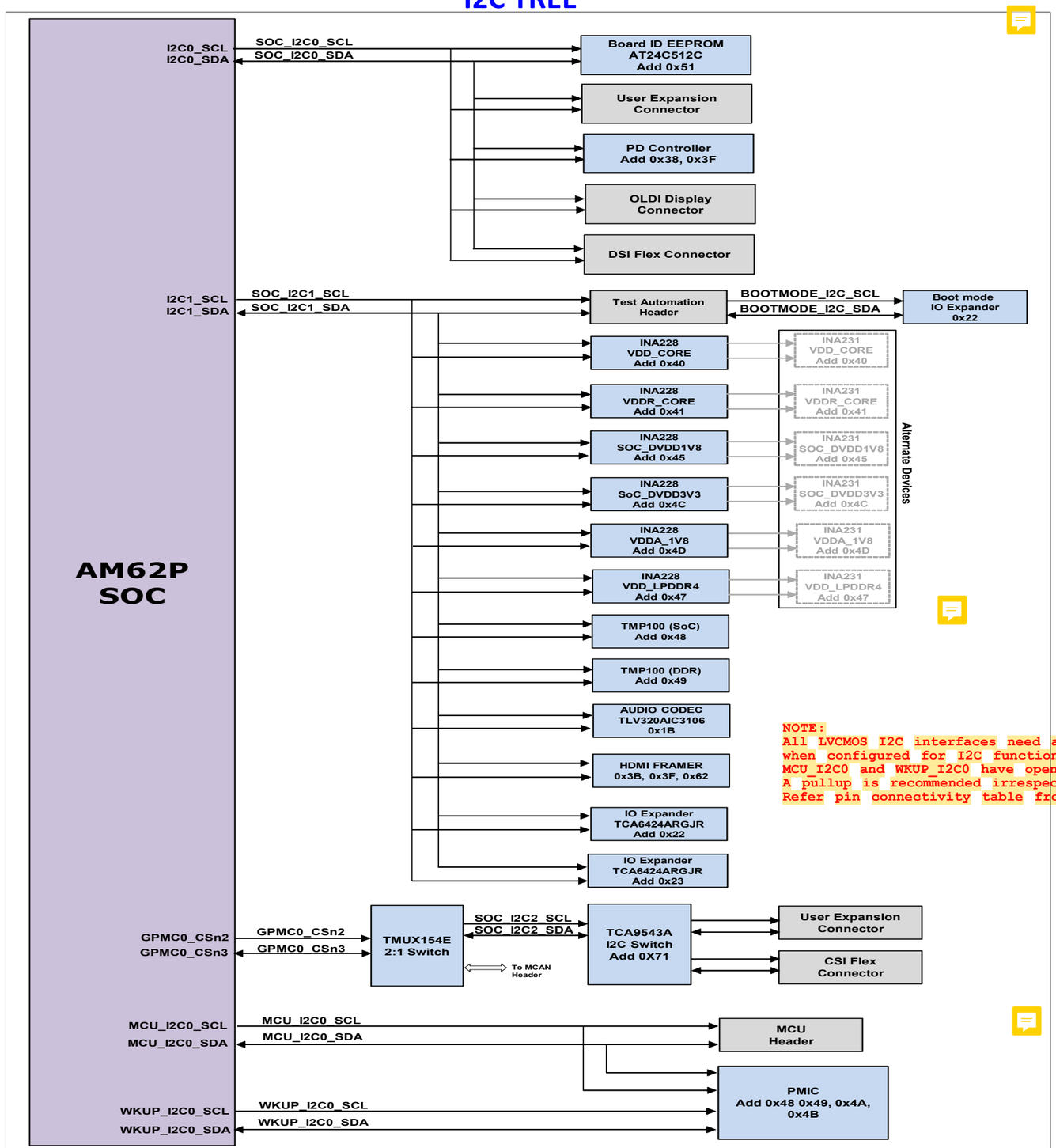
I2C TREE



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Title	I2C TREE	
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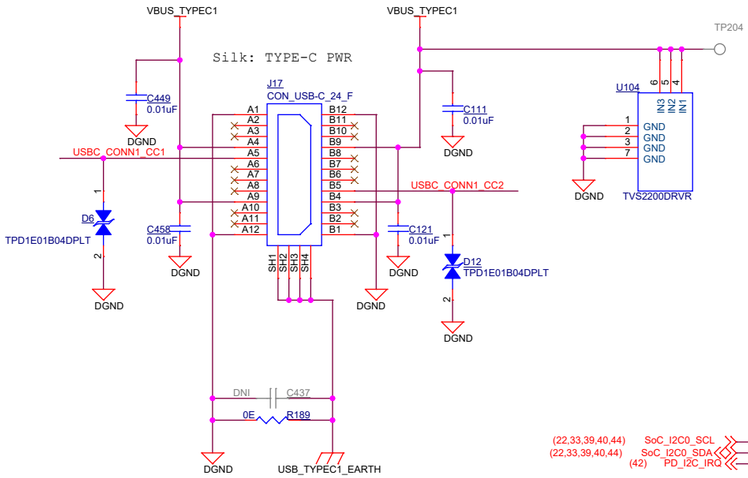
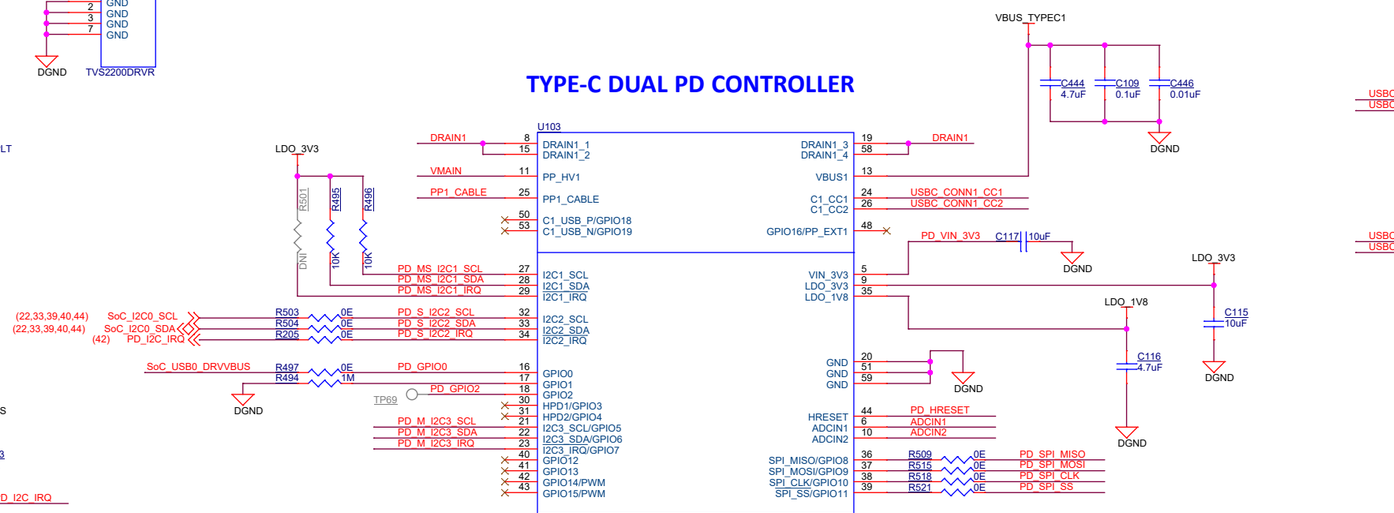
GPIO MAPPING TABLE

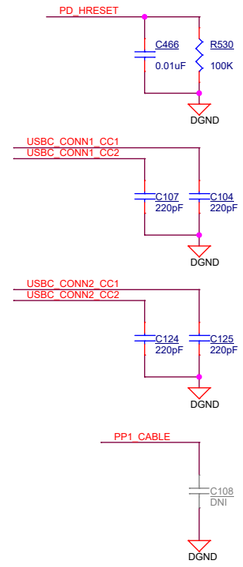
SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	MCU Interrupt	MCU_INTn	INTERRUPT	MCU_GPIO0_0	MCU_SPI0_CS0	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
9	PMIC Interrupt	PMIC_INTn	INTERRUPT	GPIO0_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_INH	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
11	CAN-FD fast wake signal from MCU header	CAN_FD_WKUP_HDR_INH								
12	User test LED control signal	SOC_GPIO1_49	ENABLE	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	User Interrupt									
15	Low power mode enable	PMIC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
16	SD Card I/O Voltage Selection	VSEL_SD_SOC	SELECTION	GPIO0_31	GPMC0_CLK	OUTPUT	NA	NA	VDDSHV2	SoC_DVDD3V3
IO EXPANDER – 01										
1	Interrupt from OLDI display	OLDI_INT#	INTERRUPT	IO EXPANDER-P00		INPUT	HIGH	LOW		VCC_3V3_SYS
2	x8 NAND Card Presence Dectect	x8_NAND_DETECT	DETECTION	IO EXPANDER-P01		INPUT	HIGH	LOW		VCC_3V3_SYS
3	MCASP1 Enable and Direction Control	UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P02		OUTPUT	HIGH	-		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	SOC UART1 Mux Select	UART1_FET_BUF_EN	ENABLE	IO EXPANDER-P06		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	DSI Display GPIO0	DSI_GPIO0	GPIO	IO EXPANDER-P10		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
10	DSI Display GPIO1	DSI_GPIO1	GPIO	IO EXPANDER-P11		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
11	OLDI to HDMI Card Device ID interrupt	OLDI_EDID	INTERRUPT	IO EXPANDER-P12		INPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC_3V3	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	USB Type A overcurrent indicator	USB_TYPEA_OC_INDICATION	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
16	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	-		VCC_3V3_SYS
22	DSI to HDMI Card Device ID interrupt	DSI_EDID	INTERRUPT	IO EXPANDER-P25		INPUT	HIGH	LOW		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER – 02										
1	M.2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
2	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P01		OUTPUT	LOW	HIGH		VCC_3V3_SYS
3	Wilink Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	SoC I2C2 & MCAN MUX Selection	SoC_I2C2_MCAN_SEL	CONTROL	IO EXPANDER-P20		OUTPUT	HIGH	-		VCC_3V3_SYS
5	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P21		OUTPUT	HIGH	LOW		VCC_3V3_SYS
6	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P23		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	OLDI display Reset control GPIO	GPIO_OLDI_RSTn	RESET	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS

USB TYPE-C POWER

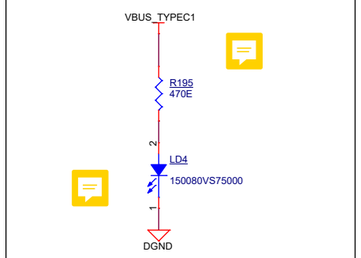
TYPE-C DUAL PD CONTROLLER



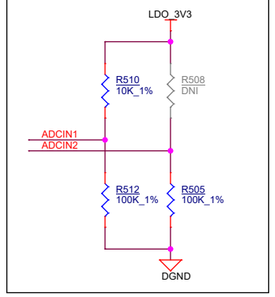




POWER INDICATION LED: VBUS_TYPEC1

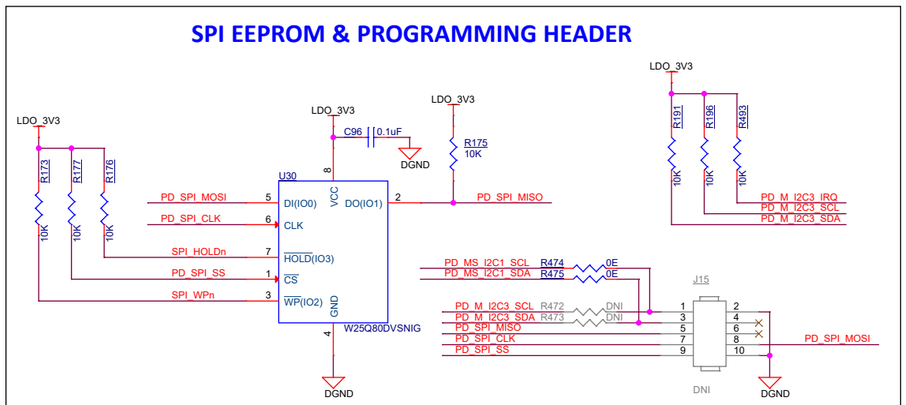


BP_NoWait Safe Configuration

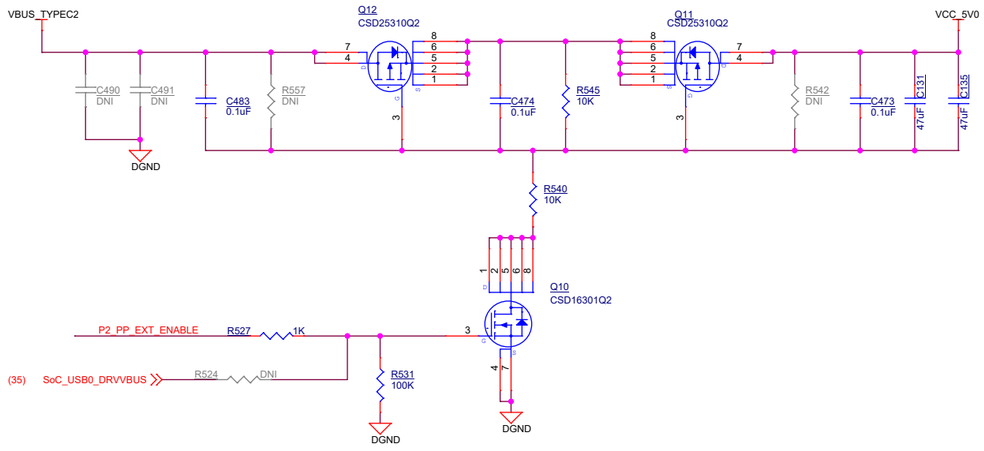


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

SPI EEPROM & PROGRAMMING HEADER



EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



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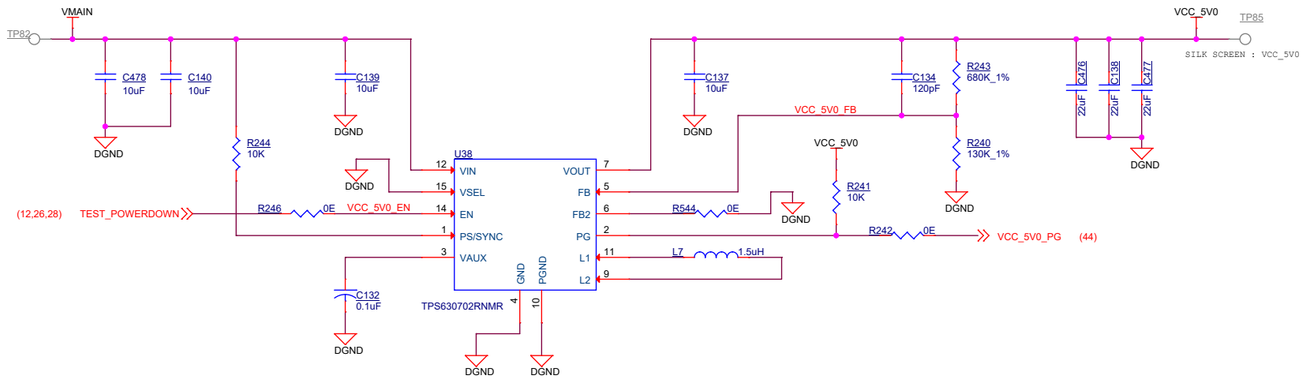
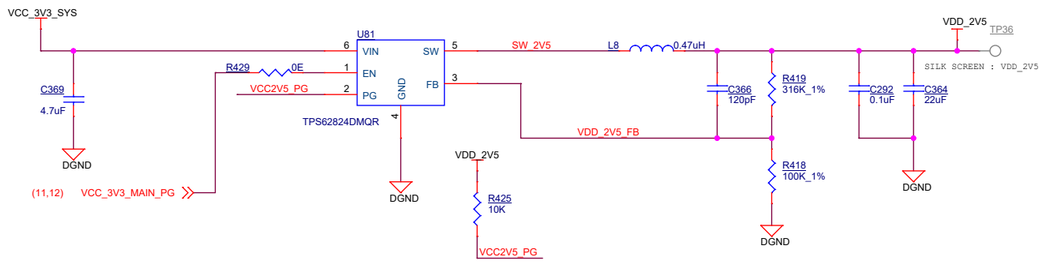
PERIPHERAL POWER SUPPLY-1

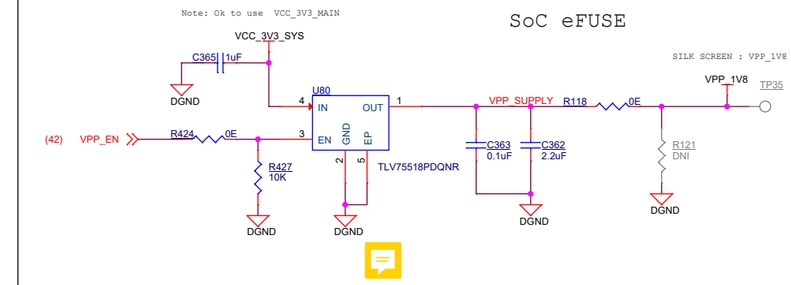
VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A



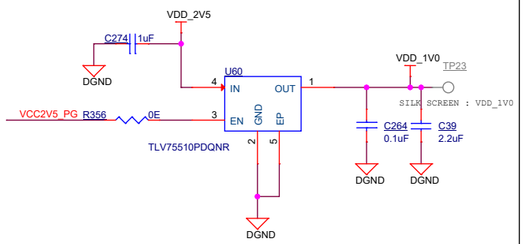
2.5V (ETHERNET PHY), 1.0AMPS SUPPLY



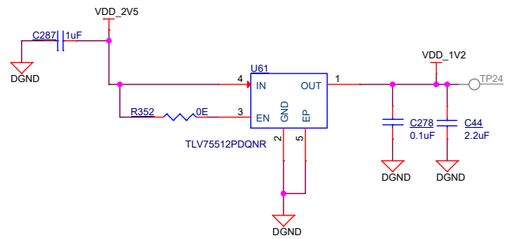
1.8V VPP (eFUSE), 0.5AMPS SUPPLY



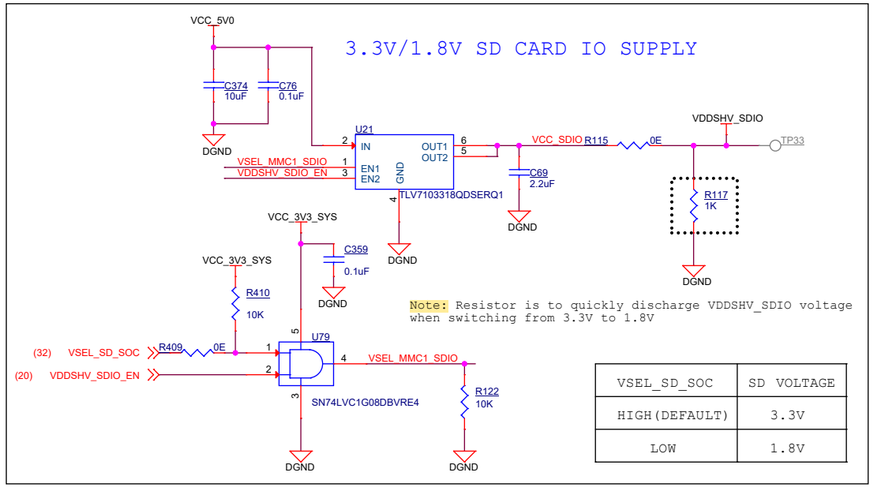
1.0V (ETHERNET PHY), 0.5AMPS SUPPLY



1.2V (HDMI), 0.5AMPS SUPPLY



3.3V/1.8V SD CARD IO SUPPLY



VSEL_SD_SOC	SD VOLTAGE
HIGH(DEFAULT)	3.3V
LOW	1.8V

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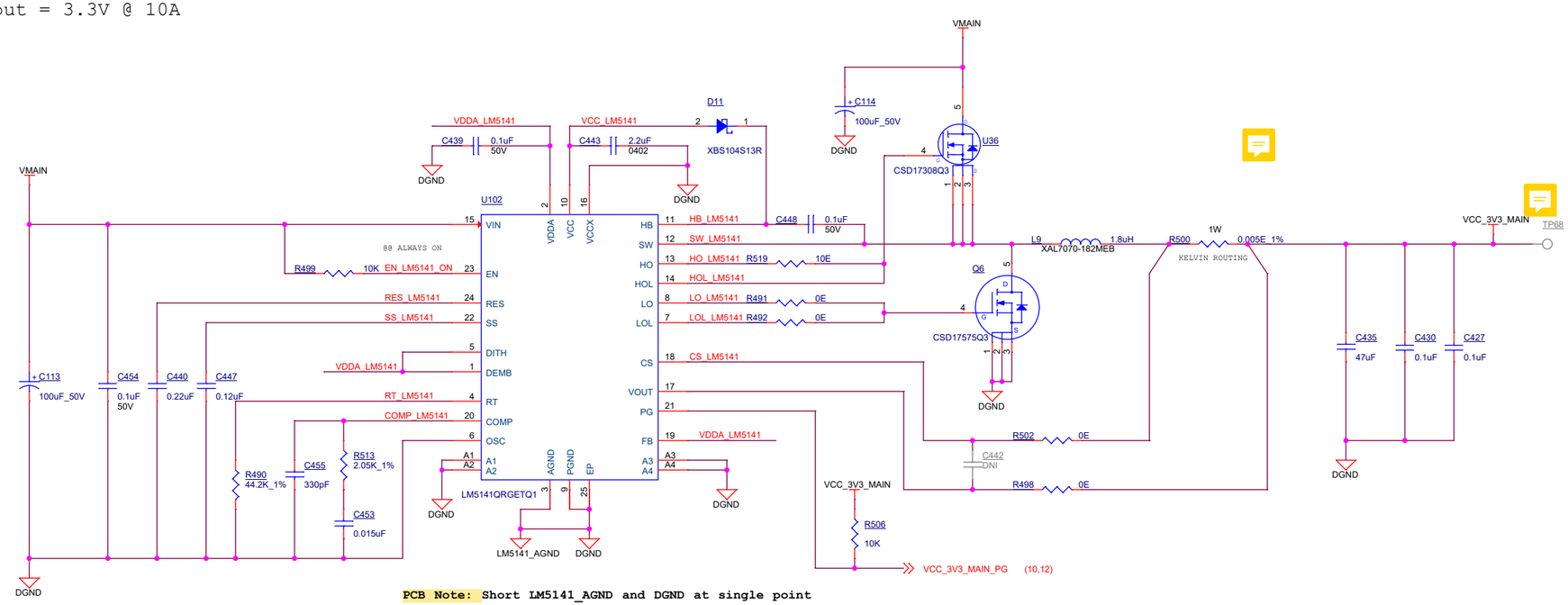
PERIPHERAL POWER SUPPLY-2

VinMin = 4.5V
VinMax = 15V
Vout = 3.3V @ 10A

3.3V, 10.0 AMPS SUPPLY



PCB Note: Short LM5141_AGND and DGND at single point

(34) ETH_CAN_INH_PREREG — DNI R75 — EN_LM5141_ON

GND TEST POINTS

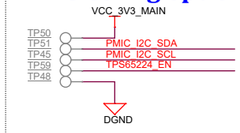
TP9 TP101 TP100 TP2 TP1 TP194 TP193 TP60 — DGND

Designed for TI by Mistral Solutions Pvt Ltd

Title	PERIPHERAL POWER SUPPLY-2		
Size	C	PROC164E1-1	Rev E1-1
Date:	Thursday, November 16, 2023	Sheet 11 of 47	

SOC POWER SUPPLY PMIC

PMIC Config option



Silk: PMIC_PROG

PMIC PUSH BUTTON LOGIC

R157	VDD_CORE VOLTAGE
Mounted	0.85 V (DEFAULT)
Not Mounted	0.75 V

Note: When R157 is DNI, Push Button (SW2) becomes operational through internal pullup on PMIC GPIO3

PMIC POWER INDICATION LED

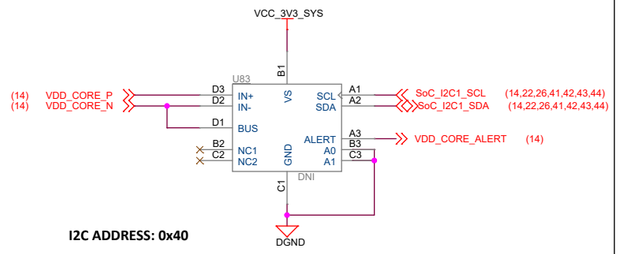
VCC_3V3_SYS LOAD SWITCH

Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC POWER SUPPLY PMIC	
Size: C	PROC164E1-1	Rev: E1-1
Date: Friday, December 01, 2023	Sheet 12 of 47	

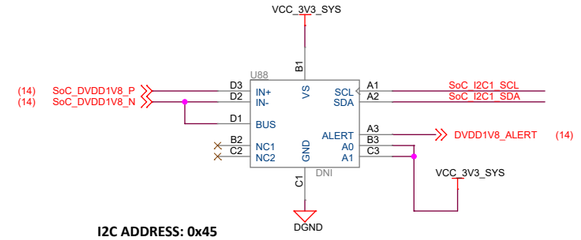
CURRENT MONITORING DEVICES - 1

VDD_CORE



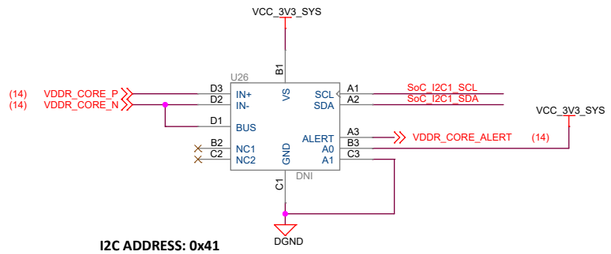
I2C ADDRESS: 0x40

SoC_DVDD1V8



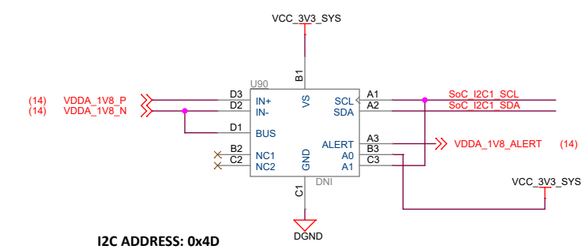
I2C ADDRESS: 0x45

VDDR_CORE



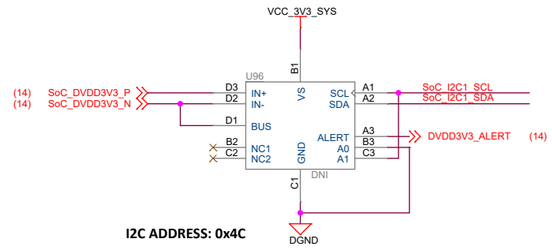
I2C ADDRESS: 0x41

VDDA_1V8



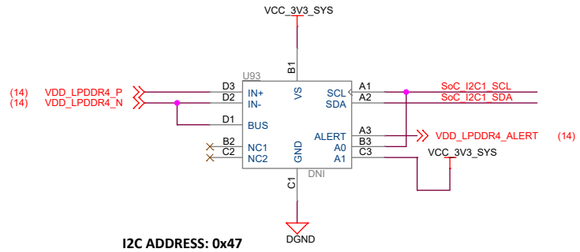
I2C ADDRESS: 0x4D

SoC_DVDD3V3



I2C ADDRESS: 0x4C

VDD_LPDDR4



I2C ADDRESS: 0x47

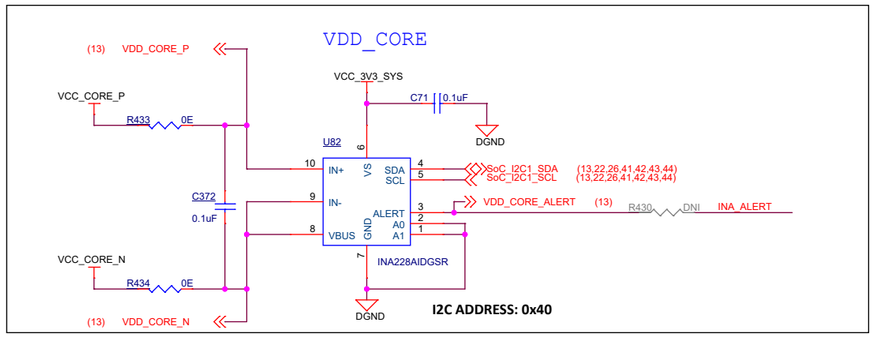
Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

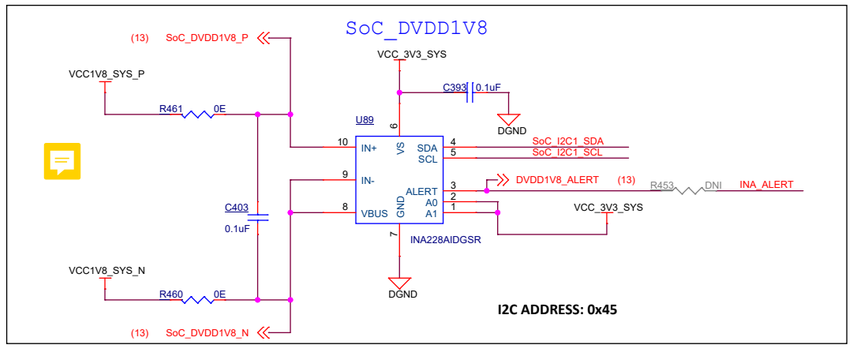
INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

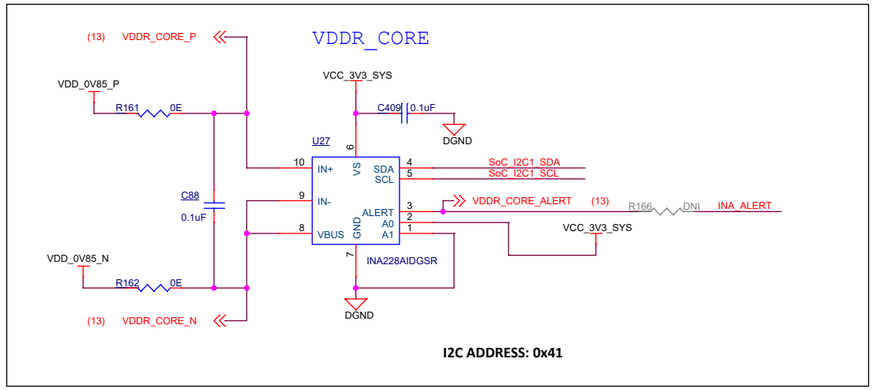
Designed for TI by Mistral Solutions Pvt Ltd

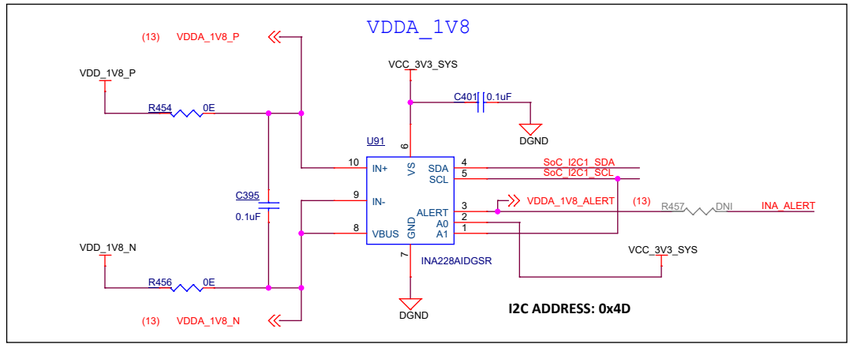
Title	CURRENT MONITORING DEVICES - 1	
Size C	PROC164E1-1	Rev E1-1
Date: Thursday, November 16, 2023	Sheet 13 of 47	

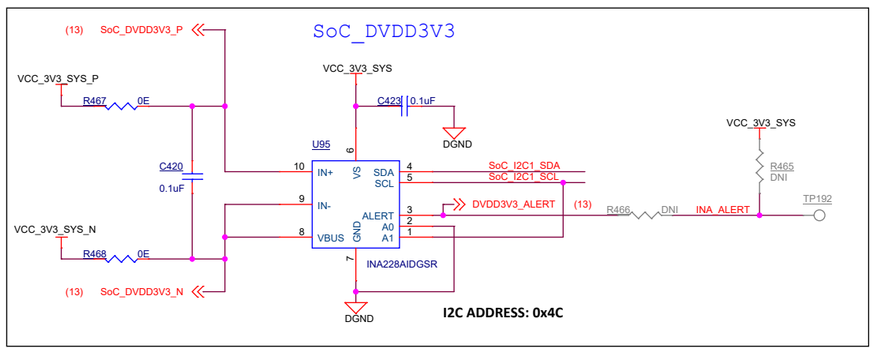
CURRENT MONITORING DEVICES - 2

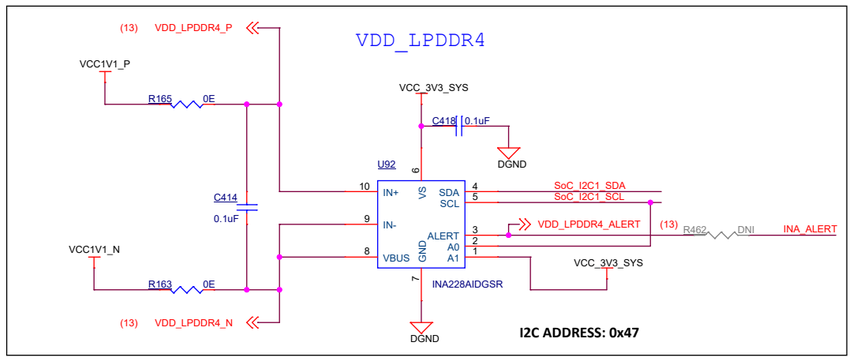












Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

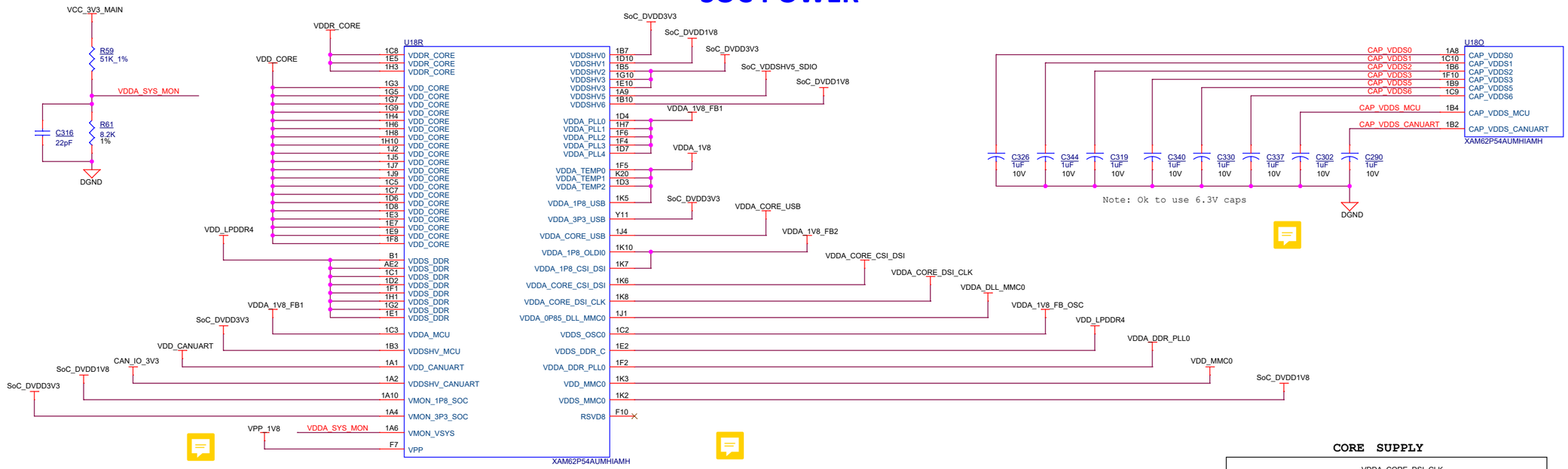
INA I2C SLAVE ADDRESS

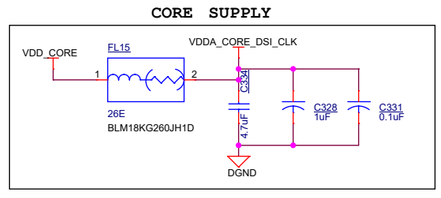
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

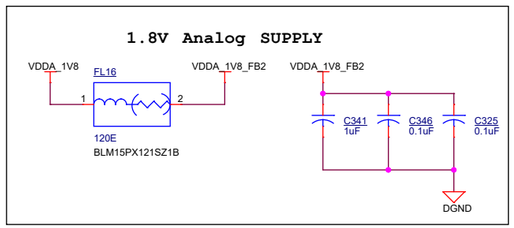
Designed for TI by Mistral Solutions Pvt Ltd

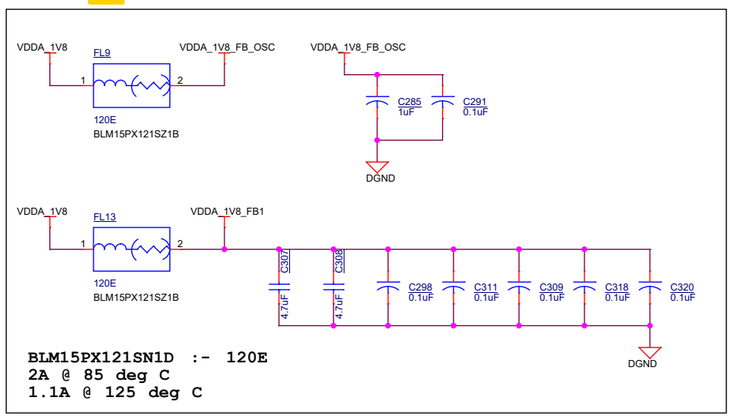
Title	CURRENT MONITORING DEVICES - 2	
Size C	PROC164E1-1	Rev E1-1
Date: Thursday, November 16, 2023	Sheet 14 of 47	

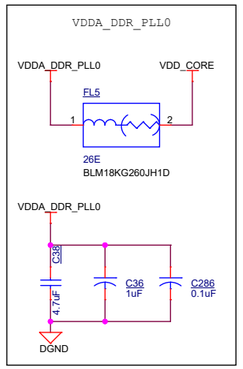
SOC POWER

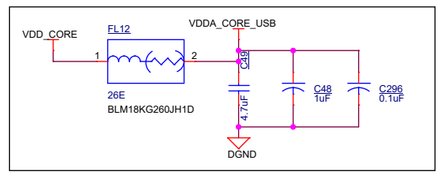


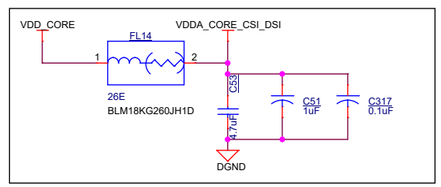


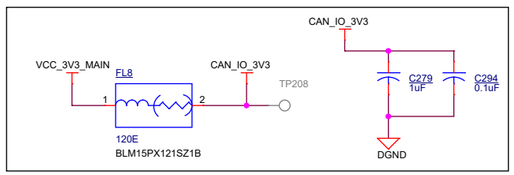


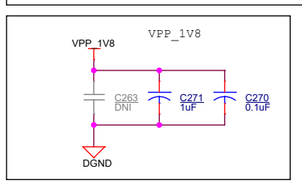


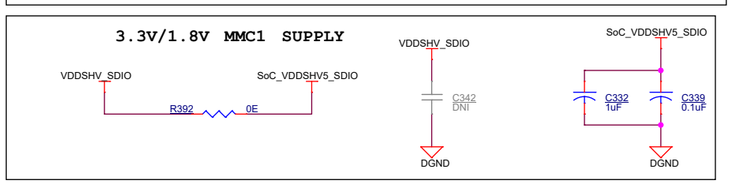


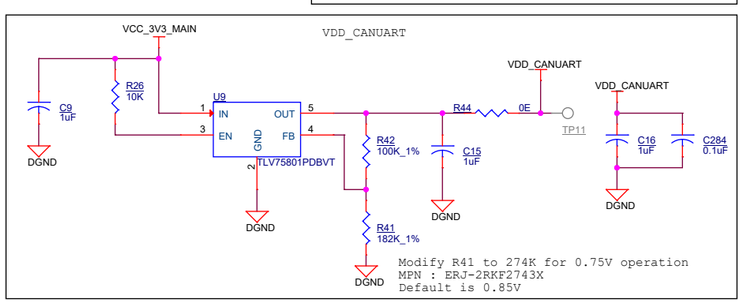


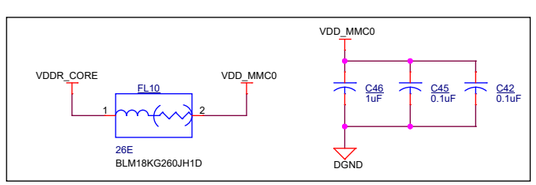


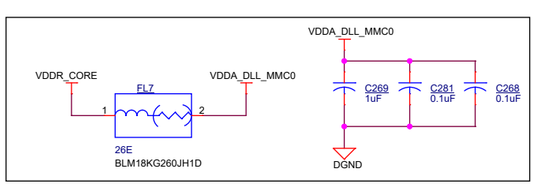












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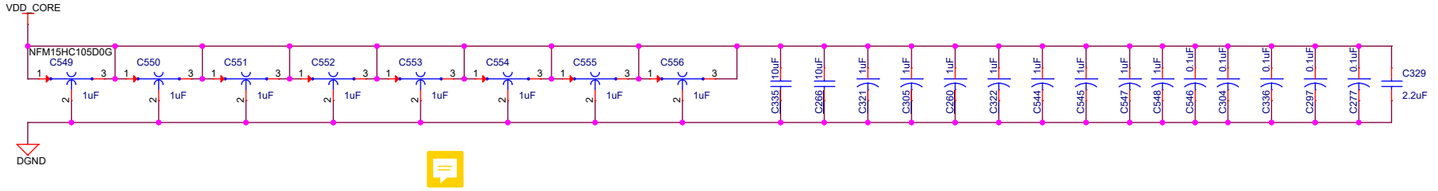
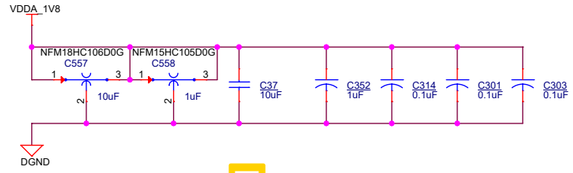
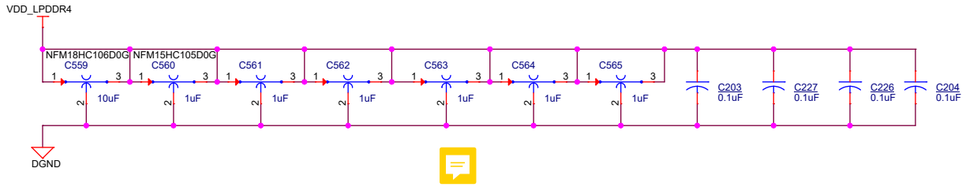
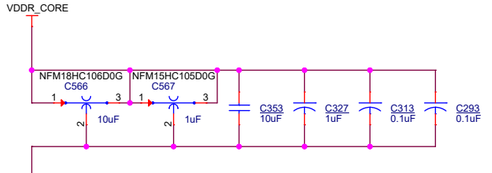
Title	SOC POWER	
Size	PROC164E1-1	Rev
C		E1-1
Date:	Friday, December 01, 2023	Sheet 15 of 47

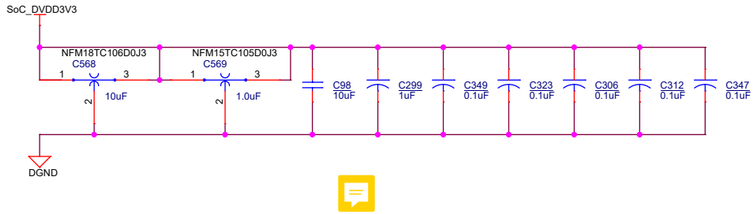
SOC POWER DECAPS

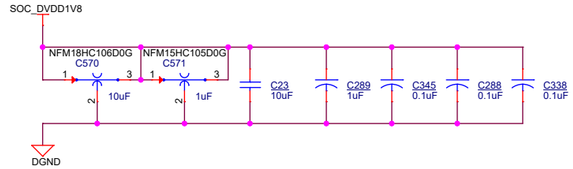




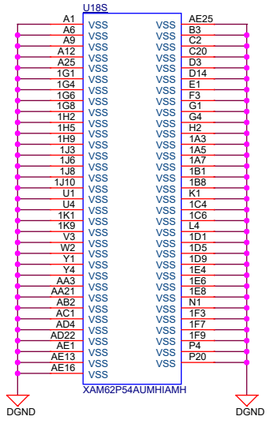








SOC VSS



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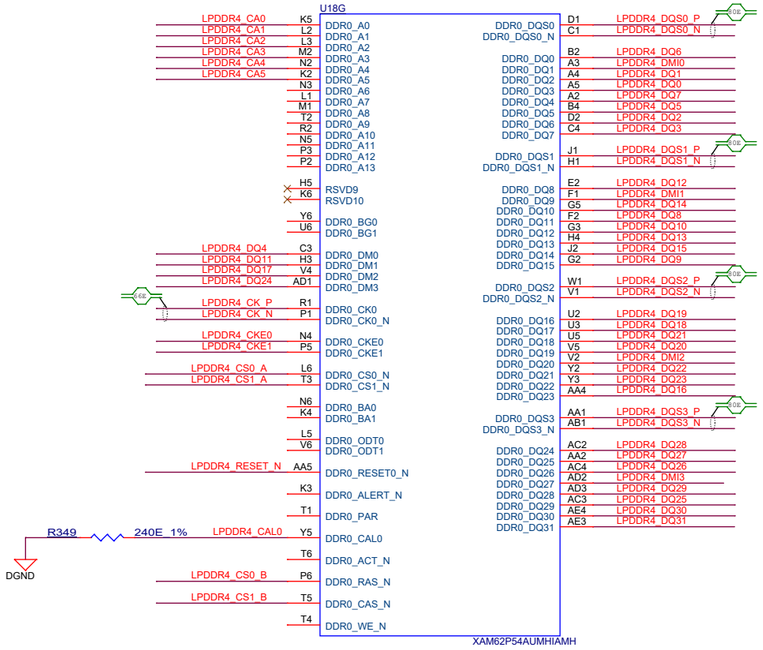
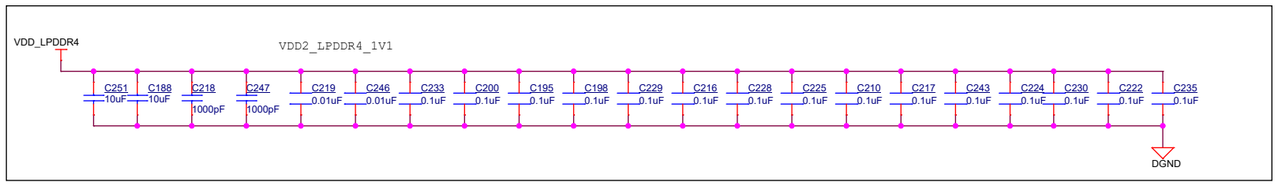
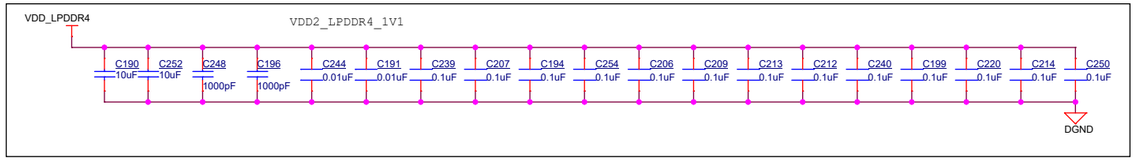
Title	SOC POWER CAPS & SOC VSS		
Size C	PROC164E1-1		Rev
Date:	Thursday, November 16, 2023	Sheet 16 of 47	

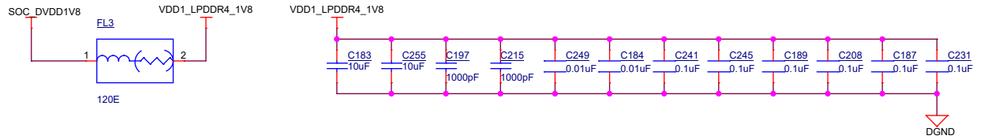
SOC LPDDR4 INTERFACE



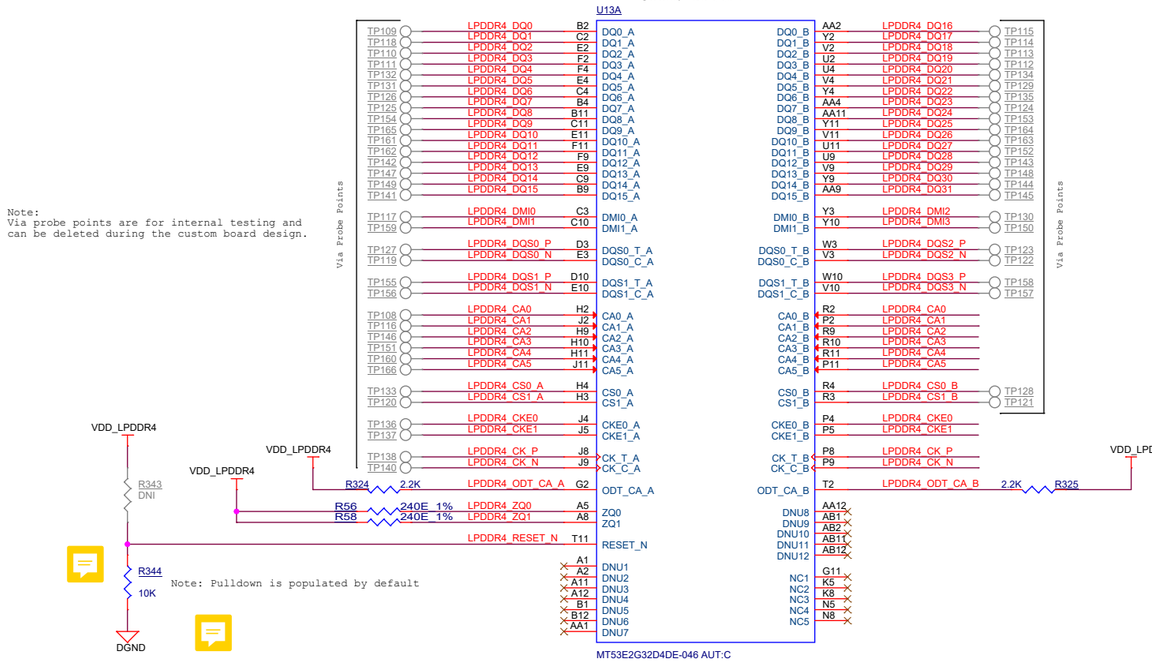
LPDDR4 POWER DECAPS

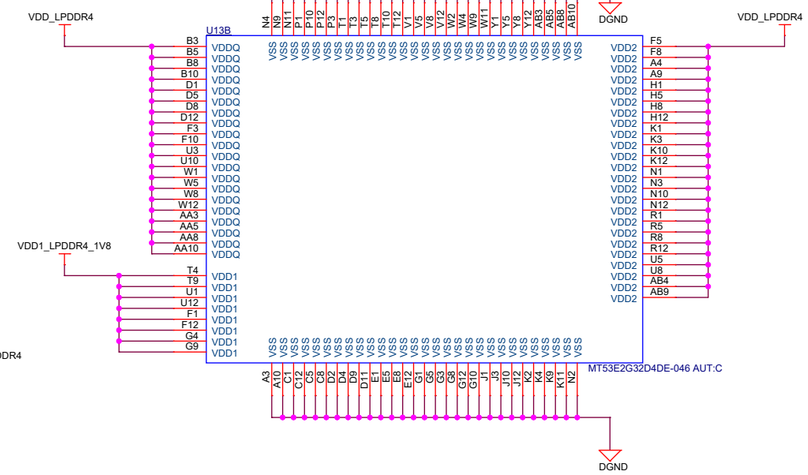






LPDDR4 DEVICE





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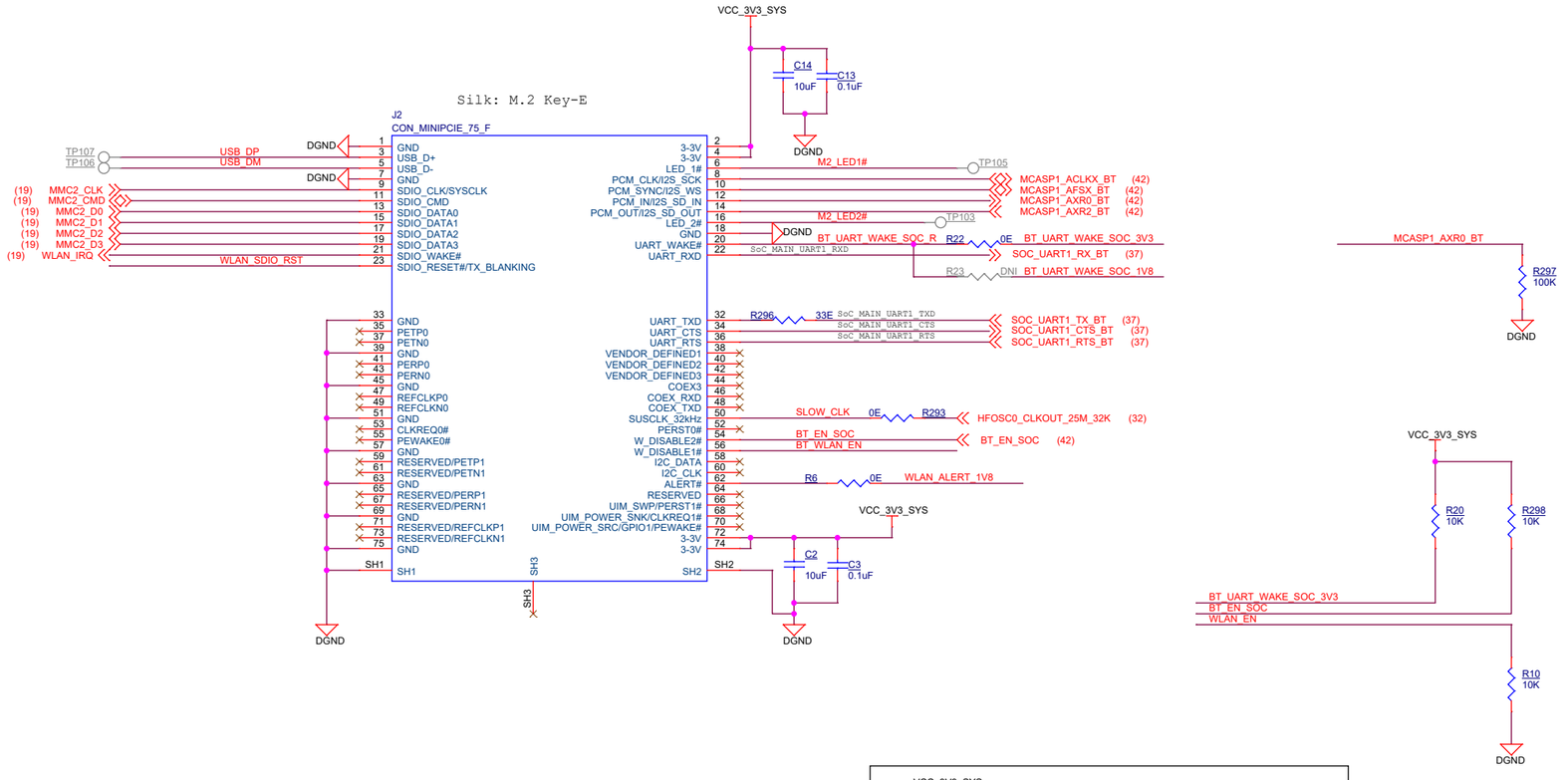
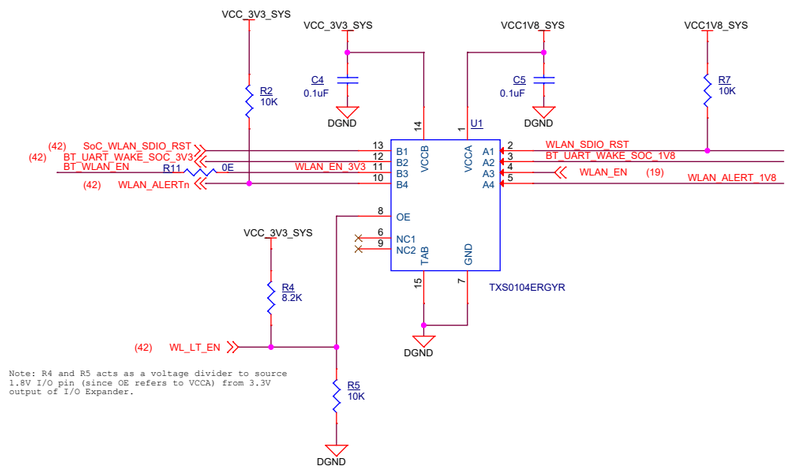
Title	SOC LPDDR4 INTERFACE	
Size C	PROC164E1-1	Rev E1-1
Date: Friday, December 01, 2023	Sheet 17 of 47	

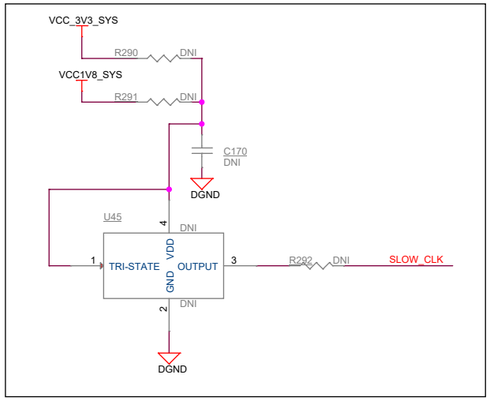
M.2 INTERFACE - SDIO

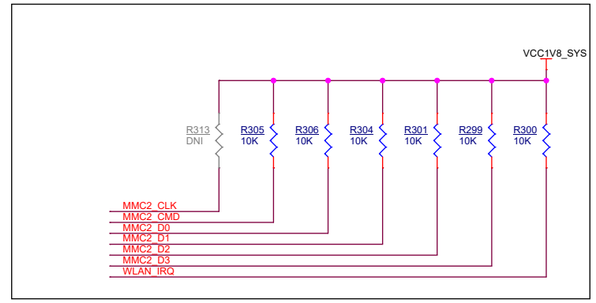


M.2 LEVEL TRANSLATOR



Note: R4 and R5 acts as a voltage divider to source 1.8V I/O pin (since OE refers to VCCA) from 3.3V output of I/O Expander.





BT_WLAN_EN DNI R9 WLAN_EN

LVCMOS 1.8V option for WLAN_EN

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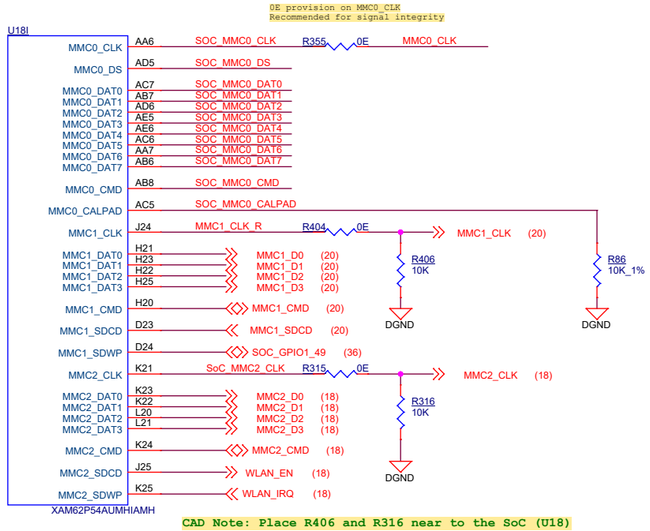
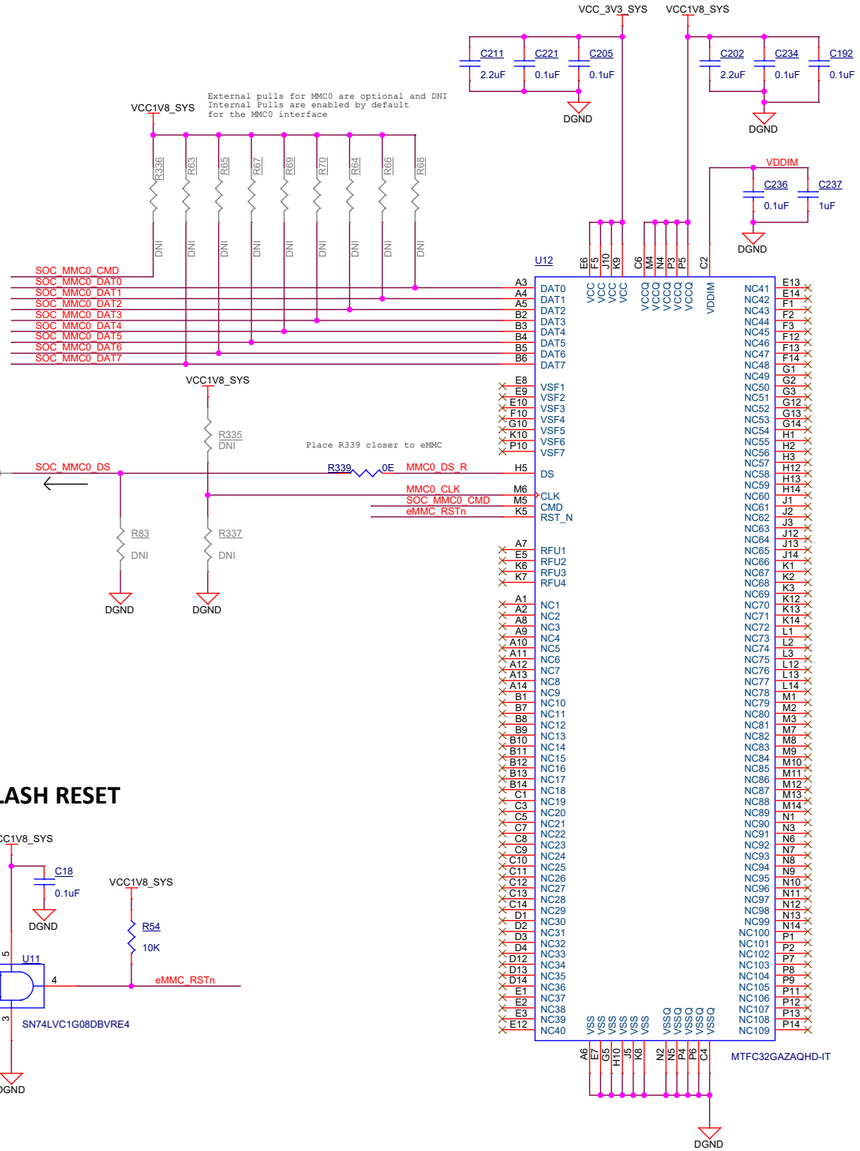
Title	M.2 CONNECTOR I/F		
Size	PROC164E1-1		Rev
C			E1-1
Date:	Thursday, November 16, 2023	Sheet 18 of 47	

SOC - MMC Interface

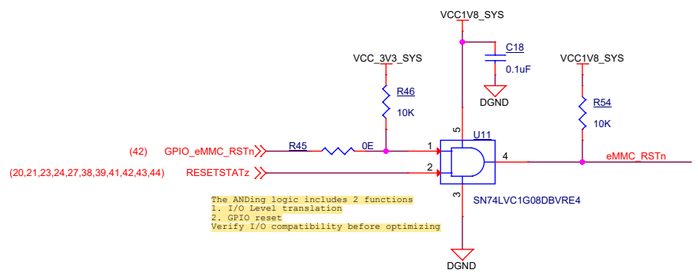


CAD Note: Place R406 and R316 near to the SoC (U18)

eMMC FLASH



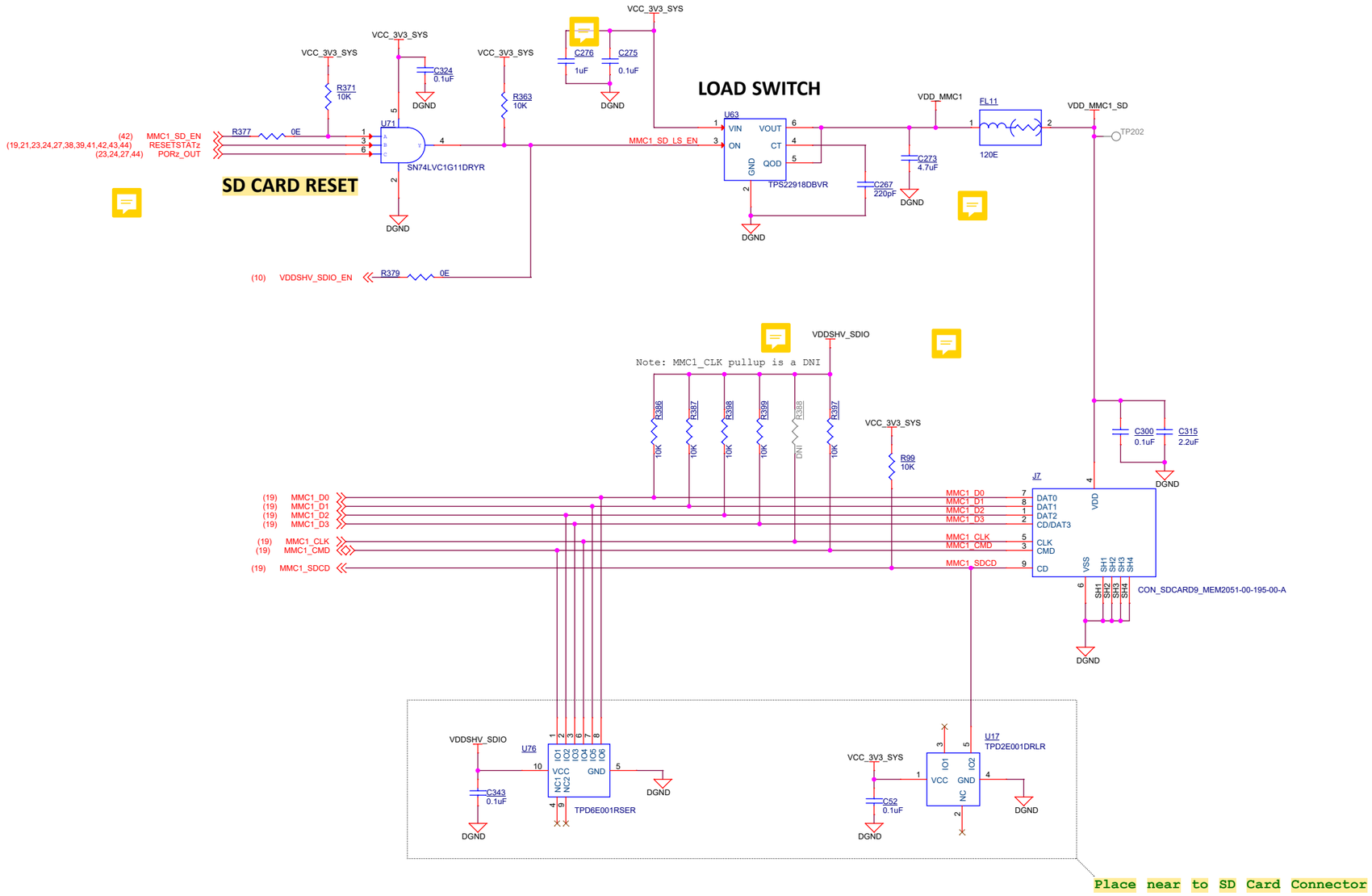
eMMC FLASH RESET



Designed for TI by Mistral Solutions Pvt Ltd

Title	eMMC FLASH INTERFACE	
Size C	PROC164E1-1	Rev E1-1
Date: Friday, December 01, 2023	Sheet 19 of 47	

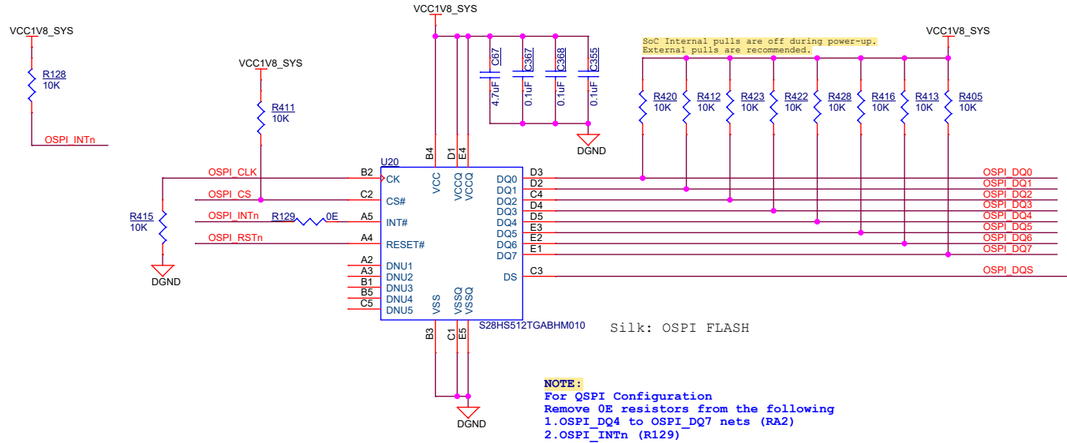
SD CARD INTERFACE



Designed for TI by Mistral Solutions Pvt Ltd

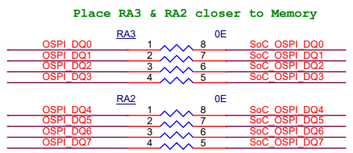
Title	SD CARD INTERFACE	
Size C	PROC164E1-1	Rev E1-1
Date: Friday, December 01, 2023	Sheet 20 of 47	

OSPI FLASH



NOTE:
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (RA2)
2.OSPI_INTn (R129)
OSPI NOR Flash can be replaced with the Footprint compatible OCTAL NAND Flash (Mfr Part# W35N01JWTBAG)

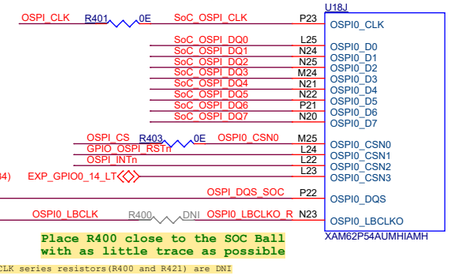
Place RA3 & RA2 closer to Memory



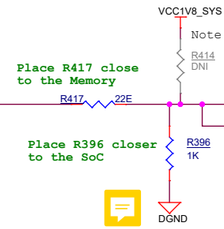
These series resistors are for enabling OSPI and QSPI
These are specific to SK and optional if the interface is fixed

SOC OSPI INTERFACE

Recommended 0E provision on
OSPI0 clock for signal integrity

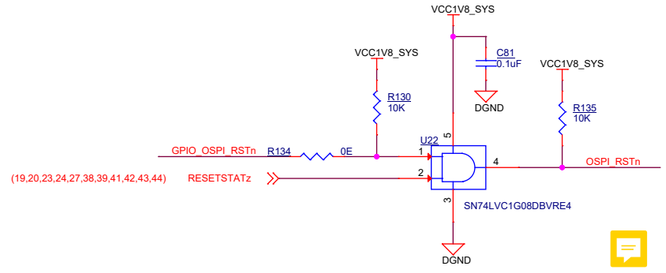


OSPIO_LBCLK series resistors(R400 and R421) are DNI



Place R400 close to the SOC Ball with as little trace as possible

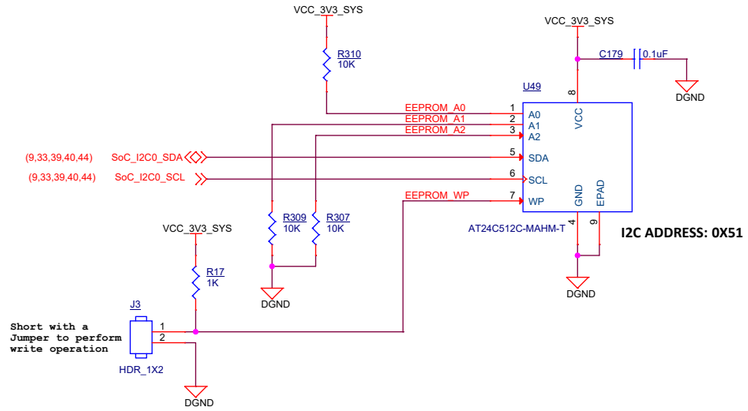
OSPI FLASH RESET



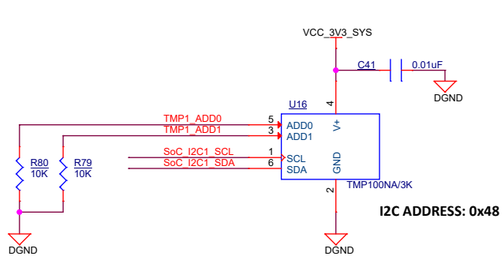
Designed for TI by Mistral Solutions Pvt Ltd

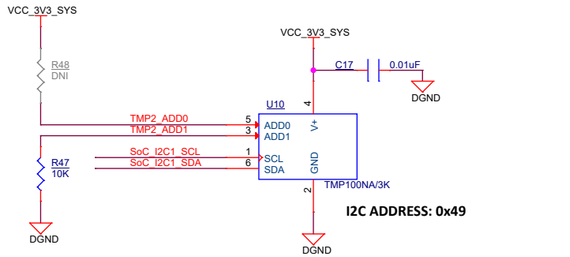
Title	OSPI INTERFACE	
Size: C	PROC164E1-1	Rev: E1-1
Date: Friday, December 01, 2023	Sheet 21 of 47	

BOARD ID EEPROM



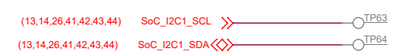
TEMPERATURE SENSORS





CAD NOTE: PLACE TEMP SENSOR U16 CLOSE TO SoC

CAD NOTE: PLACE TEMP SENSOR U10 CLOSE TO LPDDR4

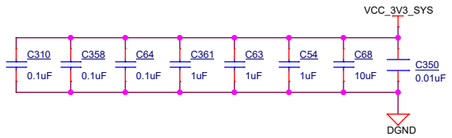


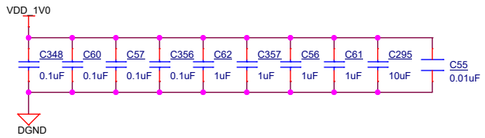
Silk: SOC_I2C1

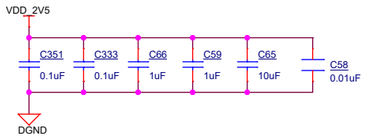
Designed for TI by Mistral Solutions Pvt Ltd

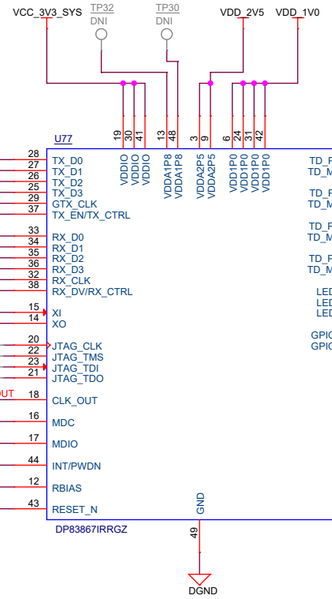
Title	BOARD ID EEPROM & TEMPERATURE SENSORS		
Size C	PROC164E1-1		Rev E1-1
Date: Thursday, November 16, 2023		Sheet 22 of 47	

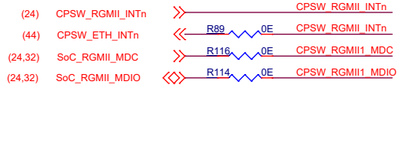
CPSW3G RGMII 1 - PHY

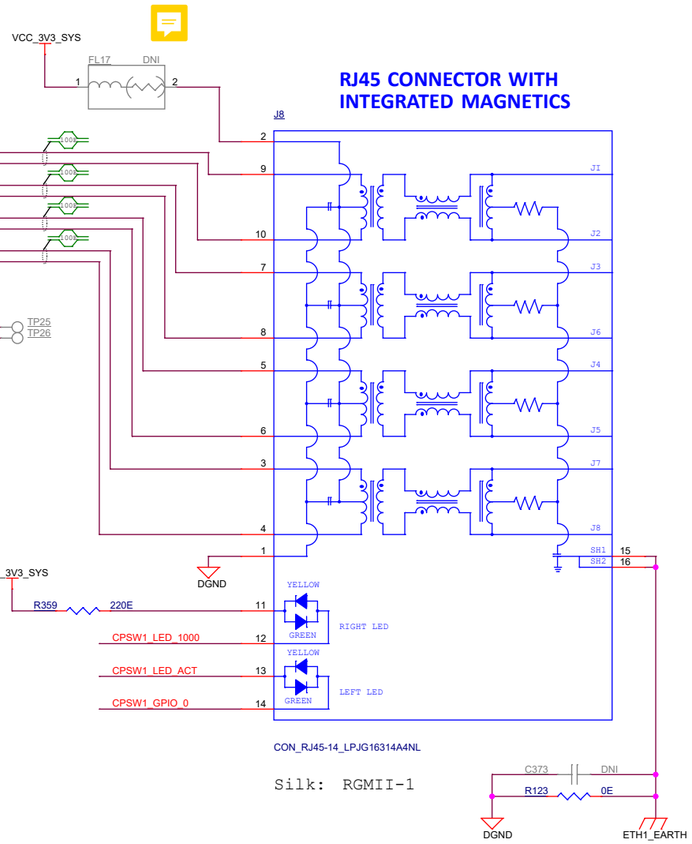


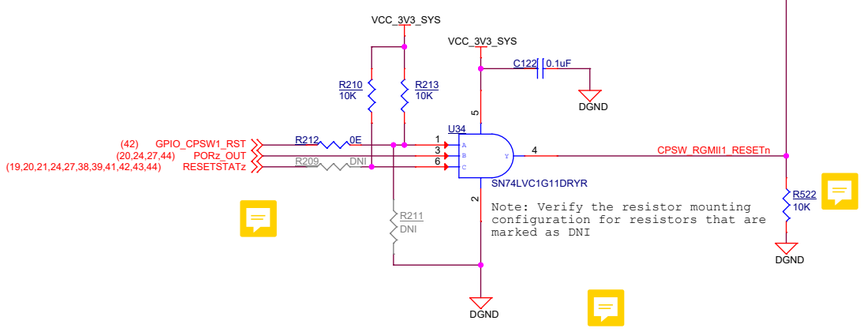


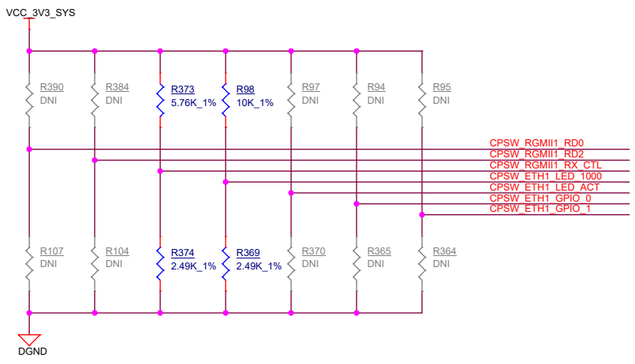


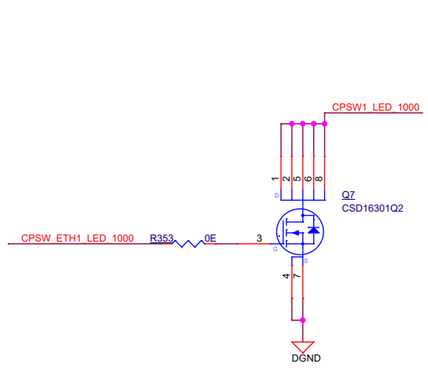


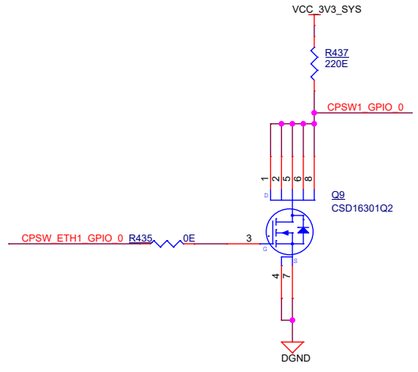


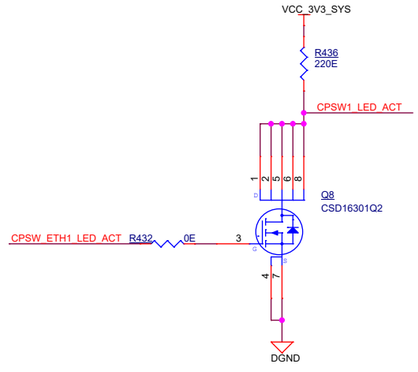












PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW3G RGMII 1 - PHY	
Size C	PROC164E1-1	Rev E1-1
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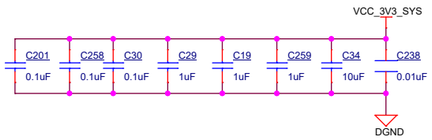
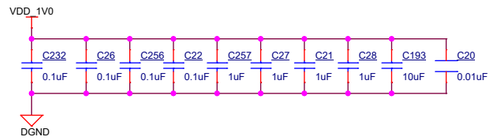
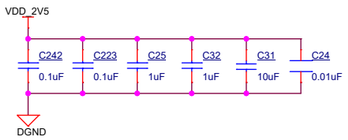
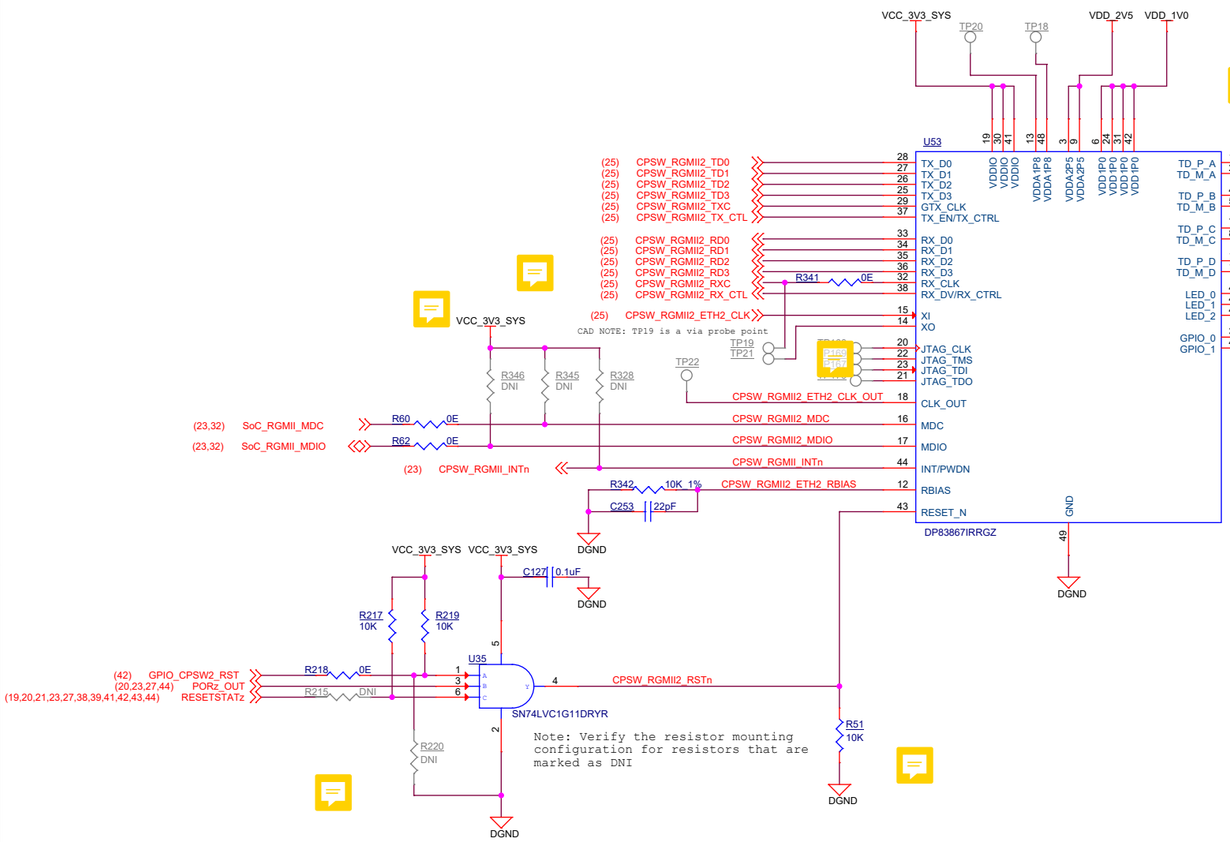
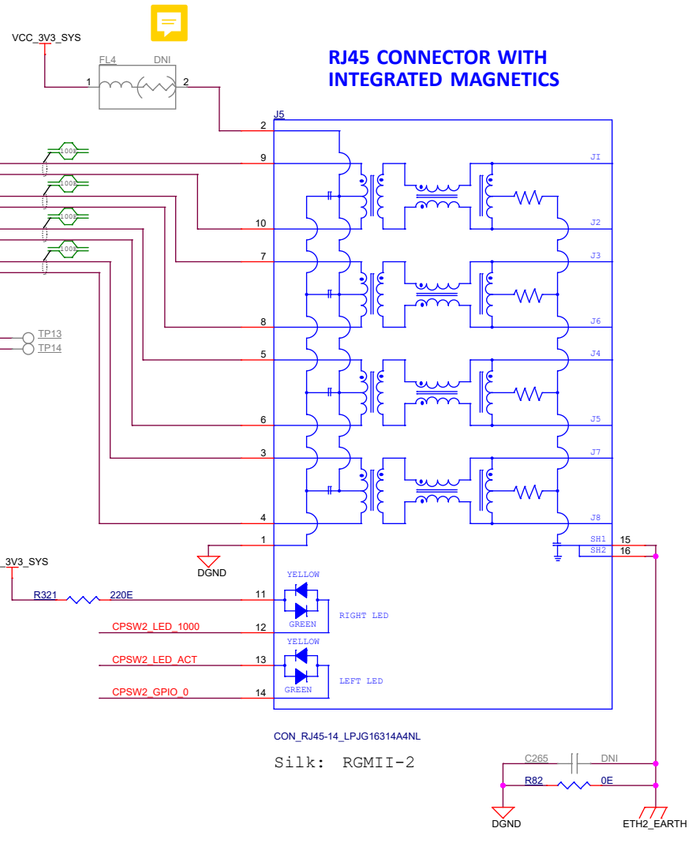
CPSW3G RGMII 2 - PHY

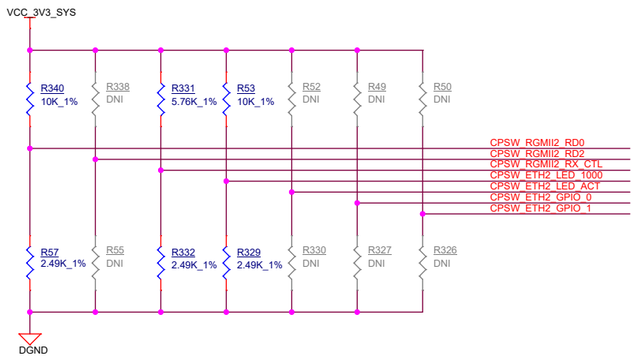


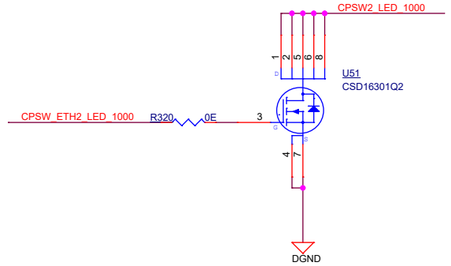


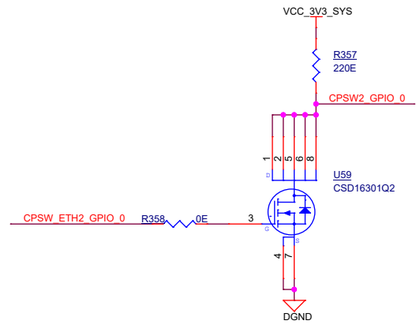


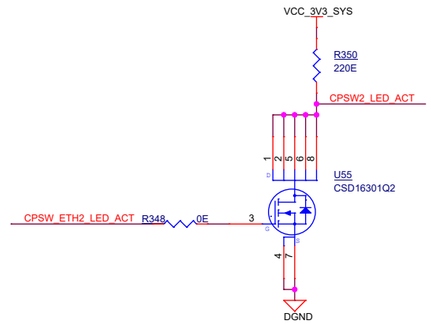












PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW3G RGMII 2 - PHY	
Size C	PROC164E1-1	Rev E1-1
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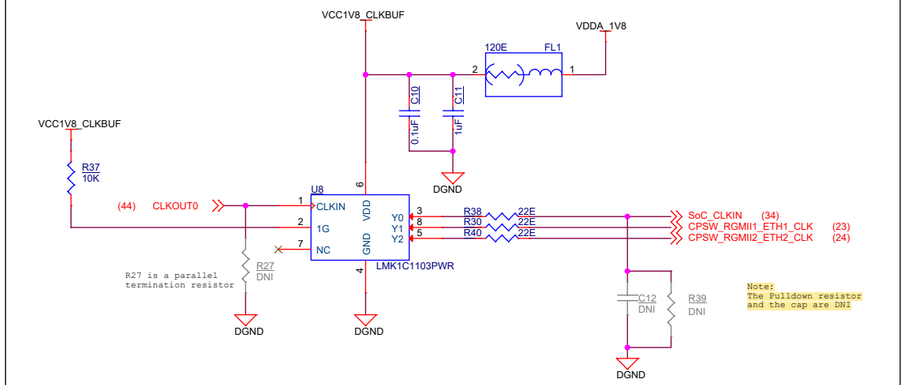
SOC CPSW3G ETHERNET INTERFACE

SOC & ETHERNET PHY CLOCK BUFFER



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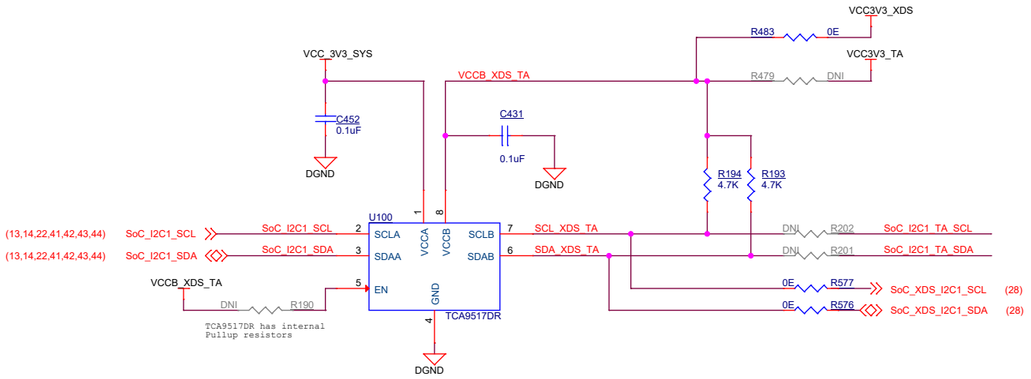
Title	ETHERNET PHY CLOCK BUFFER & LED DRIVER	
Size C	PROC164E1-1	Rev E1-1
Date: Friday, December 01, 2023	Sheet 25 of 47	

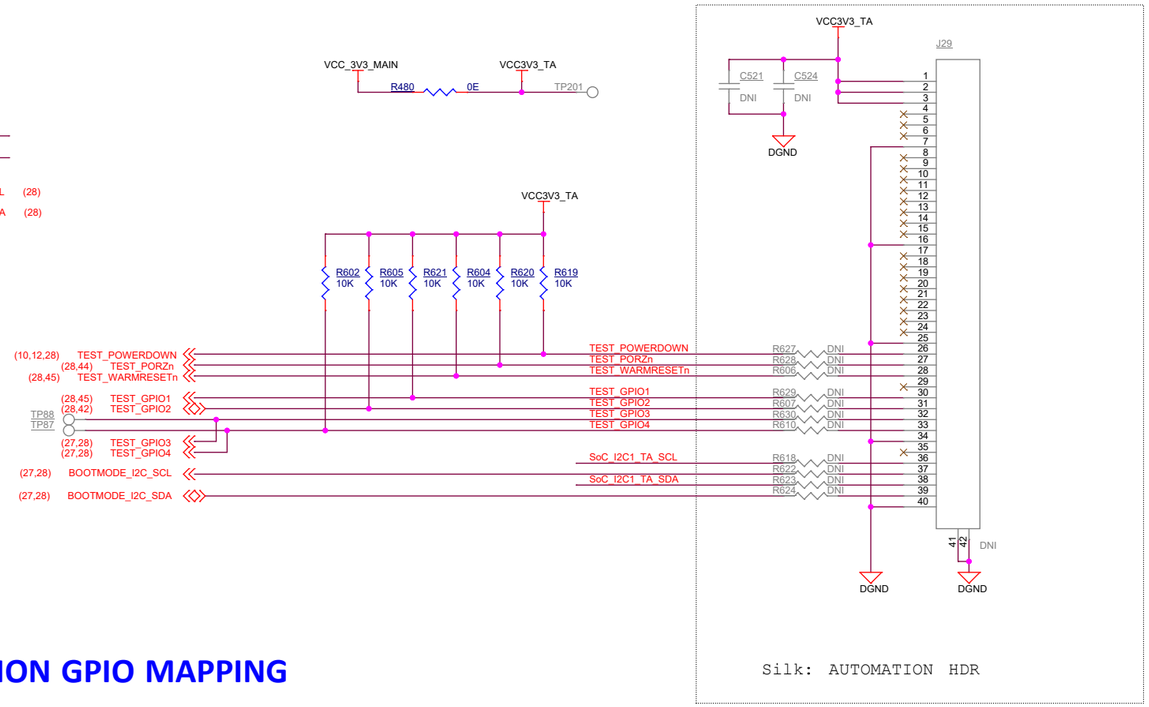
I2C BUS BUFFER



TA Header Configuration

Mount : R201, R202, R479
Demount: R483, R576, R577

40-PIN TEST AUTOMATION HEADER



Silk: AUTOMATION HDR

TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

Designed for TI by Mistral Solutions Pvt Ltd

Title	TEST AUTOMATION		
Size	PROC164E1-1		Rev
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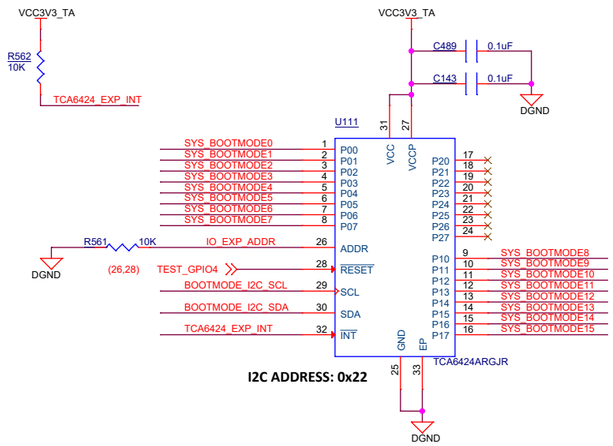
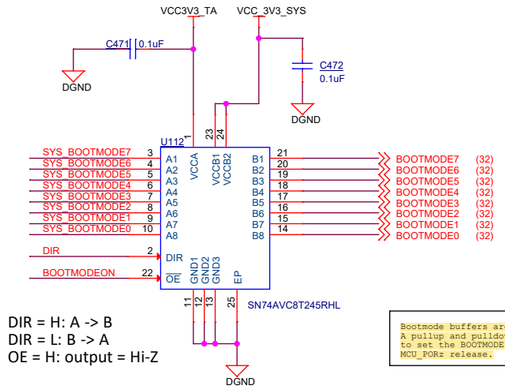
BOOTMODE IO EXPANDER



(26,28) BOOTMODE_I2C_SCL — TP86

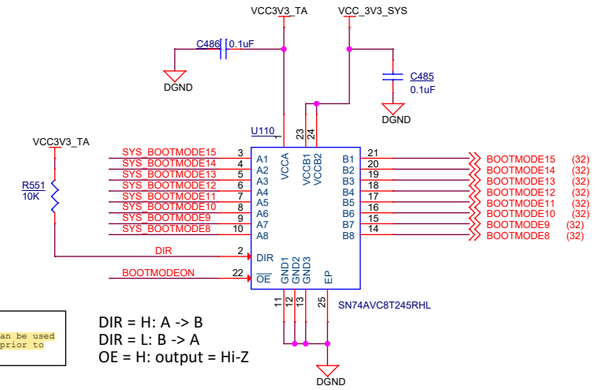
(26,28) BOOTMODE_I2C_SDA — TP96

BOOT MODE BUFFERS

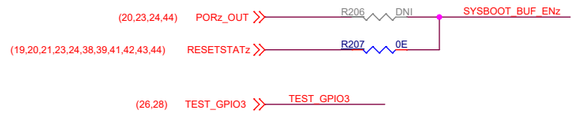


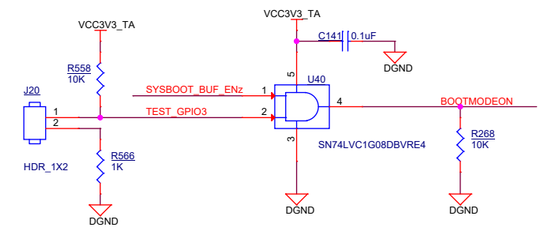
DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z

Bootmode buffers are optional.
A pullup and pulldown resistor can be used to set the BOOTMODE input state prior to MCU_PORz release.



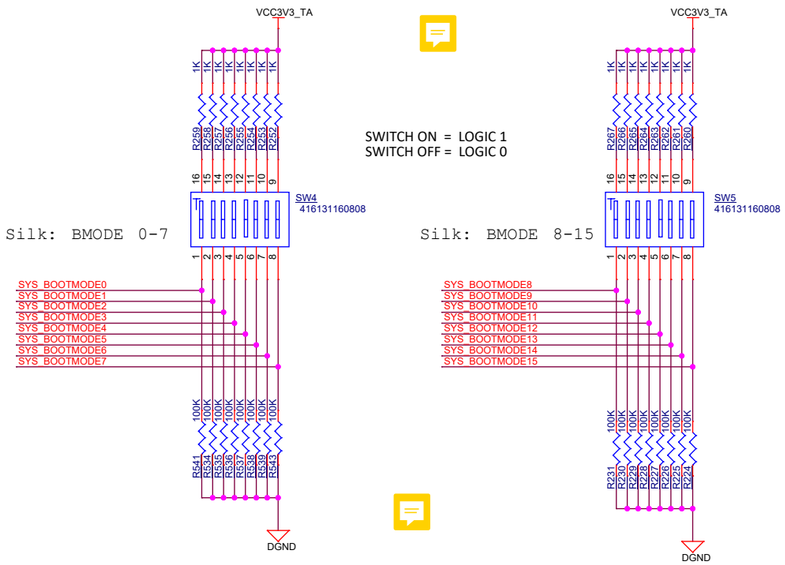
DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z





BOOT MODE SWITCHES

Note: VCC3V3_TA supply is used for test automation.
Connect SoC_DVDD3V3 in the custom board design when buffers are not used



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

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Title	BOOT MODE BUFFER & SWITCHES		
Size C	PROC164E1-1		Rev E1-1
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XDS110 DEBUGGER

TP98 DNI
SILK SCREEN : XDS_USB_VBUS
XDS_USB_VBUS
C156 4.7uF
D10 TPD1E10B06DPYR
C501 2.2uF
R579 0E
U116
IN1 IN2 EN GND PAD OUT1 OUT2 NR/FB NC
TPS79601DRBR
R560 51K_1%
C487 15pF
C492 1uF
R559 30K_1%
VCC3V3_XDS
TP90 DNI
SILK SCREEN : VCC3V3_XDS
U42B
TM4C1294NCPDTT3R
C500 1uF
C514 0.1uF
C148 0.1uF
C157 0.01uF
C151 0.01uF
C167 0.01uF
C168 1uF
C165 0.01uF
C155 2.2uF
C154 1uF
C495 0.1uF
VDDC_1V2
R250 49.9E_1%
C145 0.1uF

Silk: JTAG

J22
CON_MUSB-B_5_F
XDS_USB_DM
XDS_USB_DP
XDS_USB_ID
R273 0E
C160 DNI
XDS_SHIELD
C519 0.1uF
U126
TPD4E004DRYR
This pulls provides a defined logic state to the Test Automation signals before XDS110 firmware is loaded

U42A
TM4C1294NCPDTT3R
XDS110_TCK
XDS110_TMS
XDS110_TDO
XDS110_TDI
XDS110_TRST#
TM4C129_TCK
TM4C129_TMS
TM4C129_TDI
TM4C129_TDO
R567 100E_1%
R251 DNI
C144 0.1uF
R286 30K
R287 20K_1%
R284 220E
R289 220E
LD9 150080VS75000 GREEN
LD10 150040RS73220 RED
XDS110_EMU0
XDS110_EMU1
BUF_BOOTMODE_I2C_SCL
BUF_BOOTMODE_I2C_SDA
SoC_XDS_I2C1_SDA
SoC_XDS_I2C1_SCL
XDS_USB_DP
XDS_USB_DM
BUF_TEST_POWERDOWN
BUF_TEST_PORZn
BUF_TEST_WARMRESETn
BUF_TEST_GPIO1
BUF_TEST_GPIO2
BUF_TEST_GPIO3
BUF_TEST_GPIO4

R281 DNI
R282 DNI
XDS110_EMU0
XDS110_EMU1

R600 1K_1%
R597 1K_1%
R592 1K_1%
R586 1K_1%
R279 DNI
R277 DNI
R276 DNI
R272 DNI
Sets the unique ID of the Debugger

VCC3V3_XDS
C133 0.1uF
U39
SN74LVC07ADGVR
Open Drain Buffer for Test Automation using XDS110
R555 0E XDS_GPIO1
R554 0E XDS_GPIO3
R553 0E XDS_GPIO4
R245 0E XDS_PORZn
R238 0E XDS_WARMRESETn
R236 0E XDS_POWERDOWN
TEST_GPIO1
TEST_GPIO3
TEST_GPIO4
TEST_PORZn
TEST_WARMRESETn
TEST_POWERDOWN
R568 10K
R569 10K
R561 10K
R239 10K
R237 10K
R235 10K

VCC3V3_TA
C481 0.1uF
C482 0.1uF
U113
TXS0102DQER
Bidirectional Translator for Test Automation using XDS110
R552 0E XDS_GPIO2
TEST_GPIO2
TP197
TP198
R556 10K
R564 1K
R563 10K
GPIO2_BUF_EN
This pulldown provides a defined logic state when VCC3V3_XDS is not sourced

R578 10K
TP89
R587 DNI
XDS_RSTn
U42C
TM4C1294NCPDTT3R
XDS_VREF
R288 4.7K
OSC0
OSC1
C147 12pF
C146 12pF
Y3 16.000MHz
R280 4.87K_1%
C162 0.01uF
C166 0.1uF
U44
LM4040B25IDCKR

R547 4.7K
R549 4.7K
C480 0.1uF
R548 1K
BOOTMODE_I2C_EN
U109
TCA9517DR
C479 0.1uF
R616 4.7K
R633 4.7K
R550 0E
R546 0E
BOOTMODE_I2C_SCL
BOOTMODE_I2C_SDA

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Title	XDS110 DEBUGGER	
Size C	PROC164E1-1	Rev E1-1
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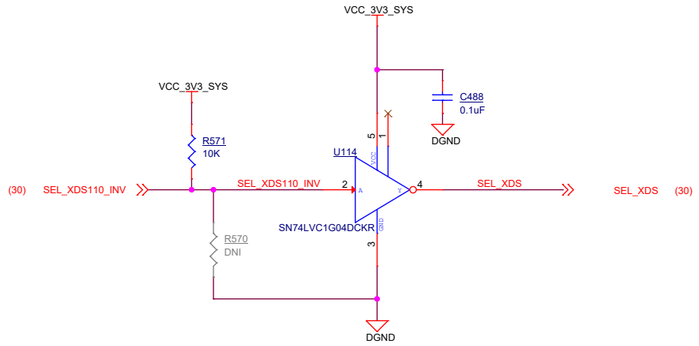
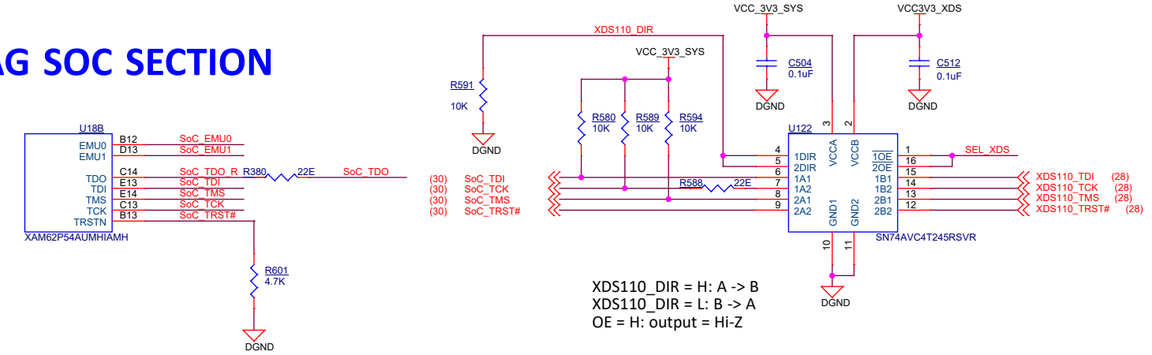
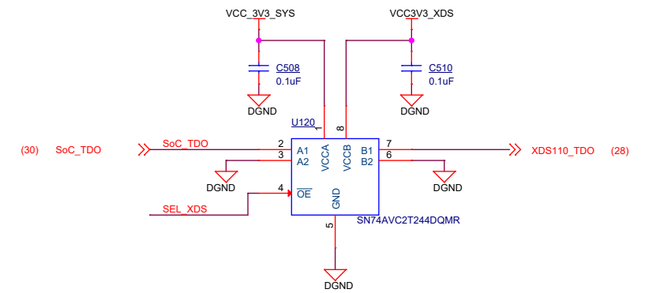
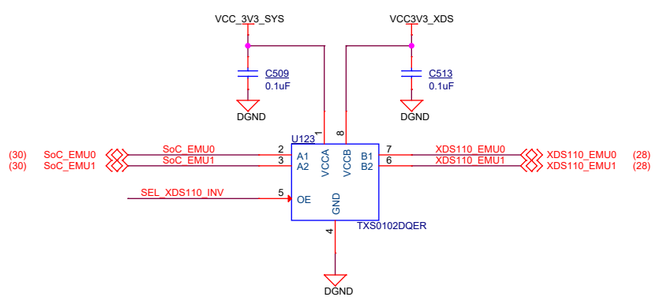


BUFFER XDS110

JTAG SOC SECTION







Designed for TI by Mistral Solutions Pvt Ltd

Title	JTAG BUFFER		
Size	PROC164E1-1		Rev
C			E1-1
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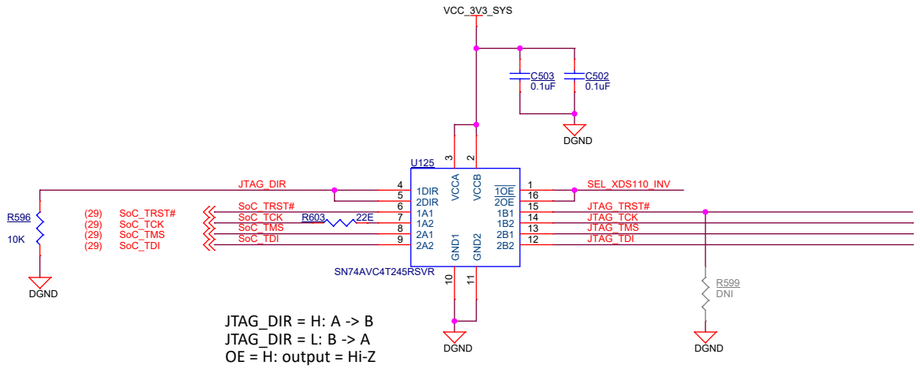
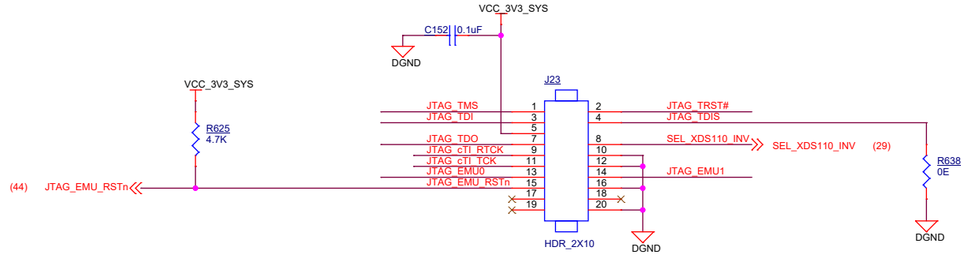
cTI20 JTAG BUFFERS

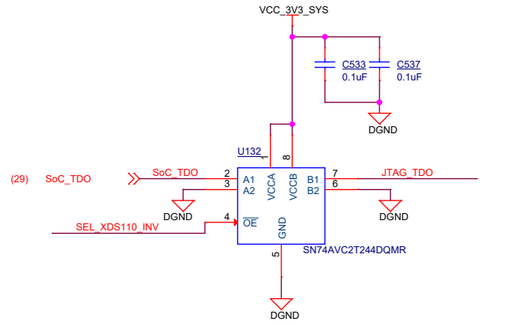


JTAG 20 PIN cTI CONNECTOR

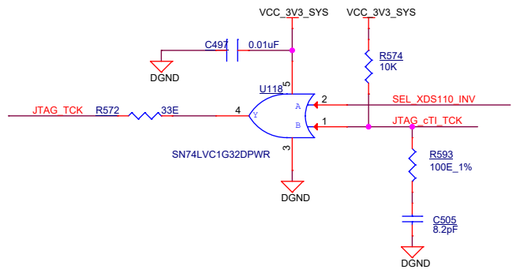


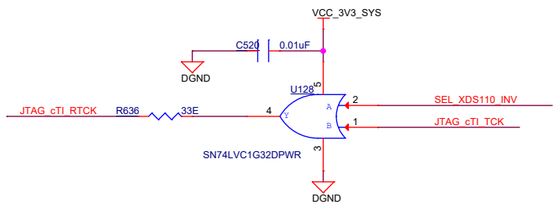
Silk: cTI

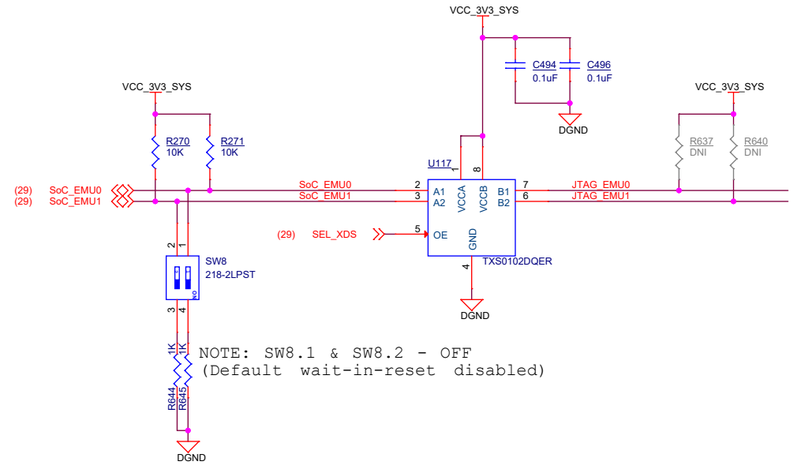
Add an external ESD protection to provide system level ESD protection



JTAG CLOCK BUFFER







NOTE: SW8.1 & SW8.2 - OFF
(Default wait-in-reset disabled)

Designed for TI by Mistral Solutions Pvt Ltd

Title	JTAG 20 PIN cTI CONNECTOR	
Size	PROC164E1-1	Rev
C		E1-1
Date: Friday, December 01, 2023	Sheet 30 of 47	

FT4232 UART

Silk: UART

FT4232_USB_VBUS
TP206
C531 10uF
C528 0.1uF
D9 TPD1E10B06DPYR
DGND

J21
CON_MUSB-B_5_F
VBUS
D-
D+
ID
GND
FT4232_USB_DM
FT4232_USB_DP
DGND

FT4232_USB_VBUS
U41 TPD2E001DRLR
IO1 IO2 VCC GND NC
C525 0.1uF
DGND

R274 0E
DGND
UART_SHIELD

VPHY_3V3_FT4232
FL18 120E
C517 0.1uF
DGND
VCC_3V3_FT4232

VPLL_3V3_FT4232
FL19 120E
C527 0.1uF
DGND
VCC_3V3_FT4232

VCC_1V8_FT4232
C507 0.1uF
C159 0.1uF
C158 0.1uF
DGND

VCC_3V3_FT4232
C506 0.1uF
C153 0.1uF
C163 0.1uF
C164 0.1uF
DGND

VPHY_3V3_FT4232
VPLL_3V3_FT4232
C511 4.7uF
DGND

VPLL_3V3_FT4232
R283 10K
FT4232_RESET
C161 0.1uF
DGND

VCC_3V3_FT4232 U43

VPHY	4	
VPLL	9	
VCORE	12	
VCORE	34	
VCORE	54	
VCCIO	20	
VCCIO	31	
VCCIO	42	
VCCIO	56	
VREGIN	50	
VREGOUT	49	
DM	7	FT4232_USB_DM
DP	8	FT4232_USB_DP
REF	6	FT4232_REF
RESET	14	FT4232_RESET
EECS	63	FT4232_EECS
EECLK	62	FT4232_EECLK
EEDATA	61	FT4232_EEDATA
OSCI	2	
OSCO	3	
TEST	13	
PWREN SUSPEND	60	FT_PWREN#
AGND	10	
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8	1 11 15 25 35 41 51	

R626 12K_1%
DGND

C149 18pF
C150 18pF
Y4 12.000MHz
DGND

ADBUS0 16 FT4232_SOC_UART0_RX_3V3
ADBUS1 17 FT4232_SOC_UART0_TX_3V3
ADBUS2 18
ADBUS3 19
ADBUS4 21
ADBUS5 22
ADBUS6 23
ADBUS7 24

BDBUS0 26 FT4232_SOC_UART1_RX_3V3
BDBUS1 27 FT4232_SOC_UART1_TX_3V3
BDBUS2 28 FT4232_SOC_UART1_CTS_3V3
BDBUS3 29 FT4232_SOC_UART1_RTS_3V3
BDBUS4 30
BDBUS5 32
BDBUS6 33
BDBUS7 34

CDBUS0 38 FT4232_WKUP_UART0_RX_3V3
CDBUS1 39 FT4232_WKUP_UART0_TX_3V3
CDBUS2 40 FT4232_WKUP_UART0_CTS_3V3
CDBUS3 41 FT4232_WKUP_UART0_RTS_3V3
CDBUS4 43
CDBUS5 44
CDBUS6 45
CDBUS7 46

DDBUS0 48 FT4232_MCU_UART0_RX_3V3
DDBUS1 52 FT4232_MCU_UART0_TX_3V3
DDBUS2 53 FT4232_MCU_UART0_CTS_3V3
DDBUS3 54 FT4232_MCU_UART0_RTS_3V3
DDBUS4 55
DDBUS5 57
DDBUS6 58
DDBUS7 59

FT4232HL

VCC_3V3_FT4232
LD8 150080VS75000
R275 220E

VCC_3V3_FT4232
C532 0.1uF
DGND
VCC_3V3_SYS
C529 0.1uF
DGND
VCC_3V3_SYS
R635 10K
VCC_3V3_SYS
R631 4.7K
R632 4.7K

U130 SN74AVC4T245RSVR
1OE 2OE 1B1 1B2 2B1 2B2 VCCB VCCA 1DIR 2DIR 1A1 1A2 2A1 2A2 GND2 GND1
FT4232_SOC_UART0_TX_3V3
FT4232_SOC_UART0_RX_3V3
SOC_UART0_TX_3V3 (44)
SOC_UART0_RX_3V3 (44)
DGND
R634 10K
DGND

VCC_3V3_FT4232
C499 0.1uF
DGND
CAN_IO_3V3
C498 0.1uF
DGND
CAN_IO_3V3
R590 10K
CAN_IO_3V3
R598 4.7K
R278 4.7K

U121 SN74AVC4T245RSVR
1OE 2OE 1B1 1B2 2B1 2B2 VCCB VCCA 1DIR 2DIR 1A1 1A2 2A1 2A2 GND2 GND1
FT4232_MCU_UART0_TX_3V3
FT4232_MCU_UART0_RTS_3V3
FT4232_MCU_UART0_RX_3V3
FT4232_MCU_UART0_CTS_3V3
MCU_UART0_TX_3V3 (34)
MCU_UART0_RTS_3V3 (34)
MCU_UART0_RX_3V3 (34)
MCU_UART0_CTS_3V3 (34)
DGND
R595 10K
DGND

VCC_3V3_FT4232
C534 0.1uF
DGND
VCC_3V3_SYS
C535 0.1uF
DGND
VCC_3V3_SYS
R639 10K
VCC_3V3_SYS
R642 4.7K
VCC_3V3_SYS
R285 4.7K

U133 SN74AVC4T245RSVR
1OE 2OE 1B1 1B2 2B1 2B2 VCCB VCCA 1DIR 2DIR 1A1 1A2 2A1 2A2 GND2 GND1
FT4232_SOC_UART1_TX_3V3
FT4232_SOC_UART1_RTS_3V3
FT4232_SOC_UART1_RX_3V3
FT4232_SOC_UART1_CTS_3V3
SOC_UART1_TXD (37)
SOC_UART1_RTS (37)
SOC_UART1_RXD (37)
SOC_UART1_CTS (37)
DGND
R641 10K
DGND

TP102 TXD
TP200 RTS
TP99 RXD
TP199 CTS
SILK SCREEN : SOC_UART1

VCC_3V3_FT4232
C526 0.1uF
DGND
CAN_IO_3V3
C522 0.1uF
DGND
CAN_IO_3V3
R614 10K
CAN_IO_3V3
R609 4.7K
CAN_IO_3V3
R615 4.7K

U129 SN74AVC4T245RSVR
1OE 2OE 1B1 1B2 2B1 2B2 VCCB VCCA 1DIR 2DIR 1A1 1A2 2A1 2A2 GND2 GND1
FT4232_WKUP_UART0_TX_3V3
FT4232_WKUP_UART0_RTS_3V3
FT4232_WKUP_UART0_RX_3V3
FT4232_WKUP_UART0_CTS_3V3
WKUP_UART0_TX_3V3 (32)
WKUP_UART0_RTS_3V3 (32)
WKUP_UART0_RX_3V3 (32)
WKUP_UART0_CTS_3V3 (32)
DGND
R613 10K
DGND

FT4232: 5V to 3.3V@500mA LDO

FT4232_USB_VBUS
VCC_3V3_FT4232
U131 TPS73533DRVR
IN OUT EN NR/FB NC GND EP
C530 2.2uF
C536 0.01uF
DGND

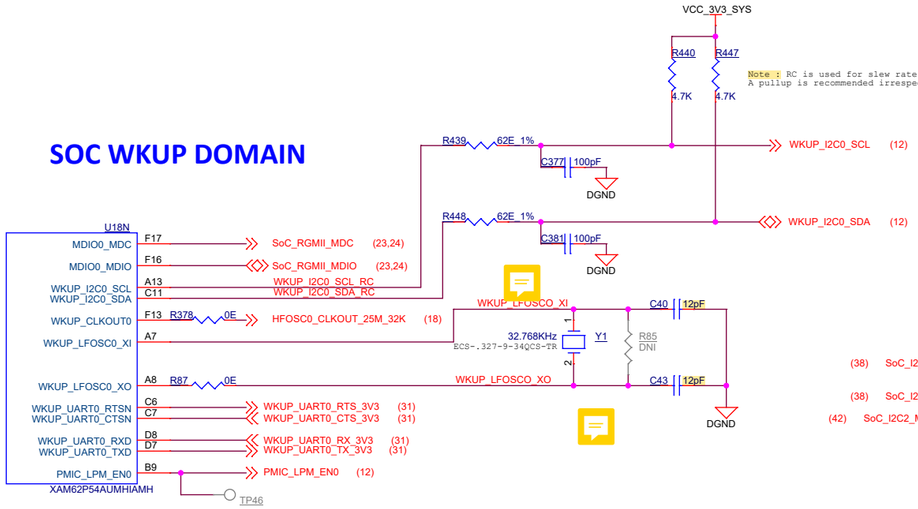
EEPROM

VCC_3V3_FT4232
R583 10K
R582 10K
R581 10K
FT4232_DO
R585 2.2K
FT4232_EEDATA
FT4232_EECLK
FT4232_EECS
VCC_3V3_FT4232
C523 0.1uF
DGND
U124 93LC46B
DI CS CLK VCC VSS DO NC1 NC2
FT4232_DO
DGND

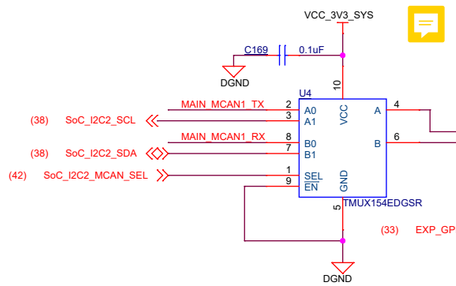
Designed for TI by Mistral Solutions Pvt Ltd

Title	FT4232 UART TO USB BRIDGE		
Size	C	PROC164E1-1	Rev E1-1
Date:	Thursday, November 16, 2023	Sheet 31 of 47	

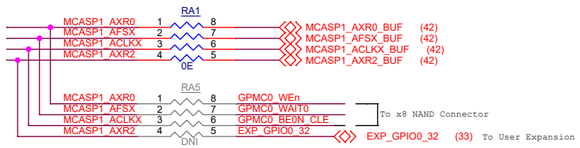
SOC WKUP DOMAIN

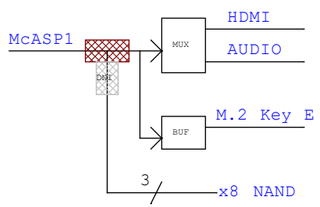


SOC I2C2/MCAN1 MUX

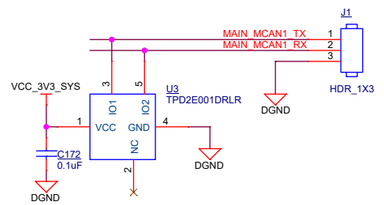


SOC GPMC

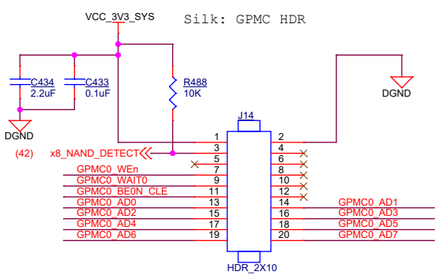




MCAN1 HEADER

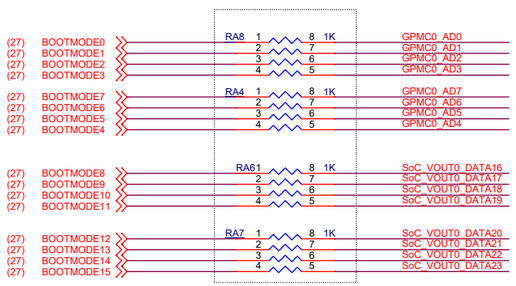


GPMC HEADER



Pulls are placed on the add-on card.
NOTE: J4, J11 & J14 will be used together when plugging in GPMC NAND (x8) Board

BOOTMODE PINS

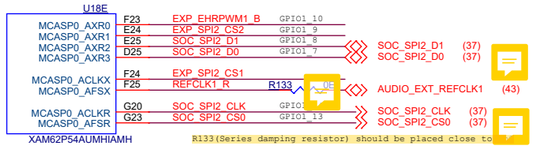


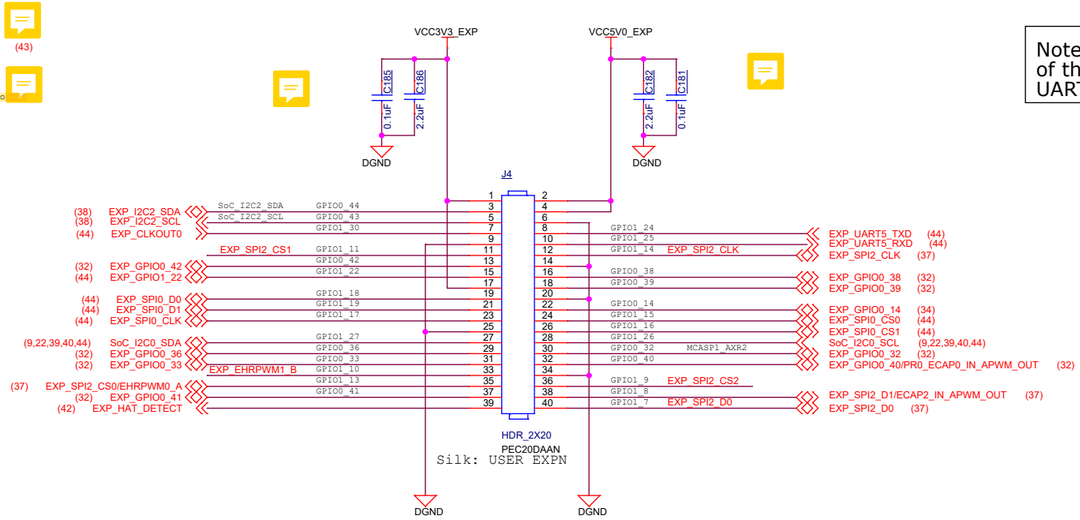
NOTE: 1K Resistor at the output of the buffer is recommended when the bootmode pins are used for alternate functions

Designed for TI by Mistral Solutions Pvt Ltd

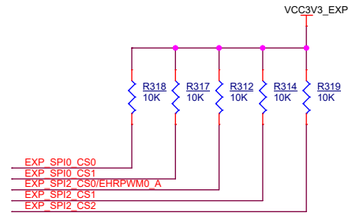
Title	SOC WKUP & GPMC		
Size	PROC164E1-1		Rev
C			E1-1
Date:	Friday, December 01, 2023	Sheet 32 of 47	

USER EXPANSION CONNECTOR

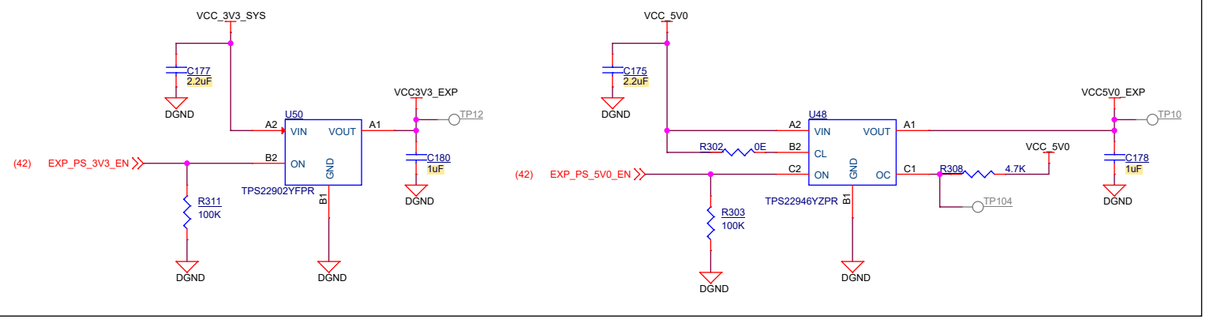




Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



LOAD SWITCHES FOR USER EXPANSION CONNECTOR



NOTE:

AM62P Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62P Starter Kit is not powered.

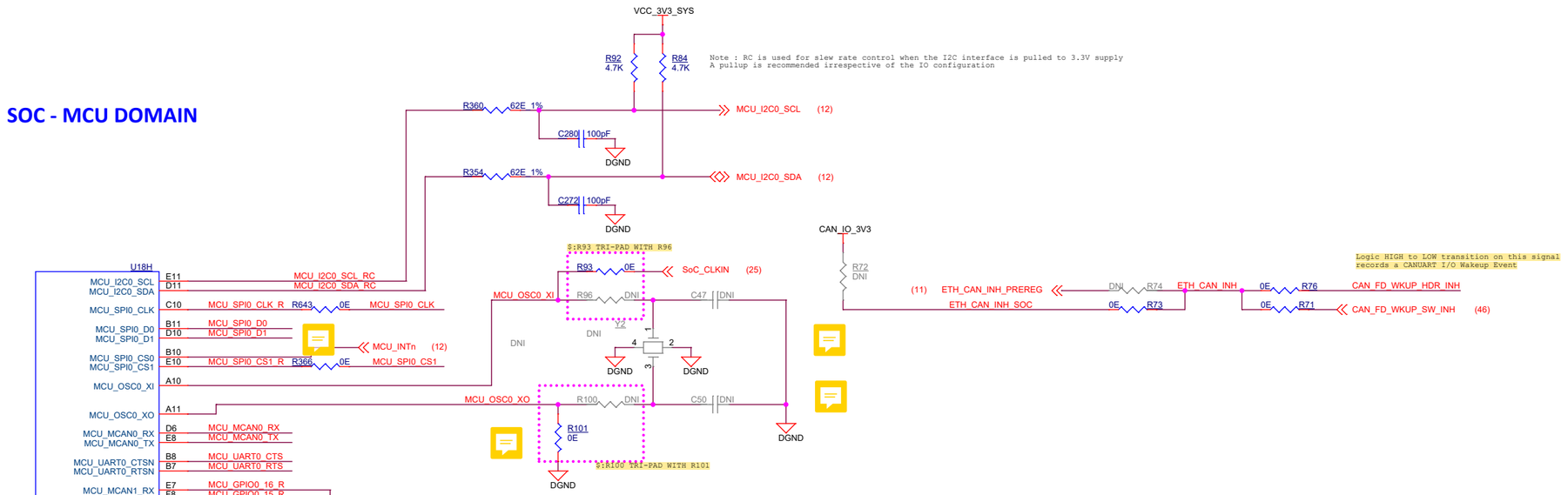
5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

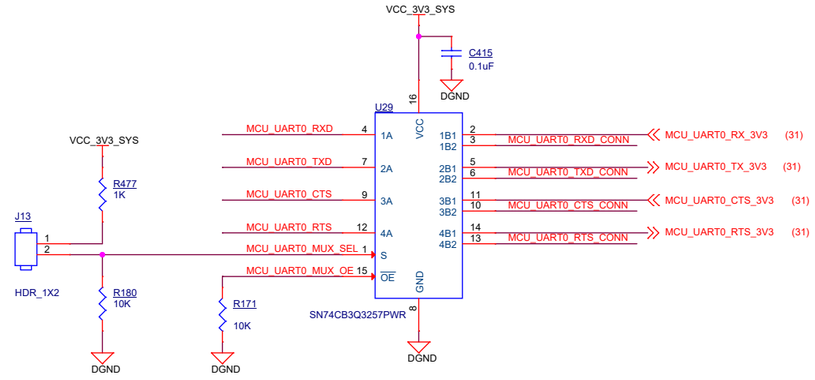
Designed for TI by Mistral Solutions Pvt Ltd

Title	USER EXPANSION CONNECTOR		
Size C	PROC164E1-1		Rev E1-1
Date: Friday, December 01, 2023		Sheet 33 of 47	

SOC - MCU DOMAIN

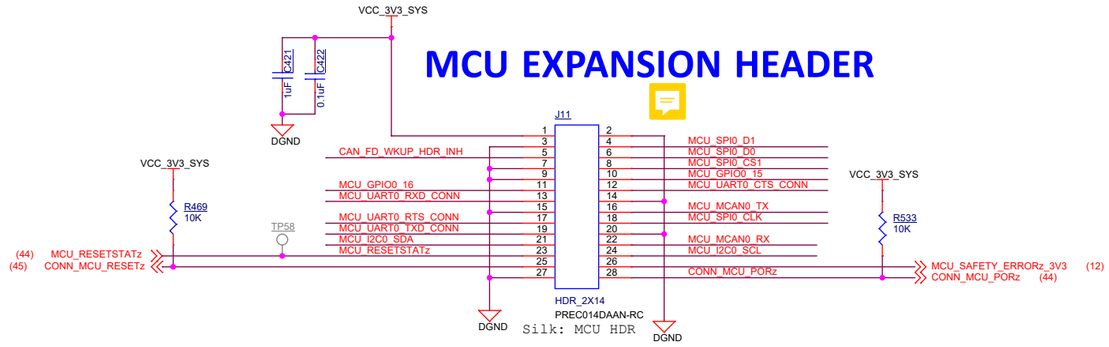


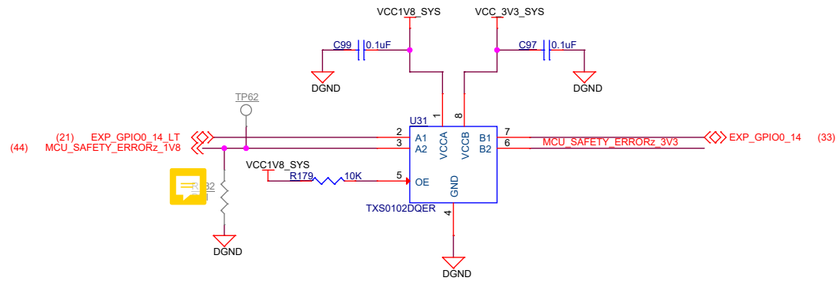
SoC MCU UART0 FET BUS SWITCH



OEn	SEL	INPUT/OUTPUT An	
L	L(DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

MCU EXPANSION HEADER

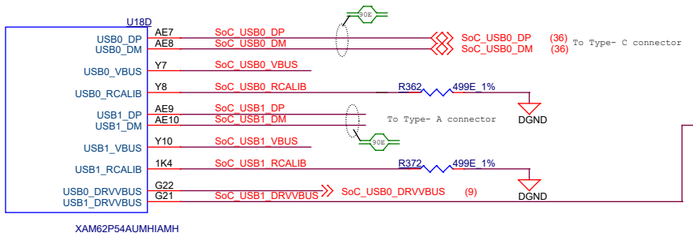


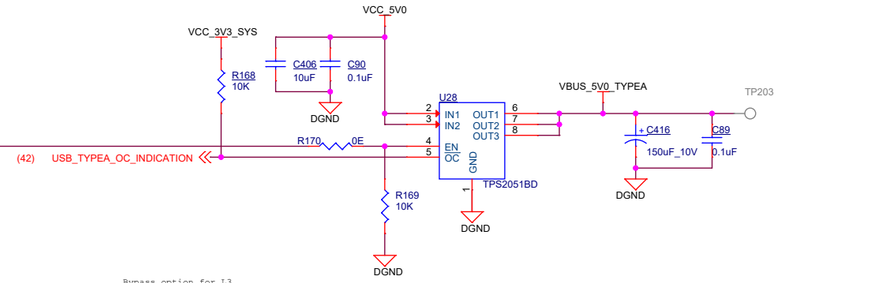


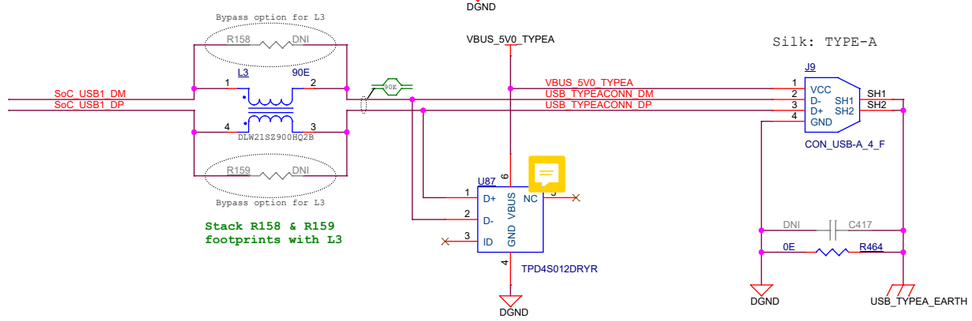
Designed for TI by Mistral Solutions Pvt Ltd

Title	MCU HEADER		
Size	C	PROC164E1-1	Rev E1-1
Date:	Friday, December 01, 2023	Sheet 34 of 47	

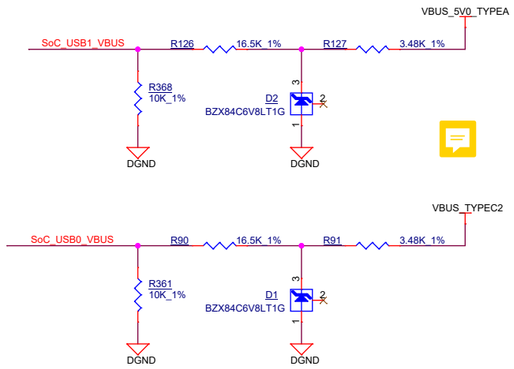
USB1 TYPE-A







Note: Refer data sheet USB VBUS Design Guidelines section.



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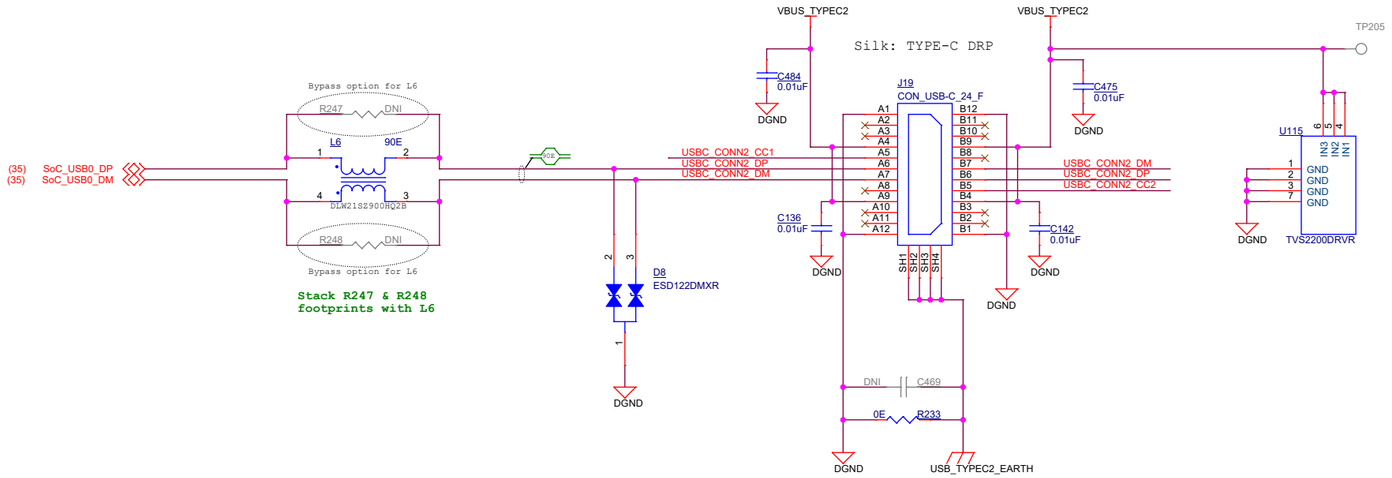
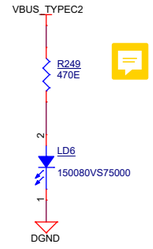
Title	USB1 TYPE-A	
Size C	PROC164E1-1	Rev E1-1
Date: Friday, December 01, 2023	Sheet 35 of 47	

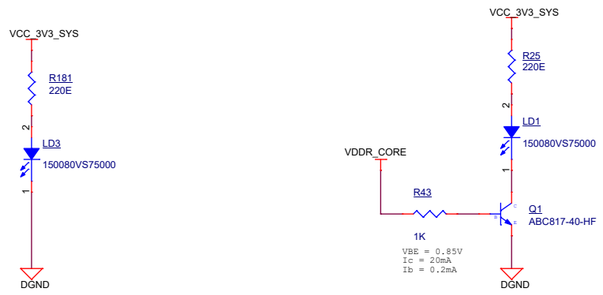
USB0 TYPE-C DRP



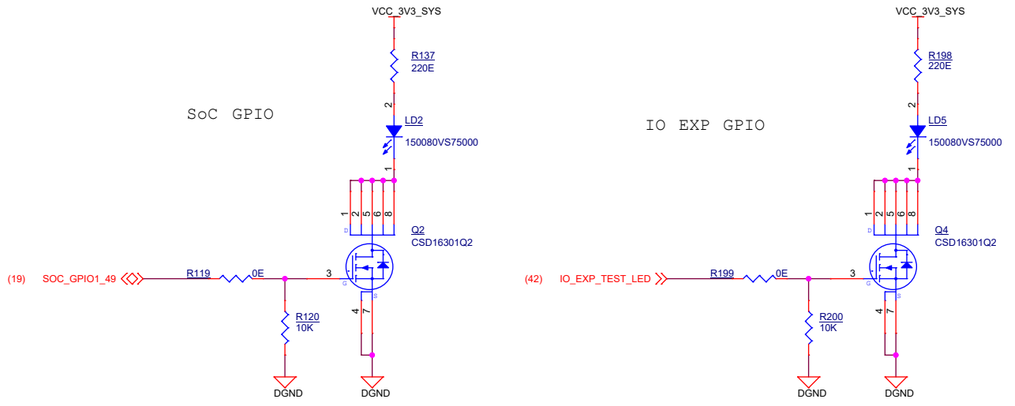
POWER INDICATION LED: VBUS_TYPEC2



POWER RAIL LEDS



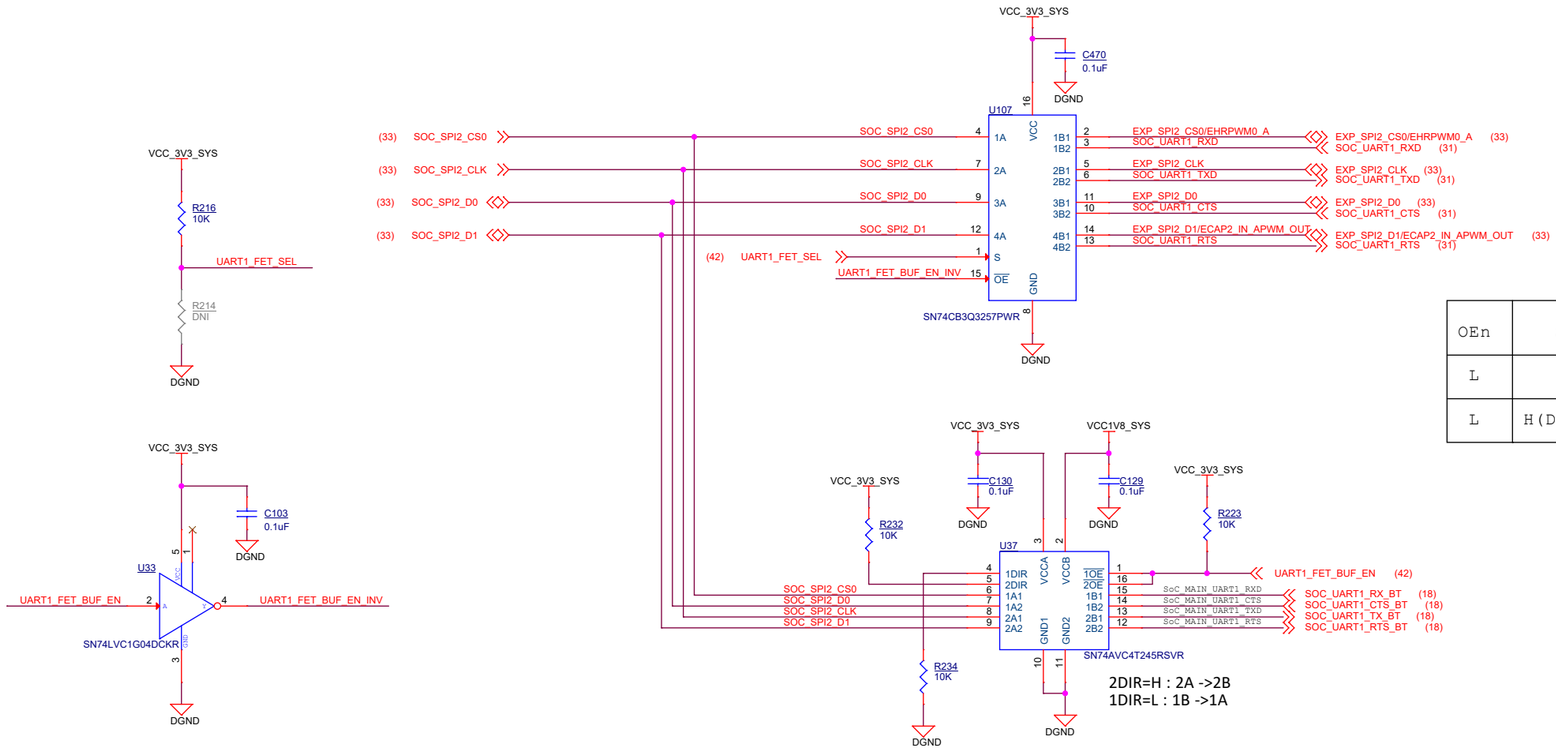
USER TEST LEDS



Designed for TI by Mistral Solutions Pvt Ltd

Title	USB0 TYPE-C DRP & USER TEST LED	
Size: C	PROC164E1-1	Rev: E1-1
Date: Thursday, November 16, 2023	Sheet 36 of 47	

SoC MAIN UART1 FET BUS SWITCH & VOLTAGE LEVEL TRANSLATOR

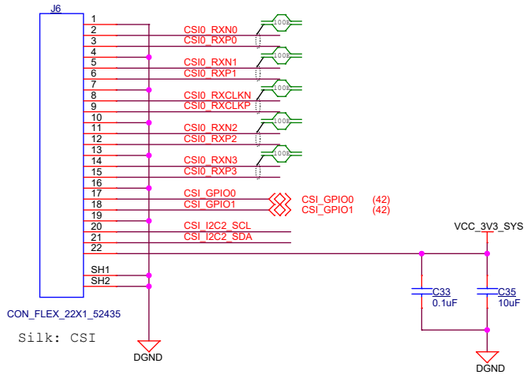


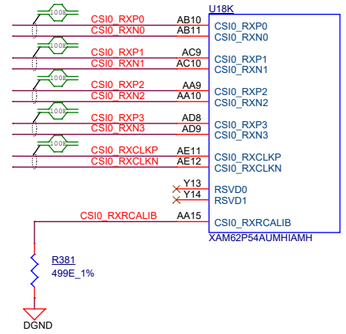
OEn	SEL	INPUT/OUTPUT An	
L	L	An=nB1	SOC - EXP CONN
L	H(DEFAULT)	An=nB2	SOC - FT4232

Designed for TI by Mistral Solutions Pvt Ltd

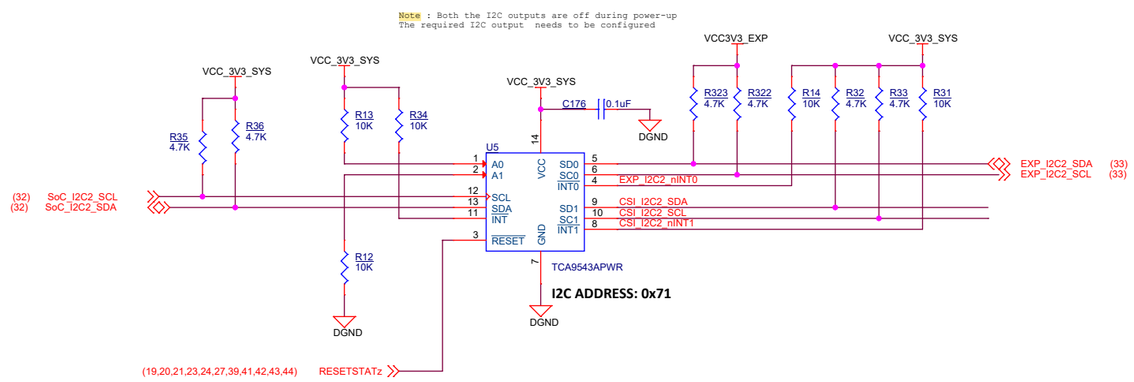
Title	SoC UART1 FET SWITCH & BUFFER		
Size	PROC164E1-1		Rev
C			E1-1
Date:	Friday, December 01, 2023	Sheet 37 of 47	

SOC CSI INTERFACE





I2C SWITCH FOR SoC MAIN I2C2



Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC CSI INTERFACE	
Size C	PROC164E1-1	Rev E1-1
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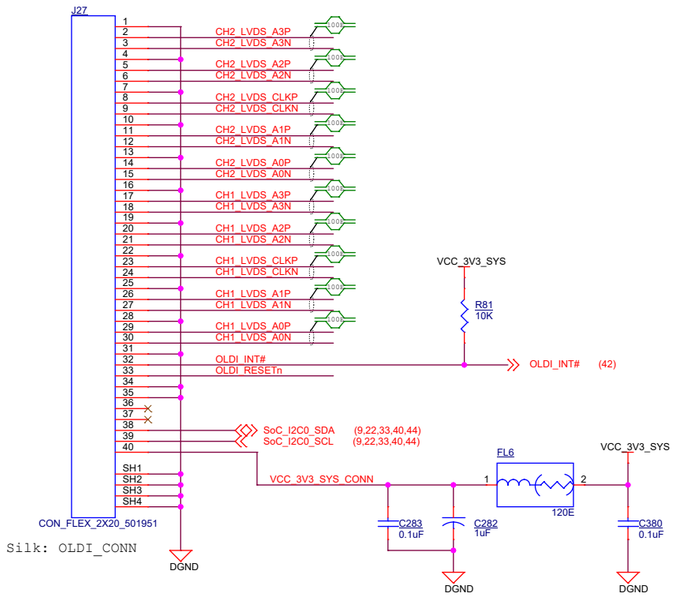
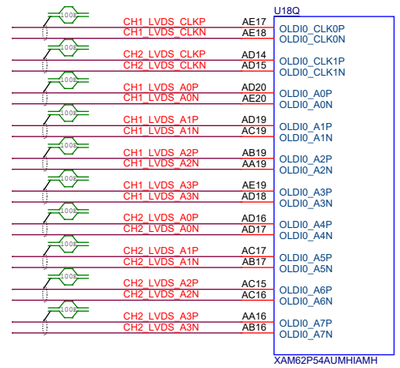
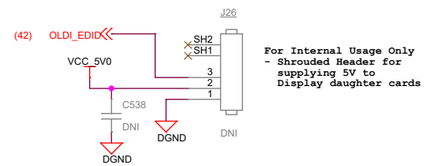
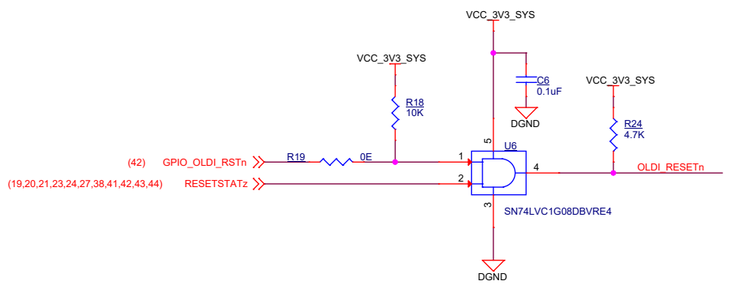
SOC OLDI INTERFACE







OLDI RESET



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Title	SOC OLDI INTERFACE	
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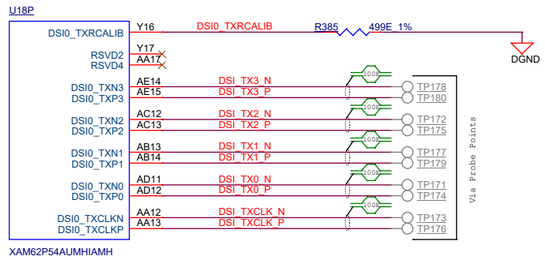
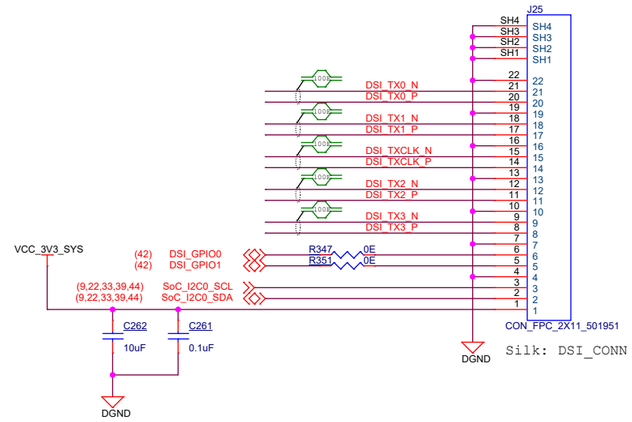
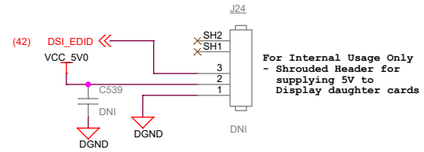
SOC DSI INTERFACE







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Title	SOC DSI INTERFACE		
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C			E1-1
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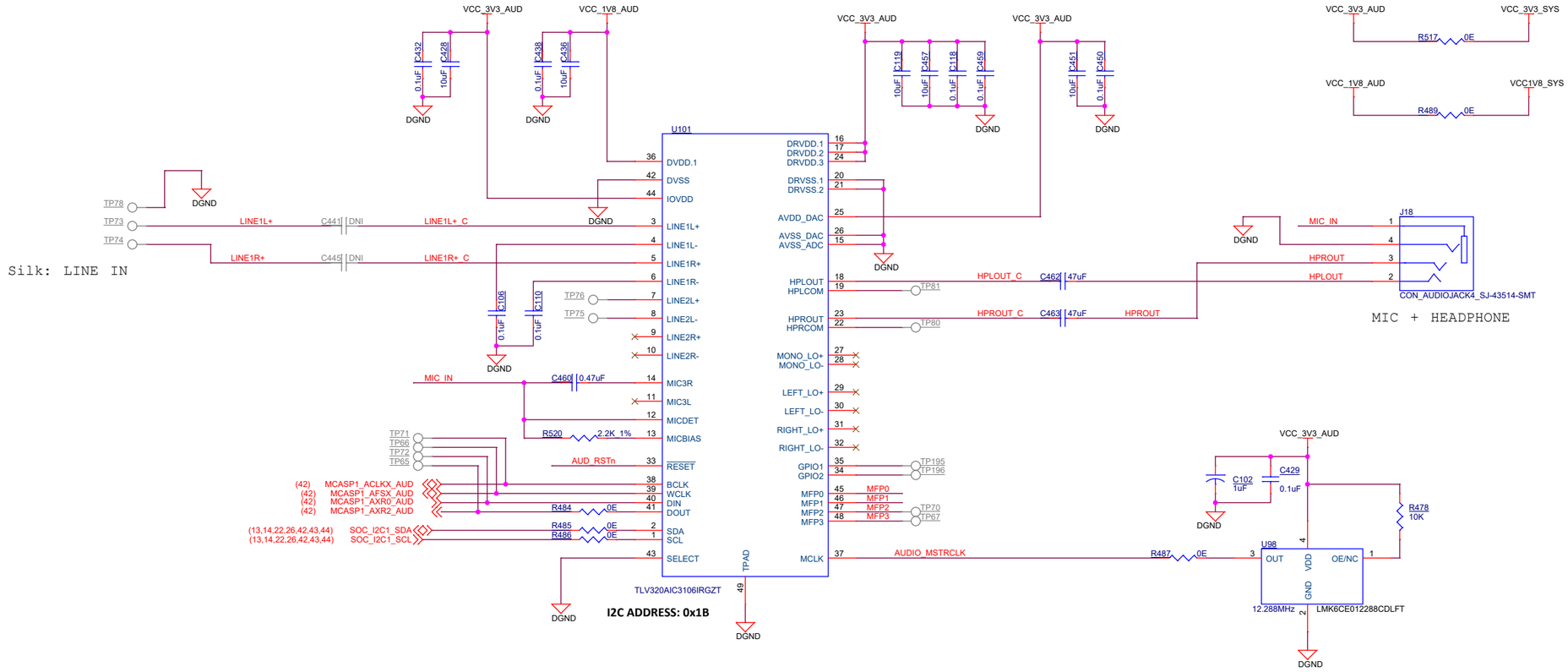
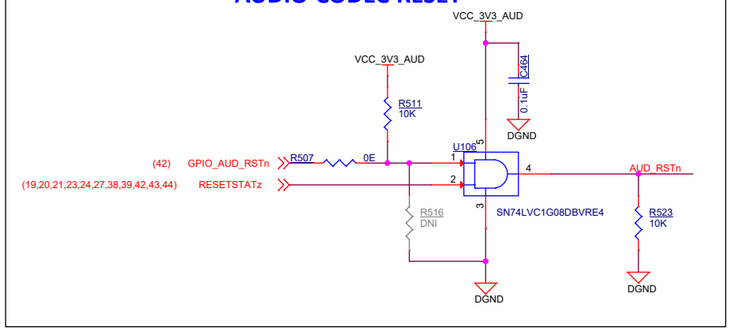
AUDIO CODEC

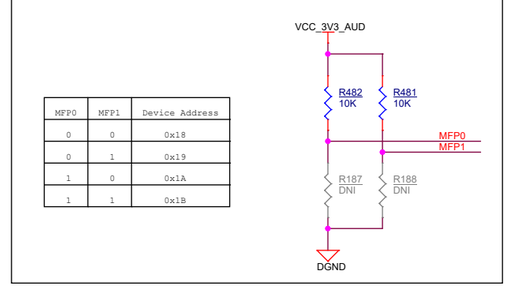


AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



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Title	AUDIO CODEC	
Size C	PROC164E1-1	Rev E1-1
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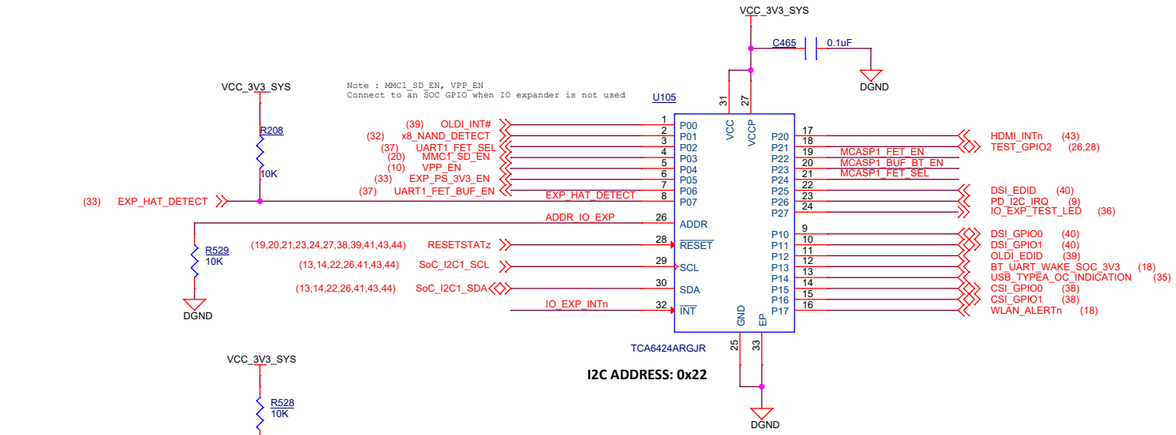
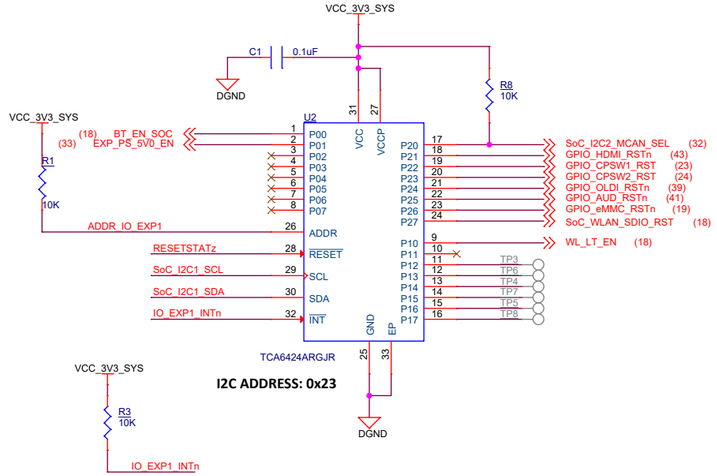
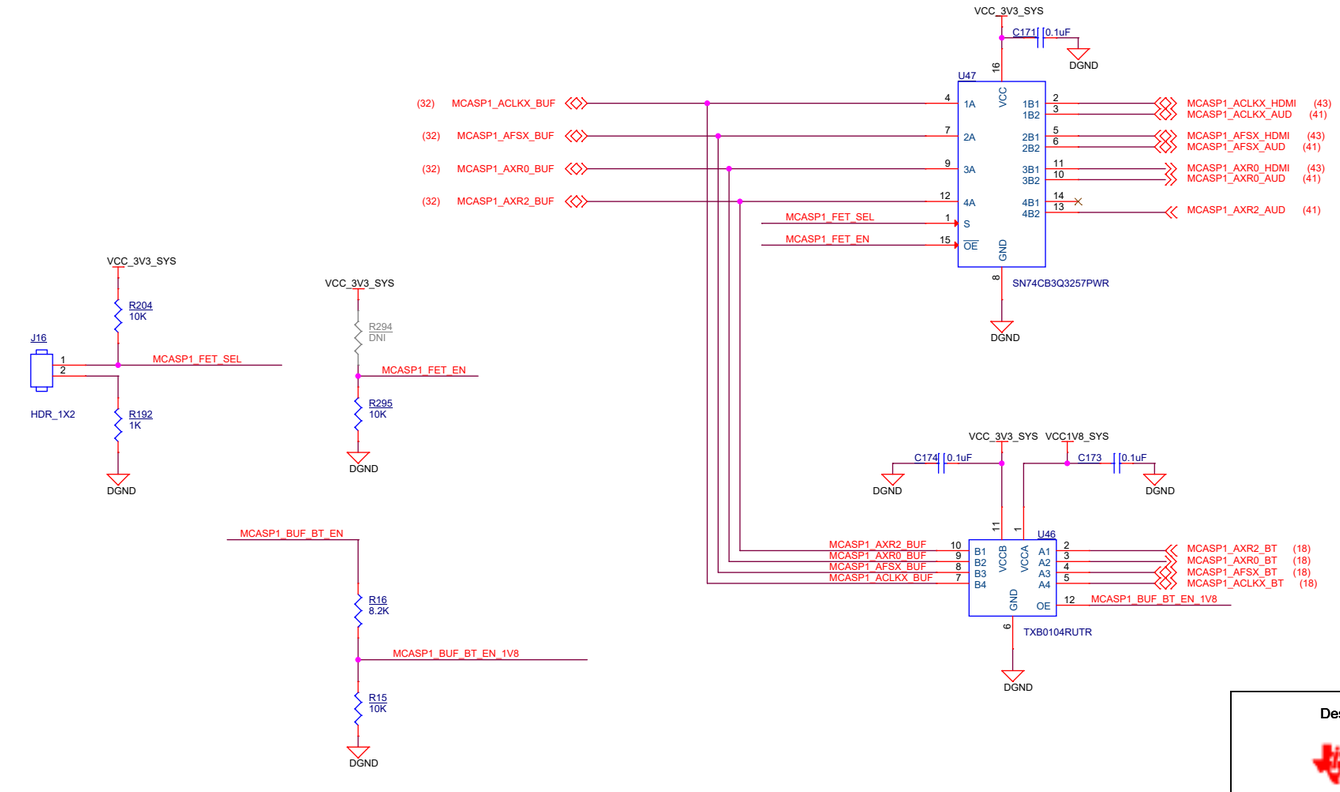
IO EXPANDER





SOC MAIN McASP1 FET BUS SWITCH & VOLTAGE LEVEL TRANSLATOR



OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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Title	IO EXPANDER	
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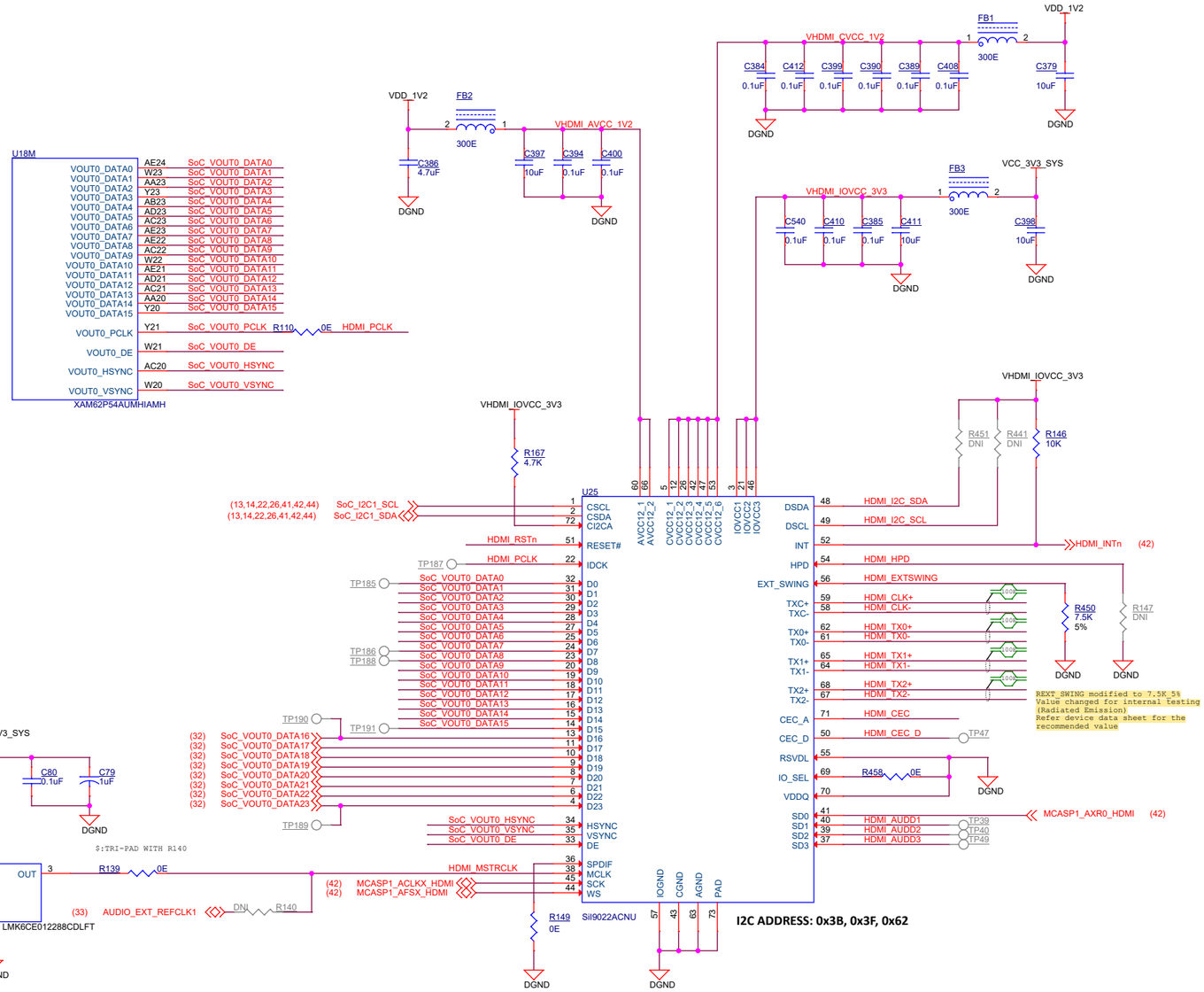
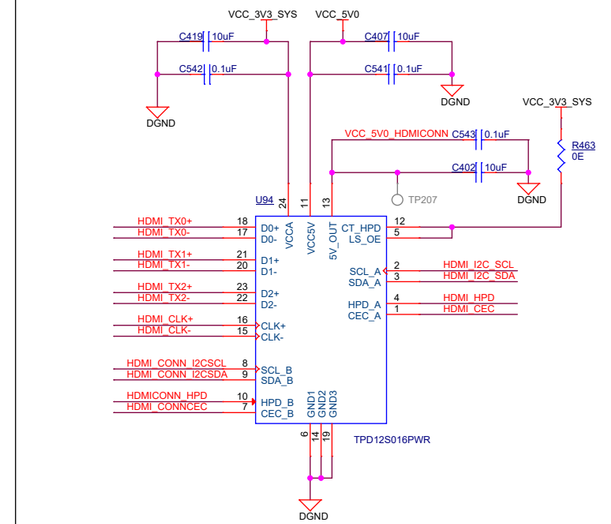
HDMI INTERFACE

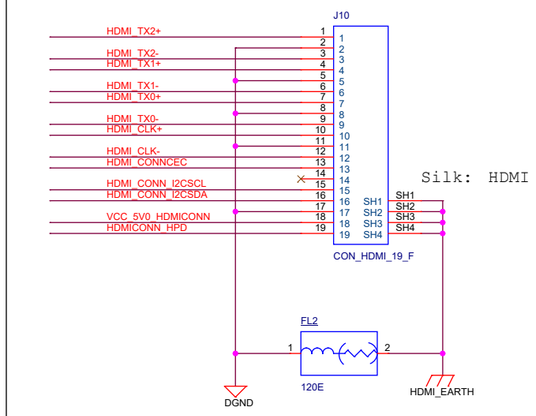


HDMI ESD DEVICE

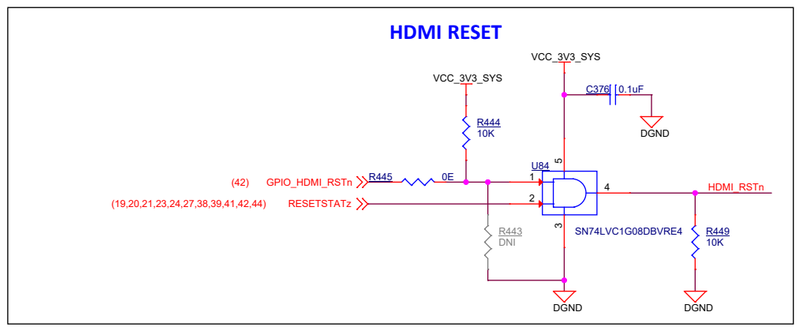


NOTE:
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR



HDMI RESET



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Title	HDMI INTERFACE		
Size	PROC164E1-1		Rev
C			E1-1
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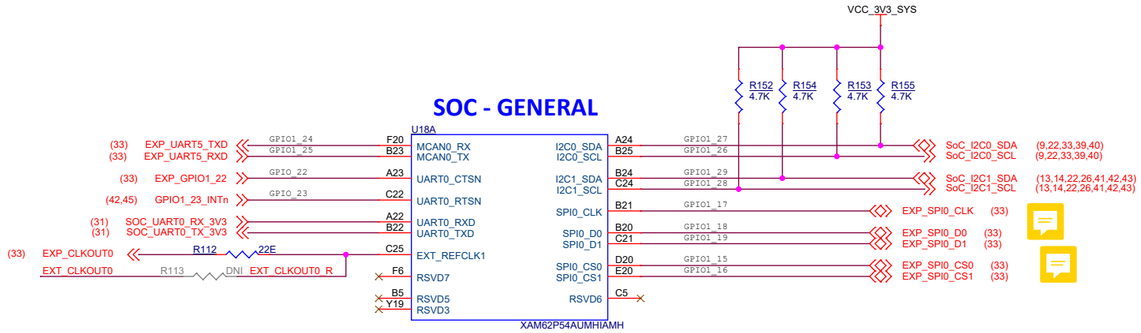
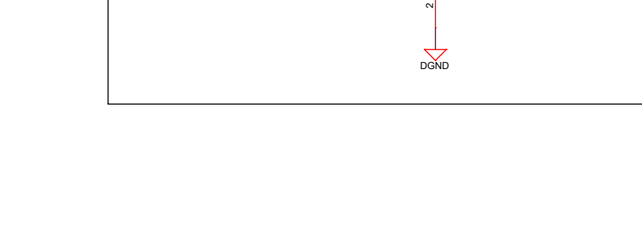
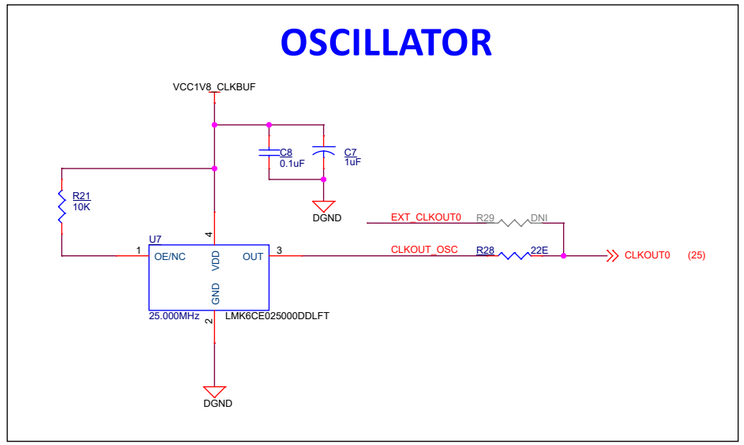
SOC - GENERAL

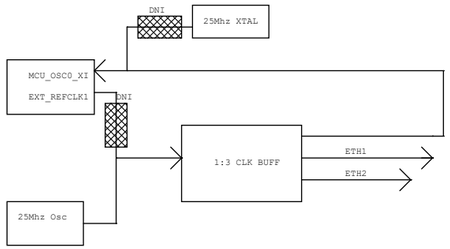


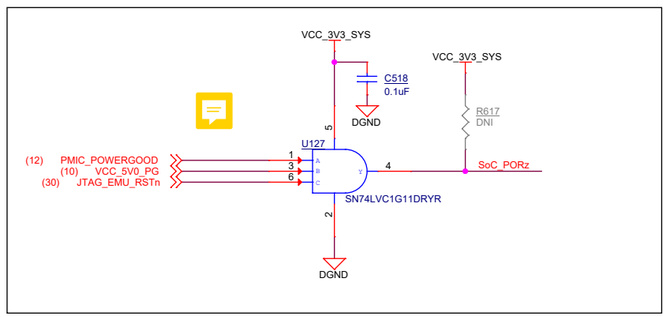
SOC - RESET



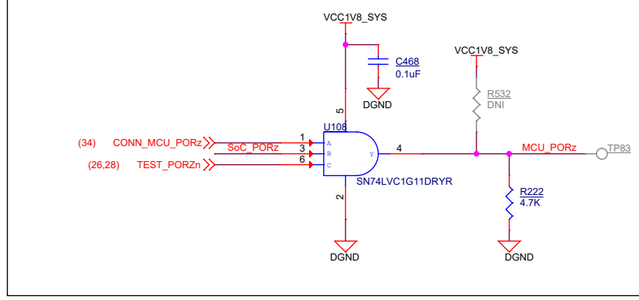
OSCILLATOR

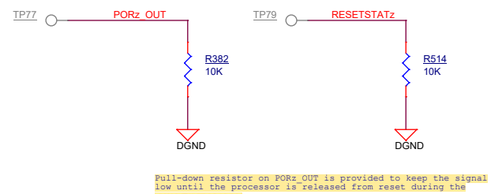






MCU POWER ON RESET





Pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up seqence

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Title	OSCILLATOR	
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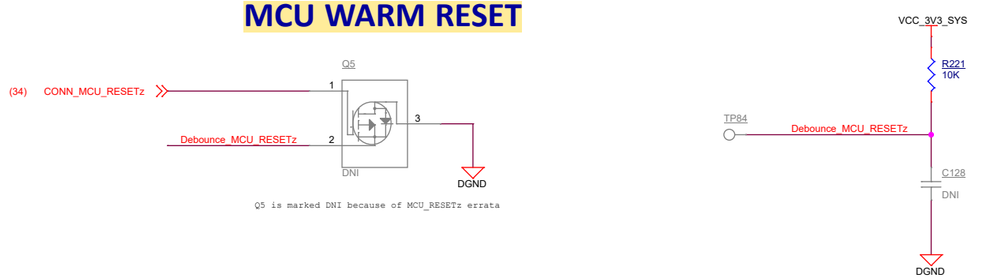
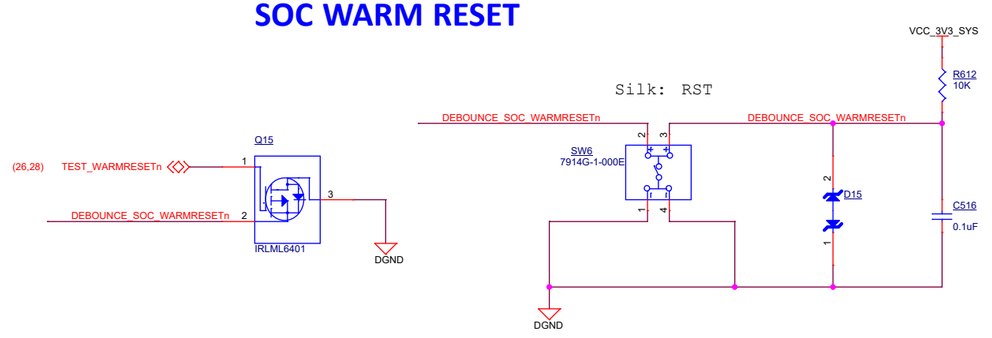
SOC RESET

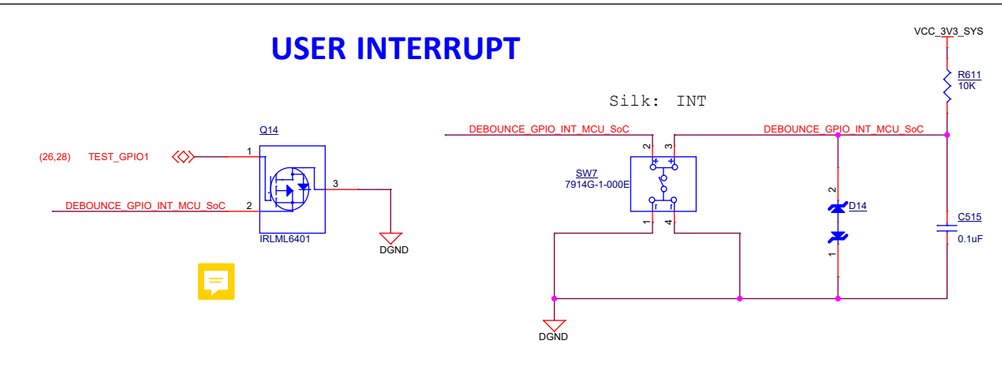
MCU WARM RESET



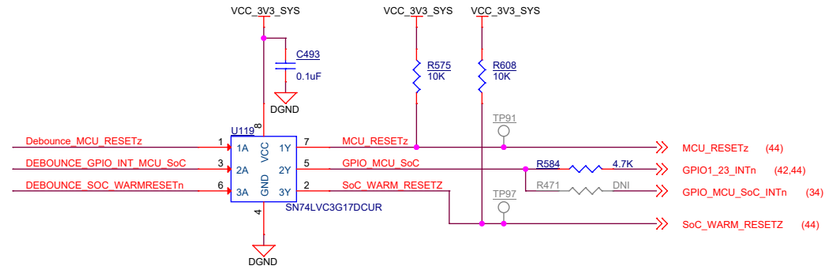
SOC WARM RESET



USER INTERRUPT



RESET & INT DEBOUNCE CIRCUIT



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Title	RESET	
Size: C	PROC164E1-1	Rev: E1-1
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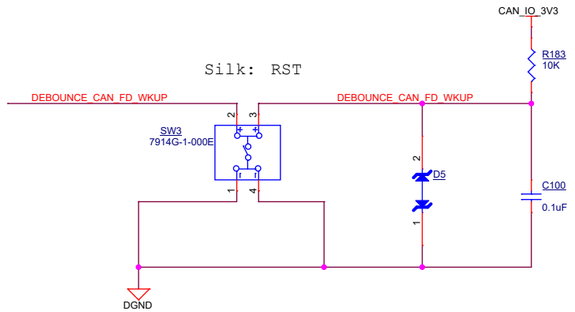
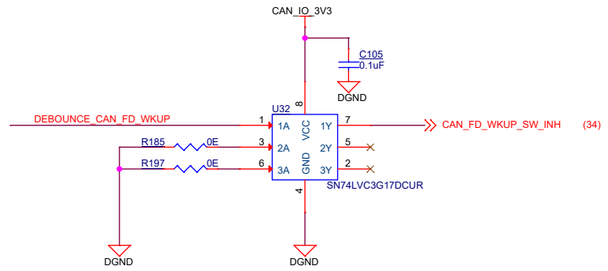
CAN-FD FAST WAKE UP SW





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Title	CAN FD WKUP SW	
Size: C	PROC164E1-1	Rev: E1-1
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HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB

PROC164E1-1

PROC164E1-1

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

AM62P SOCKET

ACC1

DNI

JUMPERS

ACC2

DNI

ACC3

DNI

FIDUCIALS

FID1 DNI

FID2 DNI

FID3 DNI

FID4 DNI

FID5 DNI

FID6 DNI

LABELS

Board Serial No.

LBL1

PCB LABEL

DNI

Assembly Revision

LBL2

PCB LABEL

DNI

SCREW & WASHER FOR PCIe M.2

ACC4

9774015243R

MH3

3356

MH5

MPMS 002 0005 PH

HOUSING & CRIMP FOR DSI AND OLDI HEADER

ACC5

DNI

ACC6

DNI

HOUSING

ACC7

DNI

ACC8

DNI

ACC9

DNI

ACC10

DNI

ACC12

DNI

ACC11

DNI

CRIMP

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Title	HARDWARE SCHEMATICS		
Size C	PROC164E1-1		Rev E1-1
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