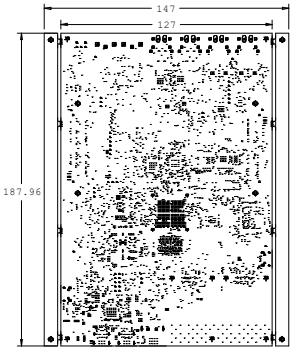
REVISIONS		
REV #	DESCRIPTION	DATE
REV E1	CCN #	290424

FABRICATION NOTES:

1. FABRICATE PCB IN ACCORDANCE WITH IPC-6012D, CLASS 2; PER IPC-6011. PCB SHALL BE MANUFACTURED USING ITEQ IT 180A OR EQUIVALENT
2. MATERIALS:
   1. LAMINATE AND PREPREG (N-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/126. (MIN.TG 170)
   2. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150. UNLESS OTHERWISE SPECIFIED. THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.15MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
4. BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. (MEANS FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
6. BOARD FINISHED SHALL BE ACCORDING TO IPC-6012D CLASS 2.
7. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
8. FINISH:
   1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG, ELECTROLESS NICKEL IMMERSION GOLD. ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.24 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
   2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES SHALL BE MASK FILLED AND COVERED WITH SOLDER MASK. ONLY SOLDER MASK IMAGES ON THE VIA PAD SHALL BE ALLOWED. SOLDER MASK SHALL BE GREEN. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE SOLDERED. DEFAULT COLOUR OF SOLDER MASK SHALL BE GREEN.
   3. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
   4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20UM [0.00079"], (MEANS OF LASER VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 12UM [0.0004"]" AND BURIED VIA'S SHALL NOT BE LESS THAN 15UM [0.0006"].
   5. ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLIANCE TO IPC6012, CLASS 2.
9. MARKING:
   1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796K WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE REQUIRED IN SILKSCREEN.
10. TEST REQUIREMENTS:
   1. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
11. THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
12. TEAR DROPS SHALL BE ADDED ON VIA'S AND THROUGH HOLE PADS IN ALL INTERNAL AND OUTER LAYERS.
13. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IF REQUIRED.
14. FINISHED PCB THICKNESS SHALL BE 0.0427" +/-10%.
15. MIN TRACE WIDTH/SPACING ON BOARD IS 0.003"/0.0030".
16. ENSURE UL REGISTERED E-FILE NUMBER SHALL BE PRINTED ON THE PCB SILKSCREEN.
17. VIA ON PAD SHALL BE RESIN FILLED AND CAP-PLATED.



DRILL CHART: TOP to BOTTOM						
ALL UNITS ARE IN MILS						
SYMBOL	FINISHED SIZE	ROTATION	TOLERANCE (MILS)	TOLERANCE (MARTS)	PLATED	QTY
•	8.0	-	+3.0/-3.0	-	PLATED	3941
■	30.0	-	+3.0/-3.0	-	PLATED	1
▲	36.0	-	+3.0/-3.0	-	PLATED	3
◆	40.0	-	+3.0/-3.0	-	PLATED	4
★	40.0	-	+3.0/-3.0	-	PLATED	18
●	44.0	-	+2.0/-2.0	-	PLATED	22
▲	46.0	-	+3.0/-3.0	-	PLATED	2
■	60.0	-	+3.0/-3.0	-	PLATED	24
■	66.0	-	+3.0/-3.0	-	PLATED	2
■	78.0	-	+3.0/-3.0	-	PLATED	4
▲	32.0	-	+3.0/-3.0	-	NON-PLATED	28
▲	34.0	-	+2.0/-2.0	-	NON-PLATED	2
■	40.0	-	+3.0/-3.0	-	NON-PLATED	4
■	48.0	-	+3.0/-3.0	-	NON-PLATED	2
▼	68.0	-	+3.0/-3.0	-	NON-PLATED	6
■	108.0	-	+3.0/-3.0	-	NON-PLATED	8
●	126.0	-	+3.0/-3.0	-	NON-PLATED	6
▬	48.0x22.0	0.000	+3.0/-3.0	+3.0/-3.0	PLATED	4
▬	42.0x24.0	90.000	+2.0/-2.0	+2.0/-2.0	PLATED	4
▬	48.0x24.0	0.000	+3.0/-3.0	+3.0/-3.0	PLATED	4
▬	82.0x24.0	90.000	+2.0/-2.0	+2.0/-2.0	PLATED	4
▬	118.0x28.0	90.000	+3.0/-3.0	+3.0/-3.0	PLATED	2
●	158.0x78.0	90.000	+3.0/-3.0	+3.0/-3.0	NON-PLATED	8

LAYER STACKUP

	LAYER NAME	FINISHED Cu	X-SECTION	DIELECTRIC THICKNESS [INCHES]
	PRIMARY SIDE SILKSCREEN			
	PRIMARY SIDE SOLDERMASK			
LO1	PRIMARY SIDE	<.35oz		0.00436
LO2	GROUND-PLANE-1	1oz.		0.003
LO3	INNER-SIGNAL-1	0.5oz.		0.00493
LO4	POWER-PLANE-1	1oz.		0.006
LO5	INNER-SIGNAL-2	1oz.		0.00493
LO6	POWER-PLANE-2	0.5oz.		0.003
LO7	GROUND-PLANE-2	1oz.		0.00436
LO8	SECONDARY SIDE	<.35oz		
	SECONDARY SIDE SOLDERMASK			
	SECONDARY SIDE SILKSCREEN			

IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH (Mils)	SPACING (Mils)	IMPEDANCE (Ohms)	REF LAYER
01	MICROSTRIP	L1, L8	7.5	NA	50	L2, L7
02	EDGE COUPLED DIFFERENTIAL	L1, L8	4.7	4	90	L2, L7
03	EDGE COUPLED MICROSTRIP	L1	8	7	120	L4
04	MICROSTRIP	L1, L8	13.4	NA	50	L2, L7
05	MICROSTRIP	L1, L8	11.5	NA	45	L2, L7
06	EDGE COUPLED MICROSTRIP	L1, L8	10.0	4	60	L2, L7
07	EDGE COUPLED MICROSTRIP	L1, L8	7	5.2	80	L2, L7
08	EDGE COUPLED STRIPLINE	L3	8.5	5.2	80	L2/L4
09	STRIPLINE	L3	5	NA	50	L2/L4
10	STRIPLINE	L3	4.8	NA	45	L2/L4
11	EDGE COUPLED STRIPLINE	L3	4	4	80	L2/L4
12	EDGE COUPLED STRIPLINE	L3	3	8.5	133	L2/L4
13	STRIPLINE	L5	6.7	NA	40	L4/L6
14	EDGE COUPLED STRIPLINE	L5	5	4.8	85	L4/L6
15	STRIPLINE	L5	8	NA	33	L4/L6
16	EDGE COUPLED STRIPLINE	L5	5.25	4	66	L4/L6

SIGNATURES		DATE
LAYOUT BY	AG	210924
REVIEWED BY	ZA	210924
APPROVED BY	AMB	210924

TEXAS INSTRUMENTS

PROC180

AM62D EVM BOARD

SIZE		REV
D		E2
SCALE: NONE		SHEET 1 OF 15