Table 10-11. Network Time Synchronization Functions in the SoC

Interface	Time Sync Functions	Supported by
2×PRU-ICSSG	IEEE 1588-2008 (1/2-step), 802.1AS, TSN	PRU-ICSSG firmware
1×PCIE	Precision time measurement (PTM)	PCIe controller hardware
1×CPSW	IEEE 1588-2008 (2-step), 802.1AS	CPTS in CPSW
External input reference clock	External time/clock reference	CPTS in SoC

Definition of Network Time Sync

Table 10-1. CPTS Allocation Across Device Domains

Instance	Domain	
	MCU	MAIN
CPTS0	-	✓
PCIE0_CPTS0	-	✓ (PCIE0)
CPSW0_CPTS0	✓ (CPSW0)	-

Definition of the 3 CPTS (MAIN/CPSW/PCIE)

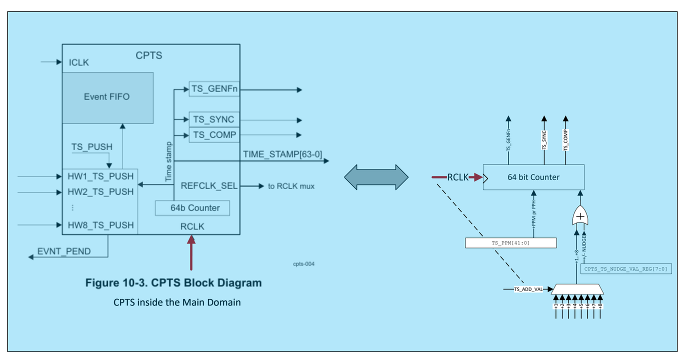


Figure 10-3. CPTS Block Diagram

CPTS inside the Main Domain

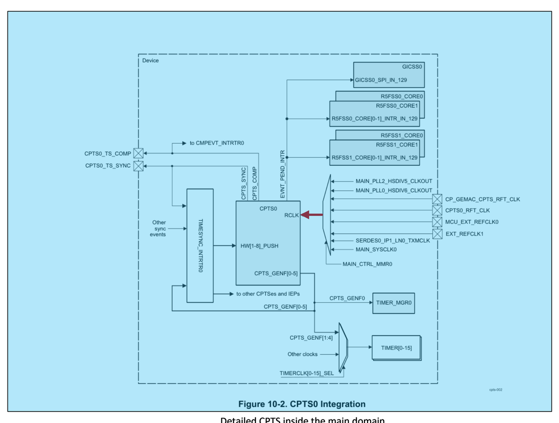


Figure 10-2. CPTS0 Integration

Detailed CPTS inside the main domain

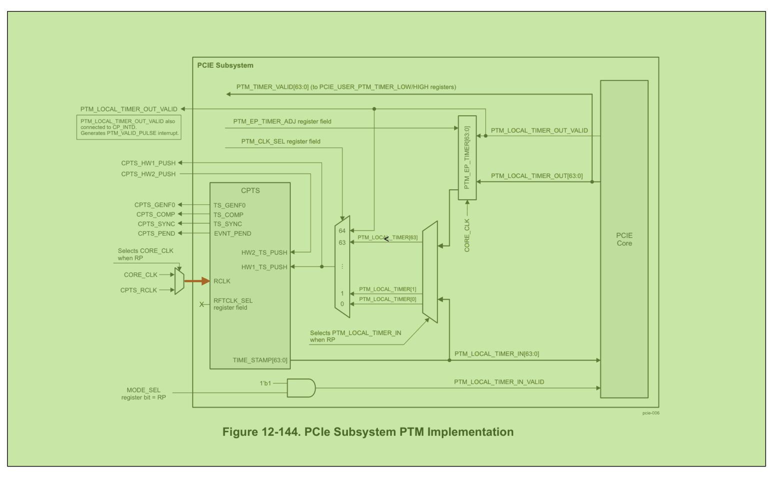


Figure 12-144. PCIe Subsystem PTM Implementation

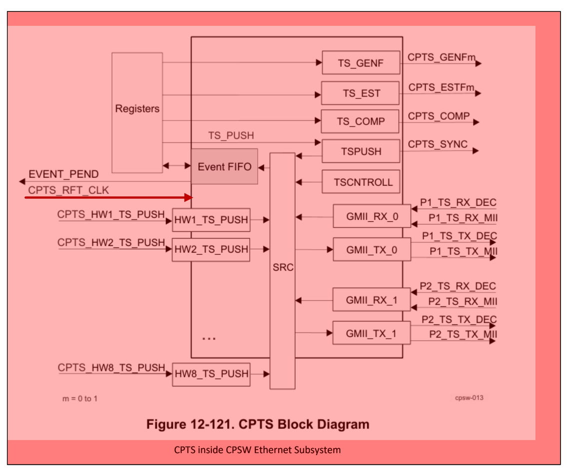


Figure 12-121. CPTS Block Diagram

CPTS inside CPSW Ethernet Subsystem

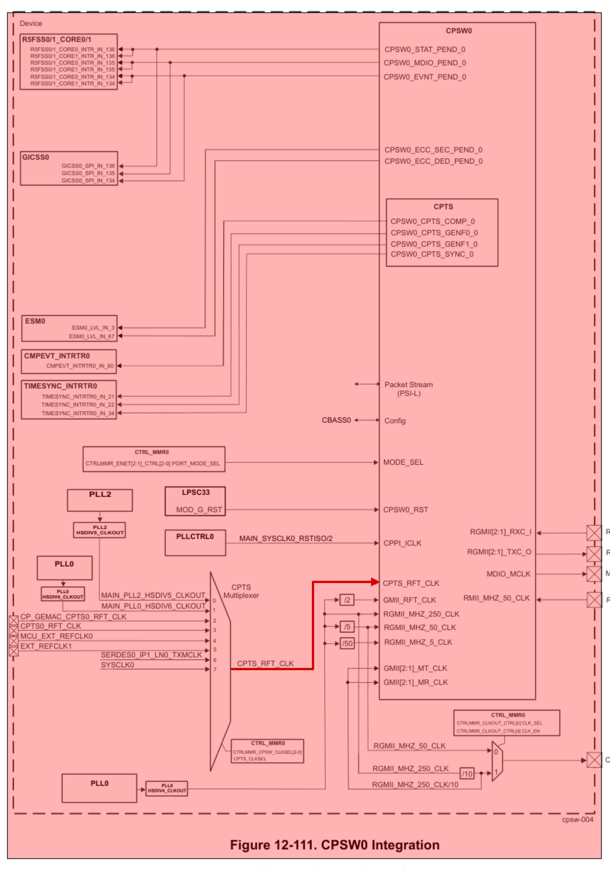
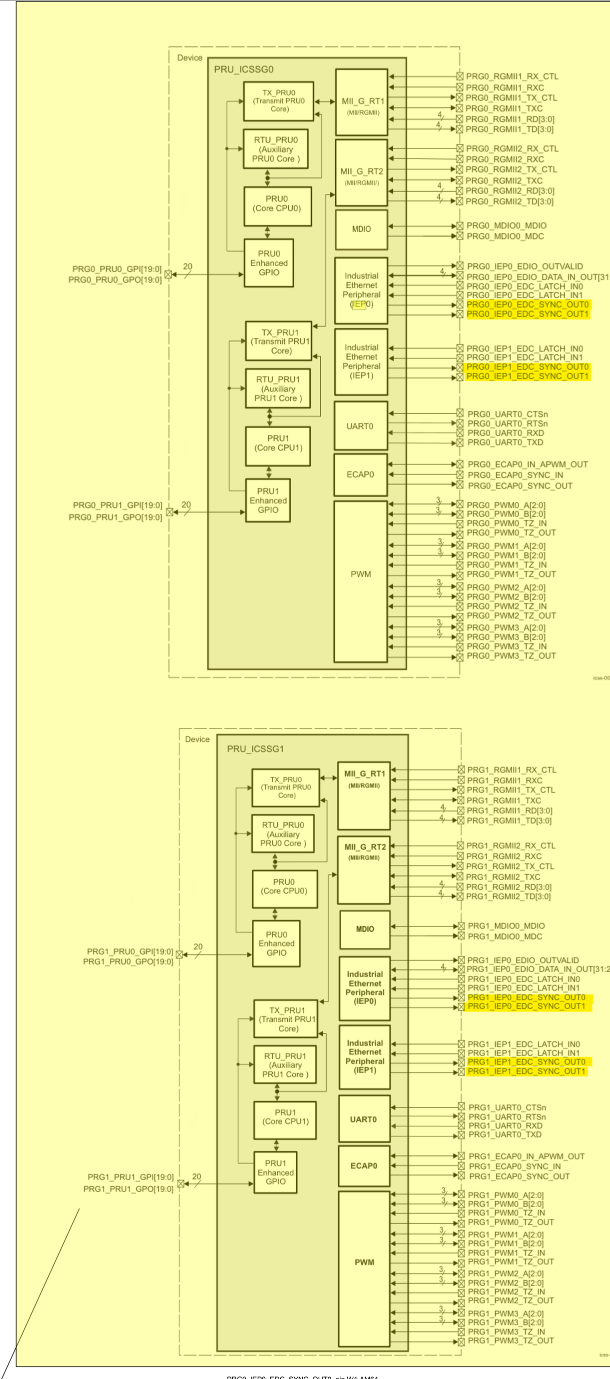


Figure 12-111. CPSW0 Integration

Detailed CPTS inside CPSW Ethernet Subsystem



PRG0_IEP0_EDC_SYNC_OUT0 pin W1 AM64
PRG0_IEP0_EDC_SYNC_OUT1 pin WU1 AM64
PRG0_IEP1_EDC_SYNC_OUT0 pin R2 AM64
PRG0_IEP1_EDC_SYNC_OUT1 pin V5 AM64

PRG1_IEP0_EDC_SYNC_OUT0 pin W7 AM64
PRG1_IEP0_EDC_SYNC_OUT2 pin U7 AM64
PRG1_IEP1_EDC_SYNC_OUT0 pin V12 AM64
PRG1_IEP1_EDC_SYNC_OUT1 pin AA14 AM64
PRG1_IEP0_EDC_LATCH_IN1 pin U13 AM64
PRG1_IEP0_EDC_LATCH_IN0 pin V7 AM64

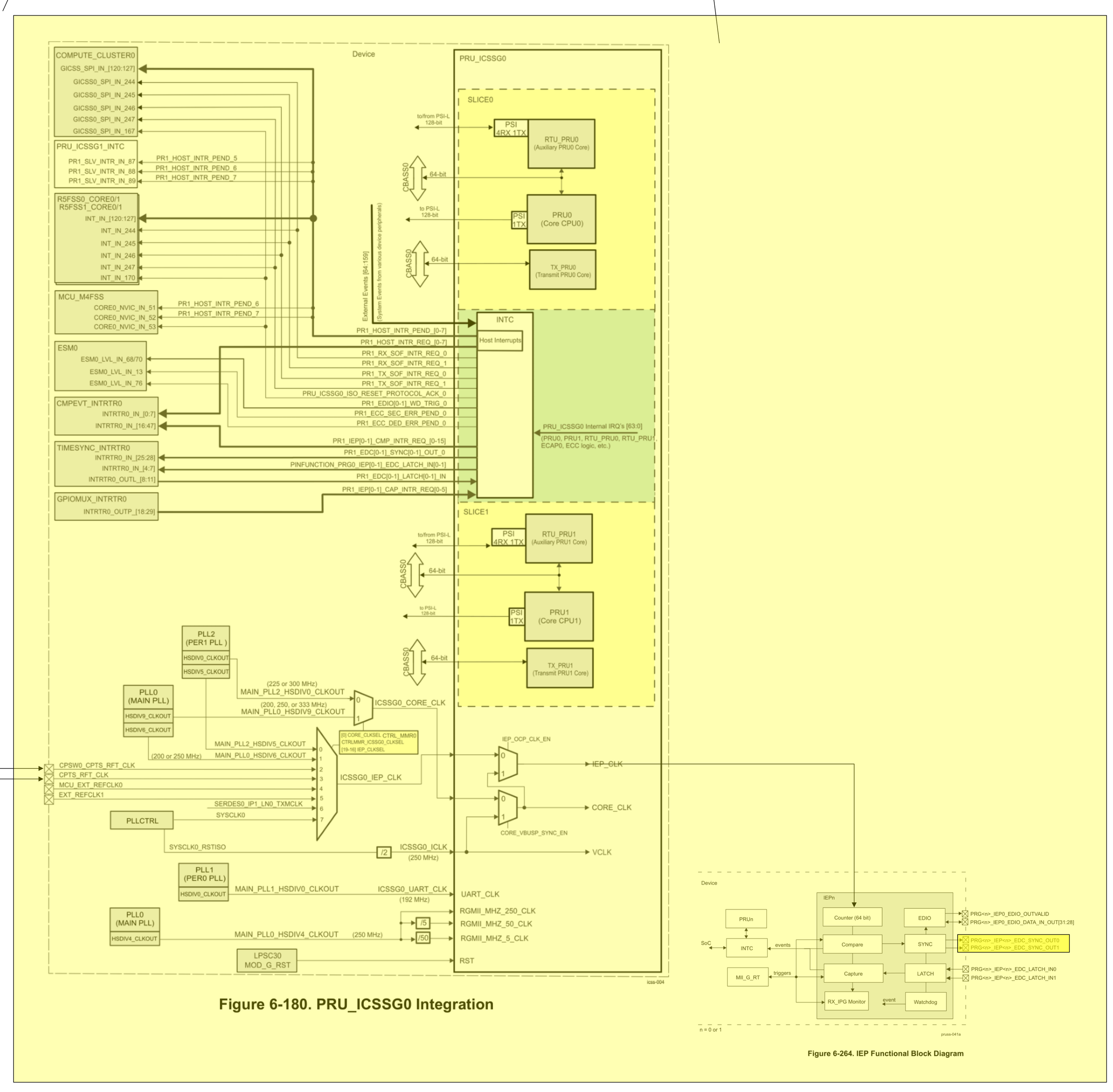


Figure 6-180. PRU_ICSSG0 Integration

Figure 6-264. IEP Functional Block Diagram

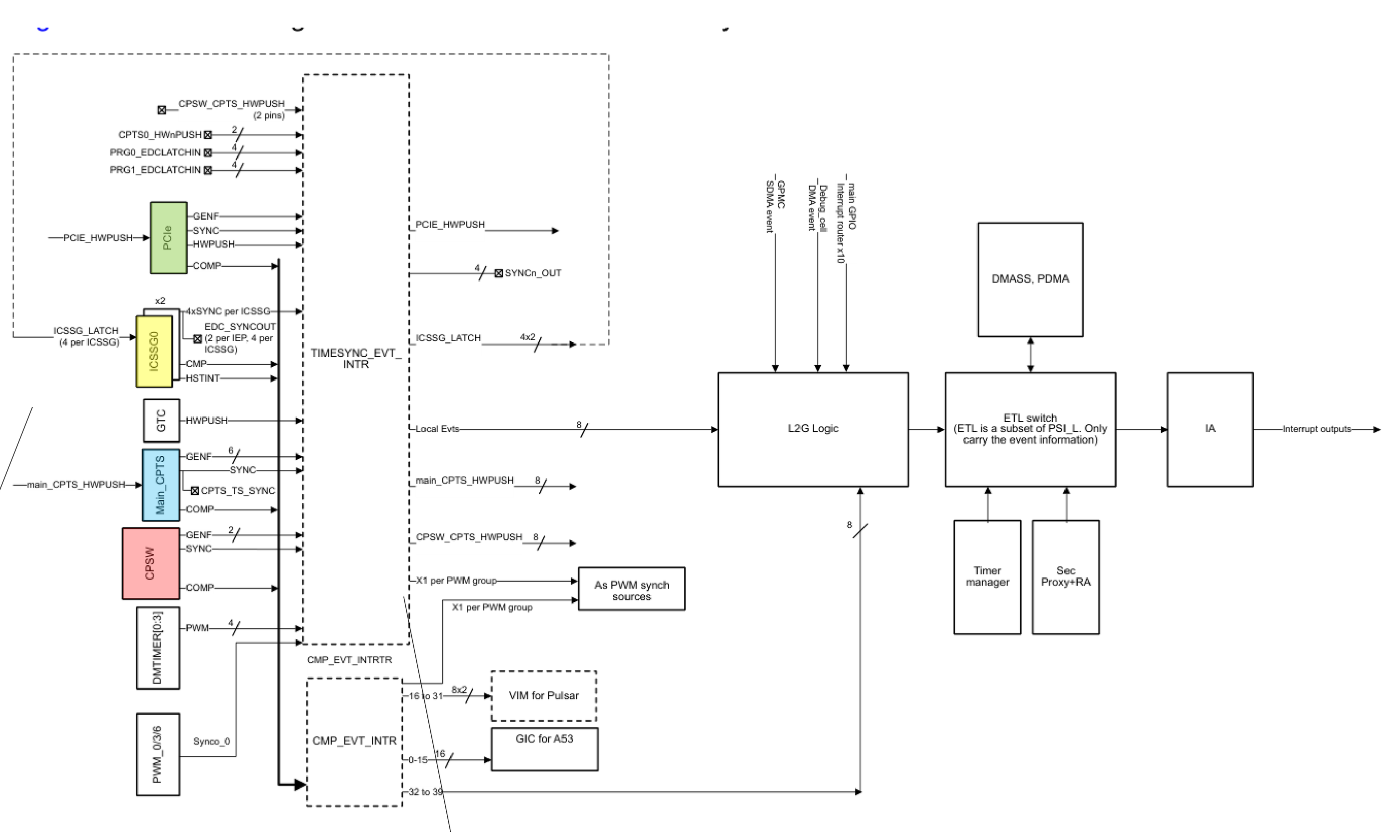


Figure 10-9. SoC Time Sync Architecture

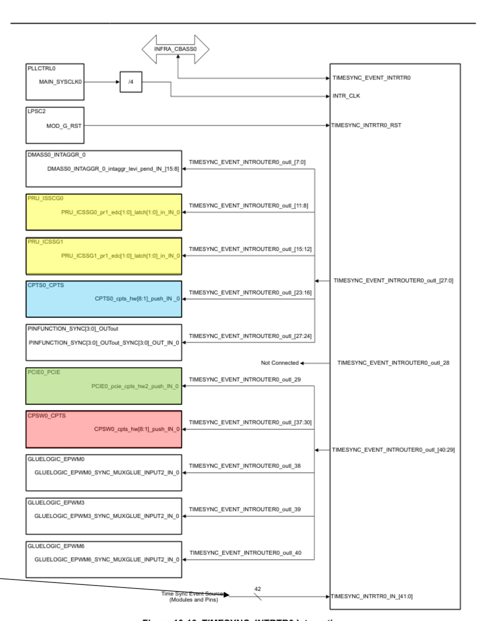


Figure 10-10. TIMESYNC_INTRTR0 Integration

Table 9-65. TIMESYNC_INTRTR0 Interrupt Map

Interrupt Input Line	ID	Source Interrupt
TIMESYNC_INTRTR0_IN_0	0	TIMER0_TIMER_PWM_0
TIMESYNC_INTRTR0_IN_1	1	TIMER1_TIMER_PWM_0
TIMESYNC_INTRTR0_IN_2	2	TIMER2_TIMER_PWM_0
TIMESYNC_INTRTR0_IN_3	3	TIMER3_TIMER_PWM_0
TIMESYNC_INTRTR0_IN_4	4	PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN0IN_PRG0_IEP0_EDC_LATCH_IN0_0
TIMESYNC_INTRTR0_IN_5	5	PINFUNCTION_PRG0_IEP0_EDC_LATCH_IN1IN_PRG0_IEP0_EDC_LATCH_IN1_0
TIMESYNC_INTRTR0_IN_6	6	PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN0IN_PRG0_IEP1_EDC_LATCH_IN0_0
TIMESYNC_INTRTR0_IN_7	7	PINFUNCTION_PRG0_IEP1_EDC_LATCH_IN1IN_PRG0_IEP1_EDC_LATCH_IN1_0
TIMESYNC_INTRTR0_IN_8	8	PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN0IN_PRG1_IEP0_EDC_LATCH_IN0_0
TIMESYNC_INTRTR0_IN_9	9	PINFUNCTION_PRG1_IEP0_EDC_LATCH_IN1IN_PRG1_IEP0_EDC_LATCH_IN1_0
TIMESYNC_INTRTR0_IN_10	10	PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN0IN_PRG1_IEP1_EDC_LATCH_IN0_0
TIMESYNC_INTRTR0_IN_11	11	PINFUNCTION_PRG1_IEP1_EDC_LATCH_IN1IN_PRG1_IEP1_EDC_LATCH_IN1_0
TIMESYNC_INTRTR0_IN_12	12	PINFUNCTION_CP_GEMAC_CPTS0_HW1TSPUSHIN_CP_GEMAC_CPTS0_HW1TSPUSH_0
TIMESYNC_INTRTR0_IN_13	13	PINFUNCTION_CP_GEMAC_CPTS0_HW2TSPUSHIN_CP_GEMAC_CPTS0_HW2TSPUSH_0
TIMESYNC_INTRTR0_IN_14	14	PINFUNCTION_CPTS0_HW1TSPUSHIN_CPTS0_HW1TSPUSH_0
TIMESYNC_INTRTR0_IN_15	15	PINFUNCTION_CPTS0_HW2TSPUSHIN_CPTS0_HW2TSPUSH_0
TIMESYNC_INTRTR0_IN_16	16	CPTS0_CPTS_GENF0_0
TIMESYNC_INTRTR0_IN_17	17	CPTS0_CPTS_GENF1_0
TIMESYNC_INTRTR0_IN_18	18	CPTS0_CPTS_GENF2_0
TIMESYNC_INTRTR0_IN_19	19	CPTS0_CPTS_GENF3_0
TIMESYNC_INTRTR0_IN_20	20	CPTS0_CPTS_GENF4_0
TIMESYNC_INTRTR0_IN_21	21	CPSW0_CPTS_GENF0_0
TIMESYNC_INTRTR0_IN_22	22	CPSW0_CPTS_GENF1_0
TIMESYNC_INTRTR0_IN_23	23	PCIE0_PCIE_CPTS_GENF0_0
TIMESYNC_INTRTR0_IN_24	24	CPTS0_CPTS_GENF5_0
TIMESYNC_INTRTR0_IN_25	25	PRU_ICSSG0_PR1_EDC0_SYNC0_OUT_0
TIMESYNC_INTRTR0_IN_26	26	PRU_ICSSG0_PR1_EDC0_SYNC1_OUT_0
TIMESYNC_INTRTR0_IN_27	27	PRU_ICSSG0_PR1_EDC1_SYNC0_OUT_0
TIMESYNC_INTRTR0_IN_28	28	PRU_ICSSG0_PR1_EDC1_SYNC1_OUT_0
TIMESYNC_INTRTR0_IN_29	29	PRU_ICSSG1_PR1_EDC0_SYNC0_OUT_0
TIMESYNC_INTRTR0_IN_30	30	PRU_ICSSG1_PR1_EDC0_SYNC1_OUT_0
TIMESYNC_INTRTR0_IN_31	31	PRU_ICSSG1_PR1_EDC1_SYNC0_OUT_0
TIMESYNC_INTRTR0_IN_32	32	PRU_ICSSG1_PR1_EDC1_SYNC1_OUT_0
TIMESYNC_INTRTR0_IN_33	33	PCIE0_PCIE_CPTS_SYNC_0
TIMESYNC_INTRTR0_IN_34	34	CPSW0_CPTS_SYNC_0
TIMESYNC_INTRTR0_IN_35	35	CPTS0_CPTS_SYNC_0
TIMESYNC_INTRTR0_IN_36	36	GTC0_GTC_PUSH_EVENT_0
TIMESYNC_INTRTR0_IN_37	37	PCIE0_PCIE_CPTS_HW1_PUSH_0
TIMESYNC_INTRTR0_IN_38	38	PCIE0_PCIE_PTM_VALID_PULSE_0
TIMESYNC_INTRTR0_IN_39	39	EPWM0_EPWM_SYNCO_O_0
TIMESYNC_INTRTR0_IN_40	40	EPWM3_EPWM_SYNCO_O_0
TIMESYNC_INTRTR0_IN_41	41	EPWM6_EPWM_SYNCO_O_0