



RMII™ Specification

1.0 Overview and Architecture

This document comprises a low pin count Reduced Media Independent Interface™ (RMII™) specification intended for use between Ethernet PHYs and Switch ASICs. Under IEEE 802.3u [2] an MII comprised of 16 pins for data and control is defined. In devices incorporating many MACs or PHY interfaces such as switches, the number of pins can add significant cost as the port counts increase. Typical switch products in the industry today offer 12 to 24 ports in a single device. At 6 pins per port and 1 pin per switch ASIC, the proposed RMII specification would save 119 pins plus the extra power and ground pins to support those additional pins for a 12 port switch ASIC.

The purpose of this interface is to provide a low cost alternative to the IEEE 802.3u [2] MII as specified in Clause 22 (hereafter referred to as simply “MII”). Architecturally, the RMII specification provides for an additional reconciliation layer on either side of the MII but can be implemented in the absence of an MII.

The management interface (MDIO/MDC) is assumed to be identical to that defined in IEEE 802.3u [2]. It is assumed that the reader is familiar with IEEE 802.3 [1] and IEEE 802.3u [2].

The RMII specification has the following characteristics:

1. It is capable of supporting 10Mb/s and 100Mb/s data rates
2. A single clock reference is sourced from the MAC to PHY (or from an external source)
3. It provides independent 2 bit wide (di-bit) transmit and receive data paths
4. It uses TTL signal levels, compatible with common digital CMOS ASIC processes

2.0 Application

The RMII specification has been optimized for use in high port density interconnect devices which require independent treatment of the data paths. The primary motivator is a switch ASIC which requires independent data streams between the MAC and PHY. Design considerations for repeaters have not been accounted for in this specification. While repeaters are not precluded from using the RMII specification, no validation of the feasibility of their implementation has gone into the definition.

The implementation of the interface is assumed to be a chip-to-chip interface implemented with traces on a printed circuit board. While other implementations are not precluded, no provision is made in this document for an exposed interface (i.e. no connector is specified).

3.0 Design Goals and Trade-offs

In choosing the signaling for the RMII specification, the following criteria was applied:

1. Clock frequency of 50 MHz or less to minimize EMI and IC I/O requirements
2. Pin count independent of port density of the PHY
3. Single synchronous clocking
4. Reduction of required control pins

By doubling the clock frequency 4 pins are saved on the data path alone without substantially impacting ASIC I/O capabilities or requiring clock frequencies of 100MHz which can cause significant system level challenges with respect to EMI performance.

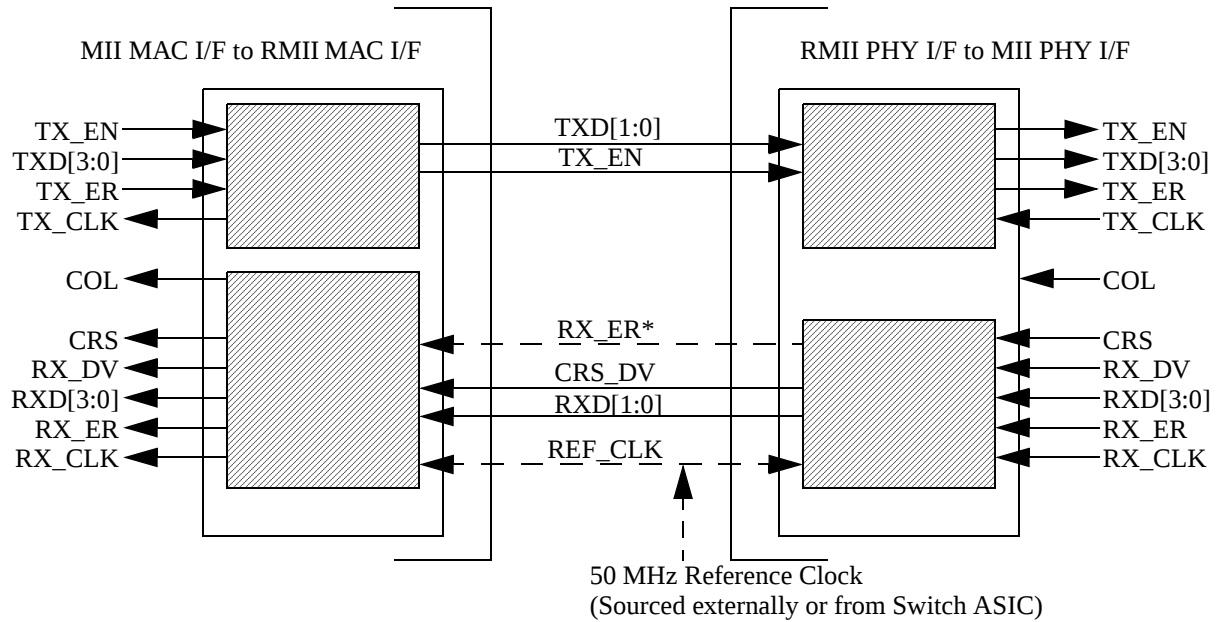
Further, as long as Start of Packet and End of Packet timing information is preserved across the interface, the MAC is able to derive the COL signal from the receive and transmit data delimiters. Of significant impact is preserving Start of Packet information in both 10 and 100 Mb/s operation since there can be a relatively large delta between the assertion of CRS and RX_DV on the standard IEEE 802.3u MII [2]. However, CRS can be collapsed together with RX_DV if some additional reconciliation assumptions are made.

RX_ER is important for meeting Hamming Distance requirements. However, PHYs have the possibility of introducing data replacement to guarantee that the CRC offers adequate protection. Similarly, in switch applications there is no need for TX_ER since a MAC will never generate errored data. The one case where TX_ER is used is with repeaters that need to ensure propagation of errors. When used in conjunction with data corruption by the PHY on RX_ER, this becomes a non-issue.

A single synchronous reference clock for transmit, receive, and control is used. This corresponds to one output from the switch ASIC. Alternatively, the clock reference could be sourced from an external device and may correspond to one input to the switch ASIC. Each PHY provides a clock reference input. However, only one input is required for multiple PHYs on a single IC. PHYs must provide enough buffering to account for worst case variation between local and recovered clock.

Since data is not looped back from transmit to receive, the codes corresponding to RXD[1:0] values and TXD[1:0] while TX_EN and/or RX_DV are de-asserted may be used for out of band MAC/PHY signalling.

FIGURE 1. Signal Reconciliation Map



*Note:RX_ER is a required output of the PHY. The switch ASIC may choose to use this input.

4.0 Conformance

This document follows IEEE 802 conventions in that the word “shall” indicates a requirement for conformance to this specification. The word “may” indicates a choice or an allowable implementation. All other text is background, explanatory, or recommendation.

5.0 Signal Definition

The PHY shall implement and conform to the requirements for REF_CLK, CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_ER. The MAC interface shall implement and conform to the requirements for REF_CLK, CRS_DV, RXD[1:0], TX_EN and TXD[1:0].

TABLE 1.

RMII Specification Signals

Signal Name	Direction (with respect to the PHY)	Direction (with respect to the MAC)	Use
REF_CLK	Input	Input or Output	Synchronous clock reference for receive, transmit and control interface
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data
TX_EN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data
RX_ER	Output	Input (Not required)	Receive Error

5.1 REF_CLK

Reference Clock

REF_CLK is a continuous clock that provides the timing reference for CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_ER. REF_CLK is sourced by the MAC or an external source. Switch implementations may choose to provide REF_CLK as an input or an output depending on whether they provide a REF_CLK output or rely on an external clock distribution device. Each PHY device shall have an input corresponding to this clock but may use a single clock input for multiple PHYs implemented on a single IC.

The REF_CLK frequency shall be 50 MHz +/- 50 ppm with a duty cycle between 35% and 65% inclusive. It is assumed that the PHY uses REF_CLK as the network clock such that no buffering is required on the transmit data path.

While the PHY may recover clock from the incoming data stream, the receiver shall account for differences between the local REF_CLK and the recovered clock through use of sufficient elasticity buffering. The elasticity buffer design shall not affect the Inter-Packet Gap (IPG) for received IPGs of 36 bits or greater. To tolerate the clock variations specified here for Ethernet MTUs, the elasticity buffer shall tolerate a minimum of +/-10 bits.* This implies that the FIFO is at least 20 bits deep and does not transfer recovered data onto RXD[1:0] until the FIFO is half full.

*Note:Some vendors desire toleration of MTUs greater than the Ethernet MTU.

5.2 CRS_DV

Carrier Sense/Receive Data Valid

CRS_DV shall be asserted by the PHY when the receive medium is nonidle. The specifics of the definition of idle for 10BASE-T and 100BASE-X are contained in IEEE 802.3 [1] and IEEE 802.3u [2]. CRS_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. That is, in 10BASE-T mode, when squelch is passed or in 100BASE-X mode when 2 non-contiguous zeroes in 10 bits are detected carrier is said to be detected.

Loss of carrier shall result in the deassertion of CRS_DV synchronous to the cycle of REF_CLK which presents the first di-bit of a nibble onto RXD[1:0] (i.e. CRS_DV is deasserted only on nibble boundaries). If the PHY has additional bits to be presented on RXD[1:0] following the initial deassertion of CRS_DV, then the PHY shall assert CRS_DV on cycles of REF_CLK which present the second di-bit of each nibble and deassert CRS_DV on cycles of REF_CLK which present the first di-bit of a nibble. The result is: Starting on nibble boundaries CRS_DV toggles at 25 MHz in 100Mb/s mode and 2.5 MHz in 10Mb/s mode when CRS ends before RX_DV (i.e. the FIFO still has bits to transfer when the carrier event ends.) Therefore, the MAC can accurately recover RX_DV and CRS.

During a false carrier event, CRS_DV shall remain asserted for the duration of carrier activity.

The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] shall be “00” until proper receive signal decoding takes place (see definition of RXD[1:0] behavior).

*Note: CRS_DV is asserted asynchronously in order to minimize latency of control signals through the PHY.

5.3 RXD[1:0]

Receive Data [1:0]

RXD[1:0] shall transition synchronously to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. In some cases (e.g. before data recovery or during error conditions) a pre-determined value for RXD[1:0] is transferred instead of recovered data. RXD[1:0] shall be “00” to indicate idle when CRS_DV is deasserted. Values of RXD[1:0] other than “00” when RX_DV as recovered from CRS_DV is deasserted are reserved for out-of-band signaling (to be defined). Values other than “00” on RXD[1:0] while RX_DV as recovered from CRS_DV is de-asserted shall be ignored by the MAC. Upon assertion of CRS_DV, the PHY shall ensure that RXD[1:0]=“00” until proper receive decoding takes place.

5.3.1 RXD[1:0] in 100 Mb/s mode

For normal reception following assertion of CRS_DV, RXD[1:0] shall be “00” until the receiver has determined that the receive event has a proper Start of Stream Delimiter.

Thereafter, preamble will appear (RXD[1:0]=01). Data capture by MACs occur following detection of SFD.

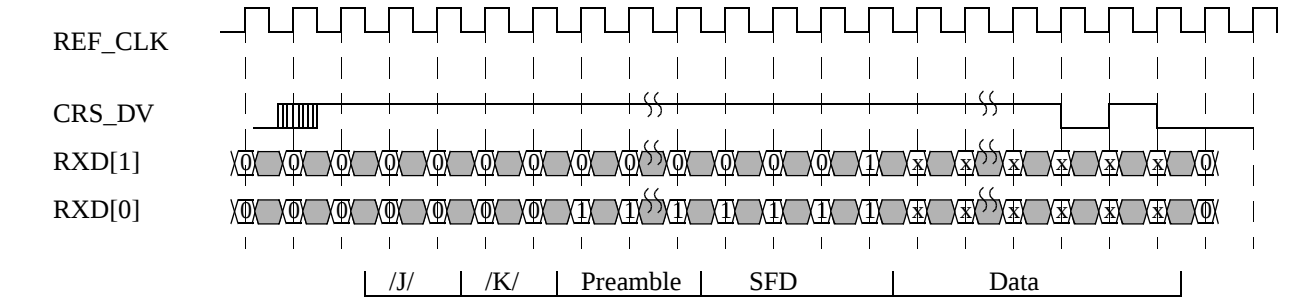


FIGURE 2. 100 Mb/s Reception with no errors

*Note: CRS_DV may toggle at 25MHz starting on a nibble boundary if bits accumulate due to the difference between local and recovered clock to allow distinction between CRS and RX_DV. The example waveform shows a single nibble accumulated in the FIFO.

If False Carrier is detected (Bad SSD), then RXD[1:0] shall be “10” until the end of the receive event. This is a unique pattern since False Carrier can only occur at the beginning of a packet where preamble will be decoded (i.e. RXD[1:0]=01).

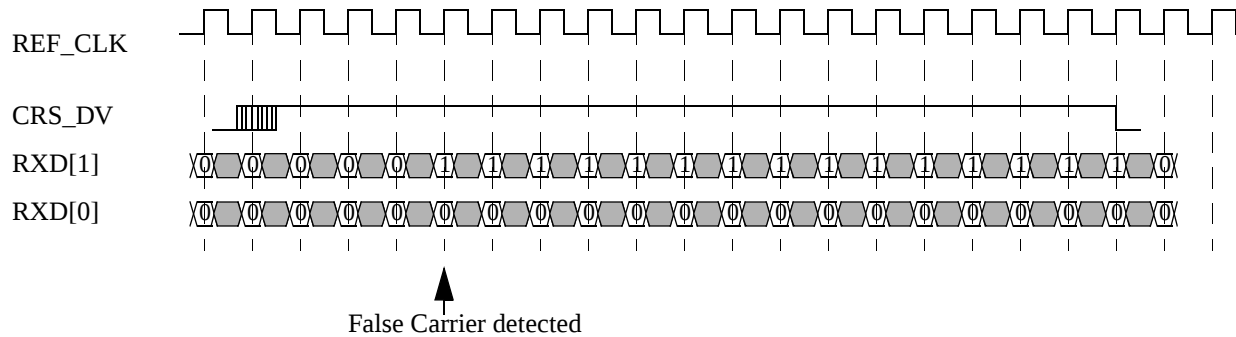


FIGURE 3. 100 Mb/s Reception with False Carrier

5.3.2 RXD[1:0] in 10 Mb/s mode

Following assertion of CRS_DV, RXD[1:0] shall be “00” until the 10BASE-T PHY has recovered clock and is able to decode the receive data. Once valid receive data is avail-

able from the 10BASE-T PHY, RXD[1:0] shall take on the recovered data values (i.e. starting with “01” for preamble).

As the REF_CLK frequency is 10 times the data rate in 10Mb/s mode the value on RXD[1:0] shall be valid such that RXD[1:0] may be sampled every 10th cycle, regardless of the starting cycle within the group and yield the correct frame data.

5.3.3 RXD[1:0] and Receive Error Detection

The MII provides the RX_ER signal to ensure propagation of errors when the 100BASE-X PHY cannot decode the receive signal properly. To eliminate the requirement for this signal and still meet the requirements for undetected error rate, RXD[1:0] shall replace the decoded data in the receive stream with “01” until the end of carrier activity. By replacing the data in the remainder of the frame with a particular pattern, the CRC check will reject the packet as errored.

Switches perform CRC checking and will not propagate errored packets. It should also be noted that the need for TX_ER is also obviated since its purpose was to enable repeaters to ensure error propagation without requiring repeaters to alter the data flowing through them.

In order to ensure the CRC error count is not affected, the PHY shall provide a 16 bit receive error counter that increments upon detection of RX_ER as defined in section 5.7 at most once per carrier event. It is recommended that the receive error counter be located at 15h within the standard MII register space. If address 15h is not available, the receive error counter register shall be contained between 10h and 1Fh such that IEEE 802.3u [2] MII register space is not affected.

5.4 TX_EN

Transmit Enable

TX_EN indicates that the MAC is presenting di-bits on TXD[1:0] for transmission. TX_EN shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented. TX_EN shall be negated prior to the first REF_CLK rising edge following the final di-bit of a frame. TX_EN shall transition synchronously with respect to REF_CLK.

5.5 TXD[1:0]

Transmit Data

TXD[1:0] shall transition synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD[1:0] shall be “00” to indicate idle when TX_EN is deasserted. Values of TXD[1:0] other than “00” when TX_EN is deasserted are reserved for out-of-band signalling (to be defined). Values other than “00” on TXD[1:0] while TX_EN is deasserted shall be ignored by the PHY.

5.5.1 TXD[1:0] in 100 Mb/s mode

TXD[1:0] shall provide valid data for each REF_CLK period while TX_EN is asserted.

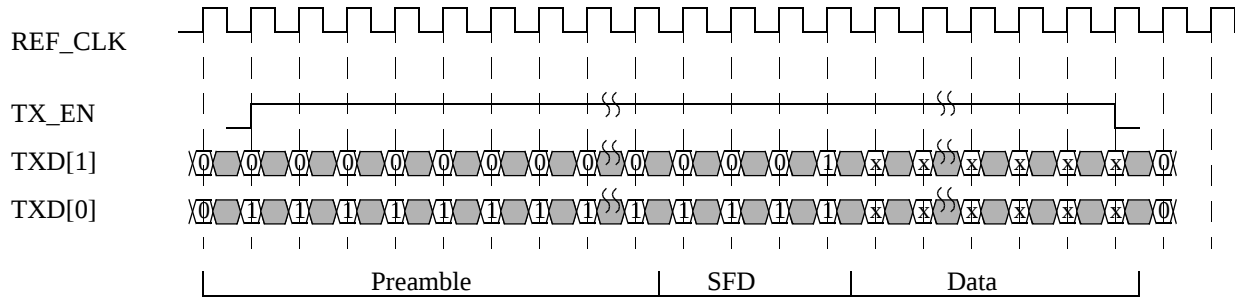


FIGURE 4. 100 Mb/s Transmission

5.5.2 TXD[1:0] in 10 Mb/s mode

As the REF_CLK frequency is 10 times the data rate in 10Mb/s mode the value on TXD[1:0] shall be valid such that TXD[1:0] may be sampled every 10th cycle, regardless of the starting cycle within the group and yield the correct frame data.

5.6 Collision Detection

Since the definition of CRS_DV and TX_EN both contain an accurate indication of the start of frame, the MAC can reliably regenerate the COL signal of the MII by ANDing TX_EN and CRS as recovered from CRS_DV. Note that TX_EN cannot be ANDed directly with CRS_DV since CRS_DV may toggle at the end of the frame to provide separation of RX_DV and CRS.

During the IPG time following the successful transmission of a frame, the COL signal is asserted by some transceivers as a self-test. The Signal Quality Error Test (SQE Test) function will not be supported by the RMII specification due to the lack of the COL signal. Historically, SQE Test was present to indicate that a transceiver located physically remote from the MAC was functioning. Since the RMII specification only supports chip-to-chip connections on a PCB, SQE Test functionality is not required.

5.7 RX_ER

The PHY shall provide RX_ER as an output according to the rules specified in IEEE 802.3u [2] (see Clause 24, Figure 24-11 - Receive State Diagram). RX_ER shall be asserted for one or more REF_CLK periods to indicate that an error (e.g. a coding error or other error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY. RX_ER shall transition synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RX_ER shall have no effect on the MAC.

*Note: A switch ASIC is not required to use an input corresponding to the RX_ER signal provided by the PHY. The RMII specification provides data replacement that ensures receive errors are caught by CRC checking in the MAC and are not propagated. The RX_ER signal is provided for those applications that may require its functionality.

5.8 Loopback

During normal operation TXD[1:0] and TX_EN shall not be loop ed back to RXD[1:0] and CRS_DV, respectively. Loopback for diagnostics is unspecified in this document. Note that loopback across this interface is impossible since the collision detection is done in the MAC, which assumes independent receive and transmit control signals.

6.0 Frame Structure

Transmitted data frames shall have the following frame format:

<inter-frame><preamble><sfd><data><efd>

Transmission and reception of each octet shall be done a di-bit at a time with the order of di-bit transmission and reception as shown below.

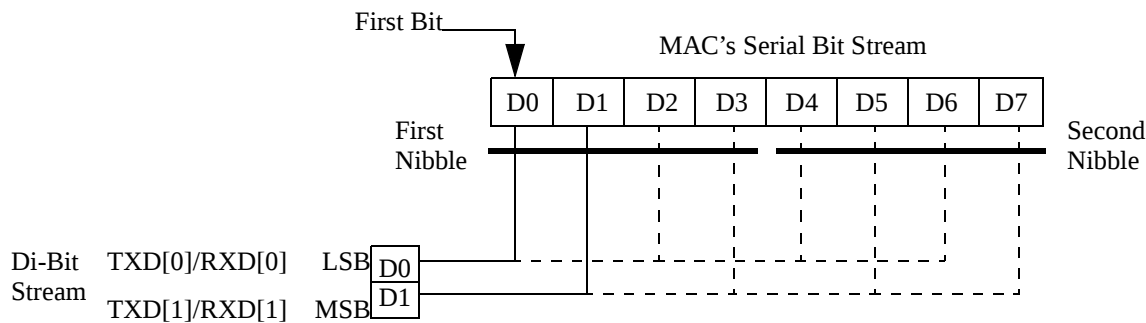


FIGURE 5. Bit Ordering

7.0 Electrical Characteristics

The electrical characteristics are very similar to those provided for in IEEE 802.3u [2] Clause 22. In many cases the exact text from that clause has been used. This has been done to achieve maximum electrical interoperability by leveraging a proven electrical interfacing standard. The AC and DC requirements listed below shall be met.

7.1 Signal Levels

TTL signal levels are used, which are compatible with devices operating at a nominal supply voltage of either 5.0 or 3.3V. In order to allow interfacing of 3.3V devices and 5.0V devices, all inputs shall be able to tolerate input potentials of 5.5V.

7.2 Signal Paths

All connections are intended to be point-to-point connections on PCBs. Typically these connections can be treated as electrically short paths and transmission line reflections can be safely ignored. Neither a connector nor a characteristic impedance for electrically long PCB traces is within the scope of this specification.

The output drive is recommended to be kept as low as possible to minimize board level noise and EMI.

7.3 DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V _{ih}		2.0			V
Input Low Voltage	V _{il}				0.8	V
Input High Current	I _{ih}	V _i =5.5V			200	uA
	I _{ih}	V _i =3.6V			200	uA
Input Low Current	I _{il}	V _i =0.0	-20			uA

7.4 AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
	REF_CLK Fre- quency		50		MHz
	REF_CLK Duty Cycle	35		65	%
T _{su}	TXD[1:0], TX_EN,RXD[1:0], CRS_DV, RX_ER Data Setup to REF_CLK rising edge	4			ns
Thold	TXD[1:0], TX_EN,RXD[1:0], CRS_DV, RX_ER Data hold from REF_CLK rising edge	2			ns

7.4.1 AC Load

Output drivers shall be capable of meeting the output requirements while driving a 25pF or greater load. This loading accommodates over 12 inches of PCB trace and input capacitance of the receiving device.

7.4.2 AC Measurement

Timing measurements shall be referenced from the point at which the REF_CLK waveform crosses the reference voltage level (1.4 V) to the valid input or output levels.

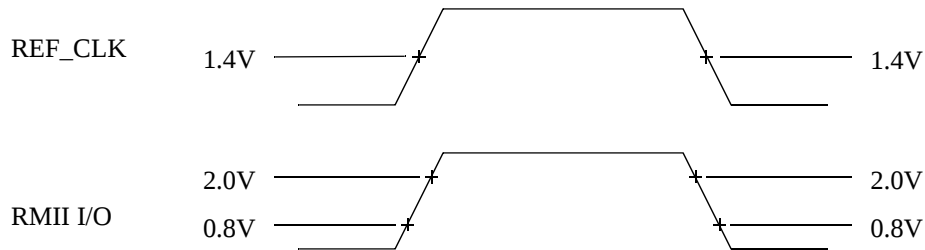


FIGURE 6. Input/Output Valid Level for AC Measurements

7.4.3 Rise and Fall Time

Output waveforms shall have a rise and fall time between 1 and 5 ns. This shall be measured between the points on the waveform which cross 0.8V and 2.0V.



FIGURE 7. Input/Output Valid Level for AC Measurements

8.0 System Considerations

8.1 Bit Budget Impact

The PHY interface is terminated into a DTE (MAC) when the RMII specification is used in a switch application. While the data may experience additional latency on receive, the control signals have been defined such that the system requirements of IEEE 802.3u [2] are met.

In the case where a device simply provides a mapping between the MII and the RMII specification at both the PHY and the MAC, the bit budget may be affected. System integrators should check the specifications of MAC and PHY chips in determining whether the bit budgets in IEEE 802.3u [2] are met.

8.2 Transmit IPG

Since the RMII specification defines an inherently full duplex interface (i.e. there is no loopback of data or carrier from transmit to receive), the delay through the PHY may increase the IPG as seen on the wire if the MAC uses a local timer that corresponds to the IPG timing parameters in IEEE 802.3 [1] and IEEE 802.3u [2]. While it is not a violation to increase this gap, switches are often measured by their ability to achieve “wire speed”.

An alternative to increasing the IPG due to lack of feedback of PHY delay is to allow the MAC’s IPG timer to be smaller than the required parameter by a programmable amount that can be modified to account for the PHY delay such that “wire speed” performance is possible. Note that this is typically the case for “wire speed” devices under IEEE 802.3 [1] and IEEE 802.3u [2] and is not an issue unique to the RMII specification.

The architecture of MACs which rely on feedback through loopback of TX_EN to CRS may be preserved by performing an internal loopback in Half Duplex mode with a delay element that can be programmed to match the delay through the PHY.

8.3 Receive IPG

In order to provide a single synchronous clock reference for all the data interfaces in a multiple port system, some buffering in the PHY is required to account for differences in local versus recovered clock. The depth of this buffer has the potential to increase the back to back receive IPG if no other precautions were taken. In order to avoid changing IPG as seen by the MAC, this buffer must be smaller than the minimum IPG encountered in real networks.

While the IEEE 802.3 standard [1] ensures that no MAC transmitter ever creates an IPG of less than 96 bits, there are real world scenarios where IPG shrinks (e.g. through repeaters). In no case should an IPG shrink below 36 bits. 36 bits gives sufficient margin for implementations to deal with clock variances over stream lengths consistent with Ethernet framing.

9.0 Future Considerations

This specification as written provides a comprehensive solution to reducing the pin count of the MII interface. It has been written to be forward compatible with ideas that are currently beyond the scope of this specification. It is envisioned that this specification may be updated or have an addendum which covers additional desired functionality.

9.1 Out of Band Signalling

The MII's MDIO/MDC management interface to the PHY provides a standard way to access registers within the PHY. It has been noted that a more real-time interface may be desirable. The values of TXD[1:0]/RXD[1:0] while TX_EN/CRS_DV are de-asserted represent unused code space. This specification specifically reserves this code space for future use. Of particular use is transferring speed, link, duplex mode information either from Auto-Negotiation to the MAC or from the MAC to configure the PHY.

10.0 References

- [1] ISO/IEC 8802-3: 1996, Information technology - Telecommunications and information exchange between systems - Local and metropolitan area networks - Specific requirements - Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications.
- [2] IEEE Std 802.3u, 1995, IEEE Standards for Local and Metropolitan Area Networks: Media Access Control (MAC) Parameters, Physical Layer, Medium Attachment Units, and Repeater for 100 Mb/s Operation, Type 100BASE-T.

RMII ConsortiumTM Addendum

1.0 Revision Control Policy

It is anticipated that additional companies will join the RMII Consortium over time. To accommodate this process this addendum will be provided along with the base specification as a single file. However, the revision reference will change independently from the revision number of the base specification to allow updated RMII Consortium membership information to be updated without implying that a change has occurred to the base specification.

2.0 Membership Updates

Updates will be provided to the RMII Consortium addendum once 5 or more companies are to be added or within 30 days of becoming an RMII Consortium member.

3.0 Web Site

The RMII Consortium maintains a web site at <http://www.rmii-consort.com>

A copy of the specification and current RMII Consortium information is maintained at this location.

4.0 Reflector

The RMII Consortium maintains a reflector to facilitate communication regarding the RMIITM specification. To join the reflector, send an email to:

listserv@jupiter.national.com

In the body, include:

subscribe rmii_consort

Send messages to rmii_consort@jupiter.national.com to communicate with other parties interested in the RMII specification.

5.0 Relationship to IEEE 802

The RMII specification is intended to be an embodiment of an interface that is logically equivalent to the MII, specified originally in IEEE 802.3u, which is optimized for a more limited application space. As such, it is anticipated that vendors may choose to conform with the RMII specification in addition to IEEE 802.3 in the implementation of products in order to obtain the benefits for that application. The RMII Consortium has made and will continue to make efforts to keep the IEEE 802.3 committee informed of developments made to the RMII specification since it is directly applicable to products which comply with the standards they produce and we share the mutual goal of interoperability.

Also, the IEEE 802.5 Working Group has established the High Speed Token Ring Task Force which is chartered to produce “P802.5t 100 Mbit/s Dedicated Token Ring over 2 or 4 pair cabling”. As part of this effort, the committee has decided to leverage the PHY technology originally specified and developed as a result of the IEEE 802.3u project. However, there are a set of additional requirements that are specific to the support of High Speed Token Ring applications which are different than that of typical 100BASE-TX physical layer products on the market as of this writing. Some of these requirements are specific to the internal functions of the physical layer, some require configuration for independent applications, and some require alterations to the signaling in the event that the RMII specification is to be used to support High Speed Token Ring.

The RMII Consortium is limited in scope to a fixed interface definition and does not control management variables that allow configuration of independent modes. Also, the RMII specification cannot mandate specifics to physical layer internals. However, the RMII Consortium feels that it is important to highlight the existence of normative requirements in the above mentioned IEEE 802.5 document and to encourage 100BASE-TX compliant physical layer products to incorporate these functions so that products based on either IEEE 802.3u or IEEE 802.5t may be built with the same silicon. The similarities between these two applications should allow physical layer vendors to build dual mode products and allow IEEE 802.5t based products to utilize the advantages of the RMII specification. Currently “P802.5t 100 Mbit/s Dedicated Token Ring over 2 or 4 pair cabling” is in draft status in the IEEE 802.5 High Speed Token Ring Task Force. Please refer to this document for the specifics of the modifications. As with IEEE 802.3, the RMII consortium will endeavor to keep the IEEE 802.5 committee informed of any specification developments.

6.0 RMII Consortium Members

3Com Corporation*

AMD Inc.

Bay Networks, Inc.*

Broadcom Corp.

National Semiconductor Corp.

Texas Instruments Inc.

The companies indicated by * are included pending execution of an Adopter's Agreement based on support for RMII Specification 1.0.
