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TMS320DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Real-Time Interrupt (RTI)

Reference Guide

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Contents

Preface **7**

1 Introduction 11

1.1 Main Features 11

1.2 Block Diagram 12

2 Module Operation 13

2.1 Counter Operation 13

2.2 Digital Watchdog 13

2.3 Suspend Mode Behavior 13

3 Registers for RTI 15

3.1 RTI Global Control Register (RTIGCTRL) 16

3.2 RTI Compare Control Register (RTICOMPCTRL) 17

3.3 RTI Free Running Counter 0 Register (RTIFRC0) 18

3.4 RTI Up Counter 0 Register (RTIUC0) 18

3.5 RTI Compare Up Counter 0 Register (RTICPUC0) 19

3.6 RTI Free Running Counter 1 Register (RTIFRC1) 20

3.7 RTI Up Counter 1 Register (RTIUC1) 20

3.8 RTI Compare Up Counter 1 Register (RTICPUC1) 21

3.9 RTI Compare 0 Register (RTICOMP0) 21

3.10 RTI Update Compare 0 Register (RTIUDCP0) 21

3.11 RTI Compare 1 Register (RTICOMP1) 22

3.12 RTI Update Compare 1 Register (RTIUDCP1) 22

3.13 RTI Compare 2 Register (RTICOMP2) 22

3.14 RTI Update Compare 2 Register (RTIUDCP2) 23

3.15 RTI Compare 3 Register (RTICOMP3) 23

3.16 RTI Update Compare 3 Register (RTIUDCP3) 24

3.17 RTI Set/Status Interrupt Register (RTISETINT) 24

3.18 RTI Clear/Status Interrupt Register (RTICLEARINT) 26

3.19 RTI Interrupt Flag Register (RTIINTFLAG) 27

3.20 Digital Watchdog Control Register (RTIDWDCTRL) 28

3.21 Digital Watchdog Preload Register (RTIDWDPRLD) 29

3.22 Watchdog Status Register (RTIWDSTATUS) 29

3.23 Watchdog Key Register (RTIWDKEY) 30

3.24 WDKEY Digital Watchdog Down Counter (RTIDWDCNTR) 31

A Revision History **33**

List of Figures

1 Block Diagram 12
2 Digital Watchdog 13
3 RTI Global Control Register (RTIGCTRL) 16
4 RTI Compare Control Register (RTICOMPCTRL) 17
5 RTI Free Running Counter 0 Register (RTIFRC0) 18
6 RTI Up Counter 0 Register (RTIUC0) 18
7 RTI Compare Up Counter 0 Register (RTICPUC0) 19
8 RTI Free Running Counter 1 Register (RTIFRC1) 20
9 RTI Up Counter 1 Register (RTIUC1) 20
10 RTI Compare Up Counter 1 Register (RTICPUC1) 21
11 RTI Compare 0 Register (RTICOMP0) 21
12 RTI Update Compare 0 Register (RTIUDCP0) 21
13 RTI Compare 1 Register (RTICOMP1) 22
14 RTI Update Compare 1 Register (RTIUDCP1) 22
15 RTI Compare 2 Register (RTICOMP2) 22
16 RTI Update Compare 2 Register (RTIUDCP2) 23
17 RTI Compare 3 Register (RTICOMP3) 23
18 RTI Update Compare 3 Register (RTIUDCP3) 24
19 RTI Set/Status Interrupt Register (RTISETINT) 24
20 RTI Clear/Status Interrupt Register (RTICLEARINT) 26
21 RTI Interrupt Flag Register (RTIINTFLAG) 27
22 Digital Watchdog Control Register (RTIDWDCTRL) 28
23 Digital Watchdog Preload Register (RTIDWDPRLD) 29
24 Watchdog Status Register (RTIWDSTATUS) 29
25 Watchdog Key Register (RTIWDKEY) 30
26 WDKEY Digital Watchdog Down Counter (RTIDWDCNTR) 31

List of Tables

1 RTI Registers 15
2 RTI Global Control Register (RTIGCTRL) Field Descriptions 16
3 RTI Compare Control Register (RTICOMPCTRL) Field Descriptions 17
4 RTI Free Running Counter 0 Register (RTIFRC0) Field Descriptions 18
5 RTI Up Counter 0 Register (RTIUC0) Field Descriptions 18
6 RTI Compare Up Counter 0 Register (RTICPUC0) Field Descriptions 19
7 RTI Free Running Counter 1 Register (RTIFRC1) Field Descriptions 20
8 RTI Up Counter 1 Register (RTIUC1) Field Descriptions 20
9 RTI Compare Up Counter 1 Register (RTICPUC1) Field Descriptions 21
10 RTI Compare 0 Register (RTICOMP0) Field Descriptions 21
11 RTI Update Compare 0 Register (RTIUDCP0) Field Descriptions 21
12 RTI Compare 1 Register (RTICOMP1) Field Descriptions 22
13 RTI Update Compare 1 Register (RTIUDCP1) Field Descriptions 22
14 RTI Compare 2 Register (RTICOMP2) Field Descriptions 22
15 RTI Update Compare 2 Register (RTIUDCP2) Field Descriptions 23
16 RTI Compare 3 Register (RTICOMP3) Field Descriptions 23
17 RTI Update Compare 3 Register (RTIUDCP3) Field Descriptions 24
18 RTI Set/Status Interrupt Register (RTISETINT) Field Descriptions 25
19 RTI Clear/Status Interrupt Register (RTICLEARINT) Field Descriptions 26
20 RTI Interrupt Flag Register (RTIINTFLAG) Field Descriptions 27
21 Digital Watchdog Control Register (RTIDWDCTRL) Field Descriptions 28
22 Digital Watchdog Preload Register (RTIDWDPRLD) Field Descriptions 29
23 Watchdog Status Register (RTIWDSTATUS) Field Descriptions 29
24 Watchdog Key Register (RTIWDKEY) Field Descriptions 30
25 Example of a WDKEY Sequence 30
26 WDKEY Digital Watchdog Down Counter (RTIDWDCNTR) Field Descriptions 31
A-1 Revisions 33

Read This First

About this Manual

This document describes the operation of the Real-Time Interrupt (RTI) module in the TMS320DRx40x/41x digital signal processors (DSPs).

Notational Conventions

This document uses the following conventions:

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in chapter and described in tables
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DRx40x/41x Digital Media System-on-Chip (DMSoC).

SPRUF06— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Real-Time Interrupt (RTI) Reference Guide.*

Describes the operation of the Real-Time Interrupt (RTI) module in the DRx40x/41x Digital Media System-on-Chip (DMSoC).

SPRUF07 — *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor ARM Subsystem Reference Guide.*

Describes the ARM subsystem in the DRx40x/41x Digital Media System-on-Chip (DMSoC). The chip's programmability comes from an ARM926 RISC processor core and a C6000™ TI DSP subsystem.

SPRUF09— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Enhanced (EDMA) Controller Reference Guide.*

Describes the operation of the enhanced direct memory access (EDMA) controller in the DRx40x/41x Digital Media System-on-Chip (DMSoC).

SPRUF12— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor External Memory Interface (EMIF) Reference Guide.*

Describes the operation of the external memory interface (EMIF) in the DRx40x/41x Digital Media System-on-Chip (DMSoC).

SPRUF13— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Multichannel Audio Serial Port (McASP) Reference Guide.*

Describes the operation of the audio serial port (ASP) audio interface in the DRx40x/41x Digital Media System-on-Chip (DMSoC).

SPRUF14— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Enhanced Capture (eCAP) Module Reference Guide.*

Describes this module's essential use in systems where accurate timing of external events is important. Includes all flash-based, ROM-based, and RAM-based devices within the DRx40x/41x Digital Media System-on-Chip (DMSoC).

SPRUF15— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Serial Peripheral Interface (SPI) Reference Guide.*

Describes the serial peripheral interface (SPI) in the DRx40x/41x Digital Media System-on-Chip (DMSoC).

SPRUF16— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Universal Asynchronous Receiver/Transmitter (UART) Reference Guide.*

Describes the universal asynchronous receiver/transmitter (UART) peripheral in the DRx40x/41x Digital Media System-on-Chip (DMSoC).

SPRUF17— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Inter-Integrated Circuit (I2C) Peripheral Reference Guide.*

Describes the inter-integrated circuit (I2C) peripheral in the DRx40x/41x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with Phillips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. This document assumes the reader is familiar with the I2C-bus specification.

SPRUF18— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor General-Purpose Input/Output (GPIO) Reference Guide.*

Describes the general-purpose input/output (GPIO) peripheral in the DRx40x/41x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of an internal register. When configured as an output you can write to an internal register to control the state driven on the output pin.

SPRUF19— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Universal Serial Bus (USB) v2.0 On The Go (OTG) Reference Guide.*

Describes the universal serial bus (USB) controller in the DRx40x/41x Digital Media System-on-Chip (DMSoC). The controller supports high-speed USB peripheral mode and high-speed limited host-mode operations. The USB controller can be operated by ARM through the memory-mapped registers.

SPRUF20— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Video Processing Front End (VPFE) Reference Guide.*

Describes the video processing front end (VPFE) controller in the DRx40x/41x Digital Media System-on-Chip (DMSoC). The DRx40x/41x video processing subsystem (VPSS) includes a video processing front-end (VPFE) controller, which is the video input portion of the DRx40x/41x system-on-chip (SoC). The VPFE controller receives input video/image data from external capture devices and stores it to external memory.

SPRUF21— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Multimedia Card (MMC)/Secure Digital (SD) Card Controller Reference Guide.*

Describes the multimedia card (MMC)/secure digital (SD) card controller in the DRx40x/41x Digital Media System-on-Chip (DMSoC). The MMC/SD card is used in a number of applications to provide removable data storage.

SPRUF22— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor High-End CAN Controller (HECC) Reference Guide.*

Gives a general description of the controller area network (CAN). This document describes the CAN controllers, the standard CAN controller (SCC), and the high-end CAN Controller (HECC) of the DRx40x/41x Digital Media System-on-Chip (DMSoC).

SPRUF23— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor (SPDIF-DOR) Reference Guide.*

Describes the operation and configuration of the S/PDIF data-only receiver module. the S/PDIF standard provides a common interface for digital audio signals.

SPRUF24— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor DSP Subsystem Reference Guide.*

Describes the digital signal processor (DSP) subsystem in the DRx04x/41x digital media system-on-chip (DMSoC).

SPRUF25— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Viterbi-Decoder Coprocessor 2 (VCP2) Reference Guide.*

Describes the VCP2 processor for the DRx40x/41x digital media processor system-on-chip (DMSoC).

SPRUF26— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor System Architecture Reference Guide.*

Describes the system architecture for the DRx40x/41x digital media processor system-on-chip (DMSoC).

SPRUF29— *DRx40x/41x Automotive Digital Radio and Infotainment Applications Processor Bootloader Reference Guide.*

Describes the features of the on-chip ARM ROM bootloader (RBL) that is on the DRx40x/41x digital media processor system-on-chip (DMSoC).

Trademarks

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Reference Guide
SPRUF06A–June 2007–Revised October 2008

TMS320DRx40x/41x DSP Real-Time Interrupt (RTI)

This guide describes the functionality of the Real-Time Interrupt Module used in TMS320DRx40x/41x DSPs.

1 Introduction

The Real-Time Interrupt (RTI) module provides general-purpose timer functionality. Two examples of how the timer may be used are for operating systems and for benchmarking code. For operating systems, the module incorporates several counters which define the timebases needed for scheduling. For benchmarking, the timers give the ability to read the counter contents at the beginning and the end of the code to be benchmarked.

The processor has two RTIs: RTI0 which is accessible only by ARM, and RTI1 which can be accessed by either ARM or DSP. Since RTI0 feeds the ARM Watchdog and RTI1 feeds the DSP Watchdog, RTI0 and RTI1 would typically be associated with ARM and DSP, respectively. However, ARM can utilize RTI1 as well.

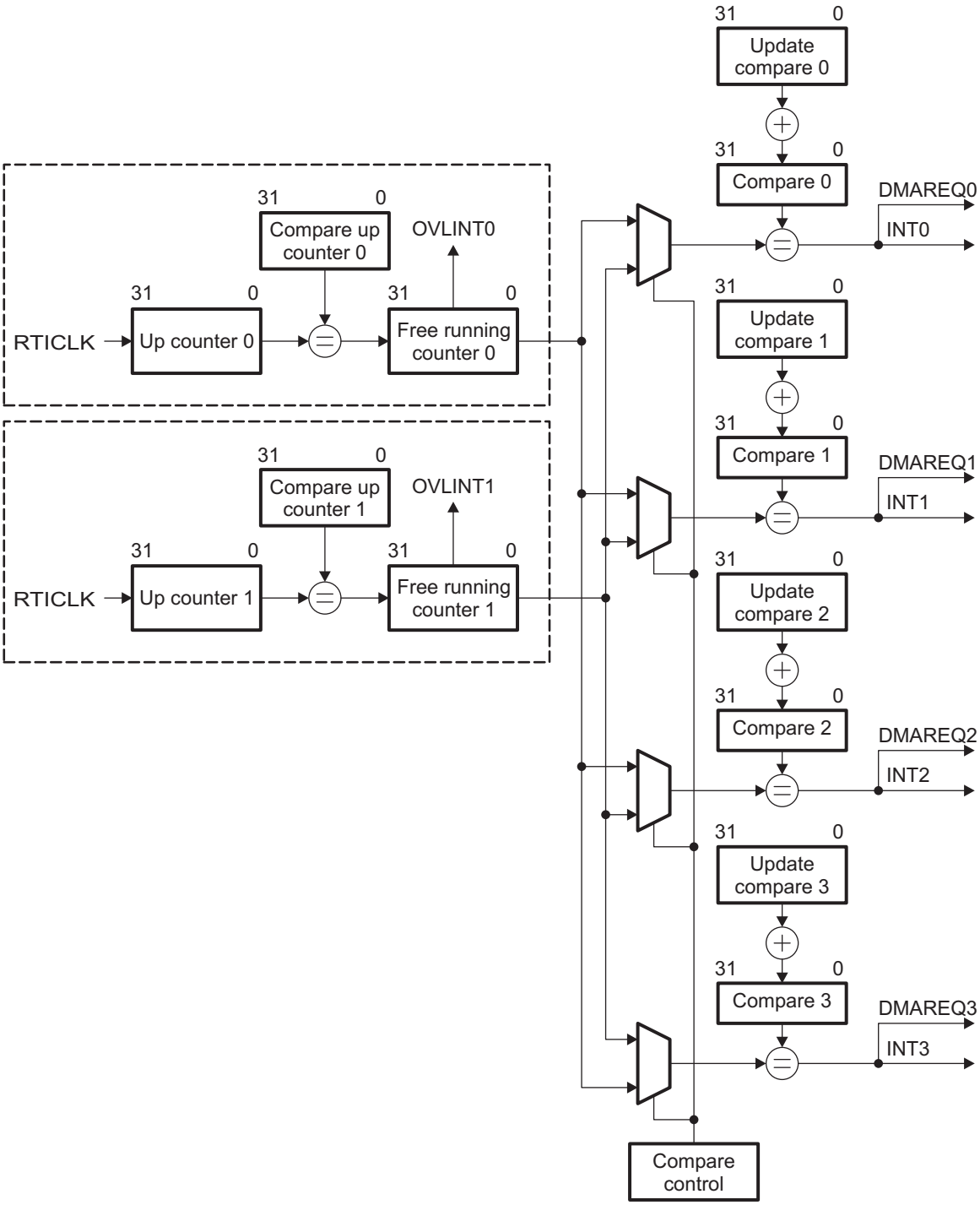
1.1 Main Features

- Two independent counter blocks for generating different timebases
  - Each block consists of:
    - One 32-bit prescale counter
    - One 32-bit free-running counter
- Free-running counters 0 and 1 can be incremented by the internal prescale counter
- Four configurable compare registers for interrupt generation, working either with counter 0 or counter 1. Compare 0 to 3 can also generate DMA request signals
- Automatic update of all compare registers on compare match to generate periodic interrupts
- Fast enabling/disabling of interrupts
- Digital Watchdog
- RTI clock input (RTICLK) can be selected via the MISC_CTL0 register of the device configuration module, either as SYSCLK8 or OSC0 AUXCLK.

1.2 Block Diagram

The RTI block diagram is shown in Figure 1.

Figure 1. Block Diagram



2 Module Operation

2.1 Counter Operation

The two counter blocks provide the same base functionality. Each block consists of two 32-bit up-counters (Up-Counter and Free-Running Counter). The Up-Counter (UCx) is driven by the RTICLK and counts up until the compare value in the Compare Up-Counter register (CPUCx) is reached. When the compare matches, the second counter, the Free-Running Counter (FRCx), is incremented. At the same time, UCx is reset to zero. If FRCx overflows, an interrupt is generated.

When both counter values need to be determined, first the Free-Running Counter register must be read to serve as a baseline and to ensure consistency. Concurrently, on the CPU cycle on which the Free-Running Counter is read, the Up-Counter value is stored in the Up-Counter register. Finally, the newly updated Up-Counter register may be read.

Four Compare registers (CPx) are available to generate interrupt requests and/or DMA events to the device. Each of the Compare registers can be configured to work with either FRC0 or FRC1. When the Free-Running Counter value matches the Compare value, an interrupt and/or DMA event is generated. All Compare registers provide an additional feature. When a match occurs, the value in the Update Compare register (UDCPx) is added to the value in the Compare registers (CPx). This enables periodic interrupts/DMA requests to be generated, without having to update the Compare registers in software.

2.2 Digital Watchdog

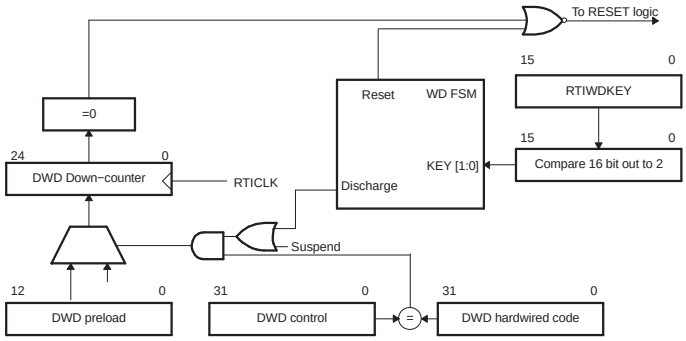
The digital watchdog (DWD) generates resets to prevent runaway code (see Figure 2). A reset is generated after a programmable period, if no correct key sequence was written to the RTIWDKEY register. By default, the digital watchdog is disabled; however, it can be enabled by writing to the RTIDWDCTRL register, a 32-bit value which is the inverted value of the hardwired code in the module. Once the DWD is enabled, it cannot be disabled.

If the correct key sequence is written to the RTIWDKEY register (0xE51A followed by 0xA35C), the 25-bit DWD Down-Counter is reloaded with the 13-bit preload value stored in RTIDWDPRLD. If the incorrect values are written, a watchdog reset will occur immediately. A reset will also be generated, when the DWD Down-Counter is decremented (with RTICLK frequency) to 0. While the device is in debug mode (suspend), the DWD Down-Counter keeps the value it had when entering debug mode. The expiration time of the DWD Down-Counter can be determined with following equation:

Equation 1:

t_{exp} = (RTIDWDPRLD+1) x 2^{13} / RTICLK
where: RTIDWDPRLD = 0...8191

Figure 2. Digital Watchdog



2.3 Suspend Mode Behavior

Once the system enters suspend mode, the behaviour of the RTI depends on the COS bit (RTIGCTRL.15). If the bit is cleared and suspend is active, all counters will stop operation. If the bit is set to one, all counters will be clocked normally and the RTI will work in normal mode.

3 Registers for RTI

The RTI registers shown in Table 1. The offset is relative to the peripheral base address (see the device's datasheet).

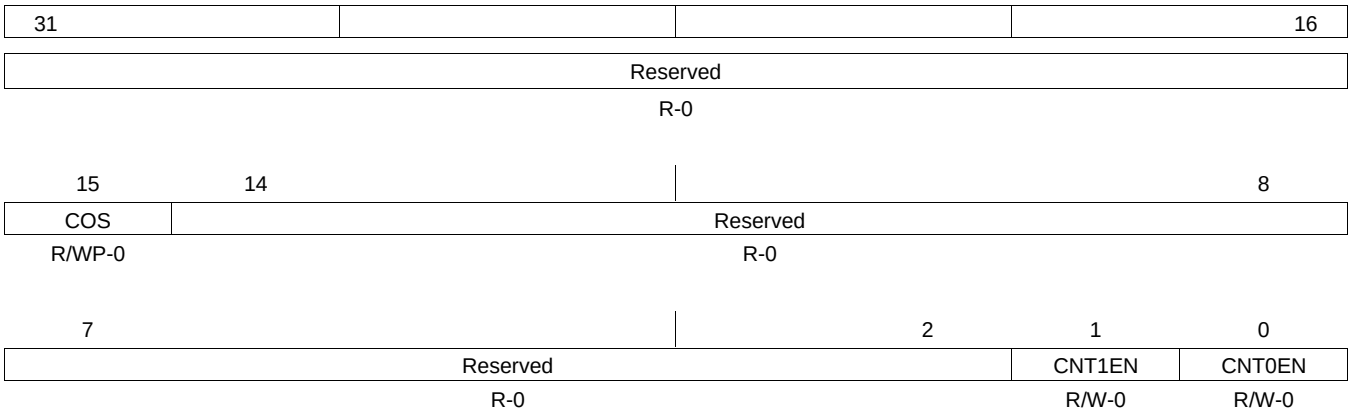
Table 1. RTI Registers

Offset	Acronym	Register Description
00h	RTIGCTRL	Global Control Register. Starts / stops the counters.
04h	Reserved	Reserved bit.
0Ch	RTICOMPCTRL	Compare Control. Controls the source for the compare registers.
10h	RTIFRC0	Free-Running Counter 0. Current value of free running counter 0.
14h	RTIUC0	Up-Counter 0. Current value of prescale counter 0.
18h	RTICPUC0	Compare Up-Counter 0. Compare value compared with prescale counter 0.
30h	RTIFRC1	Free-Running Counter 1. Current value of free running counter 1.
34h	RTIUC1	Up-Counter 1. Current value of prescale counter 1.
38h	RTICPUC1	Compare Up-Counter 1. Compare value compared with prescale counter 1.
50h	RTICOMP0	Compare 0. Compare value to be compared with the counters.
54h	RTIUDCP0	Update Compare 0. Value to be added to the compare register 0 value on compare match.
58h	RTICOMP1	Compare 1. Compare value to be compared with the counters.
5Ch	RTIUDCP1	Update Compare 1. Value to be added to the compare register 1 value on compare match.
60h	RTICOMP2	Compare 2. Compare value to be compared with the counters.
64h	RTIUDCP2	Update Compare 2. Value to be added to the compare register 2 value on compare match.
68h	RTICOMP3	Compare 3. Compare value to be compared with the counters.
6Ch	RTIUDCP3	Update Compare 3. Value to be added to the compare register 3 value on compare match.
70h	Reserved	Reserved bit.
74h	Reserved	Reserved bit.
80h	RTISETINT	Set Interrupt Enable. Sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.
84h	RTICLEARINT	Clear Interrupt Enable. Clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.
88h	RTIINTFLAG	Interrupt Flags. Interrupt pending bits.
90h	RTIDWDCTRL	Digital Watchdog Control. Enables the Digital Watchdog.
94h	RTIDWDPRLD	Digital Watchdog Preload. Sets the experation time of the Digital Watchdog.
98h	RTIWDSTATUS	Watchdog Status. Reflects the status of Analog and Digital Watchdog.
9Ch	RTIWDKEY	Watchdog Key. Correct written key values discharge the external capacitor.
A0h	RTIDWDCNTR	Digital Watchdog Down-Counter

3.1 RTI Global Control Register (RTIGCTRL)

The RTI Global Control register (RTIGCTRL) is shown in Figure 3 and described in Table 2.

Figure 3. RTI Global Control Register (RTIGCTRL)



LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 2. RTI Global Control Register (RTIGCTRL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved		Reads return 0 and writes have no effect
15	COS		Continue On Suspend. This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting.
		0	Stop counters in debug mode
		1	Continue counting in debug mode
14-2	Reserved		Reads return 0 and writes have no effect
1	CNT1EN		Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block 1 (UC1 and FRC1).
		0	Stop counters
		1	Start counters
0	CNT0EN		Counter 0 Enable. The CNT0EN bit starts and stops the operation of counter block 0 (UC0 and FRC0).
		0	Stop counters
		1	Start counters

3.2 RTI Compare Control Register (RTICOMPCTRL)

The RTI compare control register (RTICOMPCTRL) is shown in Figure 4 and described in Table 3.

Figure 4. RTI Compare Control Register (RTICOMPCTRL)

31	16
Reserved	
R-0	

15	13	12	11	9	8
Reserved		COMPSEL3	Reserved		COMPSEL2
R-0		R/W-0	R-0		R/W-0

7	5	4	3	1	0
Reserved		COMPSEL1	Reserved		COMPSEL0
R-0		R/W-0	R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

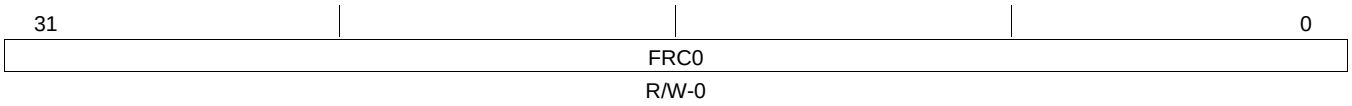
Table 3. RTI Compare Control Register (RTICOMPCTRL) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved		Reads return 0 and writes have no effect
12	COMPSEL3		Compare Select 3. This bit determines the counter with which the compare value hold in compare register 3 is compared.
		0	Enable compare with FRC 0
		1	Enable compare with FRC 1
11-9	Reserved		Reads return 0 and writes have no effect
8	COMPSEL2		Compare Select 2. This bit determines the counter with which the compare value hold in compare register 2 is compared.
		0	Enable compare with FRC 0
		1	Enable compare with FRC 1
7-5	Reserved		Reads return 0 and writes have no effect
4	COMPSEL1		Compare Select 1. This bit determines the counter with which the compare value hold in compare register 1 is compared.
		0	Enable compare with FRC 0
		1	Enable compare with FRC 1
3-1	Reserved		Reads return 0 and writes have no effect
0	COMPSEL0		Compare Select 0. This bit determines the counter with which the compare value hold in compare register 0 is compared.
		0	Enable compare with FRC 0
		1	Enable compare with FRC 1

3.3 RTI Free Running Counter 0 Register (RTIFRC0)

The RTI Free-Running counter 0 register (RTIFRC0) is shown in Figure 5 and described in Table 4.

Figure 5. RTI Free Running Counter 0 Register (RTIFRC0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

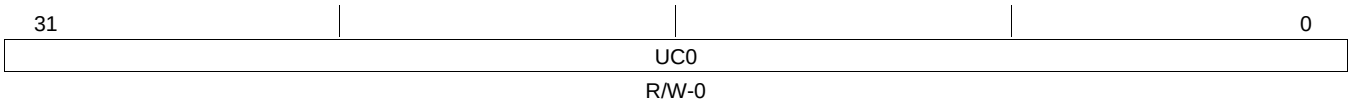
Table 4. RTI Free Running Counter 0 Register (RTIFRC0) Field Descriptions

Bit	Field	Value	Description
31-0	FRC0	0-FFFF FFFFh	Free-Running Counter 0. This register holds the current value of the Free-Running Counter 0 and will be updated continuously. The counter can be preset by writing to this register. The counter then increments from this preset value upwards. If counters have to be preset, they first have to be disabled in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.

3.4 RTI Up Counter 0 Register (RTIUC0)

The RTI Up-Counter 0 register (RTIUC0) is shown in Figure 6 and described in Table 5.

Figure 6. RTI Up Counter 0 Register (RTIUC0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5. RTI Up Counter 0 Register (RTIUC0) Field Descriptions

Bit	Field	Value	Description
31-0	UC0	0-FFFF FFFFh	Up-Counter 0. This register holds the current value of the Up-Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free-Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up-Counter 0 and Free-Running Counter 0. The counter can be preset by writing to this register. The counter then increments from this preset value upwards. If counters have to be preset, they first have to be disabled in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. If the preset value is bigger than the compare value stored in register RTICPUC0, then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.

3.5 RTI Compare Up Counter 0 Register (RTICPUC0)

The RTI Compare Up-Counter 0 register (RTICPUC0) is shown in Figure 7 and described in Table 6.

Figure 7. RTI Compare Up Counter 0 Register (RTICPUC0)

31	0
CPUC0	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 6. RTI Compare Up Counter 0 Register (RTICPUC0) Field Descriptions

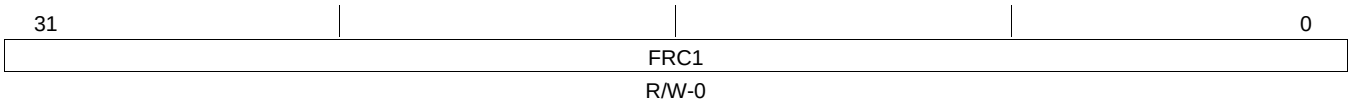
Bit	Field	Value	Description
31-0	CPUC0	0-FFFF FFFFh	Compare Up-Counter 0. This register holds the compare value, which is compared with the Up-Counter 0. When the compare matches, the Free-Running counter 0 is incremented and the Up-Counter is set to zero. The value set in this register prescales the RTI clock. See the equation below.

$$f_{FRC0} = \frac{RTCLK}{CPUC0 + 1}$$

3.6 RTI Free Running Counter 1 Register (RTIFRC1)

The RTI Free-Running Counter 1 register (RTIFRC1) is shown in Figure 8 and described in Table 7.

Figure 8. RTI Free Running Counter 1 Register (RTIFRC1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

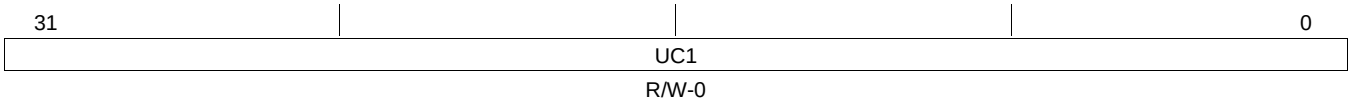
Table 7. RTI Free Running Counter 1 Register (RTIFRC1) Field Descriptions

Bit	Field	Value	Description
31-0	FRC1	0-FFFF FFFFh	Free-Running Counter 1. This register holds the current value of the Free-Running Counter 1 and will be updated continuously. This counter can be preset by writing to this register and then increments from this preset value upwards. If counters have to be preset, they have to be disabled first in the RTIGCTRL register in order to ensure consistency between UC1 and FRC1.

3.7 RTI Up Counter 1 Register (RTIUC1)

The RTI Up-Counter 1 register (RTIUC1) is shown in Figure 9 and described in Table 8.

Figure 9. RTI Up Counter 1 Register (RTIUC1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

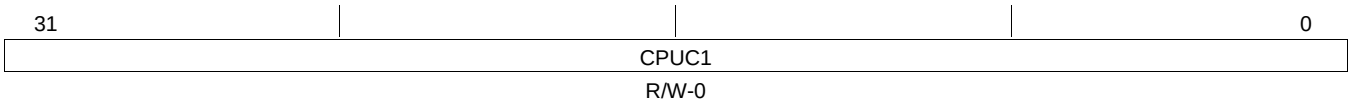
Table 8. RTI Up Counter 1 Register (RTIUC1) Field Descriptions

Bit	Field	Value	Description
31-0	UC1	0-FFFF FFFFh	Up Counter 1. This register holds the current value of the Up-Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64-bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up-Counter 1 and Free-Running Counter 1. The counter can be preset by writing to this register. The counter increments then from this written value upwards. If counters have to be preset, they first have to be disabled in the RTIGCTRL register in order to ensure consistency between UC1 and FRC1. If the preset value is bigger than the compare value stored in register RTICPUC1, then it can take a long time until a compare matches, since UC1 has to count up until it overflows.

3.8 RTI Compare Up Counter 1 Register (RTICPUC1)

The RTI Compare Up-Counter 1 register (RTICPUC1) is shown in Figure 10 and described in Table 9.

Figure 10. RTI Compare Up Counter 1 Register (RTICPUC1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

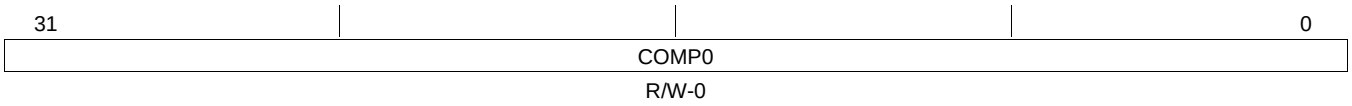
Table 9. RTI Compare Up Counter 1 Register (RTICPUC1) Field Descriptions

Bit	Field	Value	Description
31-0	CPUC1	0-FFFF FFFFh	Compare Up-Counter 1. This register holds the compare value, which is compared with the Up-Counter 1. When the compare matches, Free-Running Counter 1 is incremented and the Up-Counter is set to zero. The value set in this register prescales the RTI clock.

3.9 RTI Compare 0 Register (RTICOMP0)

The RTI Compare 0 register (RTICOMP0) is shown in Figure 11 and described in Table 10.

Figure 11. RTI Compare 0 Register (RTICOMP0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

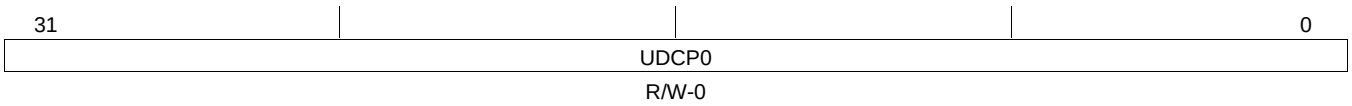
Table 10. RTI Compare 0 Register (RTICOMP0) Field Descriptions

Bit	Field	Value	Description
31-0	COMP0	0-FFFF FFFFh	Compare 0. This register holds a value, which is compared with the counter selected in the compare control logic (RTICOMPCTRL). If the Free-Running Counter matches the compare value, an interrupt is flagged and/or a DMA request is initiated, depending on the configuration of RTISETINT. A reset does not generate a compare match since the compare logic will only be active when the associated counter block is enabled in RTIGCTRL.

3.10 RTI Update Compare 0 Register (RTIUDCP0)

The RTI Update Compare 0 register (RTIUDCP0) is shown in Figure 12 and described in Table 11.

Figure 12. RTI Update Compare 0 Register (RTIUDCP0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

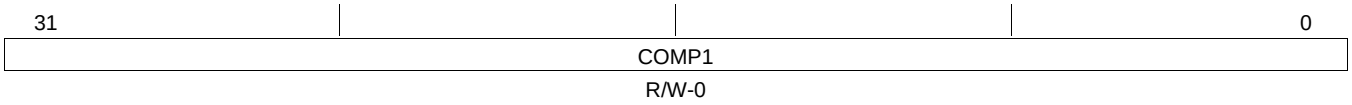
Table 11. RTI Update Compare 0 Register (RTIUDCP0) Field Descriptions

Bit	Field	Value	Description
31-0	UDCP0	0-FFFF FFFFh	Update Compare 0 Register. This register holds a value, which is added to the value in the Compare 0 register (RTICOMP0) each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.

3.11 RTI Compare 1 Register (RTICOMP1)

The RTI Compare 1 register (RTICOMP1) is shown in Figure 13 and described in Table 12.

Figure 13. RTI Compare 1 Register (RTICOMP1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

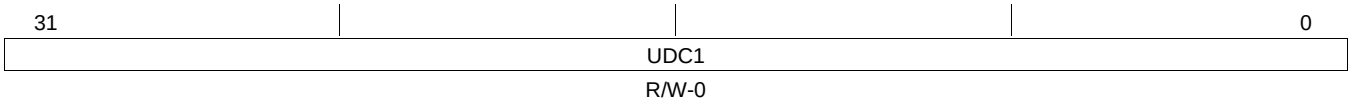
Table 12. RTI Compare 1 Register (RTICOMP1) Field Descriptions

Bit	Field	Value	Description
31-0	COMP1	0-FFFF FFFFh	Compare 1. This register holds a value, which is compared with the counter selected in the compare control logic (RTICOMPCTRL). If the Free-Running Counter matches the compare value, an interrupt is flagged and/or a DMA request is initiated, depending on the configuration of RTISETINT. A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled in RTIGCTRL.

3.12 RTI Update Compare 1 Register (RTIUDCP1)

The RTI Update Compare 1 register (RTIUDCP1) is shown in Figure 14 and described in Table 13.

Figure 14. RTI Update Compare 1 Register (RTIUDCP1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

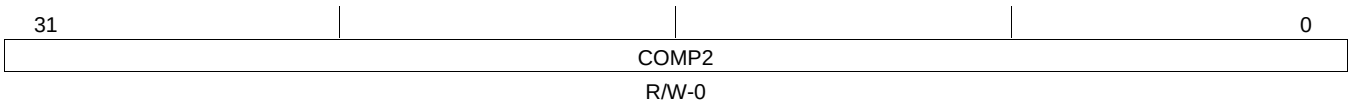
Table 13. RTI Update Compare 1 Register (RTIUDCP1) Field Descriptions

Bit	Field	Value	Description
31-0	UDCP1	0-FFFF FFFFh	Update Compare 1 Register. This register holds a value, which is added to the value in the Compare 1 register (RTICOMP0) each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.

3.13 RTI Compare 2 Register (RTICOMP2)

The RTI Compare 2 register (RTICOMP2) is shown in Figure 15 and described in Table 14.

Figure 15. RTI Compare 2 Register (RTICOMP2)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

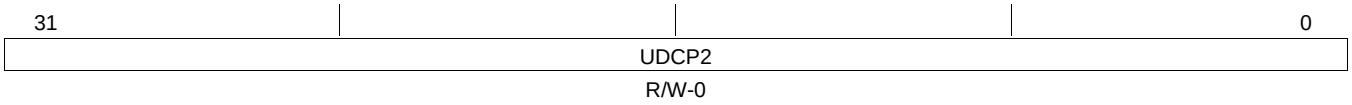
Table 14. RTI Compare 2 Register (RTICOMP2) Field Descriptions

Bit	Field	Value	Description
31-0	COMP2	0-FFFF FFFFh	Compare 2. This register holds a value, which is compared with the counter selected in the compare control logic (RTICOMPCTRL). If the Free-Running Counter matches the compare value, an interrupt is flagged and/or a DMA request is initiated, depending on the configuration of RTISETINT. A reset does not generate a compare match, since the compare logic will only be active when the associated counter block is enabled in RTIGCTRL.

3.14 RTI Update Compare 2 Register (RTIUDCP2)

The RTI Update Compare 2 register (RTIUDCP2) is shown in Figure 16 and described in Table 15.

Figure 16. RTI Update Compare 2 Register (RTIUDCP2)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

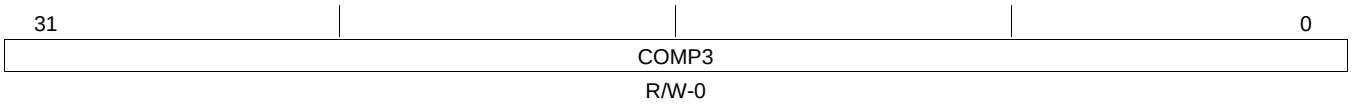
Table 15. RTI Update Compare 2 Register (RTIUDCP2) Field Descriptions

Bit	Field	Value	Description
31-0	UDCP2	0-FFFF FFFFh	Update Compare 2 Register. This register holds a value, which is added to the value in the Compare 2 register (RTICOMP0) each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.

3.15 RTI Compare 3 Register (RTICOMP3)

The RTI Compare 3 register (RTICOMP3) is shown in Figure 17 and described in Table 16.

Figure 17. RTI Compare 3 Register (RTICOMP3)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 16. RTI Compare 3 Register (RTICOMP3) Field Descriptions

Bit	Field	Value	Description
31-0	COMP3	0-FFFF FFFFh	Compare 3. This register holds a value, which is compared with the counter selected in the compare control logic (RTICOMPCTRL). If the Free-Running Counter matches the compare value, an interrupt is flagged and/or a DMA request is initiated, depending on the configuration of RTISETINT. A reset does not generate a compare match, since the compare logic will only be active when the associated counter block is enabled in RTIGCTRL.

3.16 RTI Update Compare 3 Register (RTIUDCP3)

The RTI update compare 3 register (RTIUDCP3) is shown in Figure 18 and described in Table 17.

Figure 18. RTI Update Compare 3 Register (RTIUDCP3)

31	0
UDCP3	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 17. RTI Update Compare 3 Register (RTIUDCP3) Field Descriptions

Bit	Field	Value	Description
31-0	UDCP3	0-FFFF FFFFh	Update Compare 3 Register. This register holds a value, which is added to the value in the Compare 3 register (RTICOMP0) each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.

3.17 RTI Set/Status Interrupt Register (RTISETINT)

The RTI set/status interrupt register (RTISETINT) is shown in Figure 19 and described in Table 18.

Figure 19. RTI Set/Status Interrupt Register (RTISETINT)

31	24
Reserved	
R-0	

23	19	18	17	16
Reserved		SETOVL1INT	SETOVL0INT	Reserved
R-0		R/W-0	R/W-0	R-0

15	12	11	10	9	8
Reserved		SETDMA3	SETDMA2	SETDMA1	SETDMA0
R-0		R/W-0	R/W-0	R/W-0	R/W-0

7	4	3	2	1	0
Reserved		SETINT3	SETINT2	SETINT1	SETINT0
R-0		R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

This register prevents the necessity of a read-modify-write operation if a particular interrupt should be enabled.

Table 18. RTI Set/Status Interrupt Register (RTISETINT) Field Descriptions

Bit	Field	Value	Description
31-19	Reserved		Reads return 0 and writes have no effect
18	SETOVL1INT		Set Free Running Counter 1 Overflow Interrupt
		0	Interrupt is disabled
		1	Interrupt is enabled
17	SETOVL0INT		Set Free Running Counter 0 Overflow Interrupt
		0	Interrupt is disabled
		1	Interrupt is enabled
16-12	Reserved		Reads return 0 and only writes of 0 allowed
11	SETDMA3		Set Compare DMA Request 3
		0	DMA request is disabled
		1	DMA request is enabled
10	SETDMA2		Set Compare DMA Request 2
		0	DMA request is disabled
		1	DMA request is enabled
9	SETDMA1		Set Compare DMA Request 1
		0	DMA request is disabled
		1	DMA request is enabled
8	SETDMA0		Set Compare DMA Request 0
		0	DMA request is disabled
		1	DMA request is enabled
7-4	Reserved		Reads return 0 and writes have no effect
3	SETINT3		Set Compare Interrupt 3
		0	Interrupt is disabled
		1	Interrupt is enabled
2	SETINT2		Set Compare Interrupt 2
		0	Interrupt is disabled
		1	Interrupt is enabled
1	SETINT1		Set Compare Interrupt 1
		0	Interrupt is disabled
		1	Interrupt is enabled
0	SETINT0		Set Compare Interrupt 0
		0	Interrupt is disabled
		1	Interrupt is enabled

3.18 RTI Clear/Status Interrupt Register (RTICLEARINT)

The RTI Clear/Status Interrupt (RTICLEARINT) register is shown in Figure 20 and described in Table 19.

Figure 20. RTI Clear/Status Interrupt Register (RTICLEARINT)

31	24
Reserved	
R-0	

23	19	18	17	16
Reserved		CLEAROVL1INT	CLEAROVL0INT	Reserved
R-0		R/W-0	R/W-0	R-0

15	12	11	10	9	8
Reserved		CLEARDMA3	CLEARDMA2	CLEARDMA1	CLEARDMA0
R-0		R/W-0	R/W-0	R/W-0	R/W-0

7	4	3	2	1	0
Reserved		CLEARINT3	CLEARINT2	CLEARINT1	CLEARINT0
R-0		R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

This register prevents the necessity of a read-modify-write operation if a particular interrupt should be disabled.

Table 19. RTI Clear/Status Interrupt Register (RTICLEARINT) Field Descriptions

Bit	Field	Value	Description
31-19	Reserved		Reads return 0 and writes have no effect
18	CLEAROVL1INT		Clear Free Running Counter 1 Overflow Interrupt
		0	Interrupt is disabled
		1	Interrupt is enabled
17	CLEAROVL0INT		Clear Free Running Counter 0 Overflow Interrupt.
		0	Interrupt is disabled
		1	Interrupt is enabled
16-12	Reserved		Reads return 0 and writes have no effect
11	CLEARDMA3		Clear Compare DMA Request 3
		0	DMA request is disabled
		1	DMA request is enabled
10	CLEARDMA2		Clear Compare DMA Request 2
		0	DMA request is disabled
		1	DMA request is enabled
9	CLEARDMA1		Clear Compare DMA Request 1.
		0	DMA request is disabled
		1	DMA request is enabled
8	CLEARDMA0		Clear Compare DMA Request 0.
		0	DMA request is disabled
		1	DMA request is enabled
7-4	Reserved		Reads return 0 and writes have no effect

Table 19. RTI Clear/Status Interrupt Register (RTICLEARINT) Field Descriptions (continued)

Bit	Field	Value	Description
3	CLEARINT3		Clear Compare Interrupt 3
		0	Interrupt is disabled
		1	Interrupt is enabled
2	CLEARINT2		Clear Compare Interrupt 2
		0	iIterrupt is disabled
		1	Interrupt is enabled
1	CLEARINT1		Clear Compare Interrupt 1
		0	Interrupt is disabled
		1	Interrupt is enabled
0	CLEARINT0		Clear Compare Interrupt 0
		0	Interrupt is disabled
		1	Interrupt is enabled

3.19 RTI Interrupt Flag Register (RTIINTFLAG)

The RTI interrupt flag register (RTIINTFLAG) is shown in Figure 21 and described in Table 20.

Figure 21. RTI Interrupt Flag Register (RTIINTFLAG)

31	24
Reserved	
R-0	

23	19	18	17	16
Reserved		OVL1INT	OVL0INT	Reserved
R-0		RC-0	RC-0	R-0

15	8
Reserved	
R-0	

7	4	3	2	1	0
Reserved		INT3	INT2	INT1	INT0
R-0		RC-0	RC-0	RC-0	RC-0

LEGEND: R = Read; C = Clear; -*n* = value after reset

The corresponding flags are set at every compare match of Free-Running Counterx and RTICOMPx value, regardless if the interrupt is enabled or not.

Table 20. RTI Interrupt Flag Register (RTIINTFLAG) Field Descriptions

Bit	Field	Value	Description
31-19	Reserved		Reads return 0 and writes have no effect
18	OVL1INT		Free Running Counter 1 Overflow Interrupt Flag
		0	No interrupt pending
		1	Interrupt pending
17	OVL0INT		Free Running Counter 0 Overflow Interrupt Flag
		0	No interrupt pending
		1	Interrupt pending

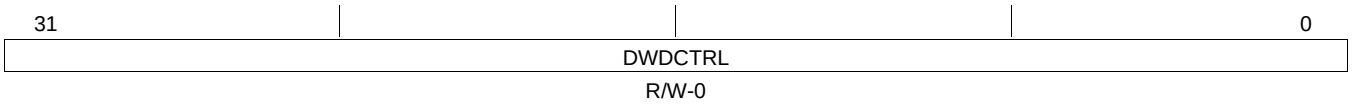
Table 20. RTI Interrupt Flag Register (RTIINTFLAG) Field Descriptions (continued)

Bit	Field	Value	Description
16-4	Reserved		Reads return 0 and writes have no effect
3	INT3		Interrupt Flag 3. Determines if an interrupt is pending
		0	No interrupt pending
		1	Interrupt pending
2	INT2		Interrupt Flag 2. Determines if an interrupt is pending
		0	No interrupt pending
		1	Interrupt pending
1	INT1		Interrupt Flag 1. Determines if an interrupt is pending
		0	No interrupt pending
		1	Interrupt pending
0	INT0		Interrupt Flag 0. Determines if an interrupt is pending
		0	No interrupt pending
		1	Interrupt pending

3.20 Digital Watchdog Control Register (RTIDWDCTRL)

The digital watchdog control register (RTIDWDCTRL) is shown in Figure 22 and described in Table 21.

Figure 22. Digital Watchdog Control Register (RTIDWDCTRL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 21. Digital Watchdog Control Register (RTIDWDCTRL) Field Descriptions

Bit	Field	Value	Description
31-0	DWDCTRL	0-FFFF FFFFh	Digital Watchdog Control 0x5312ACED = DWD counter is disabled Any other value = DWD counter is enabled By default, the digital watchdog counter is disabled. Any write other than 0x5312ACED to the DWDCTRL register enables the counter. This initial write can occur at any time during code execution. Once the initial write has occured, all other writes are ignored. TI recommends that the value 0xACED5312 be written to activate the counter. RTIDWDCTRL is a write-once register that allows the opportunity to enable or disable the DWD functionality. The register will only be writable again after a reset.

3.21 Digital Watchdog Preload Register (RTIDWDPRLD)

The digital watchdog preload register (RTIDWDPRLD) is shown in Figure 23 and described in Table 22.

Figure 23. Digital Watchdog Preload Register (RTIDWDPRLD)

31	16
Reserved	
R-0	

15	12	11	0
Reserved		DWDPRLD	
R-0		R/W-1FFFh	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 22. Digital Watchdog Preload Register (RTIDWDPRLD) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved		Reserved
11-0	DWDPRLD		Digital Watchdog Preload Value The preload value must be written prior to enabling the DWD Down Counter in RTIDWDCTRL. The expiration time of the counter can be calculated with the formula given in Equation 1.

3.22 Watchdog Status Register (RTIWDSTATUS)

The watchdog status register (RTIWDSTATUS) is shown in Figure 24 and described in Table 23.

Figure 24. Watchdog Status Register (RTIWDSTATUS)

31	16
Reserved	
R-0	

15	3	2	1	0
Reserved		KEYST	DWDST	Reserved
R-0		RCP-x	RCP-x	R-0

LEGEND: R = Read; C = Clear; -*n* = value after reset

The values of the following status bits will not be affected by a reset. Only the user can clear these bits. These bits are only intended for debug purposes.

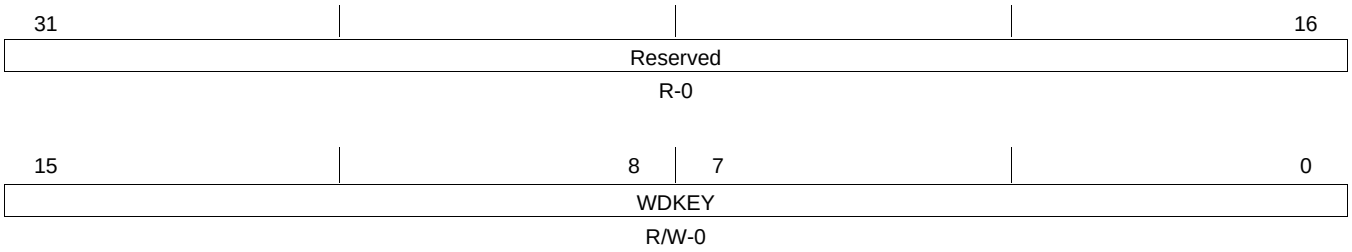
Table 23. Watchdog Status Register (RTIWDSTATUS) Field Descriptions

Bit	Field		Value	Description
31-3	Reserved			Reserved
2	KEYST			Watchdog KeyStatus. This bit denotes a reset generated by a wrong key or key sequence written to the RTIWDKEY register.
			0	No reset generated
			1	Reset generated
1	DWDST			Digital Watchdog Status.
		Write	0	Leaves the current value unchanged
			1	Sets the bit to 0
		Read	0	No reset generated
			1	Reset generated
0	Reserved			Reserved

3.23 Watchdog Key Register (RTIWDKEY)

The watchdog key register (RTIWDKEY) is shown in Figure 25 and described in Table 24.

Figure 25. Watchdog Key Register (RTIWDKEY)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 24. Watchdog Key Register (RTIWDKEY) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved		Reads return 0 and writes have no effect
15-0	WDKEY		Bit 7:0 : Watchdog Key. Key Sequence location. Reads are indeterminate. A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and reloads the counter RTIDWDCNTR with the preload value RTIDWDPRLD. Writing any other value causes a digital watchdog reset, as shown in Table 25

Table 25. Example of a WDKEY Sequence

Step	Value Written to WDKEY	Result
1	0x0A35C	No Action
2	0x0A35C	No Action
3	0x0E51A	WDKEY is enabled for reset by next 0x0A35C
4	0x0E51A	WDKEY is enabled for reset by next 0x0A35C
5	0x0E51A	WDKEY is enabled for reset by next 0x0A35C
6	0x0A35C	Watchdog is reset
7	0x0A35C	No Action
8	0x0E51A	WDKEY is enabled for reset by next 0x0A35C
9	0x0A35C	Watchdog is reset
10	0x0E51A	WDKEY is enabled for reset by next 0x0A35C
11	0x02345	System reset; incorrect value written to WDKEY

3.24 WDKEY Digital Watchdog Down Counter (RTIDWDCNTR)

The WDKEY Digital Watchdog Down Counter (RTIDWDCNTR) is shown in Figure 26 and described in Table 26.

Figure 26. WDKEY Digital Watchdog Down Counter (RTIDWDCNTR)

31 25	24 0
Reserved	DWDCNTR
R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 26. WDKEY Digital Watchdog Down Counter (RTIDWDCNTR) Field Descriptions

Bit	Field	Value	Description
31-25	Reserved		Reads return 0 and writes have no effect
24-0	DWDCNTR		Digital Watchdog Down Counter
		0	Reads return the current counter value
		1	Writes have no effect

Revision History

This document has been revised because of the following technical changes.

Table A-1. Revisions

Location	Changes, Additions, Deletions
Section 1.1	RTI clock input description changes under the Main Features heading