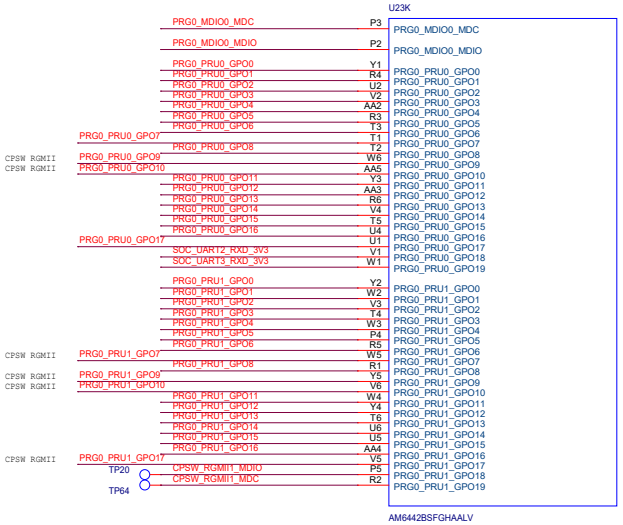
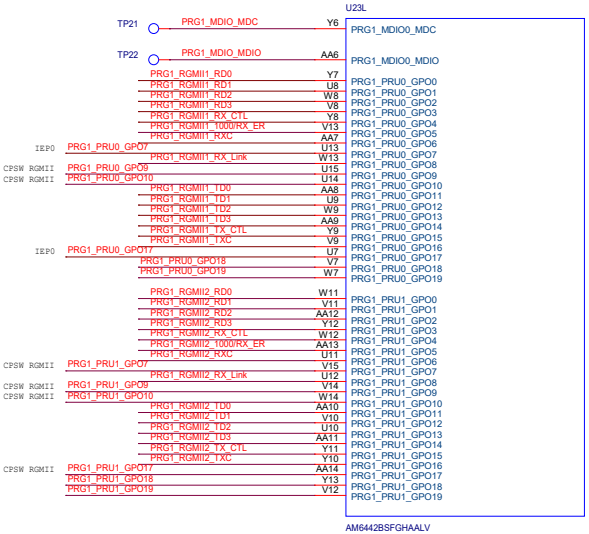
PRG0



PRG1



D-Note :-
Add series resistors 22 R on the
Ethernet interface TX (TDx) signals
near to the SoC

Off Page Connections

To and from ICSSG1 RGMII 2 Ethernet PHY

18 PRG1_RGMII2_RD0 → PRG1_RGMII2_RD0
18 PRG1_RGMII2_RD1 → PRG1_RGMII2_RD1
18 PRG1_RGMII2_RD2 → PRG1_RGMII2_RD2
18 PRG1_RGMII2_RD3 → PRG1_RGMII2_RD3
18 PRG1_RGMII2_RXC → PRG1_RGMII2_RXC
18 PRG1_RGMII2_RX_CTL → PRG1_RGMII2_RX_CTL
18 PRG1_RGMII2_1000/RX_ER → PRG1_RGMII2_1000/RX_ER
18 PRG1_RGMII2_RX_Link → PRG1_RGMII2_RX_Link
18 PRG1_RGMII2_TD0 → PRG1_RGMII2_TD0
18 PRG1_RGMII2_TD1 → PRG1_RGMII2_TD1
18 PRG1_RGMII2_TD2 → PRG1_RGMII2_TD2
18 PRG1_RGMII2_TD3 → PRG1_RGMII2_TD3
18 PRG1_RGMII2_TXC → PRG1_RGMII2_TXC
18 PRG1_RGMII2_TX_CTL → PRG1_RGMII2_TX_CTL
14,17,18,23 PRG1_MDIO_MDIO → PRG1_MDIO_MDIO
14,17,18,23 PRG1_MDIO_MDC → PRG1_MDIO_MDC

To and from ICSSG1 RGMII 1 Ethernet PHY

17 PRG1_RGMII1_RD0 → PRG1_RGMII1_RD0
17 PRG1_RGMII1_RD1 → PRG1_RGMII1_RD1
17 PRG1_RGMII1_RD2 → PRG1_RGMII1_RD2
17 PRG1_RGMII1_RD3 → PRG1_RGMII1_RD3
17 PRG1_RGMII1_RXC → PRG1_RGMII1_RXC
17 PRG1_RGMII1_RX_CTL → PRG1_RGMII1_RX_CTL
17 PRG1_RGMII1_1000/RX_ER → PRG1_RGMII1_1000/RX_ER
17 PRG1_RGMII1_RX_Link → PRG1_RGMII1_RX_Link
17 PRG1_RGMII1_TD0 → PRG1_RGMII1_TD0
17 PRG1_RGMII1_TD1 → PRG1_RGMII1_TD1
17 PRG1_RGMII1_TD2 → PRG1_RGMII1_TD2
17 PRG1_RGMII1_TD3 → PRG1_RGMII1_TD3
17 PRG1_RGMII1_TXC → PRG1_RGMII1_TXC
17 PRG1_RGMII1_TX_CTL → PRG1_RGMII1_TX_CTL
14,18,23 CPSW_RGMII1_MDIO → CPSW_RGMII1_MDIO
14,18,23 CPSW_RGMII1_MDC → CPSW_RGMII1_MDC

FOR GPMC

13 PRG1_PRU0_GPO18 → PRG1_PRU0_GPO18
13 PRG1_PRU0_GPO19 → PRG1_PRU0_GPO19

TO SOCKETS

PRG0_MDIO0_MDC → PRG0_MDIO0_MDC 23
PRG0_MDIO0_MDIO → PRG0_MDIO0_MDIO 23
14,17,18,23 PRG1_MDIO_MDIO → PRG1_MDIO_MDIO
14,17,18,23 PRG1_MDIO_MDC → PRG1_MDIO_MDC

PRG0_PRU0_GPO0 → PRG0_PRU0_GPO0 23
PRG0_PRU0_GPO1 → PRG0_PRU0_GPO1 23
PRG0_PRU0_GPO2 → PRG0_PRU0_GPO2 23
PRG0_PRU0_GPO3 → PRG0_PRU0_GPO3 23
PRG0_PRU0_GPO4 → PRG0_PRU0_GPO4 23
PRG0_PRU0_GPO5 → PRG0_PRU0_GPO5 23
PRG0_PRU0_GPO6 → PRG0_PRU0_GPO6 23
PRG0_PRU0_GPO7 → PRG0_PRU0_GPO7 23
PRG0_PRU0_GPO8 → PRG0_PRU0_GPO8 23
PRG0_PRU0_GPO9 → PRG0_PRU0_GPO9 23
PRG0_PRU0_GPO10 → PRG0_PRU0_GPO10 23
PRG0_PRU0_GPO11 → PRG0_PRU0_GPO11 23
PRG0_PRU0_GPO12 → PRG0_PRU0_GPO12 23
PRG0_PRU0_GPO13 → PRG0_PRU0_GPO13 23
PRG0_PRU0_GPO14 → PRG0_PRU0_GPO14 23
PRG0_PRU0_GPO15 → PRG0_PRU0_GPO15 23
PRG0_PRU0_GPO16 → PRG0_PRU0_GPO16 23
PRG0_PRU0_GPO17 → PRG0_PRU0_GPO17 23
SOC_UART2_RXD_3V3 → SOC_UART2_RXD_3V3 24
SOC_UART3_RXD_3V3 → SOC_UART3_RXD_3V3 24

PRG0_PRU1_GPO0 → PRG0_PRU1_GPO0 23
PRG0_PRU1_GPO1 → PRG0_PRU1_GPO1 23
PRG0_PRU1_GPO2 → PRG0_PRU1_GPO2 23
PRG0_PRU1_GPO3 → PRG0_PRU1_GPO3 23
PRG0_PRU1_GPO4 → PRG0_PRU1_GPO4 23
PRG0_PRU1_GPO5 → PRG0_PRU1_GPO5 23
PRG0_PRU1_GPO6 → PRG0_PRU1_GPO6 23
PRG0_PRU1_GPO7 → PRG0_PRU1_GPO7 23
PRG0_PRU1_GPO8 → PRG0_PRU1_GPO8 23
PRG0_PRU1_GPO9 → PRG0_PRU1_GPO9 23
PRG0_PRU1_GPO10 → PRG0_PRU1_GPO10 23
PRG0_PRU1_GPO11 → PRG0_PRU1_GPO11 23
PRG0_PRU1_GPO12 → PRG0_PRU1_GPO12 23
PRG0_PRU1_GPO13 → PRG0_PRU1_GPO13 23
PRG0_PRU1_GPO14 → PRG0_PRU1_GPO14 23
PRG0_PRU1_GPO15 → PRG0_PRU1_GPO15 23
PRG0_PRU1_GPO16 → PRG0_PRU1_GPO16 23
PRG0_PRU1_GPO17 → PRG0_PRU1_GPO17 23
CPSW_RGMII1_MDIO → CPSW_RGMII1_MDIO 14,18,23
CPSW_RGMII1_MDC → CPSW_RGMII1_MDC 14,18,23

PRG1_PRU0_GPO7 → PRG1_PRU0_GPO7 23
PRG1_PRU0_GPO9 → PRG1_PRU0_GPO9 23
PRG1_PRU0_GPO10 → PRG1_PRU0_GPO10 23
PRG1_PRU0_GPO17 → PRG1_PRU0_GPO17 23
PRG1_PRU1_GPO7 → PRG1_PRU1_GPO7 23
PRG1_PRU1_GPO9 → PRG1_PRU1_GPO9 23
PRG1_PRU1_GPO10 → PRG1_PRU1_GPO10 23
PRG1_PRU1_GPO17 → PRG1_PRU1_GPO17 23
PRG1_PRU1_GPO18 → PRG1_PRU1_GPO18 23
PRG1_PRU1_GPO19 → PRG1_PRU1_GPO19 23

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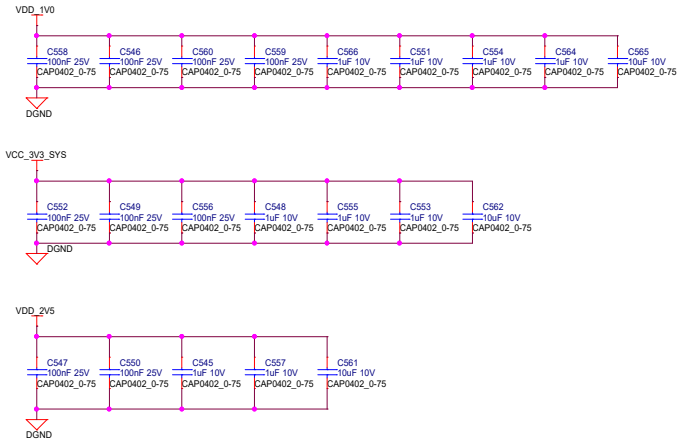
ICSSG RGMII 1 - ETHERNET PHY

Decaps



D-Note :-
The caps and values used are as per the EPHY data sheet recommendations

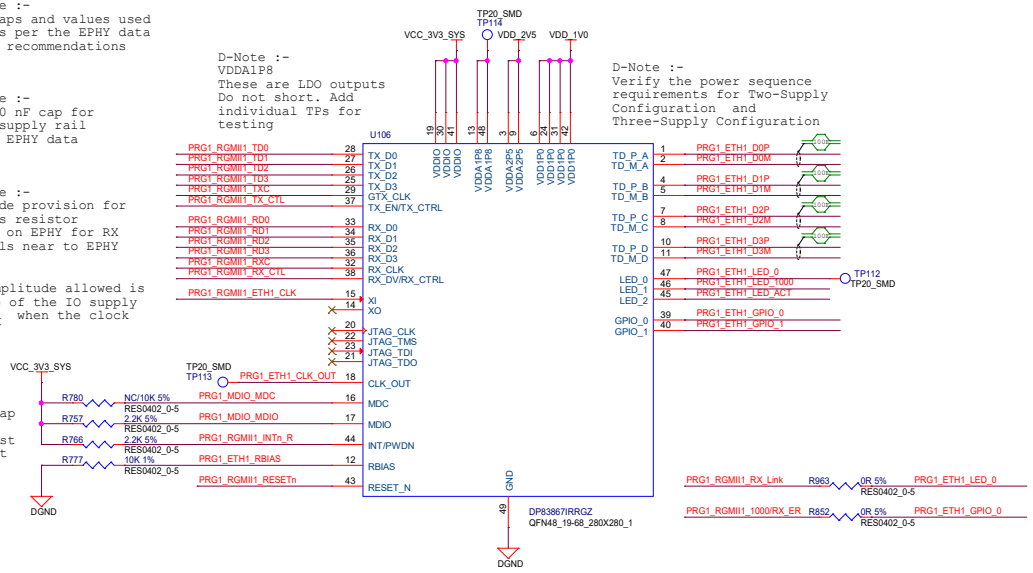
D-Note :-
Add 10 nF cap for each supply rail Refer EPHY data sheet

D-Note :-
Provide provision for Series resistor based on EPHY for RX signals near to EPHY

D-Note :-
XI clock Input amplitude allowed is 1.8V irrespective of the IO supply Use a CAP DIVIDER when the clock amplified is 3.3V

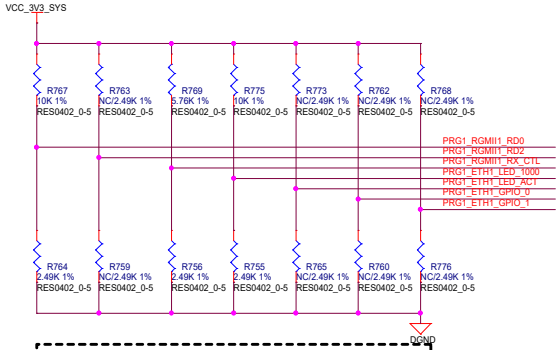
D-Note :-
VDDA1P8
These are LDO outputs Do not short. Add individual TPs for testing

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration



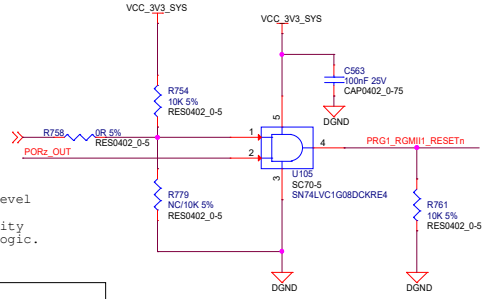
D-Note :-
Add a parallel 22 pF cap These changes are for Ethernet compliance test performance improvement

STRAPPING RESISTORS



PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

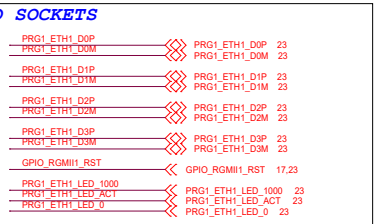
PRG1 (ICSSG) ETH1 RESET



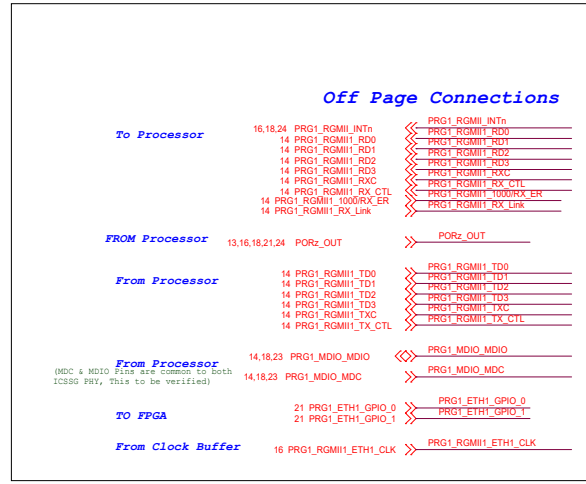
D-Note :-
Add an isolation resistor (0R) to SoC GPIO for debug and testing

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

TO SOCKETS



Off Page Connections



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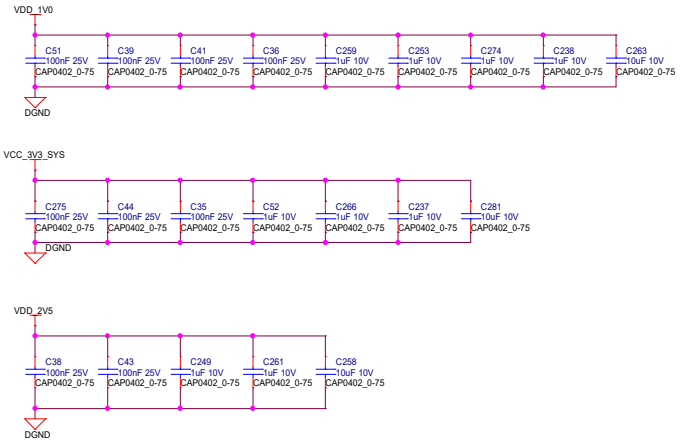
ICSSG RGMII 2 - ETHERNET PHY

Decaps



D-Note :-
The caps and values used are as per the EPHY data sheet recommendations

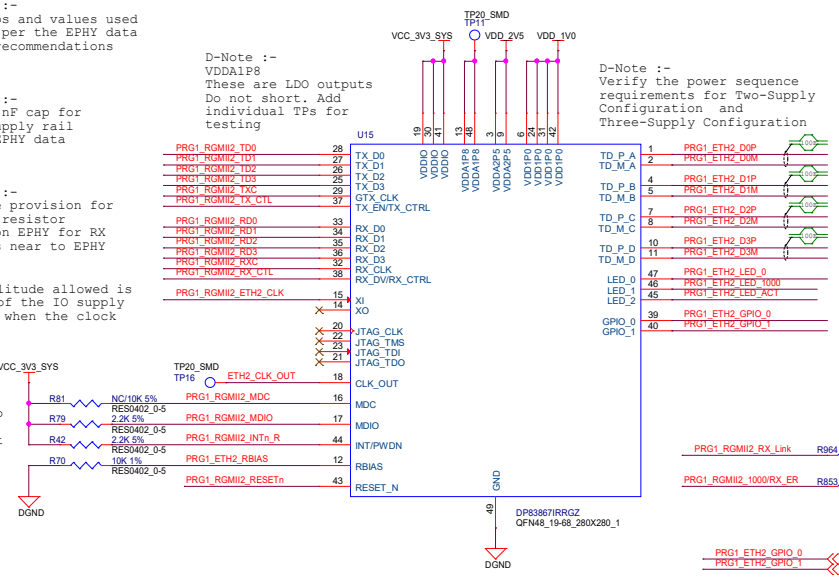
D-Note :-
Add 10 nF cap for each supply rail
Refer EPHY data sheet

D-Note :-
Provide provision for Series resistor based on EPHY for RX signals near to EPHY

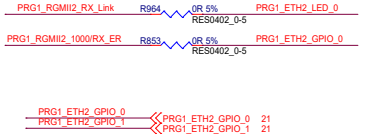
D-Note :-
XI clock Input amplitude allowed is 1.8V irrespective of the IO supply
Use a CAP DIVIDER when the clock amplified is 3.3V

D-Note :-
VDDA1P8 These are LDO outputs Do not short. Add individual TPs for testing

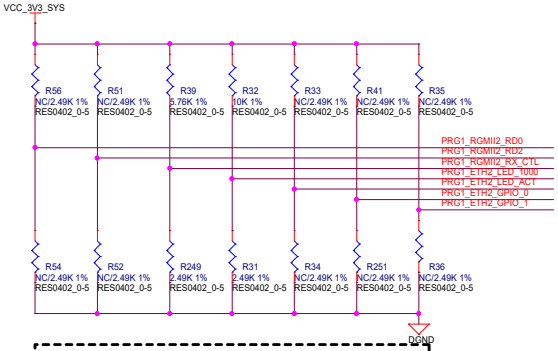
D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration



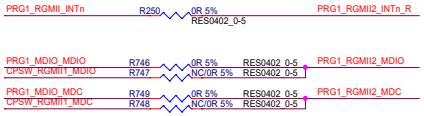
D-Note :-
Add a parallel 22 pF cap These changes are for Ethernet compliance test performance improvement



STRAPPING RESISTORS



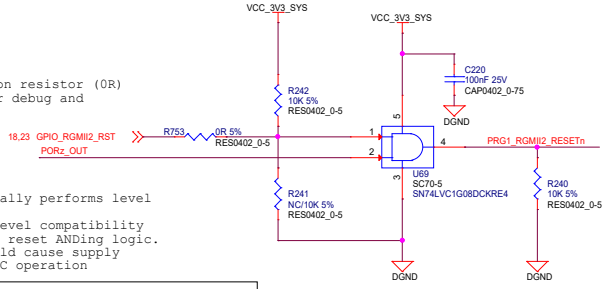
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns



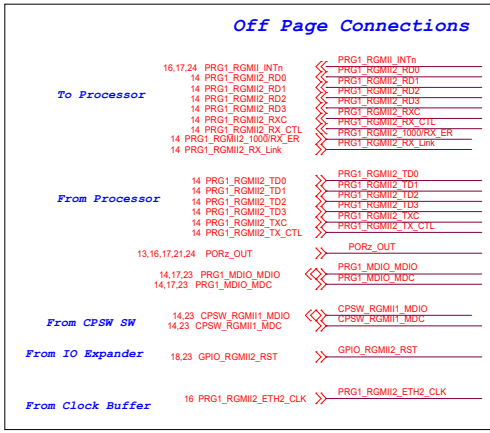
PRG1 (ICSSG) ETH2 RESET

D-Note :-
Add an isolation resistor (0R) to SoC GPIO for debug and testing

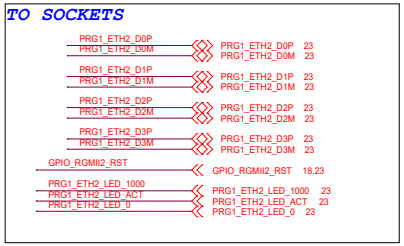
D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation



Off Page Connections



TO SOCKETS



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