REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
v1.0	2024/11				

Title	SOM_AM6442+PH1A90	
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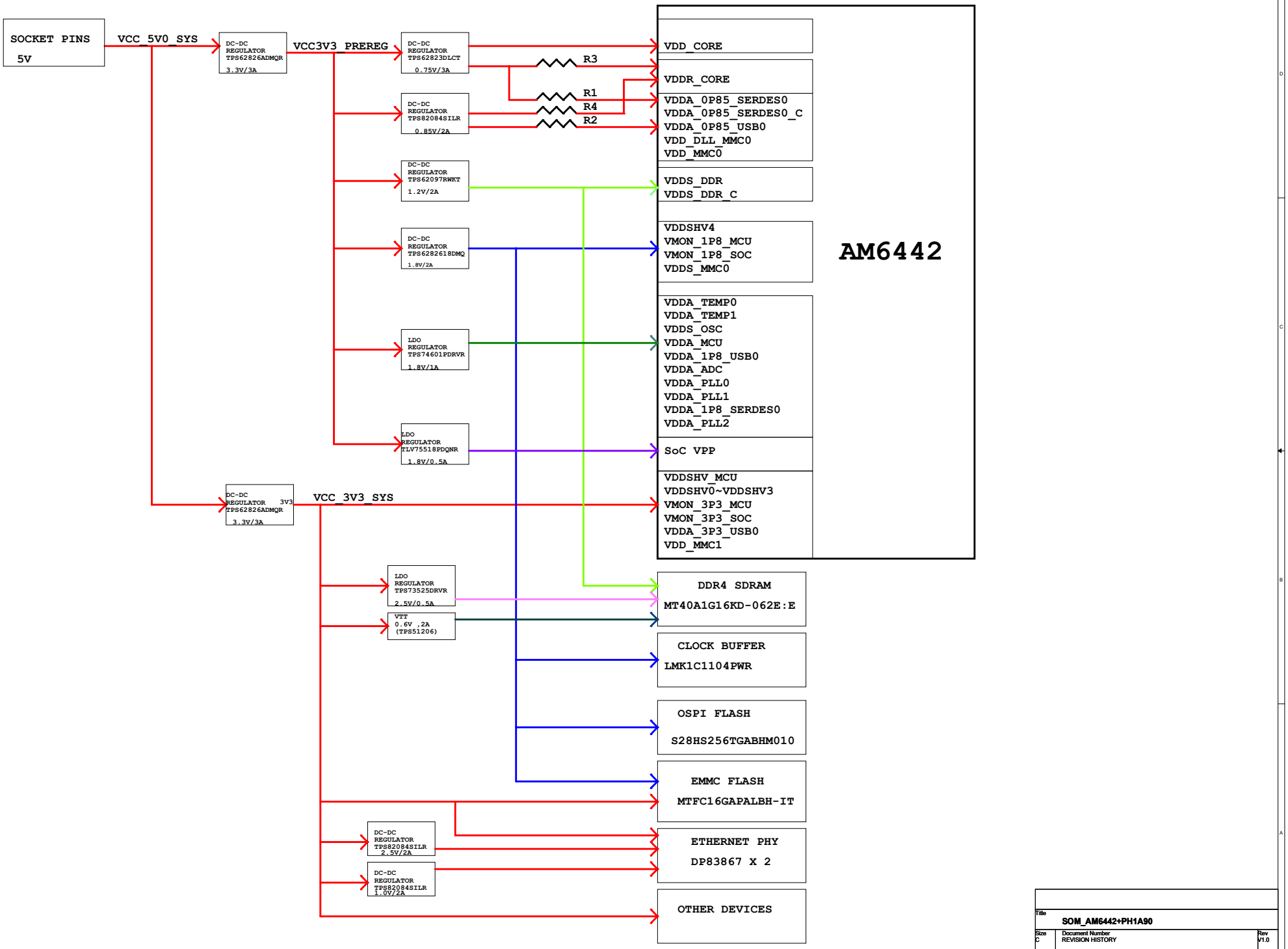
POWER BLOCK DIAGRAM 1



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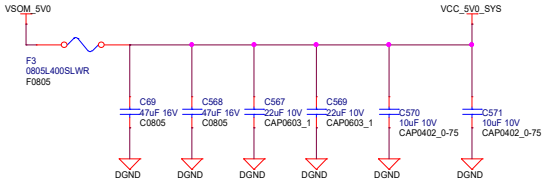
VCC_5V0_SYS POWER SUPPLY



TO SOCKETS

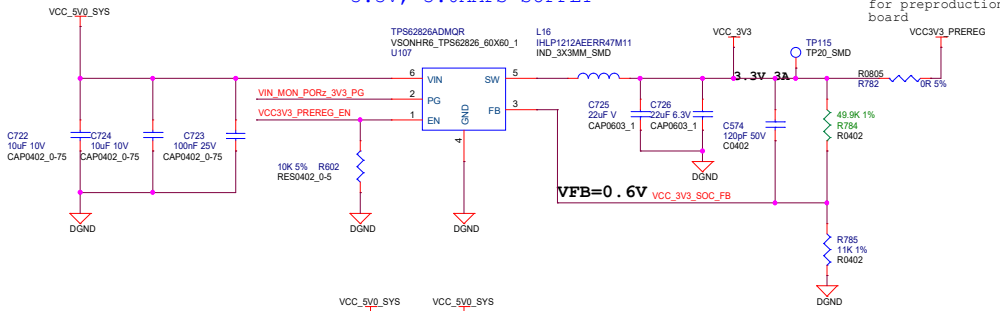
VIN_5V0_PG — VIN_5V0_PG 23

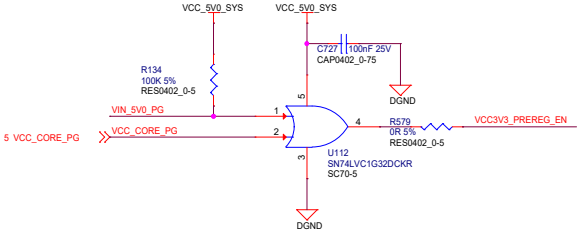
SOC_POWER_RSTn — SOC_POWER_RSTn 24

VCC_3V3_SYS POWER SUPPLY

3.3V, 3.0AMPS SUPPLY

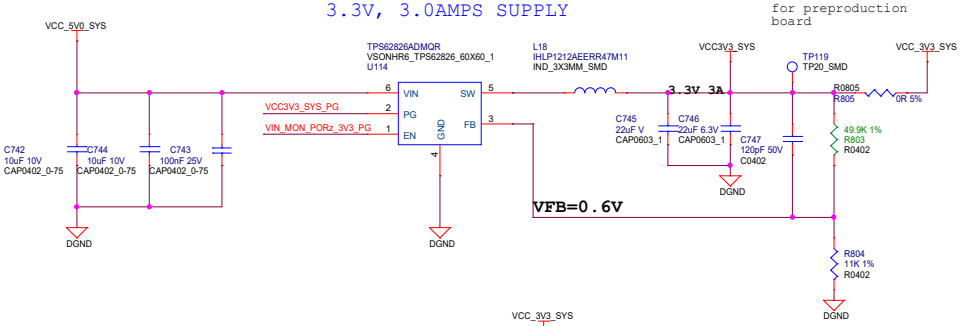
D-Note :-
Add a Jumper or OR for isolation or Current measurement for preproduction board

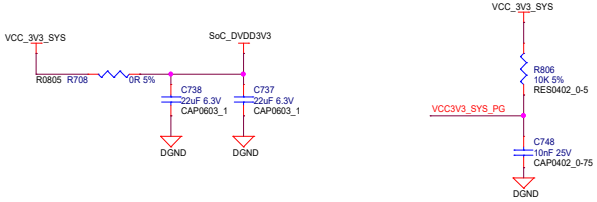




3.3V, 3.0AMPS SUPPLY

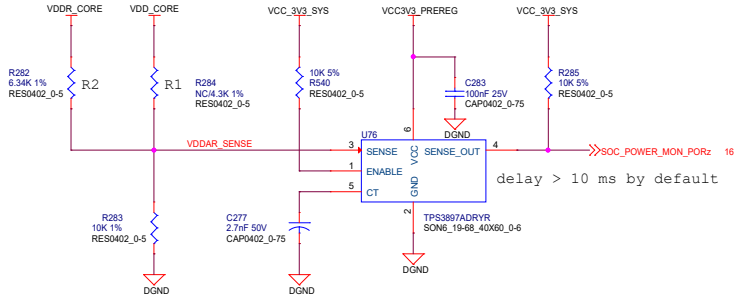
D-Note :-
Add a Jumper or OR for isolation or Current measurement for preproduction board





VOLTAGE SUPERVISOR

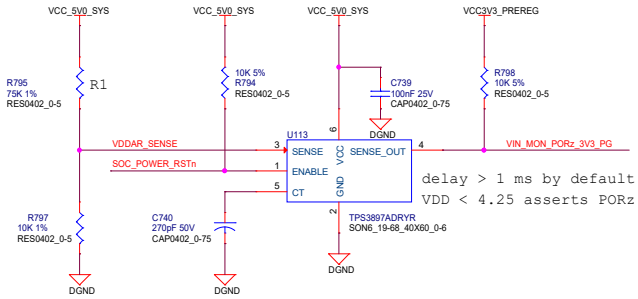
Core Voltage Monitor (VDDAR_CORE/VDD_CORE)

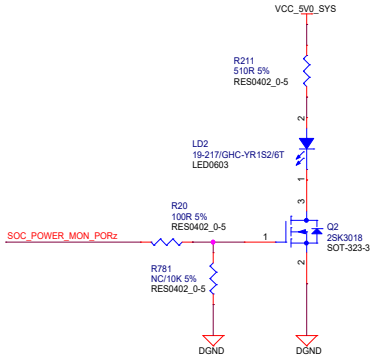


For 0.75: VDD_CORE < 0.715 assert PORz
For 0.85: VDD_CORE < 0.82 asserts PORz

CORE VOLTAGE	RES TO BE PLACED
0.75V	R1 = 4.3K
0.85V	R2 = 6.34K

VCC_5V0_SYS MONITOR





Off Page Connections

VIN_MON_PORz_3V3_PG — VIN_MON_PORz_3V3_PG 6,16

VCC3V3_SYS_PG — VCC3V3_SYS_PG 5,24

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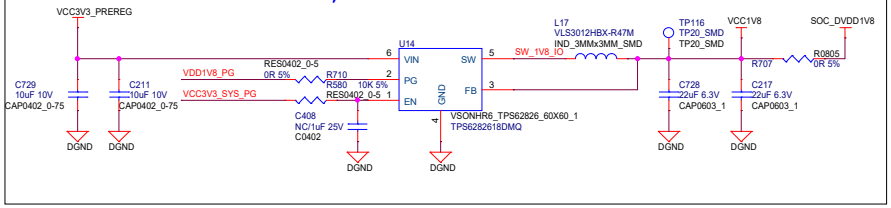
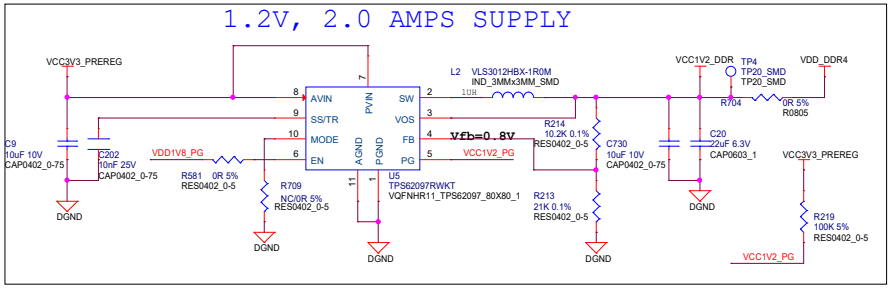
SoC POWER SUPPLIES

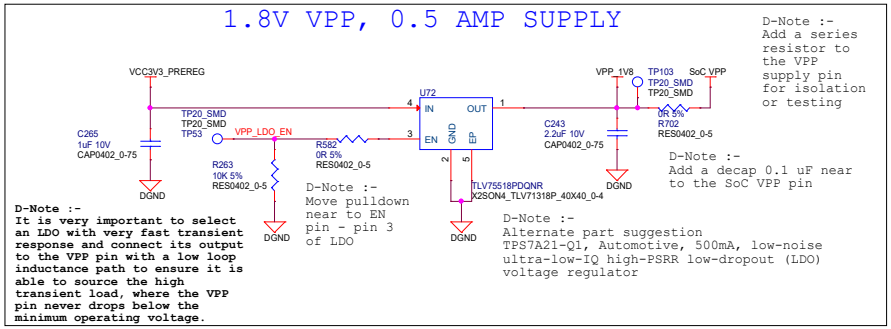
1.8V IO, 3.0 AMPS SUPPLY



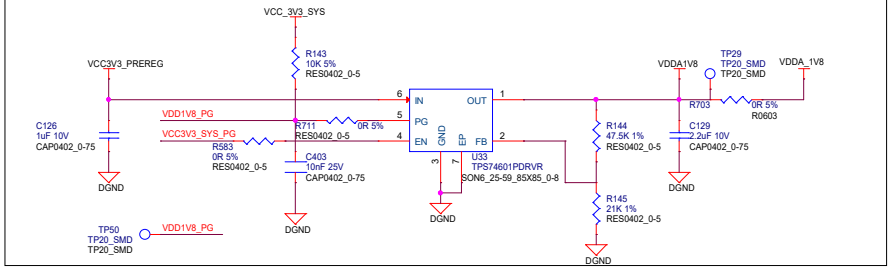
1.2V, 2.0 AMPS SUPPLY



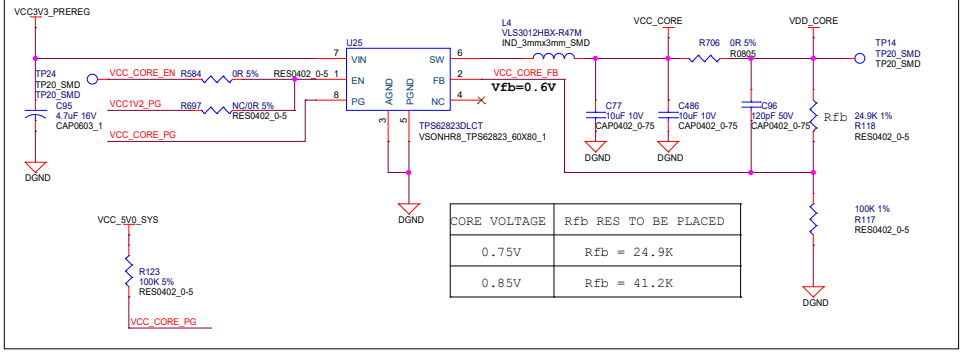
1.8V VPP, 0.5 AMP SUPPLY



1.8V Analog , 1 AMP SUPPLY

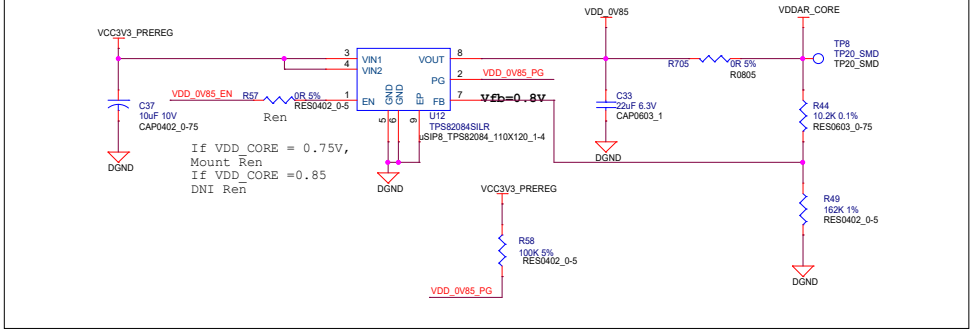


0.75 /0.85V, 3.0 AMPS SUPPLY



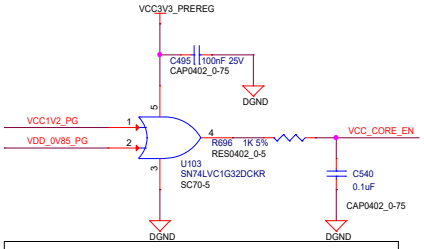
CORE VOLTAGE	Rfb RES TO BE PLACED
0.75V	Rfb = 24.9K
0.85V	Rfb = 41.2K

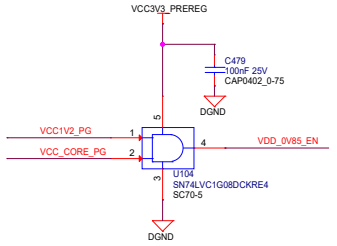
0.85 V, 1.5 AMPS SUPPLY



D-Note :-
An alternative way to source the VPP is to use an external supply. The required caps and termination/Discharge resistor are recommended to be placed near to the SoC VPP pin.
SOC GPIO output can be used to control or time the external power supply output

D-Note :-
Given the transient current requirement during eFuse programming, using load switch or FET switch may not be a recommended approach,
It is recommended to use an LDO. A load or FET switch is likely to have too much voltage drop that can't be compensated like when using an LDO.





TO SOCKETS

5,24 VPP_LDO_EN → VPP_LDO_EN

Off Page Connections

4 VCC_CORE_PG → VCC_CORE_PG

5,24 VPP_LDO_EN
4,6,16 VIN_MON_PORz_3V3_PG → VPP_LDO_EN
VIN_MON_PORz_3V3_PG

VCC_CORE_EN → VCC_CORE_EN 19

VDD_0V85_EN → VDD_0V85_EN 19

VCC3V3_SYS_PG → VCC3V3_SYS_PG 4,24

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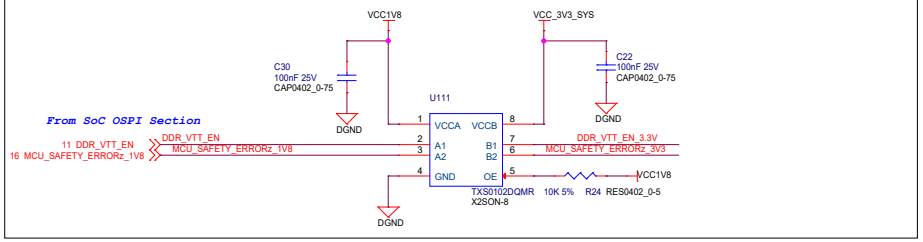
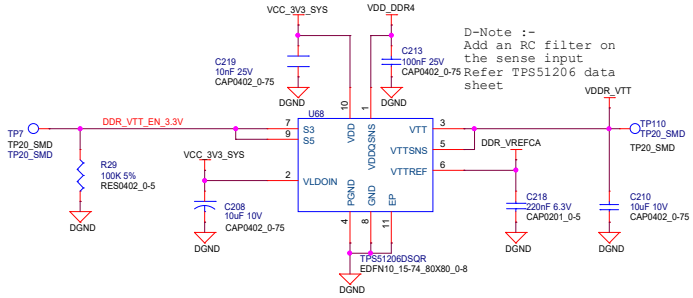
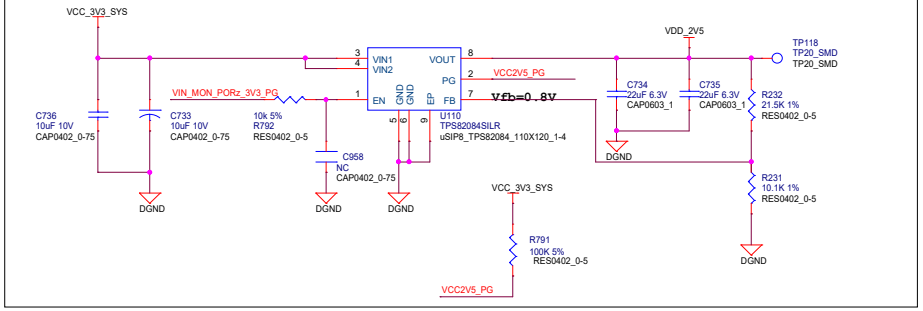
LEVEL TRANSLATOR



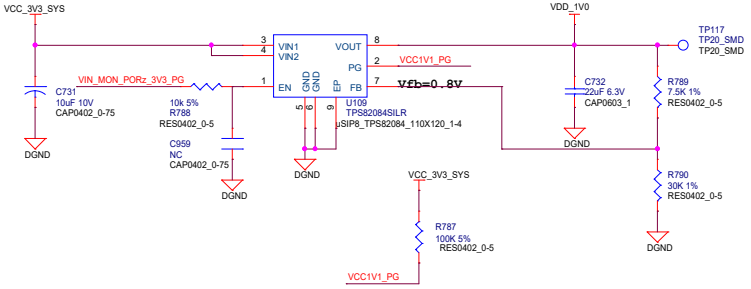
VTT SUPPLY FOR DDR4



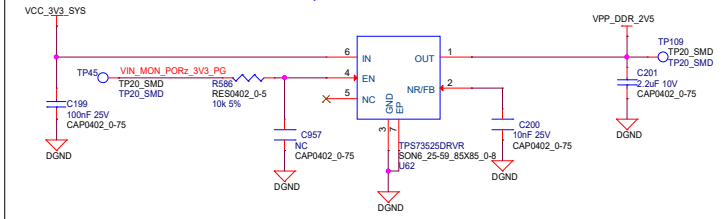
2.5 V, 2.0 AMPS SUPPLY



1.0 V, 2.0 AMPS SUPPLY FOR ETHERNET PHY



2.5V, 0.5 AMP SUPPLY



Off Page Connections

4,16 VIN_MON_PORz_3V3_PG >> VIN_MON_PORz_3V3_PG

24 MCU_SAFETY_ERRORz_3V3 >> MCU_SAFETY_ERRORz_3V3

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SoC POWER

D-Note :-
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure
It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the PCB. For example, 5, 12, or 24 volts.
The error associated with this monitor would require you to set the threshold significantly lower than the nominal to avoid false trigger
Refer System Power Supply Monitor Design Guidelines section of the data sheet

D-Note :-
Use 1% tolerance resistor

D-Note :-
Changing the core voltage is not allowed after the device has been released from reset. If you turn off the core supply, we expect you to turn off all power rails and ramp them down per the power-down sequence and wait until all supply rails decay below 300mv before turning on power again.

D-Note :-
Add a filter cap Refer System Power Supply Monitor Design Guidelines section of SoC data sheet

D-Note :-
VDDAR_0P85_SERDES0, VDDA_1V8_SERDES
Refer usage note in the Pin connectivity table

D-Note :-
VDDA_3P3_SDIO Connect to output of load switch when UHS-I speed is used

D Note :-
Mount R699 and DNI R698 when SR2.0 Device is used
Mount R698 and DNI R699 when SR1.0 Device is used
Currently shipped device are SR2.0

D-Note :-
VDDSHV_SD_IO
Refer pin connectivity table when SD card interface is not used

D-Note :-
Select a capacitor with ESR < 1 O.
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package
Refer SoC Data sheet

D-Note :-
Increase voltage rating to 10V or 16V to include the effect of DC bias

R-Note
Connecting 1.8V supply source directly to VPP continuously is not allowed

CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

D-Note :-
A Trace connected to SOC is effectively an antenna that will pick up noise.
A potential will be generated on the signal when noise couples into the antenna.
This potential will be largest on the highest impedance end of the signal.
By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

CORE SUPPLY

D-Note :-
Ferrite is optional when SERDES0 is not used

D-Note :-
Bulk caps are optional when SERDES0 is not used

1.8V Analog SUPPLY

D-Note :-
Ferrite is optional when SERDES0 is not used

D-Note :-
Bulk caps are optional when SERDES0 is not used

D-Note :-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IOs
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

1.8V Analog SUPPLY

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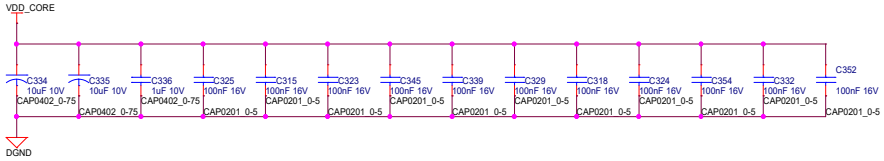
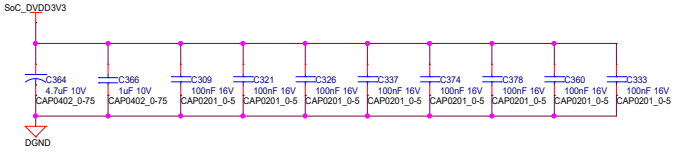
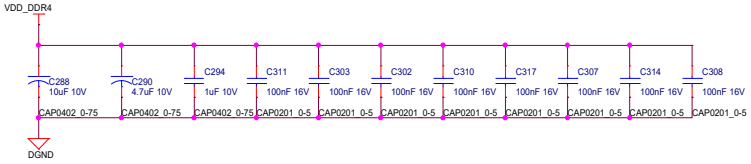
SOC POWER SUPPLIES - DECAPS



Cad Note :- Place 0.1 uF caps near to SoC pins



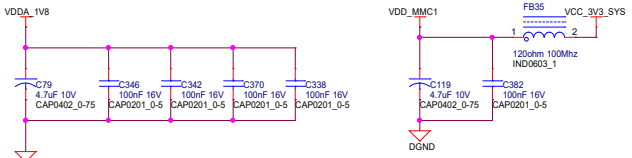
Cad Note :- Place 0.1 uF caps near to SoC pins



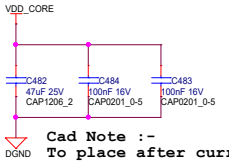
Cad Note :- Place 0.1 uF caps near to SoC pins

VDD ARRAY CORE

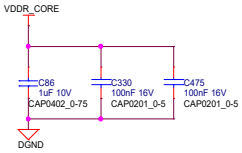
VDDA_3P3_SDIO

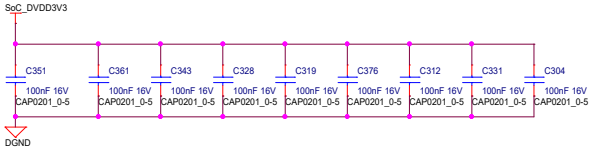


Cad Note :- Place 0.1 uF caps near to SoC pins

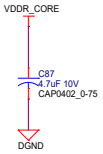


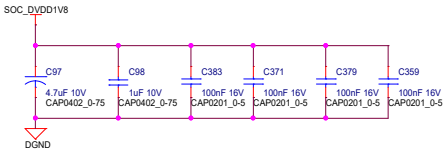
Cad Note :-
To place after current sense resistor on VDD_CORE plane

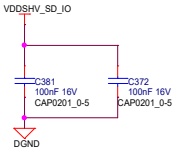




Cad Note :- Place 0.1 uF caps near to SoC pins

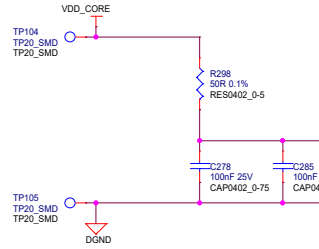


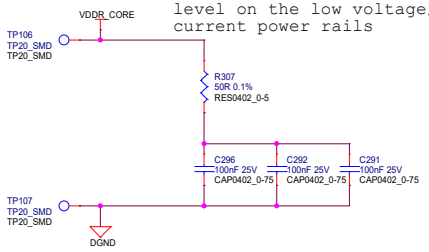




Cad Note :- Place 0.1 uF caps near to SoC pins

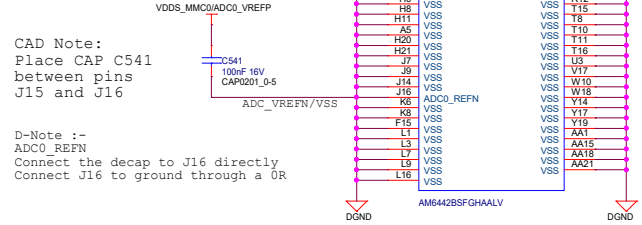
Core & Array Core Supply Kelvin Sensing





R-Note :-
Internal testing
Circuit for testing of noise level on the low voltage/high current power rails

SoC POWER - VSS



CAD Note:
Place CAP C541 between pins J15 and J16

D-Note :-
ADC0_REFN
Connect the decap to J16 directly
Connect J16 to ground through a 0R

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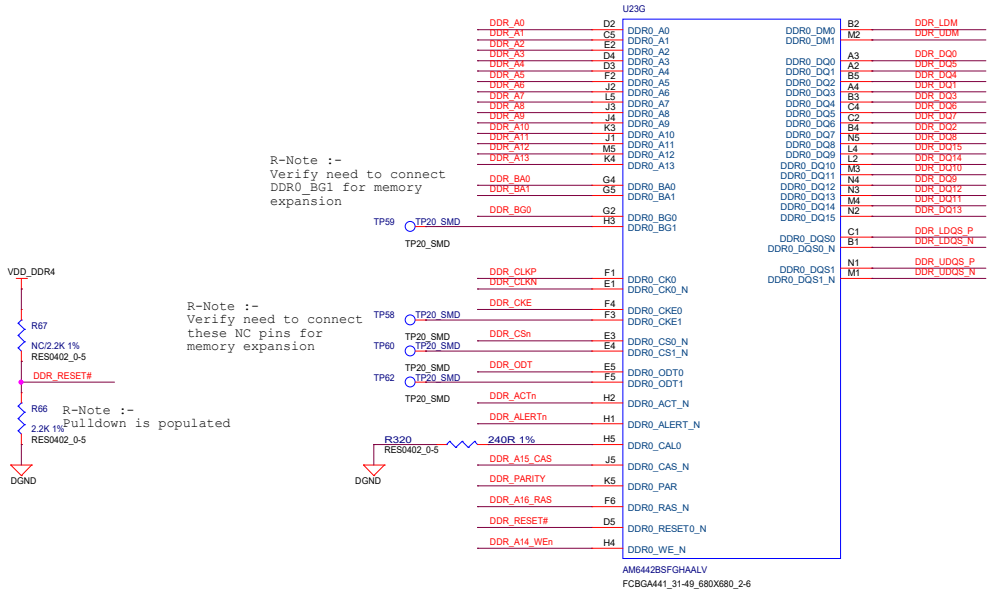
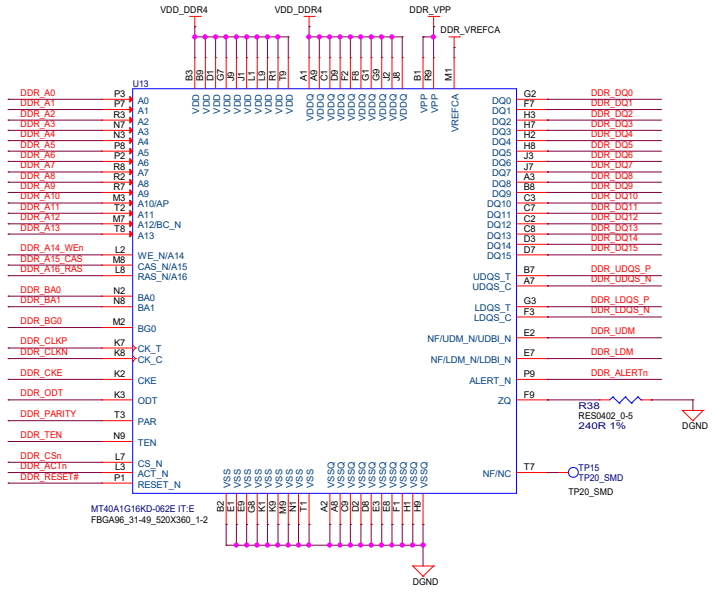
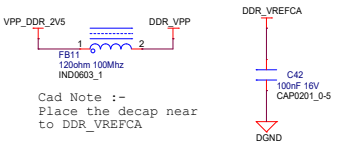
SoC DDR INTERFACE

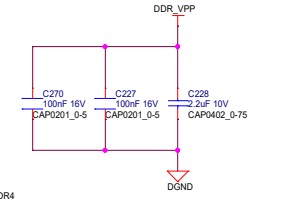


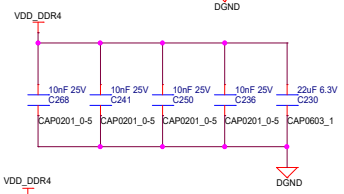
D-Note :-
DDR DQ Lines Swapped With Data Byte

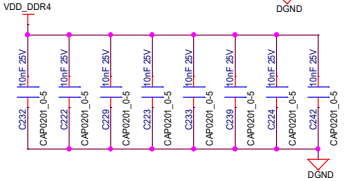
DDR4 DEVICE



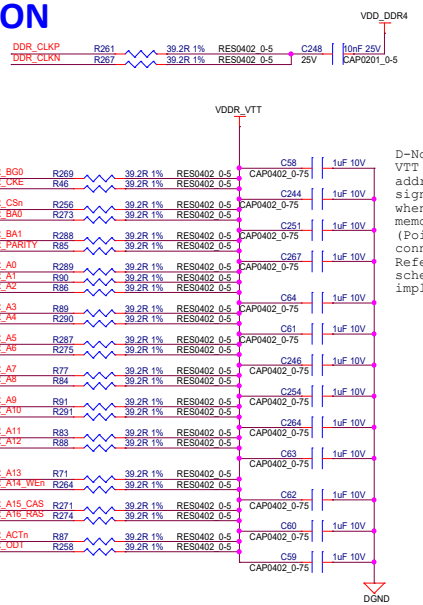








DDR TERMINATION



D-Note:-
VTT terminations for address and control signals is optional when a single DDR4 memory is used (Point-Point) connection
Refer SK-AM62B-P1 schematics for implementation

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eMMC FLASH

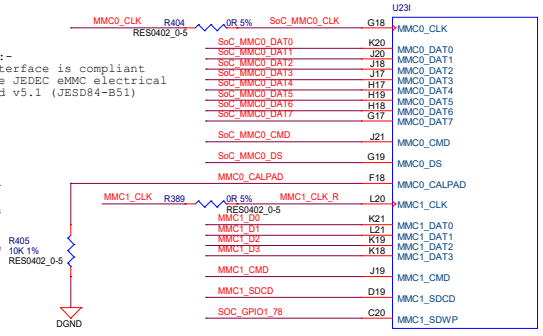
D-Note :-
This family of processor implements a hard and dedicated PHY for eMMC interface.
The pull required for D0..D7, Clock and other eMMC interface control signals are enabled internal to the SOC during reset
Refer pin connectivity table for guidelines when eMMC is not used

SOC - MMC INTERFACE

D-Note :-
0E provision on MMC0_CLK
Helps improve signal integrity

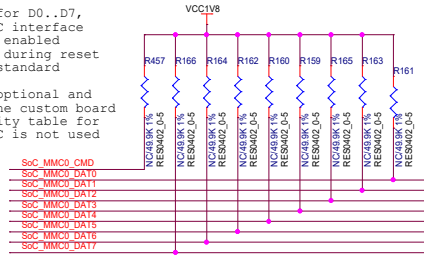
D-Note :-
MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)

R-Note :-
What is the reason we selected pulldown instead of pullup for EMMC, SD card or other peripherals?
Because there are cases where the clock is stopped or paused in a low logic state and the pull-down option is consistent with this logic state.

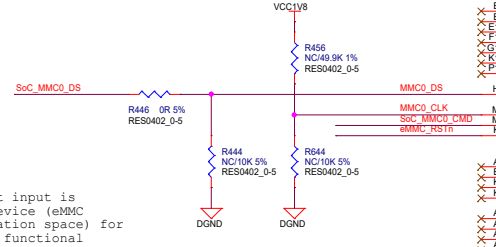


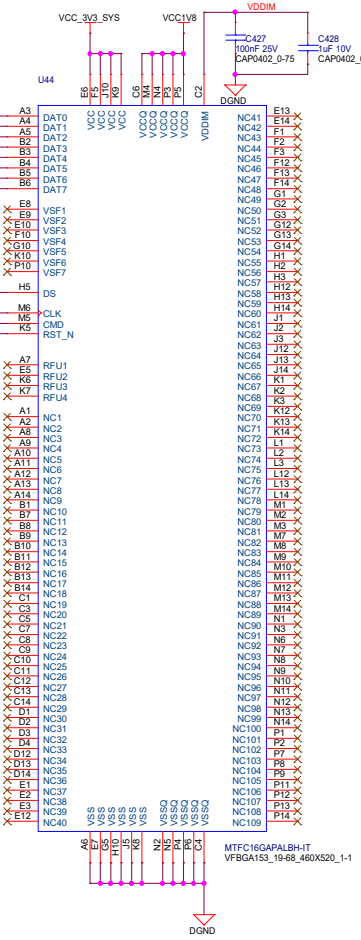
CAD Note :-
Place SOC clock output pulldown resistor near to the clock input pin of the attached (memory) device

D-Note :-
The pulls required for D0..D7, Clock and other eMMC interface control signals are enabled internal to the SOC during reset and are eMMC JEDEC standard compliant
External pullup is optional and can be deleted on the custom board
Refer pin connectivity table for guidelines when eMMC is not used

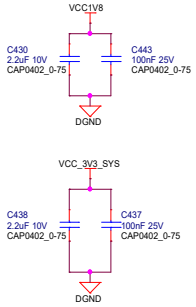


D-Note :-
Ensure eMMC_RSTn Reset input is enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional





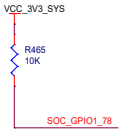
D-Note :-
Add additional decaps as required
Refer SK-AM62P-LP schematics



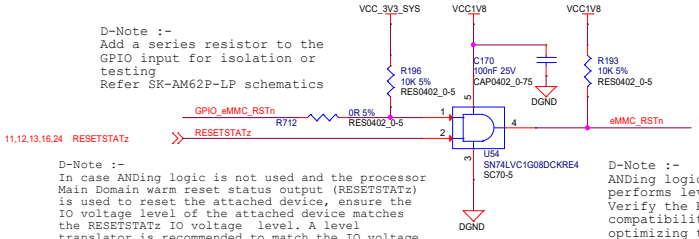
eMMC FLASH RESET

D-Note :-
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or OLDI0 or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

D-Note :-
You could eliminate the GPIO option and only use the reset output (Warm or Cold), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.



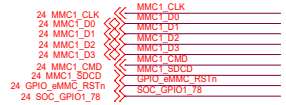
D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics



D-Note :-
In case ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is selected. If too high the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If too low it will cause the AM62x to source too much steady-state current during normal operation.

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

TO SOCKETS



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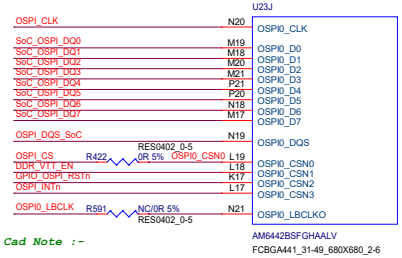
SOC OSPI INTERFACE

D-Note :-
Connecting OSPI interface to multiple devices is not recommended or supported

D-Note :-
These 0R resistors are used for configuring QSPI and OSPI
This is optional during custom board design



Cad Note :-

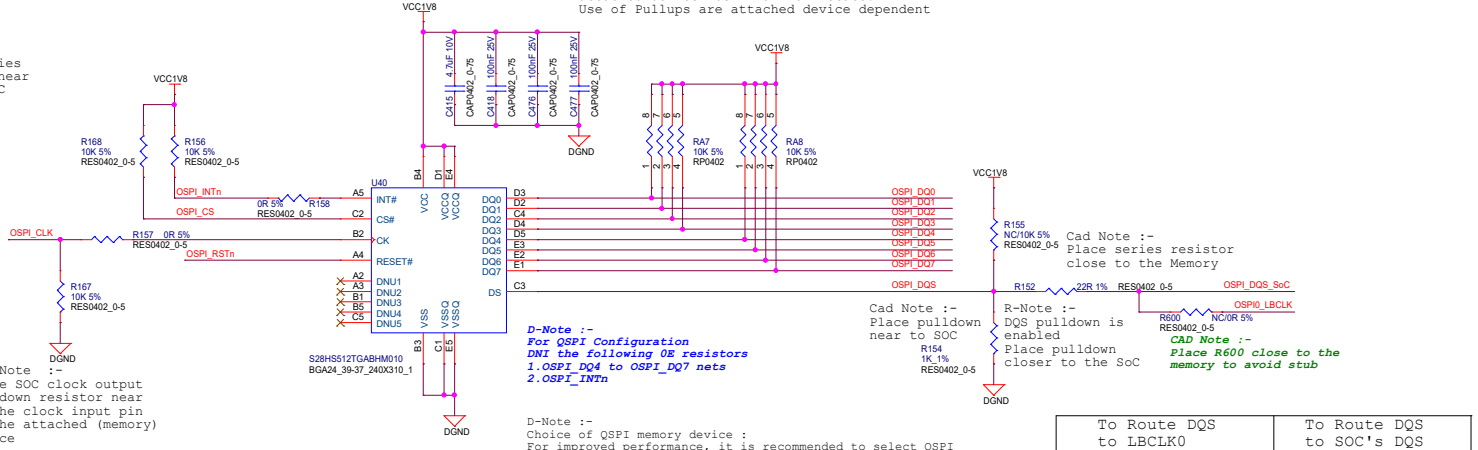
Place R591 close to the ball with as little trace as possible

D-Note :-
External loopback clock series resistors are DNI when DQS is connected

OSPI FLASH

R-Note :-
SOC IO buffers are off during power-up. A pullup is recommended near to the attached device, to hold the attached device IOs in a known state.
Use of Pullups are attached device dependent

D-Note :-
Place series resistor near to the SoC



CAD Note :-
Place SOC clock output pulldown resistor near to the clock input pin of the attached (memory) device

D-Note :-
For QSPI Configuration
DNI the following 0E resistors
1.OSPI_DQ4 to OSPI_DQ7 nets
2.OSPI_INTn

Cad Note :-
Place pulldown near to SOC

R-Note :-
DQS pulldown is enabled
Place pulldown closer to the SoC

Cad Note :-
Place series resistor close to the Memory

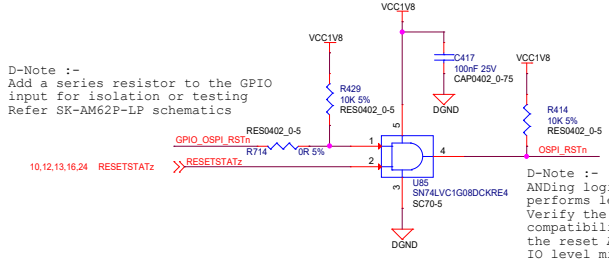
CAD Note :-
Place R600 close to the memory to avoid stub

D-Note :-
Choice of QSPI memory device :
For improved performance, it is recommended to select QSPI memory device with an external reset input pin
The reset pin is recommended to be controlled using SOC reset status output or an ANDing logic as implemented in the starter kit

To Route DQS to LBCLK0	To Route DQS to SOC's DQS
Mount R591 & R600	DNI R591 & R600

OSPI FLASH RESET

D-Note :-
Add a series resistor to the GPIO input for isolation or testing
Refer SK-AM62P-LP schematics



D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

Off Page Connections

To Level Translator DDR_VTT_EN → DDR_VTT_EN 6

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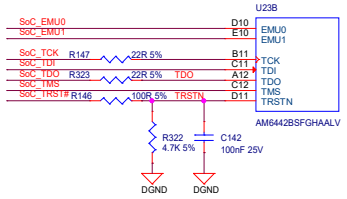
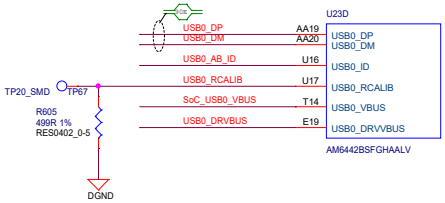
SoC JTAG



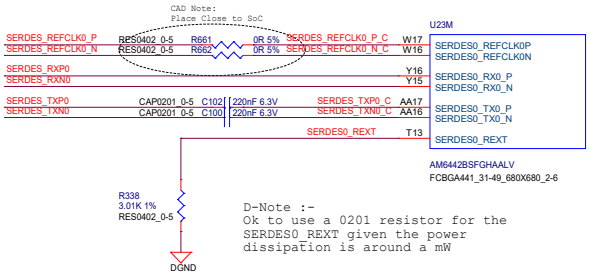
D-Note :-
Place pulls on JTAG signals near to the SoC
Refer AM62P schematics

D-Note :-
TRSTn is the reset to the JTAG logic. For normal operation, this is pulled low, and thus the JTAG remains in reset as it is not being used. When a JTAG pod is connected, the pod will eventually drive this signal high to release the JTAG logic from reset and enable a JTAG connection.

SOC USB 2.0



SOC SERDES

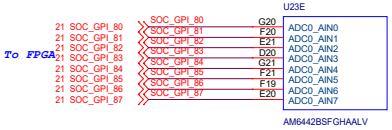


D-Note :-
Ok to use a 0201 resistor for the SERDES0_REXT given the power dissipation is around a mW

ADC CONNECTOR

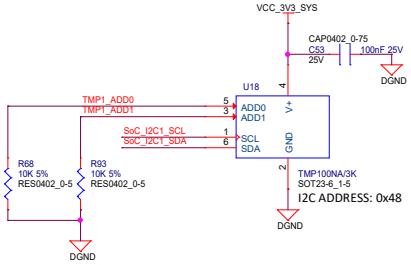
D-Note :-
ADC inputs are not fail-safe. No input voltage should be apply before the SOC supply ramps. The SOC functionality could be affected if ADC inputs are applied before the SOC supply ramps
Use a FET or similar switch to control the input voltage in case they are available before the SOC supply ramps
The Switch needs to be enabled after the SOC supply ramps

D-Note :-
For connecting the ADC0 signals, Refer Pin connectivity table when entire ADC0 is not used or any ADC input is not used



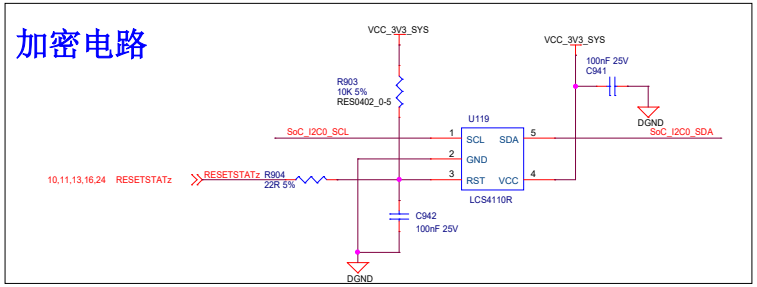
D-Note :-
ADC0_AIN when not used for ADC function can be used as General Purpose Input
The assignment of each ADC0 pin to the GPIO1 module is defined in the ADC0 Signal Description table found in the data sheet.

DIGITAL TEMPERATURE SENSOR



Cad Note :- PLACE TEMP SENSOR CLOSE TO SoC

加密电路



Off Page Connections

SoC_I2C1_SDA
SoC_I2C1_SCL
SoC_I2C1_SDA 15,24
SoC_I2C1_SCL 15,24

SoC_I2C0_SDA
SoC_I2C0_SCL
SoC_I2C0_SDA 15,24
SoC_I2C0_SCL 15,24

To sockets

SoC_EMU0
SoC_EMU1
SoC_EMU0 24
SoC_EMU1 24

SoC_TCK
SoC_TDI
SoC_TDO
SoC_TMS
SoC_TRST#
SoC_TCK 24
SoC_TDI 24
SoC_TDO 24
SoC_TMS 24
SoC_TRST# 24

SERDES_REFCLK0_P
SERDES_REFCLK0_N
SERDES_REFCLK0_P 23
SERDES_REFCLK0_N 23

SERDES_RXP0
SERDES_RXN0
SERDES_RXP0 23
SERDES_RXN0 23

SERDES_TXP0
SERDES_TXN0
SERDES_TXP0 23
SERDES_TXN0 23

USB0_DP
USB0_DM
USB0_DP 23
USB0_DM 23

USB0_AB_ID
SoC_USB0_VBUS
USB0_DRVBUS
USB0_AB_ID 24
SoC_USB0_VBUS 24
USB0_DRVBUS 24

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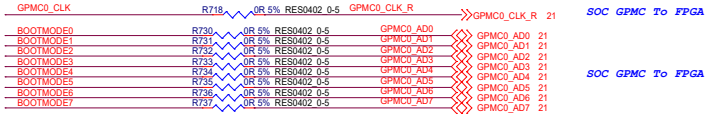
D-Note :-
SOC IO buffers for signals used for GPMC interface are disabled during reset
The required pulls for the interfaced signals are provided on the GPMC interface card

D-Note :-
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot
Shorting the bootmode pins directly to VCC or ground directly is not recommended
Connect each of the bootmode pins through separate resistor
Choose the bootmode resistor value based on the use case (10K or similar)

D-Note :-
Add a series resistor 0R when used as GPMC0_CLK

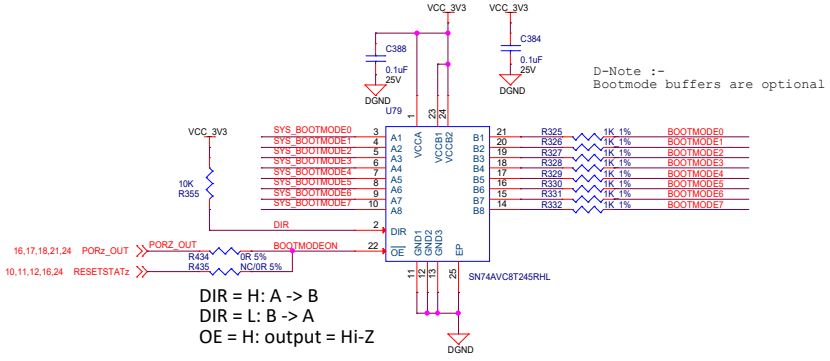
GPMC

To Boot Mode Buffer , GPMC

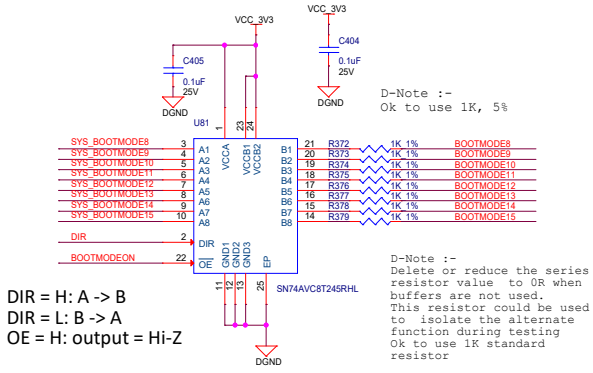


R900 和 R951,R901 和 R950 相互 靠 近 减少分支

BOOT MODE BUFFER



D-Note :-
Bootmode buffers are optional



D-Note :-
Ok to use 1K, 5%

D-Note :-
Delete or reduce the series resistor value to 0R when buffers are not used.
This resistor could be used to isolate the alternate function during testing
Ok to use 1K standard resistor

D-Note :-
When bootmode Isolation buffers are not used, connect the bootmode configuration resistors directly to the SOC bootmode input pins.
Connect the SOC bootmode signal used for alternate function to the attached device through 0R for isolation or testing.

R-Note :-
Resistors are used to isolate the BOOTMODE control logic after the value is latched

TO SOCKETS

Off Page Connections

To SOC

14 PRG1_PRU0_GPO18 PRG1_PRU0_GPO18
14 PRG1_PRU0_GPO19 PRG1_PRU0_GPO19

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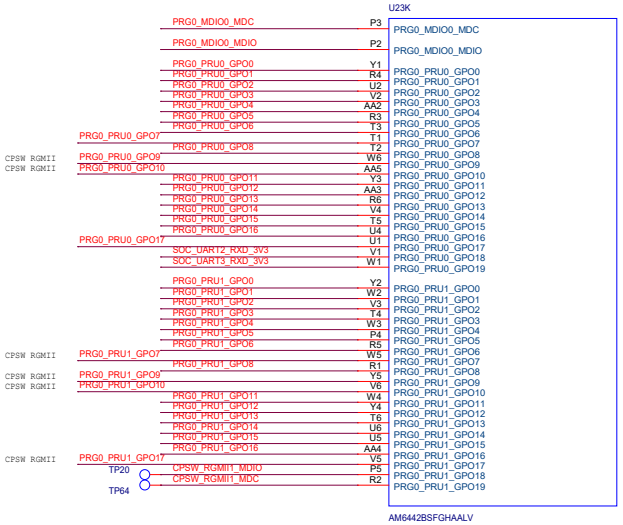
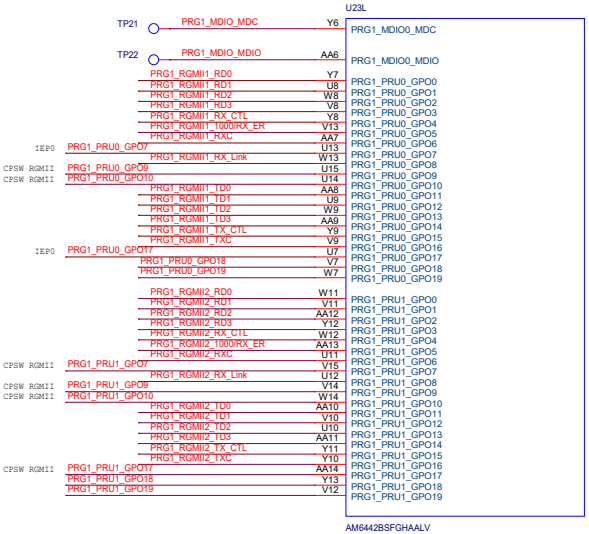
PRG0



PRG1



D-Note :-
Add series resistors 22 R on the
Ethernet interface TX (TDx) signals
near to the SoC

Off Page Connections

To and from ICSSG1 RGMII 2 Ethernet PHY

18 PRG1_RGMII2_RD0 → PRG1_RGMII2_RD0
18 PRG1_RGMII2_RD1 → PRG1_RGMII2_RD1
18 PRG1_RGMII2_RD2 → PRG1_RGMII2_RD2
18 PRG1_RGMII2_RD3 → PRG1_RGMII2_RD3
18 PRG1_RGMII2_RXC → PRG1_RGMII2_RXC
18 PRG1_RGMII2_RX_CTL → PRG1_RGMII2_RX_CTL
18 PRG1_RGMII2_1000/RX_ER → PRG1_RGMII2_1000/RX_ER
18 PRG1_RGMII2_RX_Link → PRG1_RGMII2_RX_Link
18 PRG1_RGMII2_TD0 → PRG1_RGMII2_TD0
18 PRG1_RGMII2_TD1 → PRG1_RGMII2_TD1
18 PRG1_RGMII2_TD2 → PRG1_RGMII2_TD2
18 PRG1_RGMII2_TD3 → PRG1_RGMII2_TD3
18 PRG1_RGMII2_TXC → PRG1_RGMII2_TXC
18 PRG1_RGMII2_TX_CTL → PRG1_RGMII2_TX_CTL
14,17,18,23 PRG1_MDIO_MDIO → PRG1_MDIO_MDIO
14,17,18,23 PRG1_MDIO_MDC → PRG1_MDIO_MDC

To and from ICSSG1 RGMII 1 Ethernet PHY

17 PRG1_RGMII1_RD0 → PRG1_RGMII1_RD0
17 PRG1_RGMII1_RD1 → PRG1_RGMII1_RD1
17 PRG1_RGMII1_RD2 → PRG1_RGMII1_RD2
17 PRG1_RGMII1_RD3 → PRG1_RGMII1_RD3
17 PRG1_RGMII1_RXC → PRG1_RGMII1_RXC
17 PRG1_RGMII1_RX_CTL → PRG1_RGMII1_RX_CTL
17 PRG1_RGMII1_1000/RX_ER → PRG1_RGMII1_1000/RX_ER
17 PRG1_RGMII1_RX_Link → PRG1_RGMII1_RX_Link
17 PRG1_RGMII1_TD0 → PRG1_RGMII1_TD0
17 PRG1_RGMII1_TD1 → PRG1_RGMII1_TD1
17 PRG1_RGMII1_TD2 → PRG1_RGMII1_TD2
17 PRG1_RGMII1_TD3 → PRG1_RGMII1_TD3
17 PRG1_RGMII1_TXC → PRG1_RGMII1_TXC
17 PRG1_RGMII1_TX_CTL → PRG1_RGMII1_TX_CTL
14,18,23 CPSW_RGMII1_MDIO → CPSW_RGMII1_MDIO
14,18,23 CPSW_RGMII1_MDC → CPSW_RGMII1_MDC

FOR GPMC

13 PRG1_PRU0_GPO18 → PRG1_PRU0_GPO18
13 PRG1_PRU0_GPO19 → PRG1_PRU0_GPO19

TO SOCKETS

PRG0_MDIO0_MDC → PRG0_MDIO0_MDC 23
PRG0_MDIO0_MDIO → PRG0_MDIO0_MDIO 23
14,17,18,23 PRG1_MDIO_MDIO → PRG1_MDIO_MDIO
14,17,18,23 PRG1_MDIO_MDC → PRG1_MDIO_MDC

PRG0_PRU0_GPO0 → PRG0_PRU0_GPO0 23
PRG0_PRU0_GPO1 → PRG0_PRU0_GPO1 23
PRG0_PRU0_GPO2 → PRG0_PRU0_GPO2 23
PRG0_PRU0_GPO3 → PRG0_PRU0_GPO3 23
PRG0_PRU0_GPO4 → PRG0_PRU0_GPO4 23
PRG0_PRU0_GPO5 → PRG0_PRU0_GPO5 23
PRG0_PRU0_GPO6 → PRG0_PRU0_GPO6 23
PRG0_PRU0_GPO7 → PRG0_PRU0_GPO7 23
PRG0_PRU0_GPO8 → PRG0_PRU0_GPO8 23
PRG0_PRU0_GPO9 → PRG0_PRU0_GPO9 23
PRG0_PRU0_GPO10 → PRG0_PRU0_GPO10 23
PRG0_PRU0_GPO11 → PRG0_PRU0_GPO11 23
PRG0_PRU0_GPO12 → PRG0_PRU0_GPO12 23
PRG0_PRU0_GPO13 → PRG0_PRU0_GPO13 23
PRG0_PRU0_GPO14 → PRG0_PRU0_GPO14 23
PRG0_PRU0_GPO15 → PRG0_PRU0_GPO15 23
PRG0_PRU0_GPO16 → PRG0_PRU0_GPO16 23
PRG0_PRU0_GPO17 → PRG0_PRU0_GPO17 23
SOC_UART2_RXD_3V3 → SOC_UART2_RXD_3V3 24
SOC_UART3_RXD_3V3 → SOC_UART3_RXD_3V3 24

PRG0_PRU1_GPO0 → PRG0_PRU1_GPO0 23
PRG0_PRU1_GPO1 → PRG0_PRU1_GPO1 23
PRG0_PRU1_GPO2 → PRG0_PRU1_GPO2 23
PRG0_PRU1_GPO3 → PRG0_PRU1_GPO3 23
PRG0_PRU1_GPO4 → PRG0_PRU1_GPO4 23
PRG0_PRU1_GPO5 → PRG0_PRU1_GPO5 23
PRG0_PRU1_GPO6 → PRG0_PRU1_GPO6 23
PRG0_PRU1_GPO7 → PRG0_PRU1_GPO7 23
PRG0_PRU1_GPO8 → PRG0_PRU1_GPO8 23
PRG0_PRU1_GPO9 → PRG0_PRU1_GPO9 23
PRG0_PRU1_GPO10 → PRG0_PRU1_GPO10 23
PRG0_PRU1_GPO11 → PRG0_PRU1_GPO11 23
PRG0_PRU1_GPO12 → PRG0_PRU1_GPO12 23
PRG0_PRU1_GPO13 → PRG0_PRU1_GPO13 23
PRG0_PRU1_GPO14 → PRG0_PRU1_GPO14 23
PRG0_PRU1_GPO15 → PRG0_PRU1_GPO15 23
PRG0_PRU1_GPO16 → PRG0_PRU1_GPO16 23
PRG0_PRU1_GPO17 → PRG0_PRU1_GPO17 23
CPSW_RGMII1_MDIO → CPSW_RGMII1_MDIO 14,18,23
CPSW_RGMII1_MDC → CPSW_RGMII1_MDC 14,18,23

PRG1_PRU0_GPO7 → PRG1_PRU0_GPO7 23
PRG1_PRU0_GPO9 → PRG1_PRU0_GPO9 23
PRG1_PRU0_GPO10 → PRG1_PRU0_GPO10 23
PRG1_PRU0_GPO17 → PRG1_PRU0_GPO17 23
PRG1_PRU1_GPO7 → PRG1_PRU1_GPO7 23
PRG1_PRU1_GPO9 → PRG1_PRU1_GPO9 23
PRG1_PRU1_GPO10 → PRG1_PRU1_GPO10 23
PRG1_PRU1_GPO17 → PRG1_PRU1_GPO17 23
PRG1_PRU1_GPO18 → PRG1_PRU1_GPO18 23
PRG1_PRU1_GPO19 → PRG1_PRU1_GPO19 23

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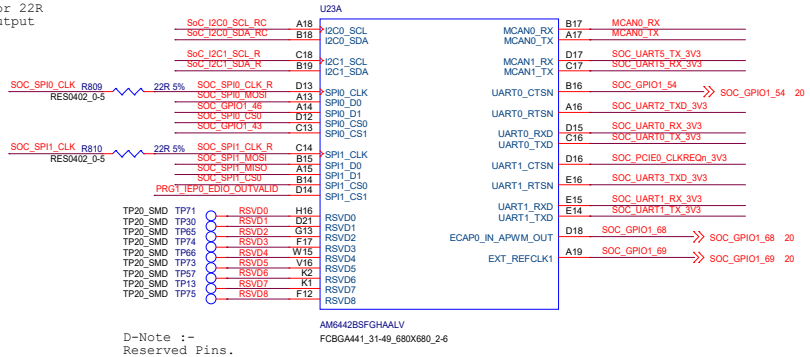
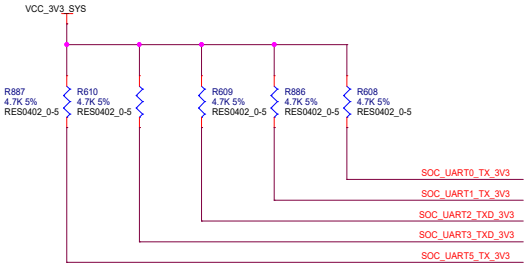
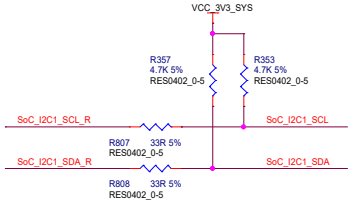
D-Note :-
Add a series resistor 22R to the SPI0 clock output near to the SoC

D-Note :-
Add a series resistor 22R to the SPI1 clock output near to the SoC

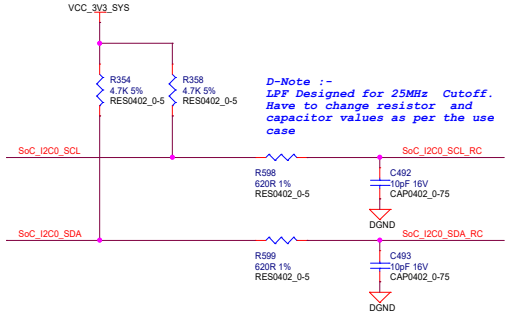


D-Note :-
Reserved Pins.
Leave unconnected



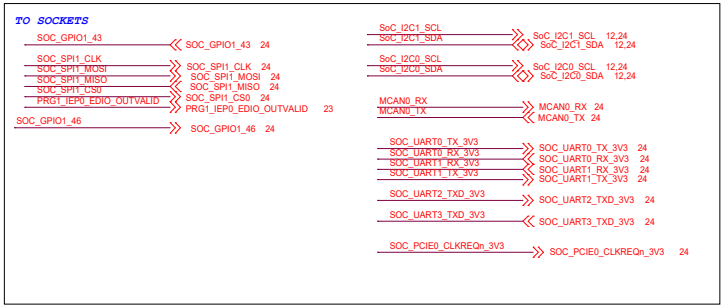


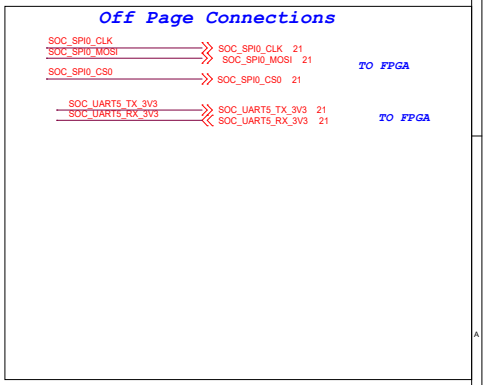
D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO



D-Note :-
RC for Open drain output type I2C interface for slew rate control when pulled to 3.3V
Refer SOC Data sheet

D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V. An RC is recommended for slew rate control. Refer SK-AM62P-LP schematics





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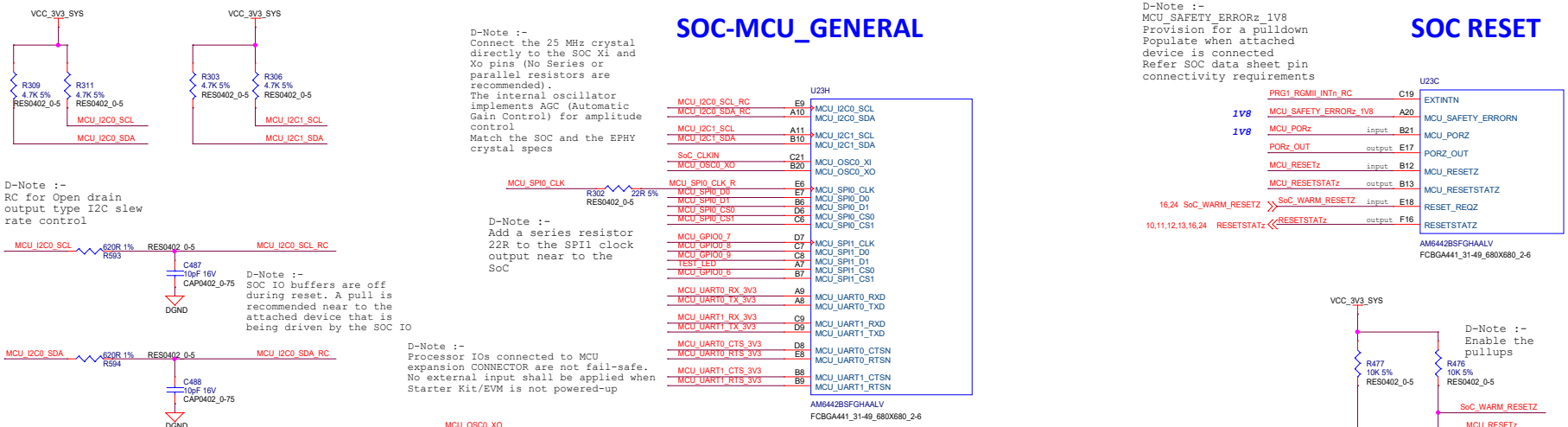
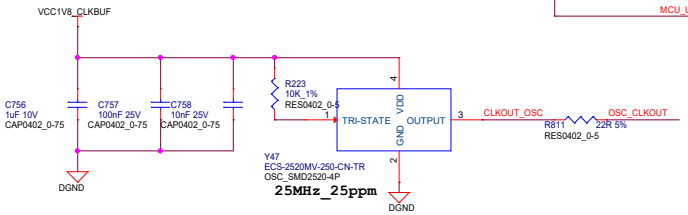
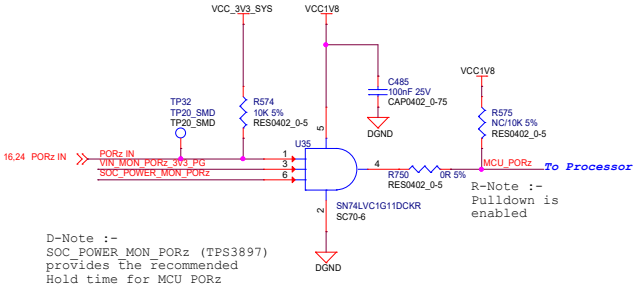
SOC-MCU_GENERAL

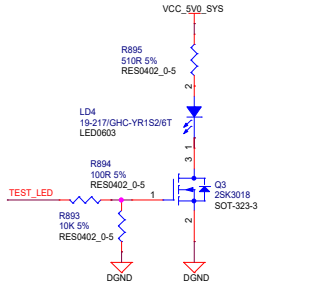


SOC RESET

SYS CLOCK SOURCE







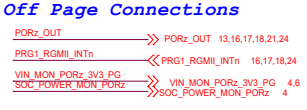
D-Note :-
SOC_POWER_MON_PORz (TPS3897) provides the recommended Hold time for MCU_PORz active (low) at Power-up after supplies valid (using external crystal circuit)

D-Note :-
Not connecting a valid MCU_PORz could cause unpredictable and probably random behavior, since the device is not getting a valid reset, internal circuits would be in random states. Slow rising reset signal could cause glitches internal to the SOC reset circuit. Use a discrete buffer and have the fast rising output of the buffer drive the MCU_PORz is recommended

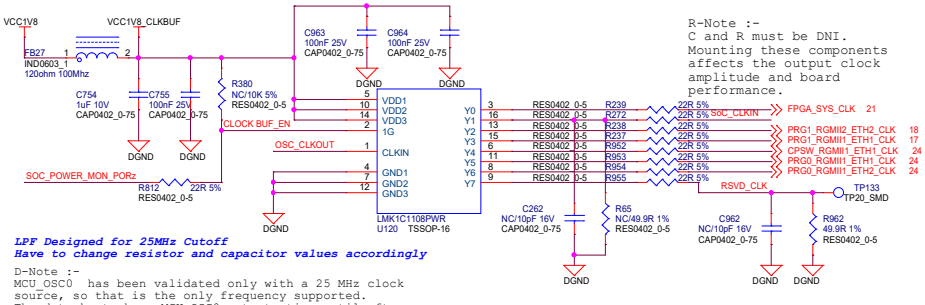
D-Note :-
It is recommended to connect the output from logic gate or discrete buffer (with fast rise time) as MCU_PORz input rather than slow rising open drain output (could glitch internally).

D-Note :-
MCU_PORz input have a maximum rise/fall time requirements when PMIC_POWERGOOD or similar signal is connected to the MCU_PORz. Adjust the pullup to minimize the rise time (100..200 ns) when using open drain output.
MCU_PORz is fail-safe and 3.3v tolerant. Therefore, you can pull the MCU_PORz signal to 1.8V or 3.3V.

Off Page Connections



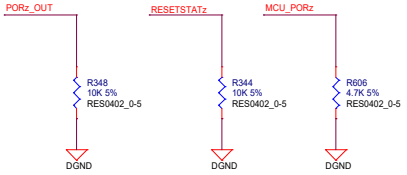
SYSTEM CLOCK BUFFER



R-Note :-
C and R must be DNI.
Mounting these components affects the output clock amplitude and board performance.

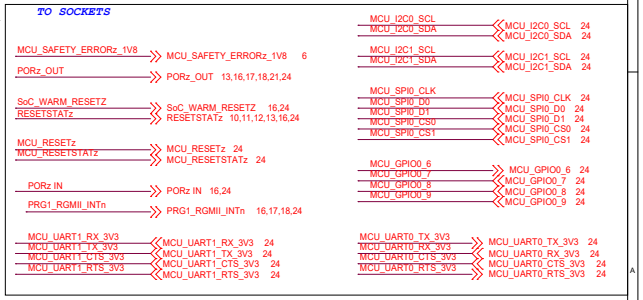
LPF Designed for 25MHz Cutoff
Have to change resistor and capacitor values accordingly

D-Note :-
MCU_OSC0 has been validated only with a 25 MHz clock source, so that is the only frequency supported.
The datasheet shows MCU_OSC0 not starting until after the core voltage because there are some cases where the oscillator may not start until VDD_CORE is valid.
In most cases it will start as early as VDDS_OSC0, but this may not always be the case.
This diagram in the datasheet is showing the maximum start-up time, which must include the case where the delay is based on VDD_CORE being valid.



D-Note :-
Pull-down resistors on PORz OUT and RESETSTATz are provided to keep the signal low until the processor is released from reset during the power-up sequence

TO SOCKETS



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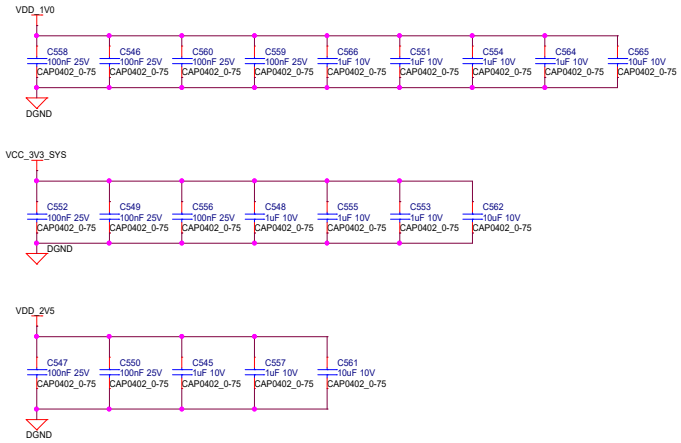
ICSSG RGMII 1 - ETHERNET PHY

Decaps



D-Note :-
The caps and values used are as per the EPHY data sheet recommendations

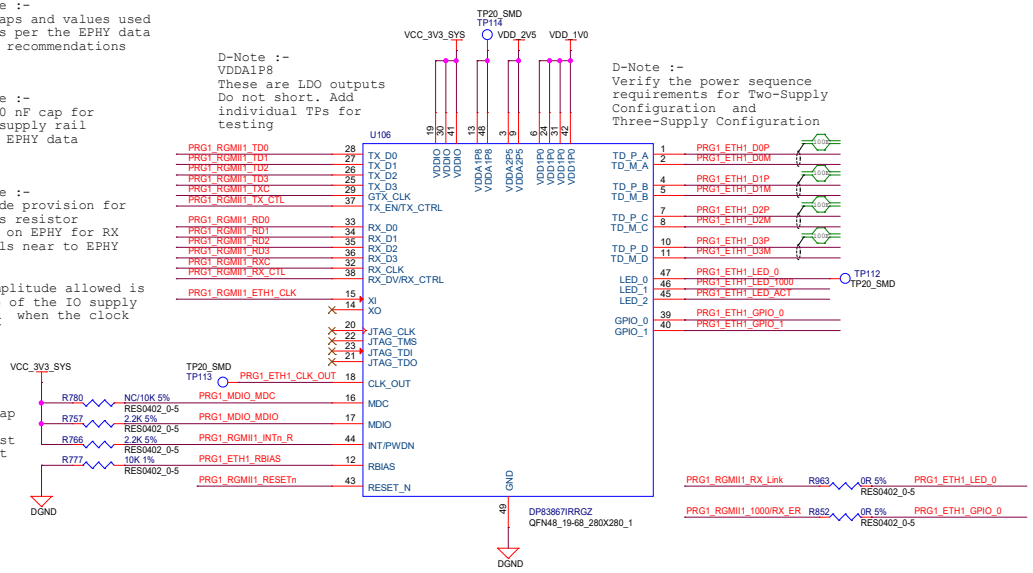
D-Note :-
Add 10 nF cap for each supply rail Refer EPHY data sheet

D-Note :-
Provide provision for Series resistor based on EPHY for RX signals near to EPHY

D-Note :-
XI clock Input amplitude allowed is 1.8V irrespective of the IO supply Use a CAP DIVIDER when the clock amplified is 3.3V

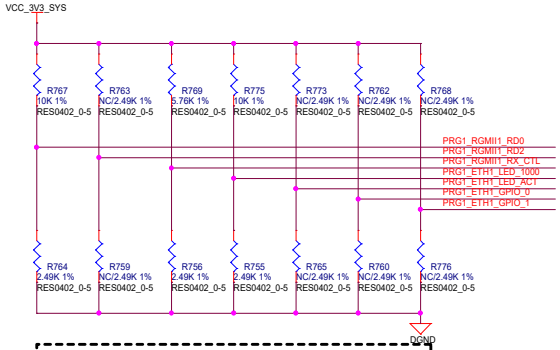
D-Note :-
VDDA1P8
These are LDO outputs Do not short. Add individual TPs for testing

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration



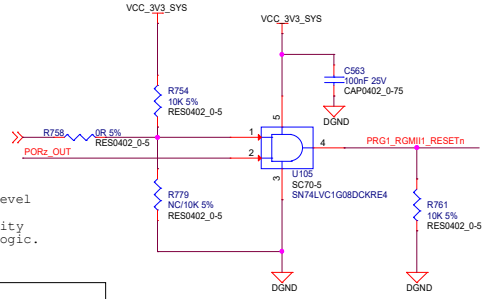
D-Note :-
Add a parallel 22 pF cap These changes are for Ethernet compliance test performance improvement

STRAPPING RESISTORS



PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

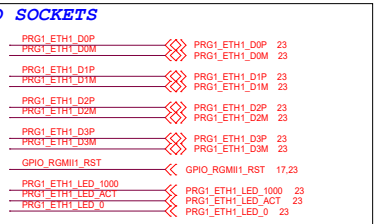
PRG1 (ICSSG) ETH1 RESET



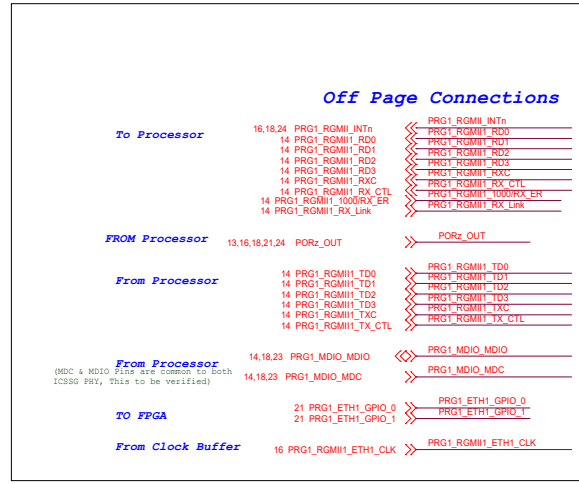
D-Note :-
Add an isolation resistor (0R) to SoC GPIO for debug and testing

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

TO SOCKETS



Off Page Connections



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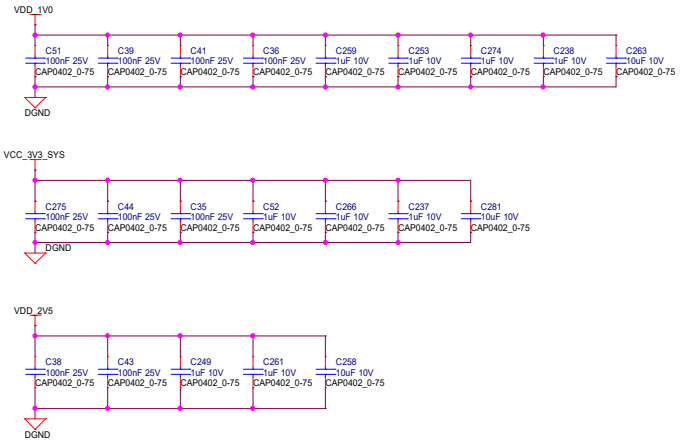
ICSSG RGMII 2 - ETHERNET PHY

Decaps



D-Note :-
The caps and values used are as per the EPHY data sheet recommendations

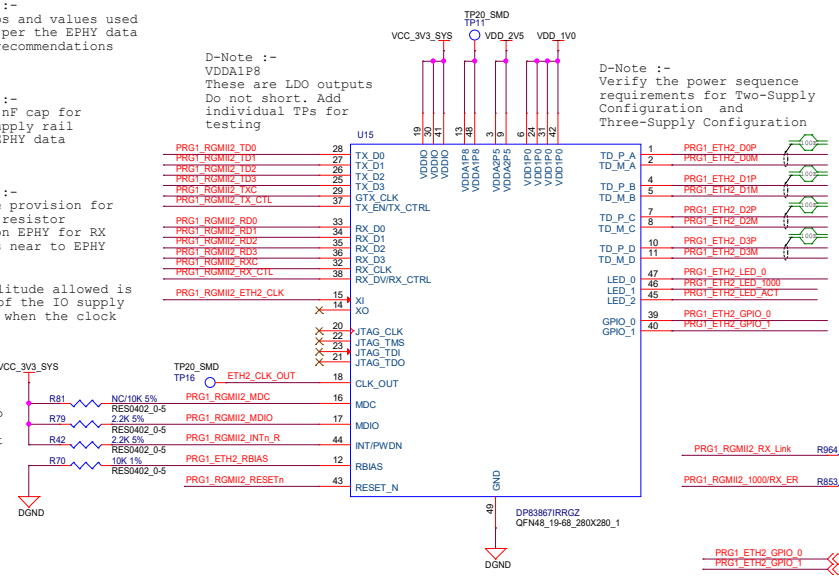
D-Note :-
Add 10 nF cap for each supply rail
Refer EPHY data sheet

D-Note :-
Provide provision for Series resistor based on EPHY for RX signals near to EPHY

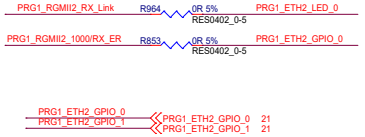
D-Note :-
XI clock Input amplitude allowed is 1.8V irrespective of the IO supply
Use a CAP DIVIDER when the clock amplified is 3.3V

D-Note :-
VDDA1P8 These are LDO outputs Do not short. Add individual TPs for testing

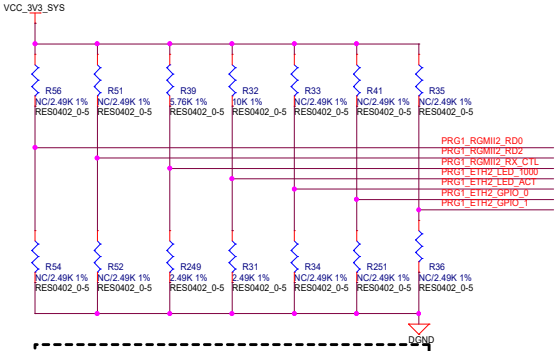
D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration



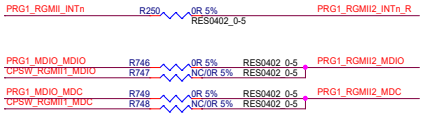
D-Note :-
Add a parallel 22 pF cap These changes are for Ethernet compliance test performance improvement



STRAPPING RESISTORS



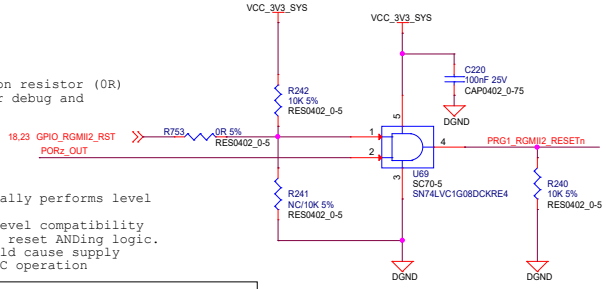
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns



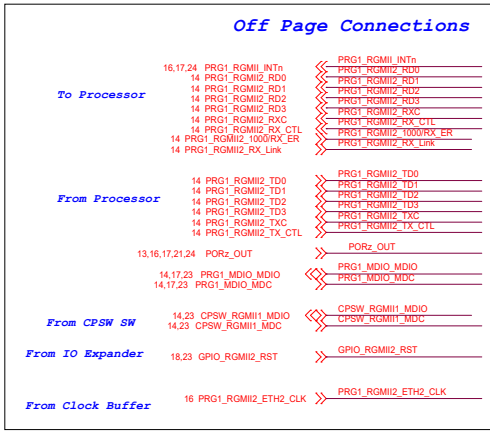
PRG1 (ICSSG) ETH2 RESET

D-Note :-
Add an isolation resistor (0R) to SoC GPIO for debug and testing

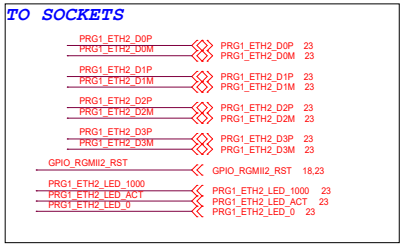
D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation



Off Page Connections



TO SOCKETS



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