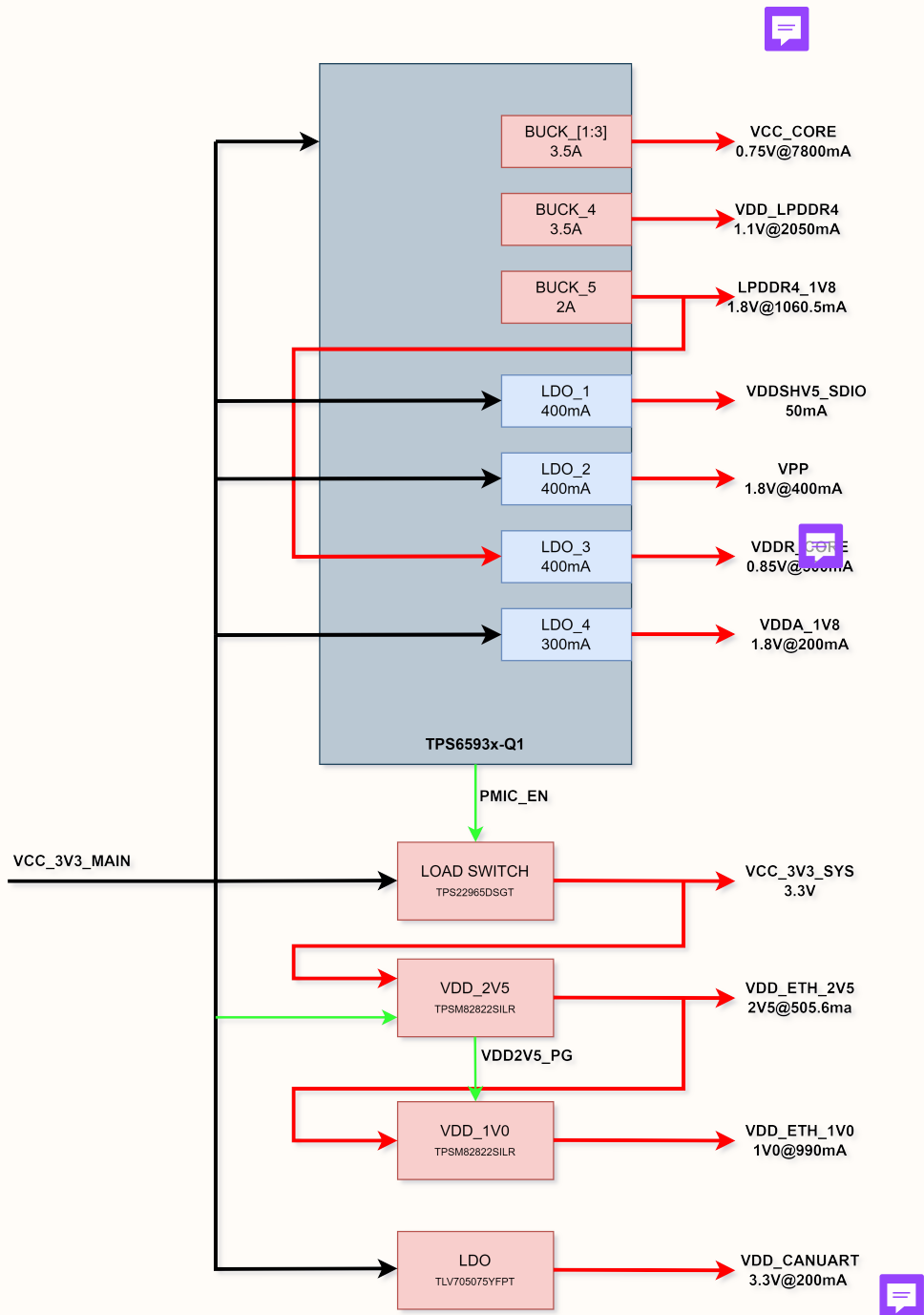


AM62A7x - System On Module

POWER SUPPLY DIAGRAM



SOM BLOCK DIAGRAM

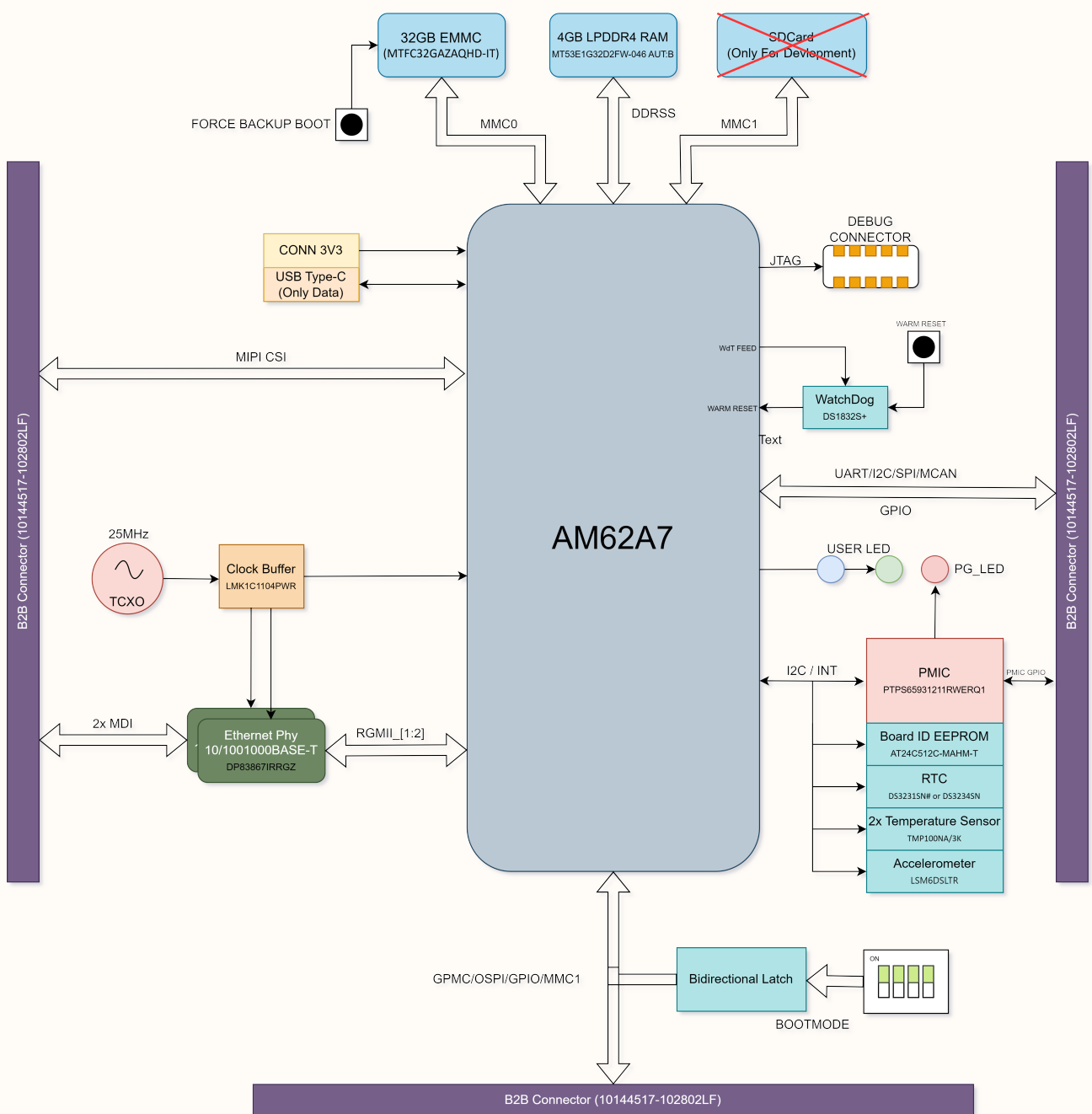


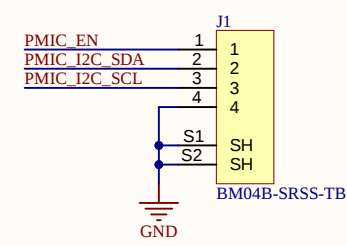
Table of Contents

ID	Discription	Page No.
1	CONTENTS	1
2	PMIC	2
3	SoC Power	3
4	SoC Power Decaps	4
5	LPDDR4	5
6	MMC,OSPI,USB	6
7	DEBUG, RESET	7
8	GPMC	8
9	ClockBuffer	9
10	Peripheral	10
11	CPSW RGMII1 PHY	11
12	CPSW RGMII2 PHY	12
13	B2B Connector	13

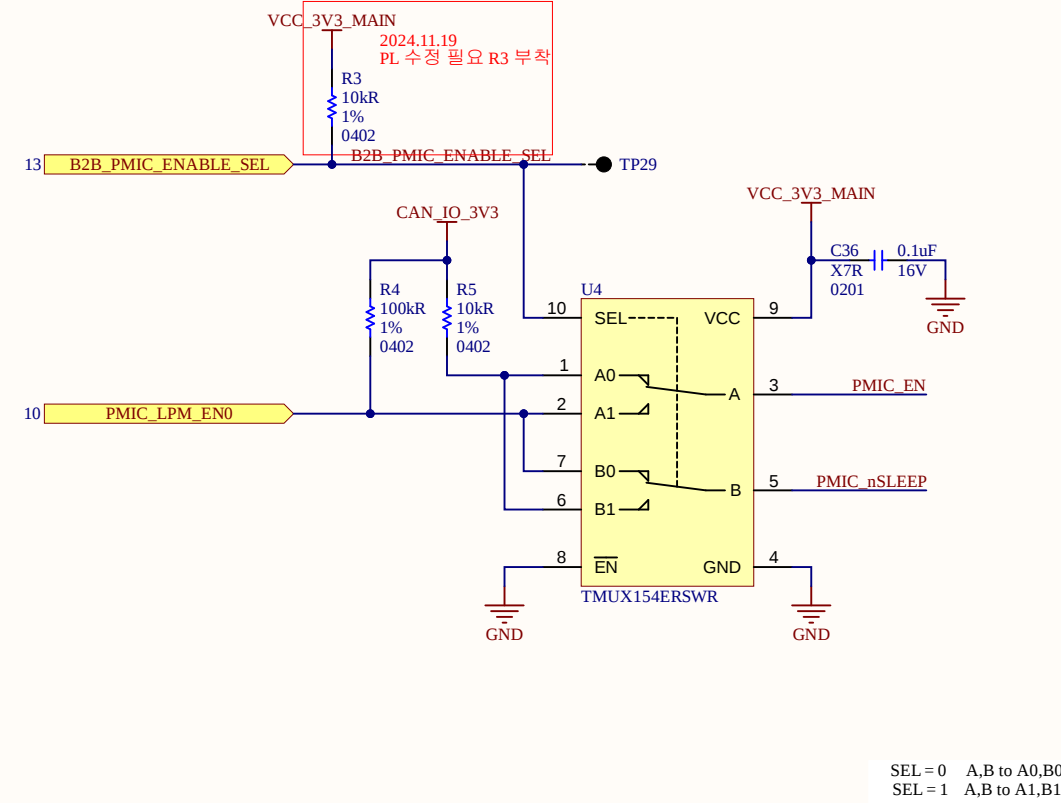
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Project :	SoM-AM62A7x			Revision : R1.0
Sheet Name :	CONTENTS			Page : 1 OF 13
Variant :	Prototype			Size : C
Status :	Preliminary			
NOTE :	*			

TPS6593 - PMIC

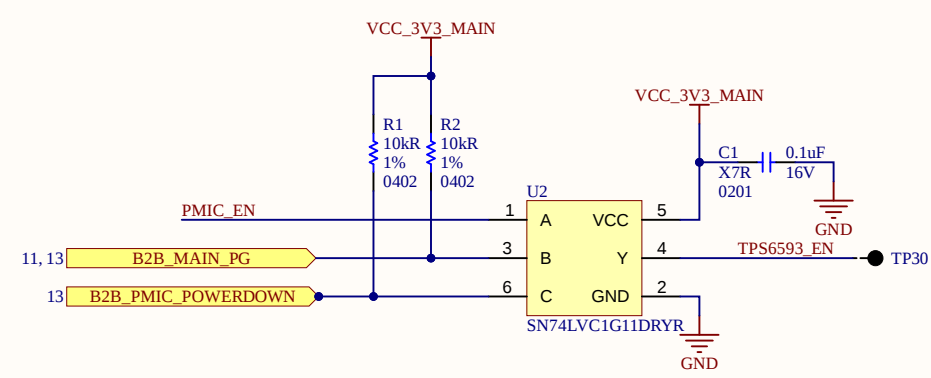
PMIC CONFIG



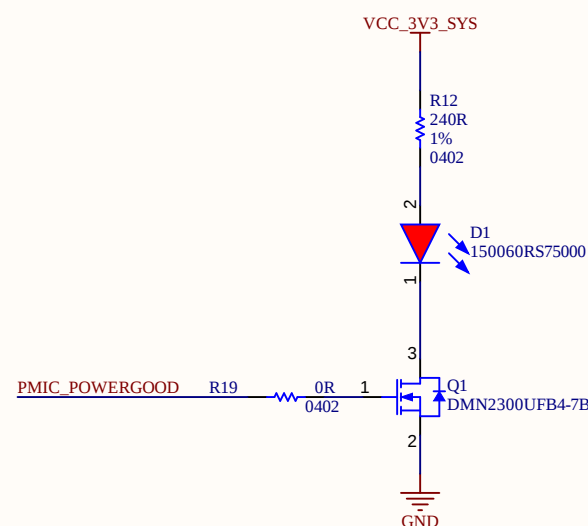
PMIC LPM LOGIC



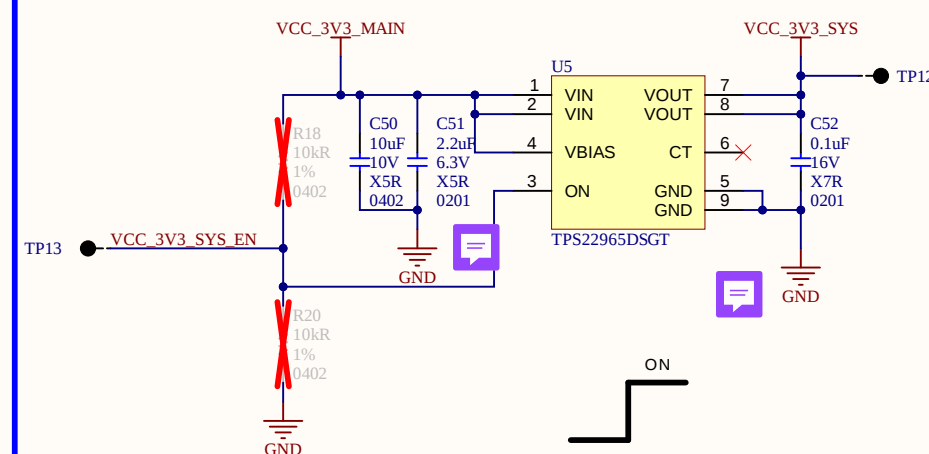
PMIC ENABLE



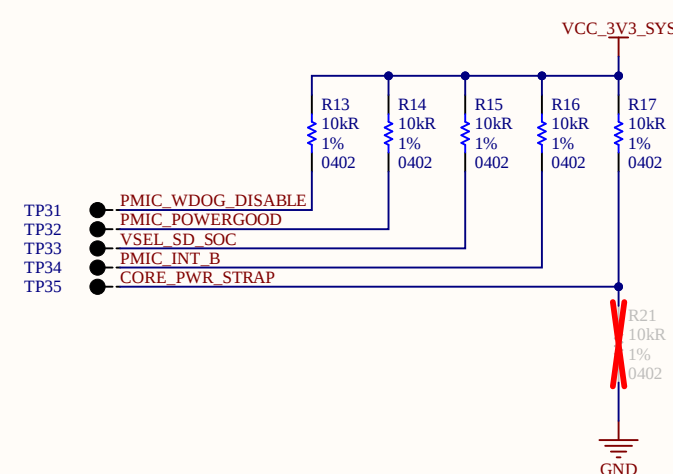
POWER INDICATION LED



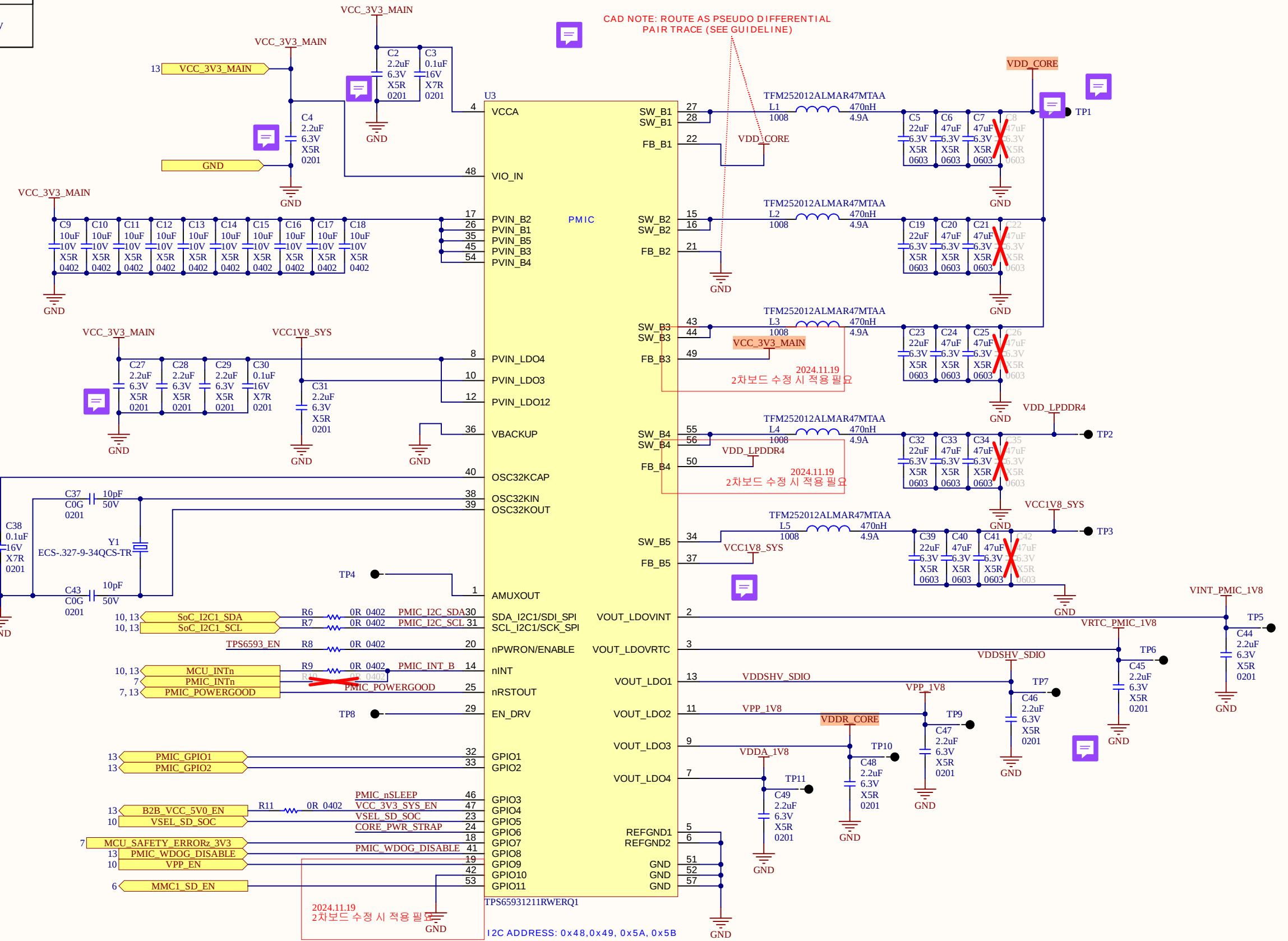
VCC_3V3_SYS POWER SWITCH



PU/PD RESISTORS



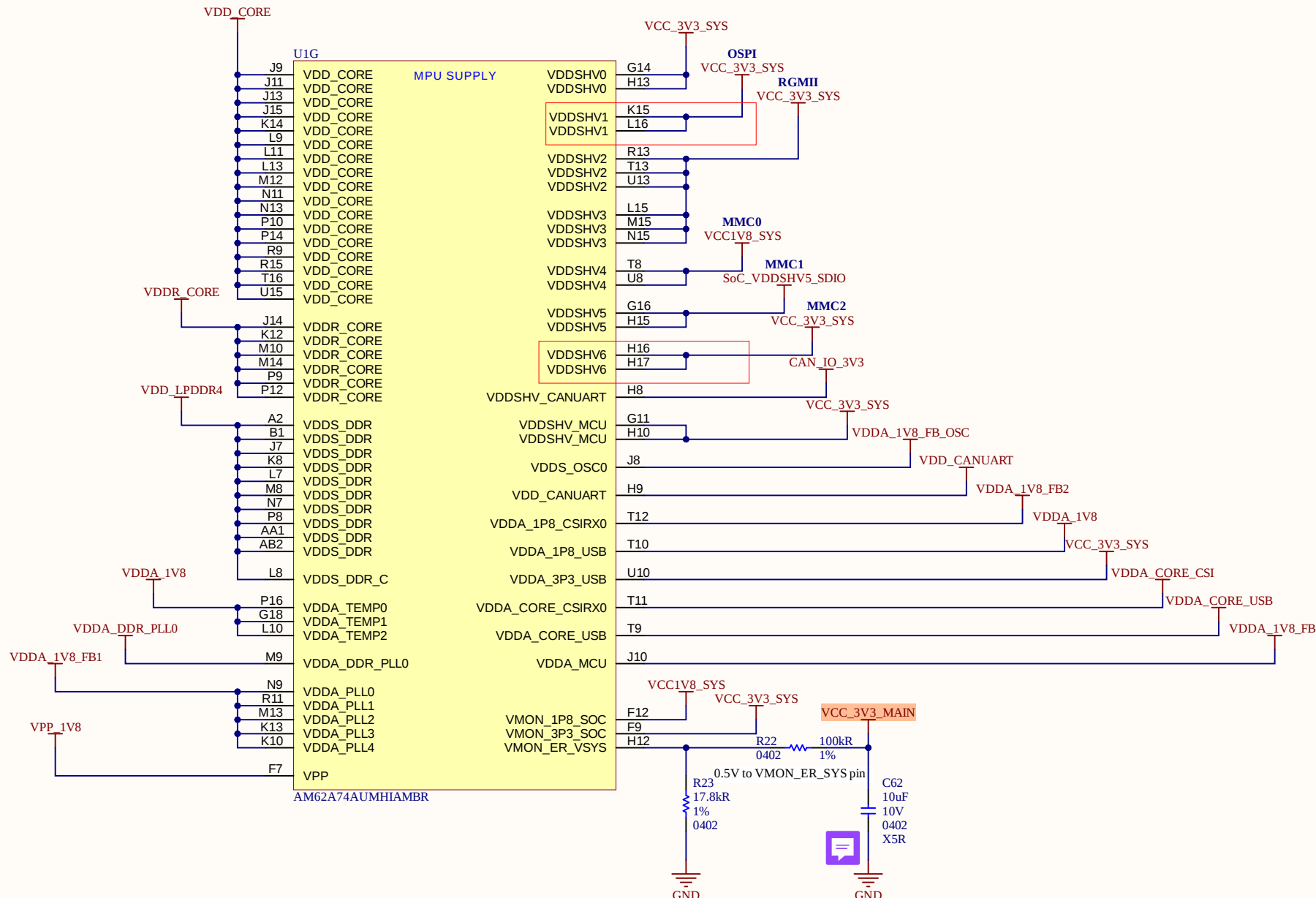
TP1	0.85V	TP7	3.3V
TP2	1.1V	TP9	0V
TP3	1.8V	TP10	0.85V
TP5	1.8V	TP11	1.8V
TP6	1.8V	TP12	3.3V



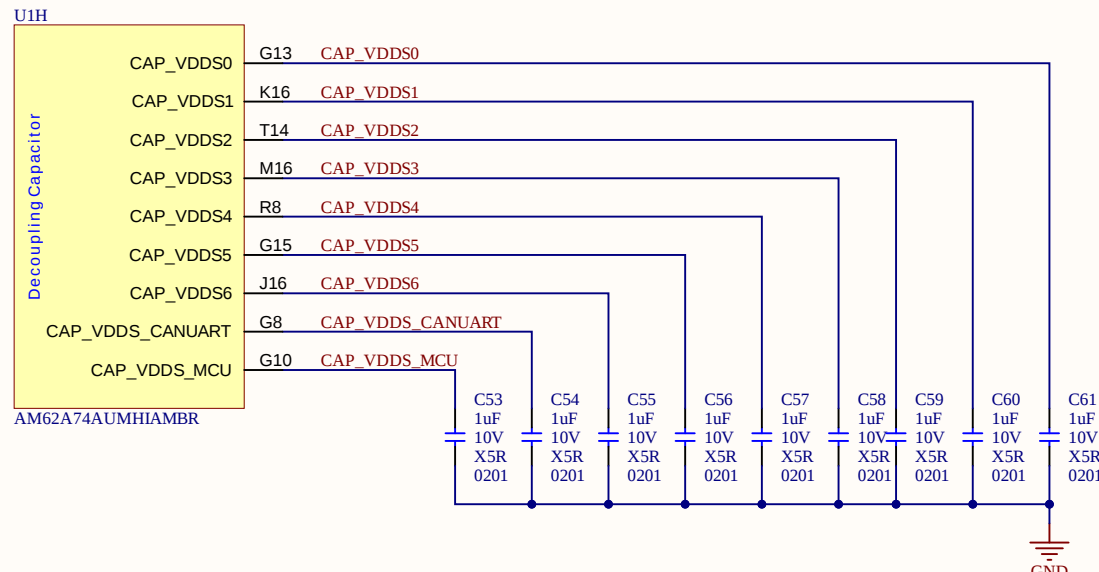
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Sheet Name :	TPS6593 - PMIC		R1.0
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Status :	Preliminary		2 of 13
NOTE :	*		Size :
			C

SoC Power

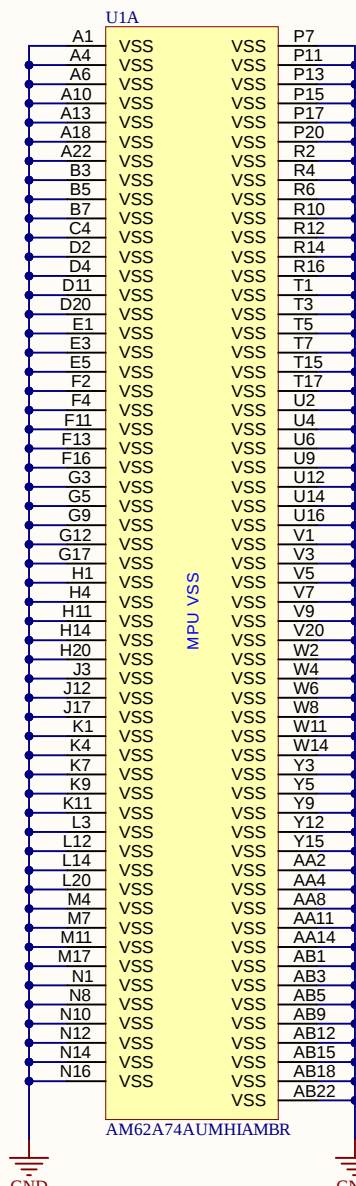
SOC POWER SUPPLY



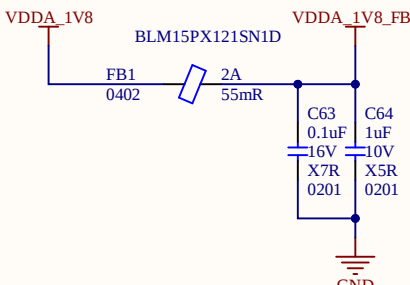
SOC DECOUPLING



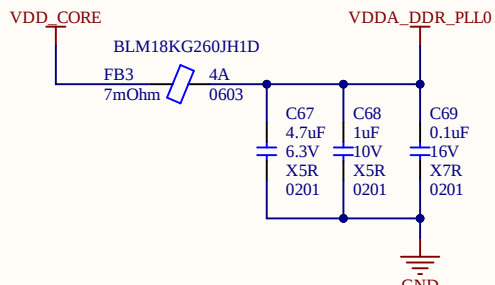
SOC GND



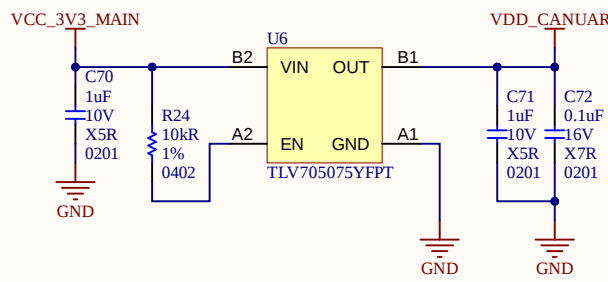
1.8V Analog SUPPLY



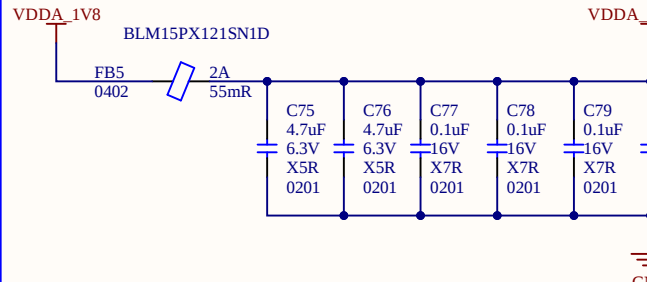
VDDA DDR PLLC



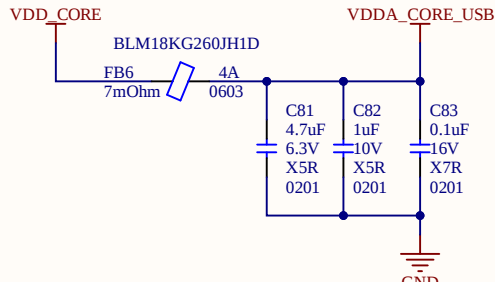
VDD CANUART



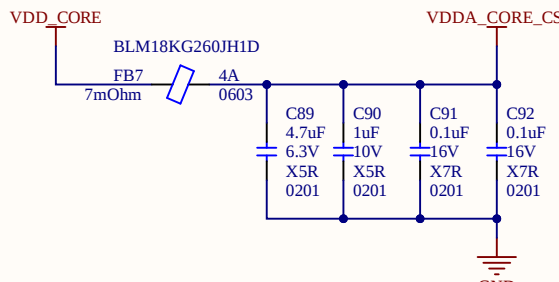
PLL / MCU SUPPLY



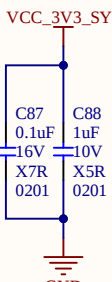
VDDA CORE USE



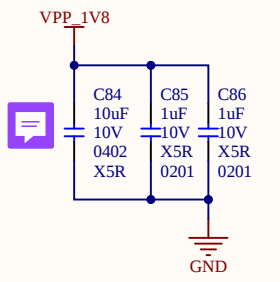
VDDA CORE CSI



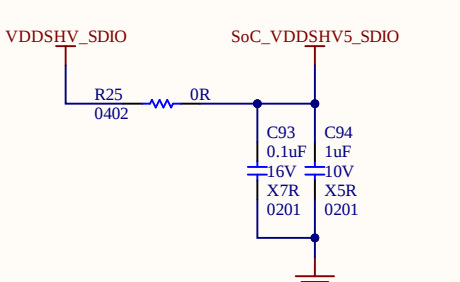
VDDA 3P3 USE



VPP 1V8

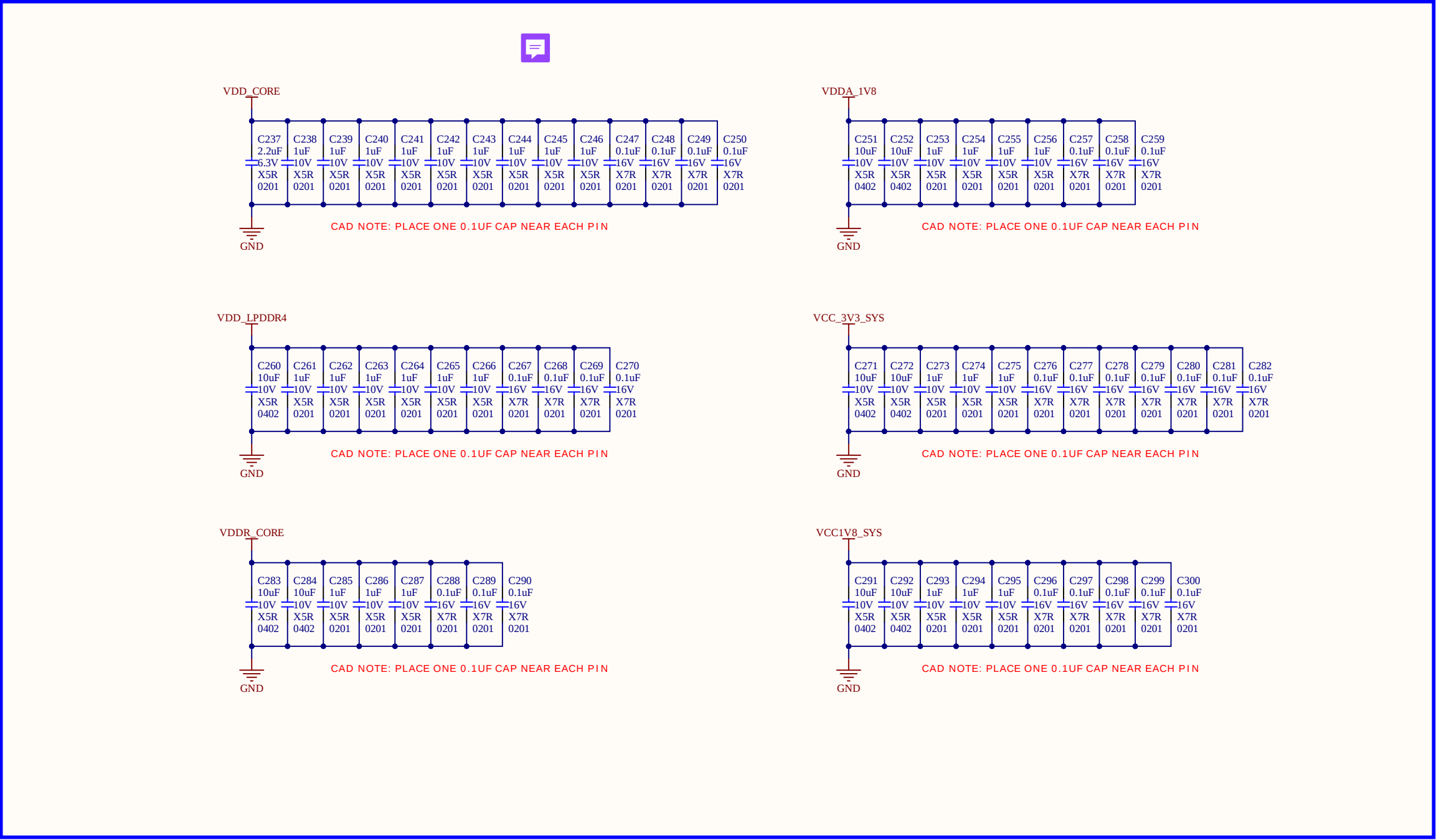


3 3V / 1.8V MMC1 SUPPLY



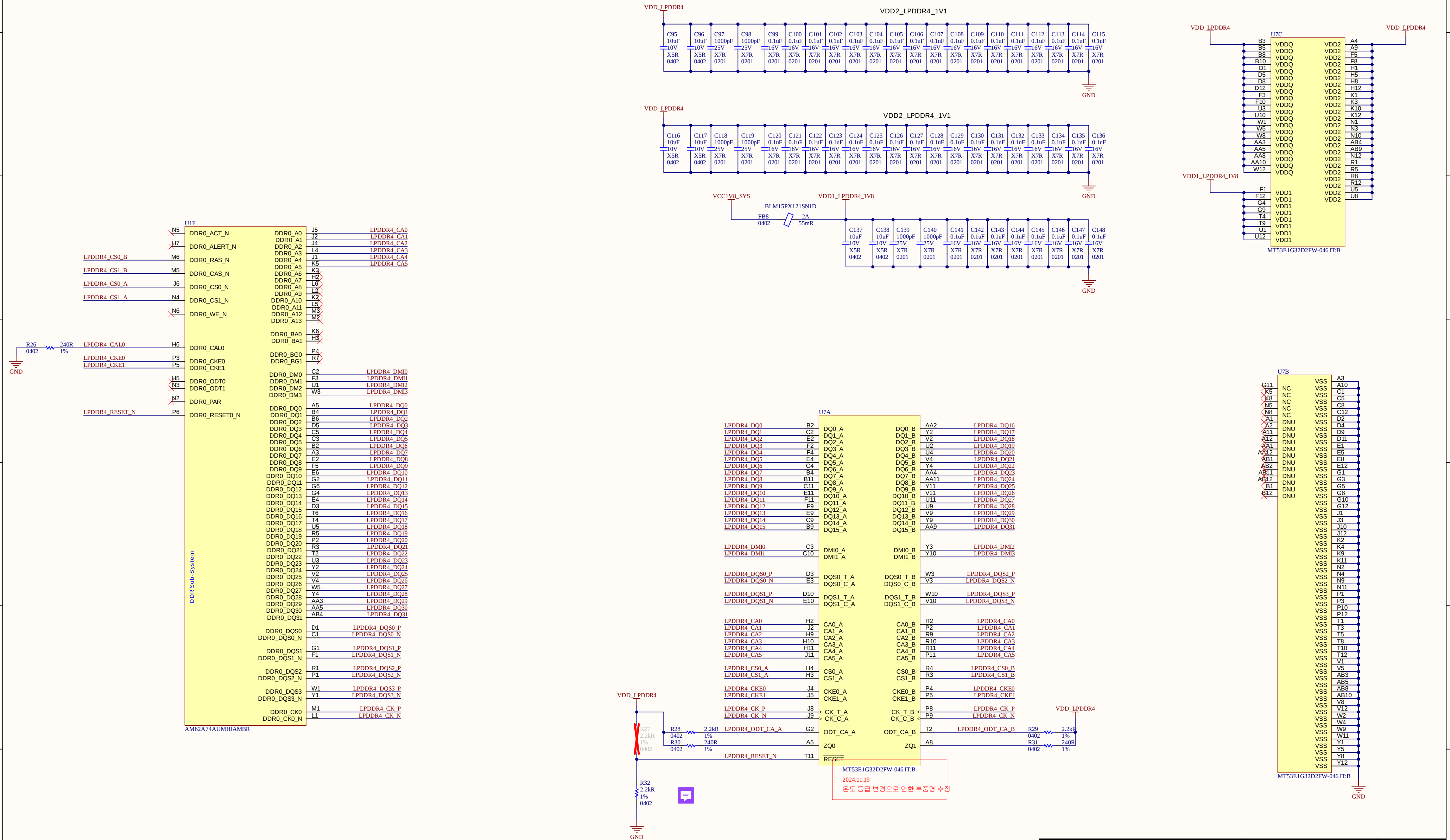
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Sheet Name :	SoC Power		R1.0
Variant :	Prototype		Page :
Status :	Preliminary		3 of 13
NOTE :	*		Size :
			C

SoC Power Decaps



		Drafted	Checked	Approved
Project :	SoM-AM62A7x			Revision : R1.0
Sheet Name :	SoC Power Decaps			Page : 4 OF 13
Variant :	Prototype			Size : C
Status :	Preliminary			
NOTE :	*			

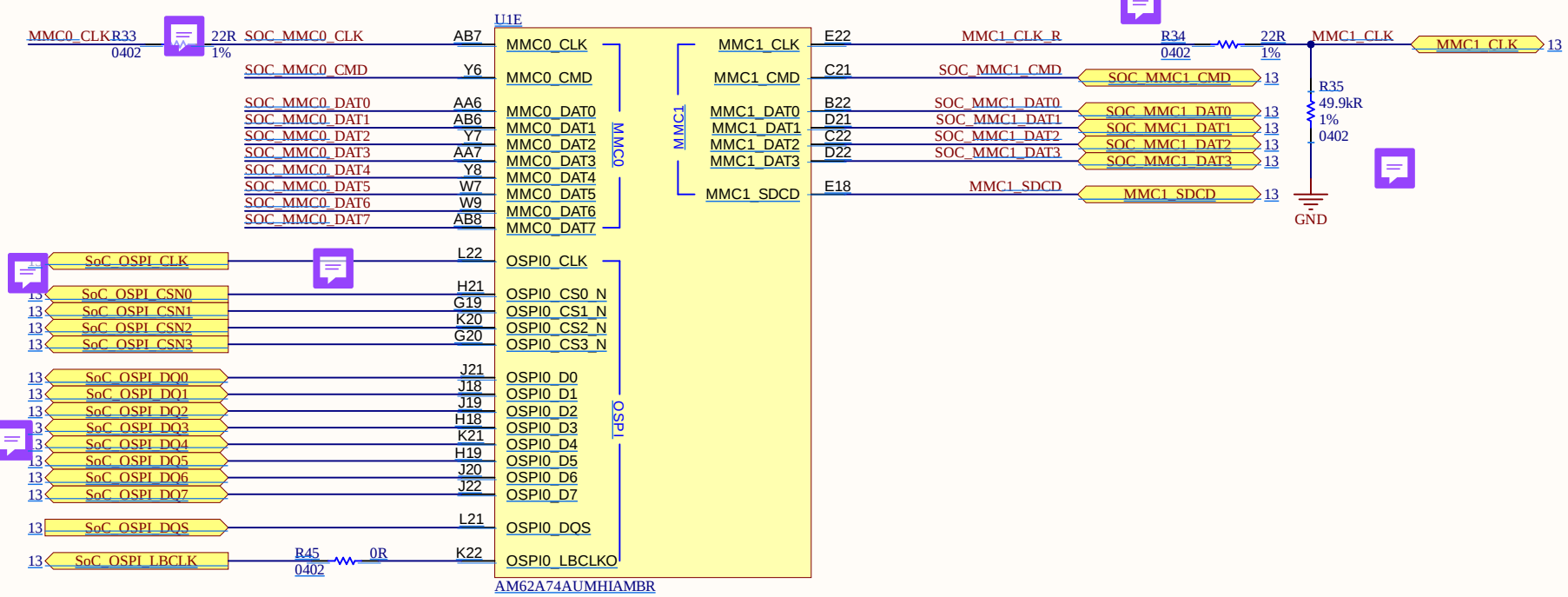
LPDDR4 (4GB)



		Drafted	Checked	Approved
Project :	SoM-AM62ATx			Revision :
Sheet Name :	LPDDR4 (4GB)			R1.0
Variant :	Prototype			Page :
Status :	Preliminary			5 OF 13
NOTE :				Size :
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MMC, OSPI and USB Interface

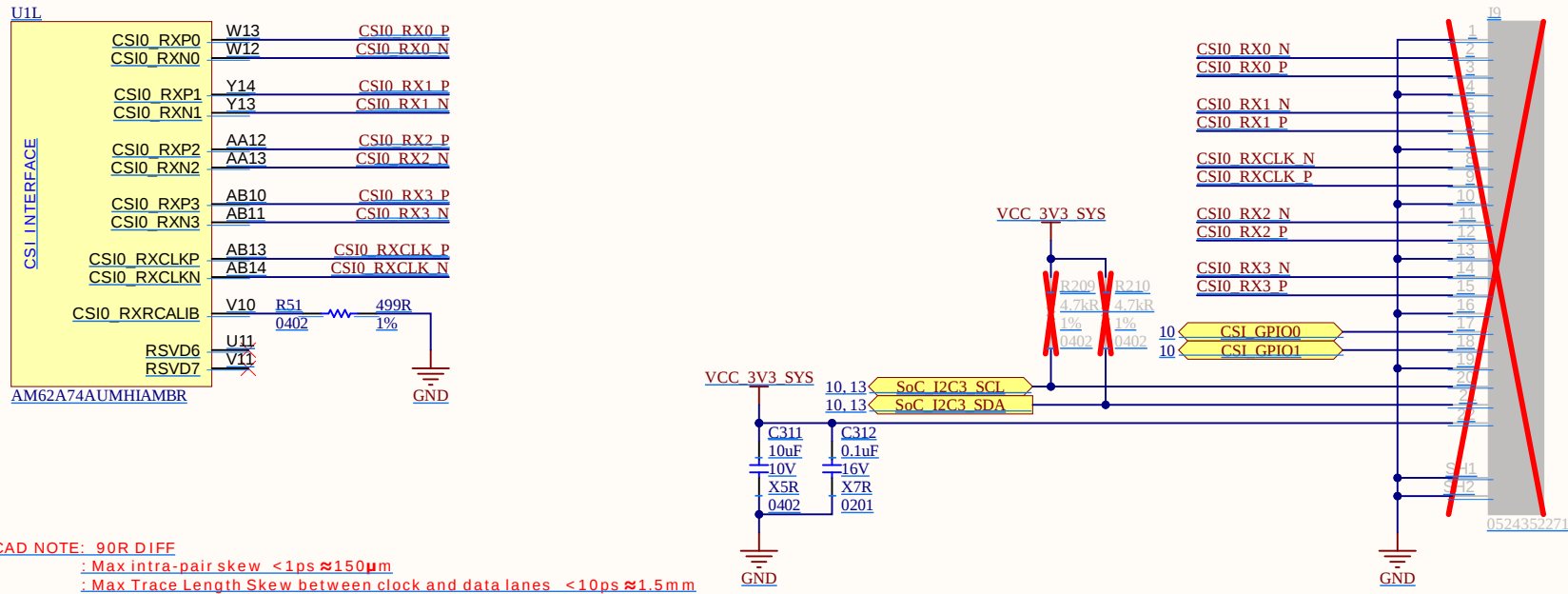
SoC - MMC, OSPI Interface



CAD NOTE: PLACE R45 CLOSE TO THE SOC BALL WITH AS LITTLE TRACE AS POSSIBLE

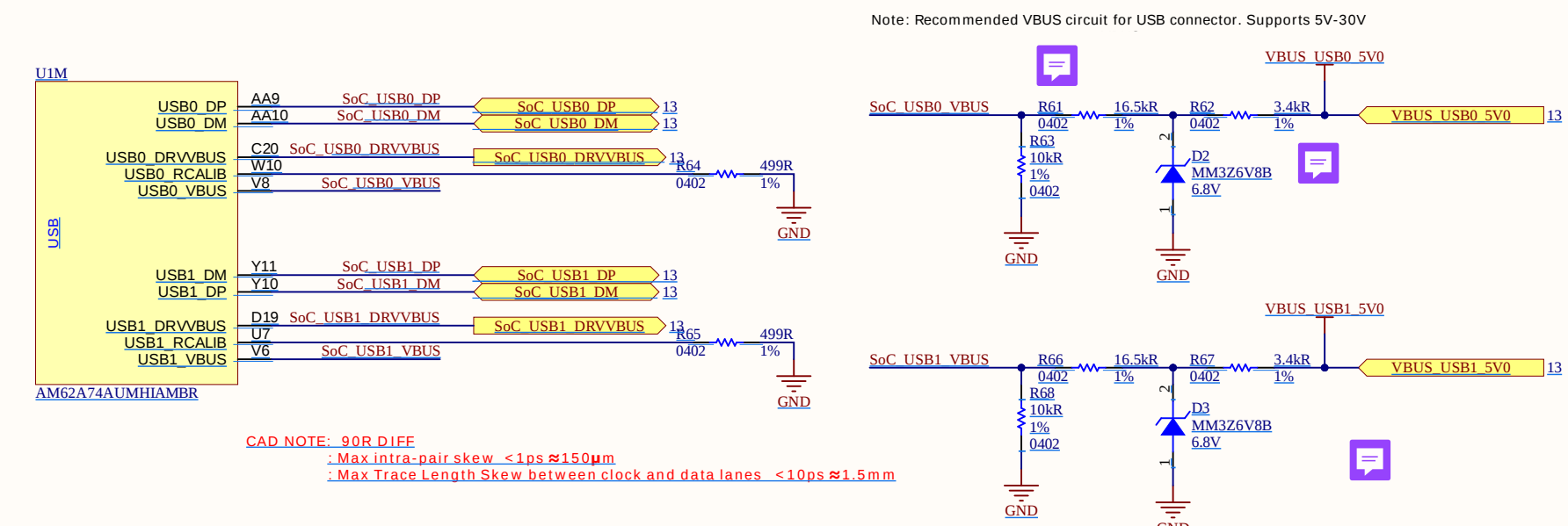
CAD NOTE: 50R SE (OSPI)
:Max Trace Length Skew between clock and data lanes <10ps≒1.5mm

SoC - CSI Interface



CAD NOTE: 90R DIFF
:Max intra-pair skew <1ps≒150μm
:Max Trace Length Skew between clock and data lanes <10ps≒1.5mm

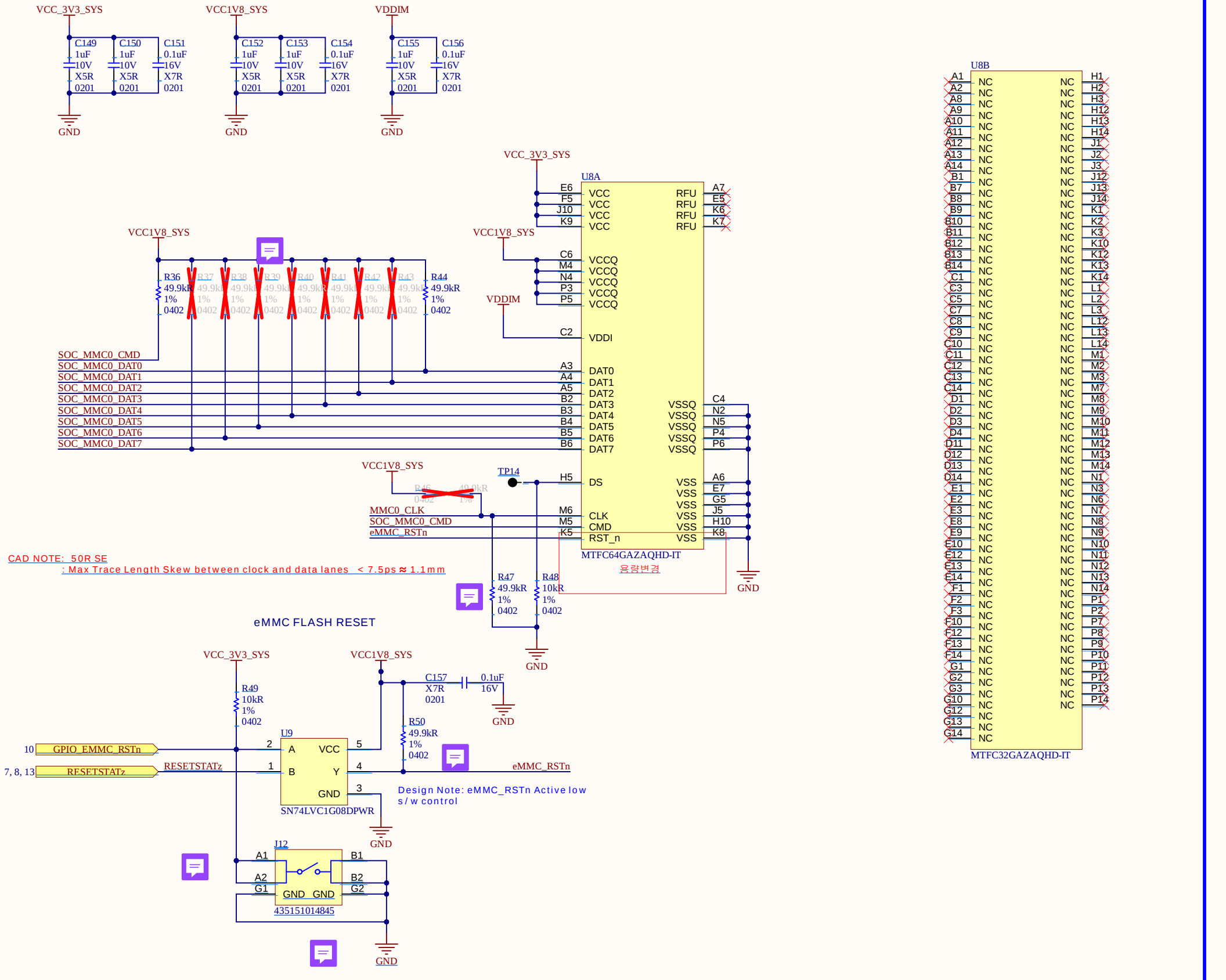
SoC - USB Interface



CAD NOTE: 90R DIFF
:Max intra-pair skew <1ps≒150μm
:Max Trace Length Skew between clock and data lanes <10ps≒1.5mm

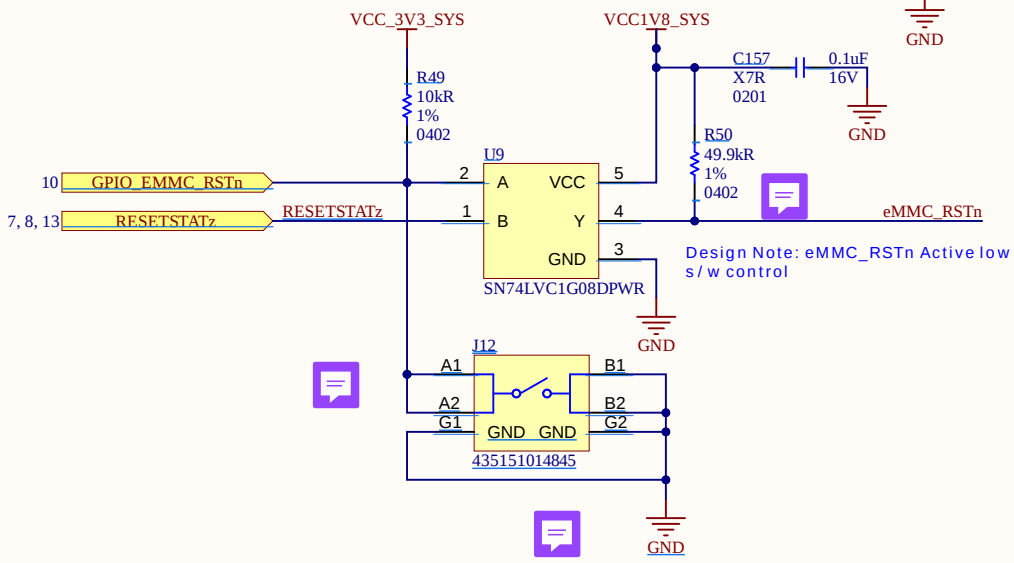
eMMC (32GB)

2차 제작 시 64GB로 변경



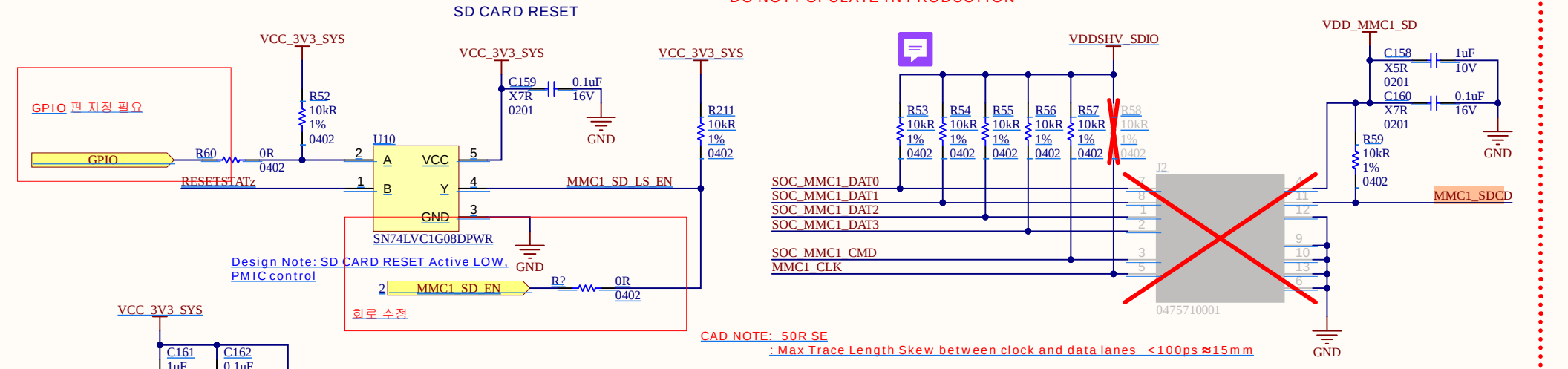
CAD NOTE: 50R SE
:Max Trace Length Skew between clock and data lanes <7.5ps≒1.1mm

eMMC FLASH RESET



SD Card Interface

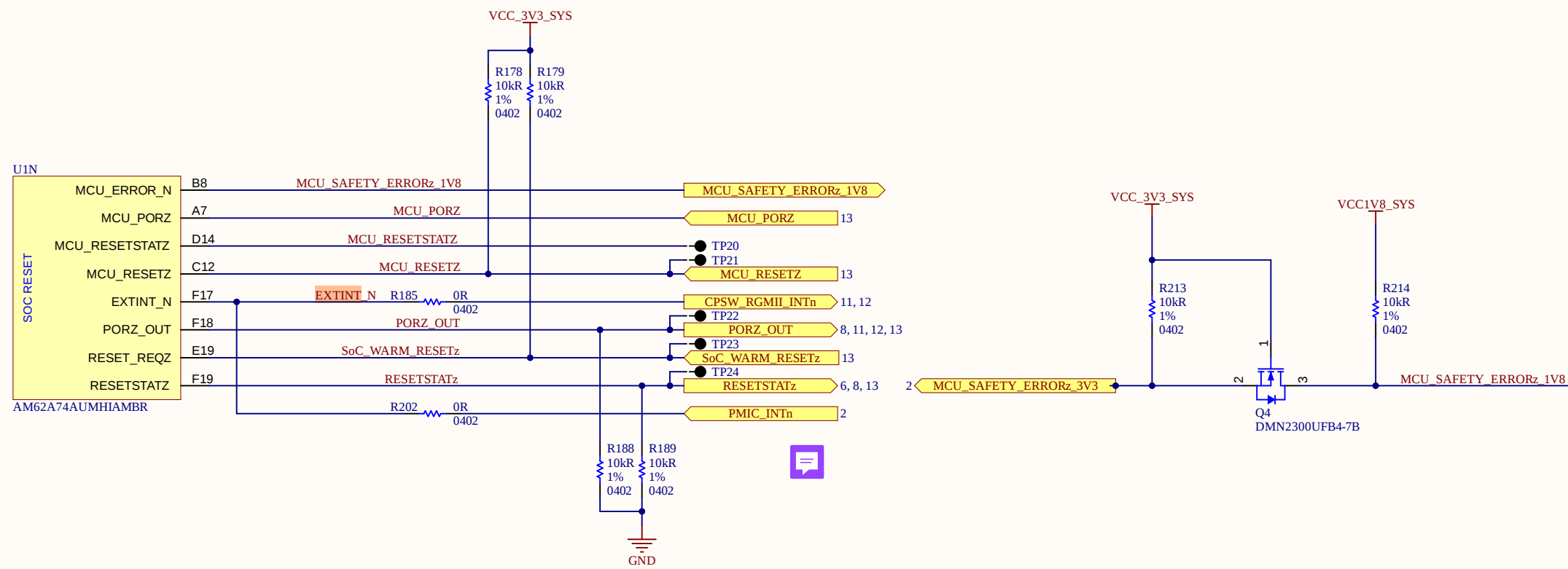
INTERNAL USE ONLY
DO NOT POPULATE IN PRODUCTION



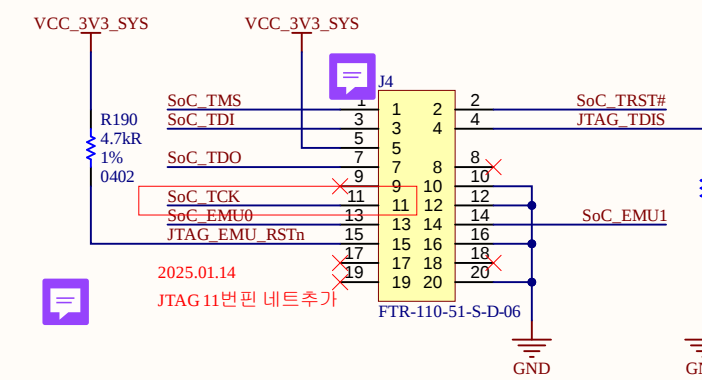
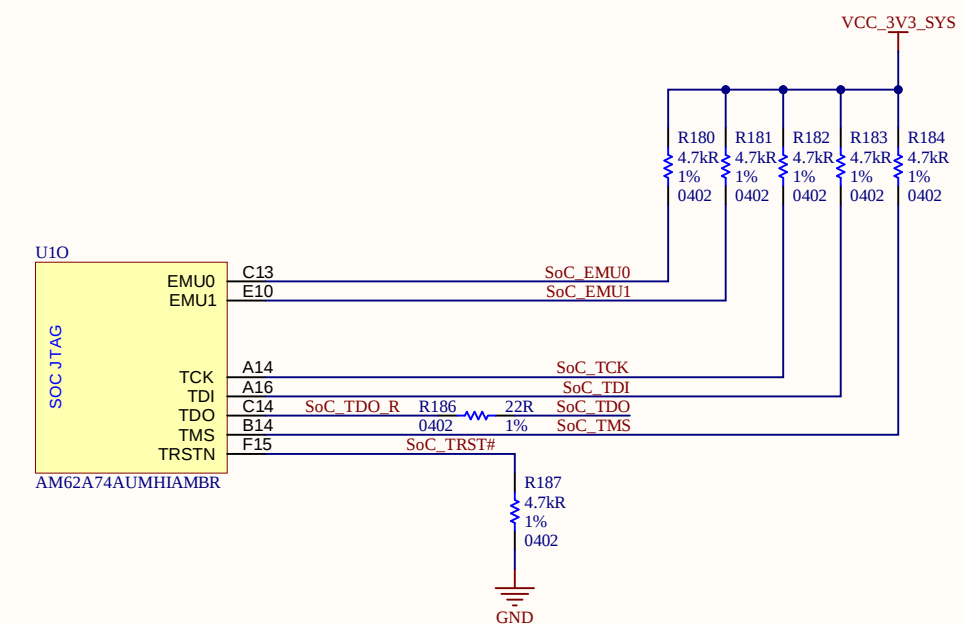
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Sheet Name :	MMC, OSPI and USB Interface		
Variant :	Prototype		
Status :	Preliminary		
NOTE :			
Revision :	R1.0		
Page :	6 OF 13		
Size :	C		

DEBUG, RESET

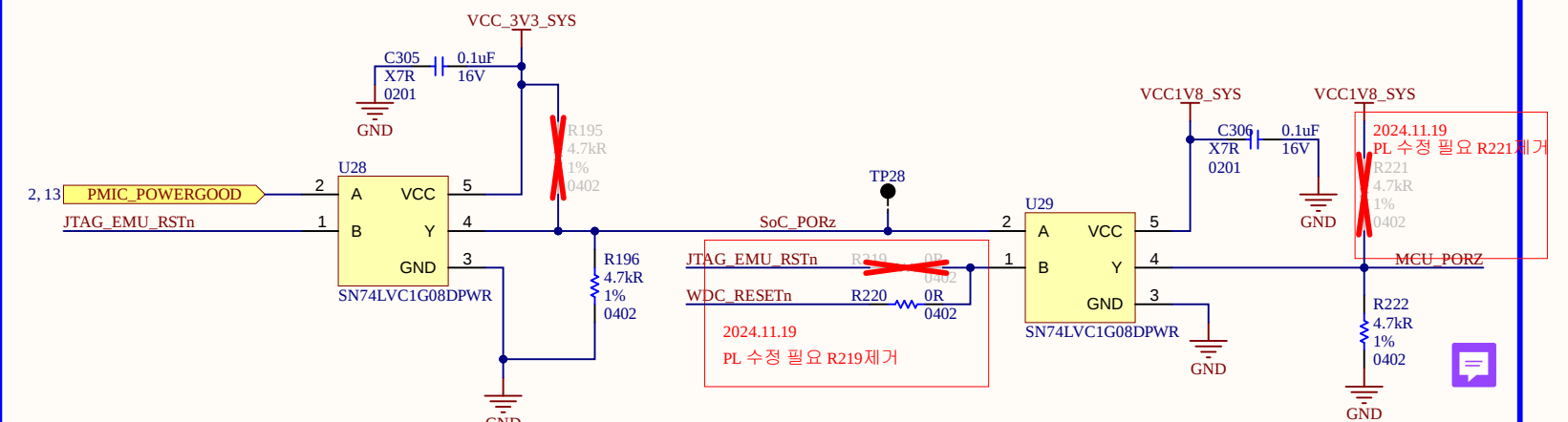
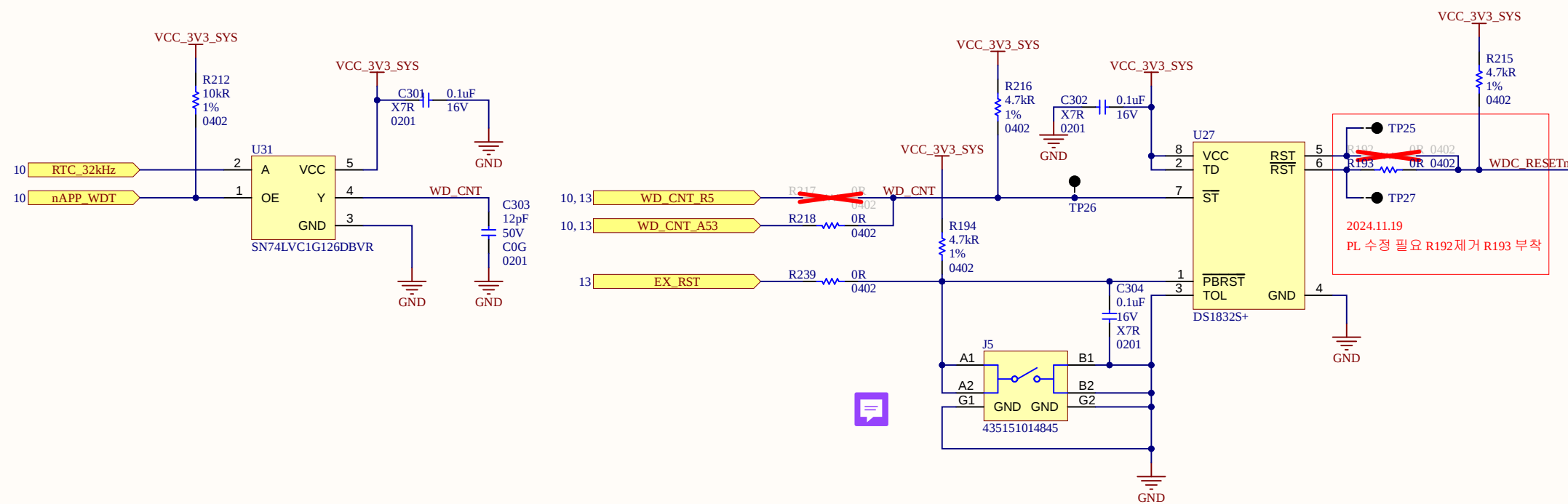
SoC RESET



SoC JTAC



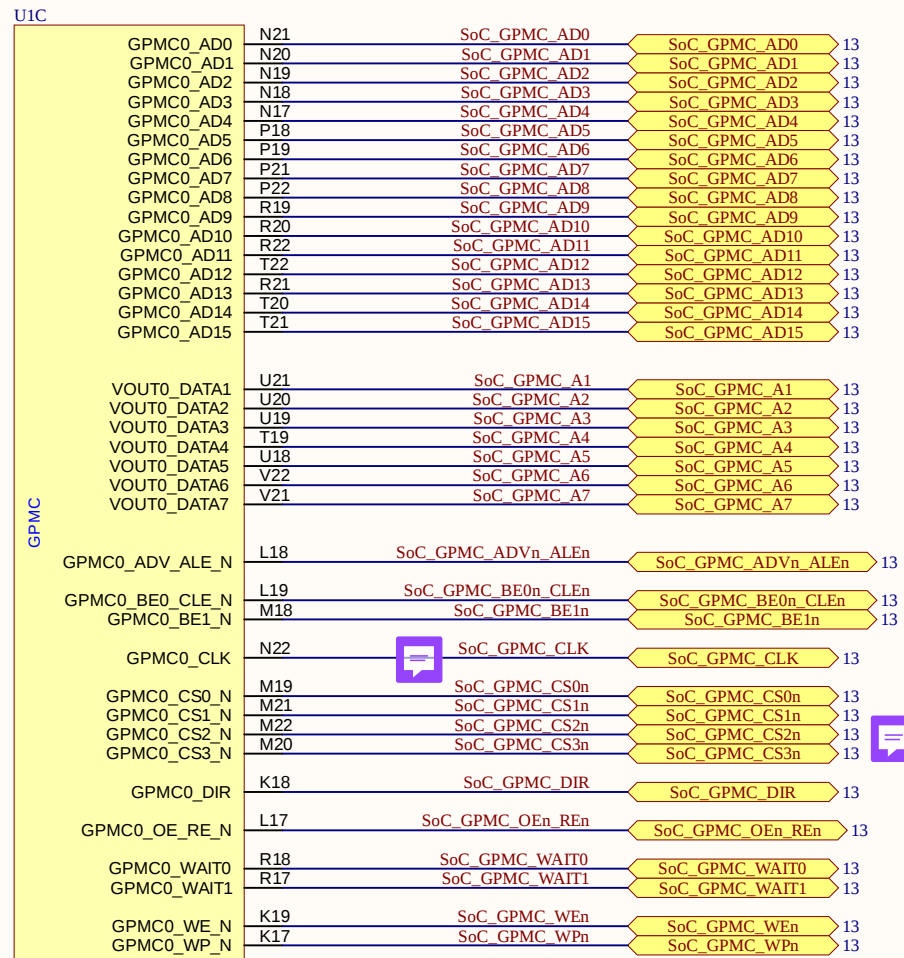
WATCHDOG TIMER



	Drafted	Checked	Approved
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Sheet Name :	DEBUG, RESET		R1.0
Variant :	Prototype		Page :
Status :	Preliminary		7 of 13
NOTE :	*		Size :
			C

GPMC Interface

GPMC



AM62A74UMHIAMBR

CAD NOTE: 50R SE

: Max Trace Length Skew between clock and data lanes < 7.5ps ≈ 1.1mm

BOOTCONFIG TABLE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserv	Reserv	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode						PLL Config

PLL Config Pins			Ref Clock (MHz)		
B2	B1	B0			
0	0	0	19.2		
0	0	1	20		
0	1	0	24		
0	1	1	25		
1	0	0	26		
1	0	1	27 ⁽¹⁾		
1	1	0	Reserved		
1	1	1	Reserved		

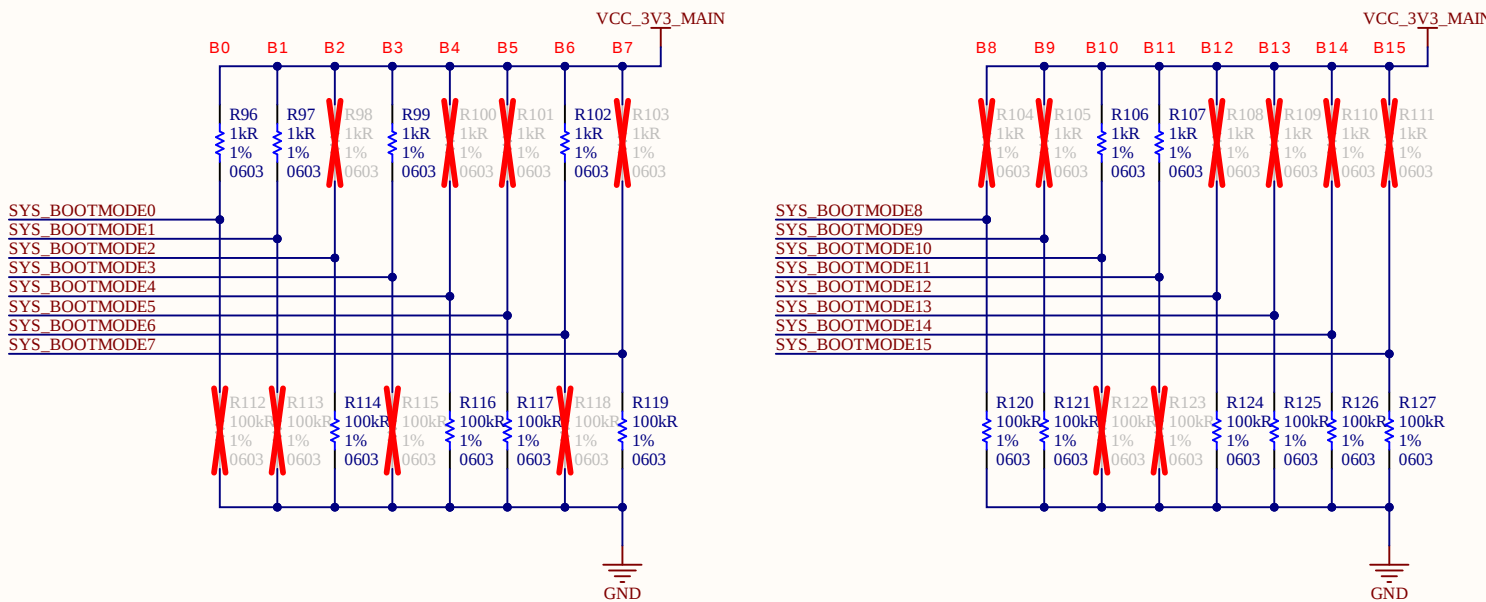
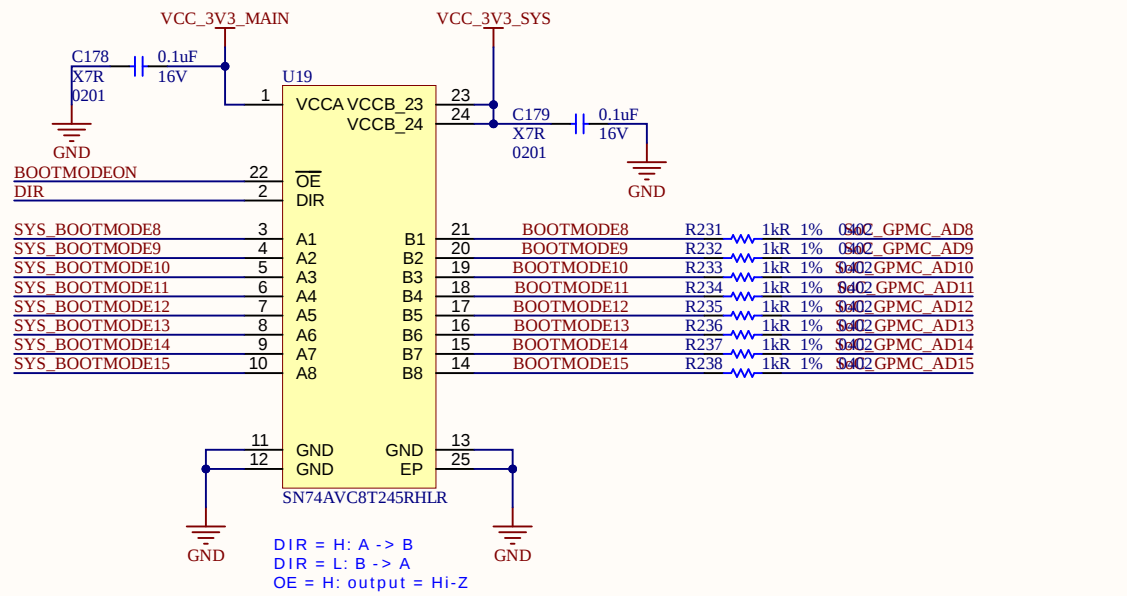
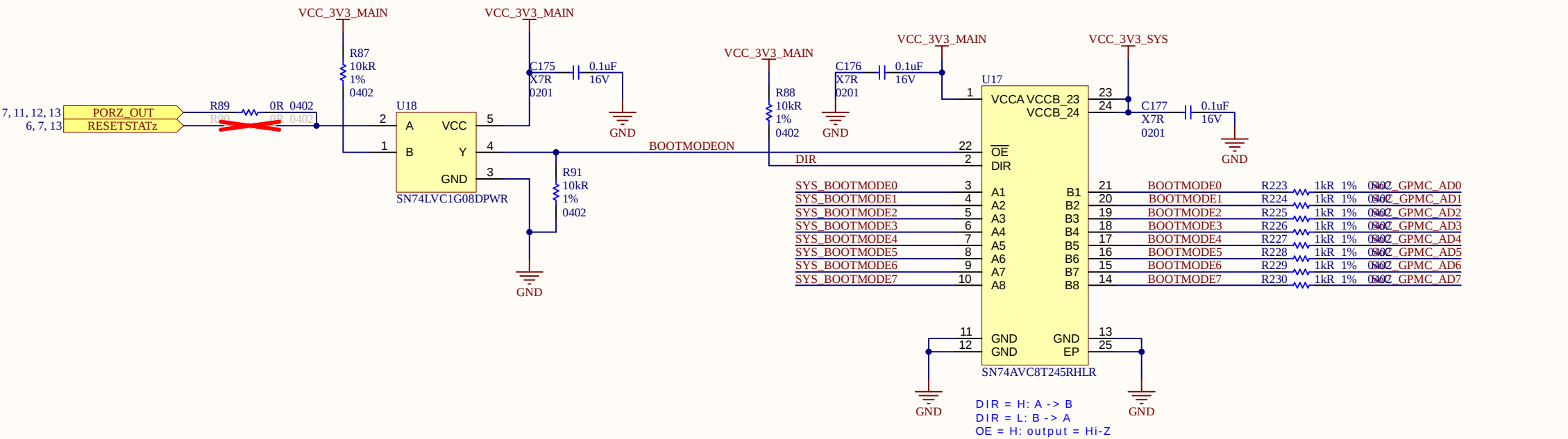
Primary Boot Mode Config				Primary Boot Mode		
B9	B8	B7	B6	B5	B4	B3
Reserved	Mode	Csel	0	0	1	1
0	0	Link Info	0	1	0	0
Clkout	Clk src	0	0	1	0	1
Bus reset	Reserved	Addr	0	1	1	0
Reserved	Reserved	Reserved	0	1	1	1
Port	Reserved	Fs/raw	1	0	0	0
Reserved	Reserved	Reserved	1	0	0	1
Core Volt	Mode	Lane Swap	1	0	1	0
Reserved	Reserved	Reserved	1	0	1	1
Reserved	Reserved	Reserved	1	1	0	0
Reserved	Reserved	Reserved	1	1	0	1
SFPD	Read Cmd	Mode	1	1	1	0
Reserved	ARM/Thumb	No/Dev	1	1	1	1

Backup Boot Mode Selection				Backup Boot Mode Selected	
B13	B12	B11	B10		
Reserved	0	0	0		None
Mode	0	0	1		USB
Reserved	0	1	0		Reserved
Reserved	0	1	1		UART
IF	1	0	0		Ethernet
Port	1	0	1		MMCSDBoot (SD Card Boot or eMMC Boot)
Reserved	1	1	0		SPI
Reserved	1	1	1		I2C

PRIMARY BOOT MODE	B6	B5	B4	B3
UART	0	1	1	1
MMCSDBoot	1	0	0	0
EMMC(DEFAULT)	1	0	0	1
USB	1	0	1	0

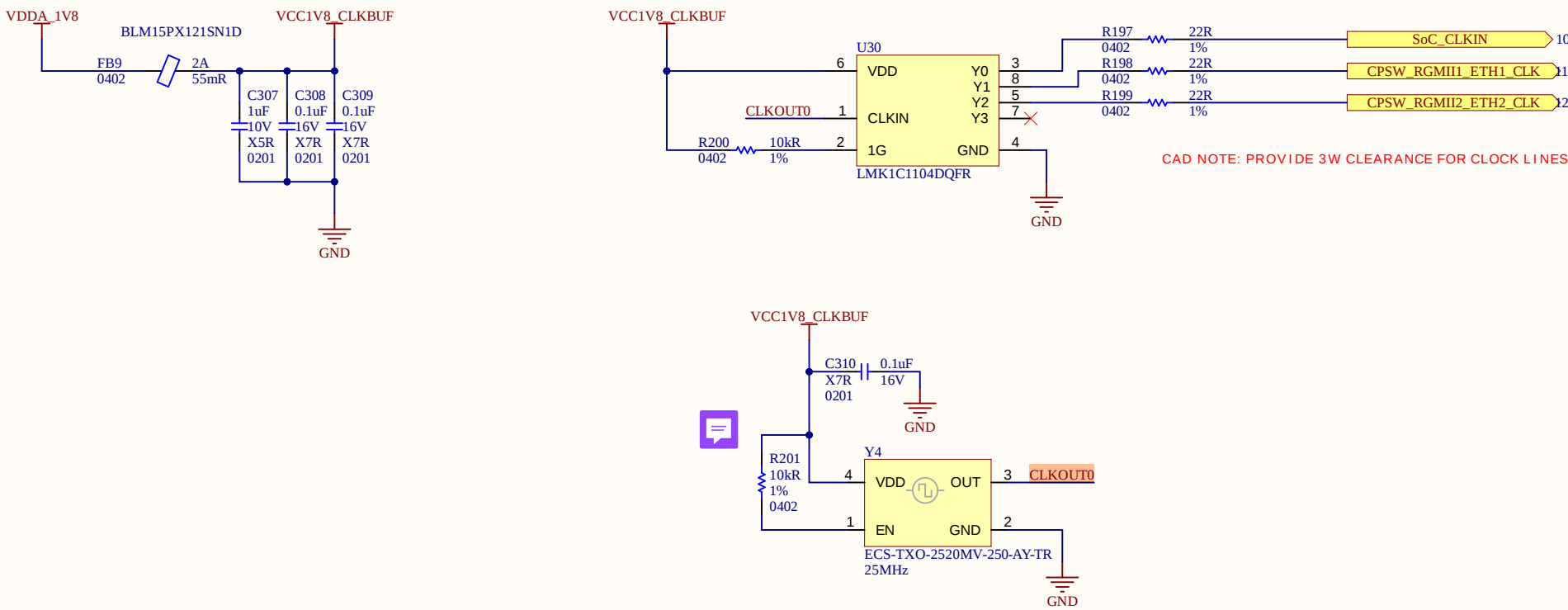
BACKUP BOOT MODE	B13	B12	B11	B10
UART(DEFAULT)	X	0	1	1
MMCSDBoot	1	1	0	1
USB	X	0	0	1

BOOTMODE CONFIG



CAD NOTE: PLACE RESISTORS WITH SINGLE PAD OVERLAP

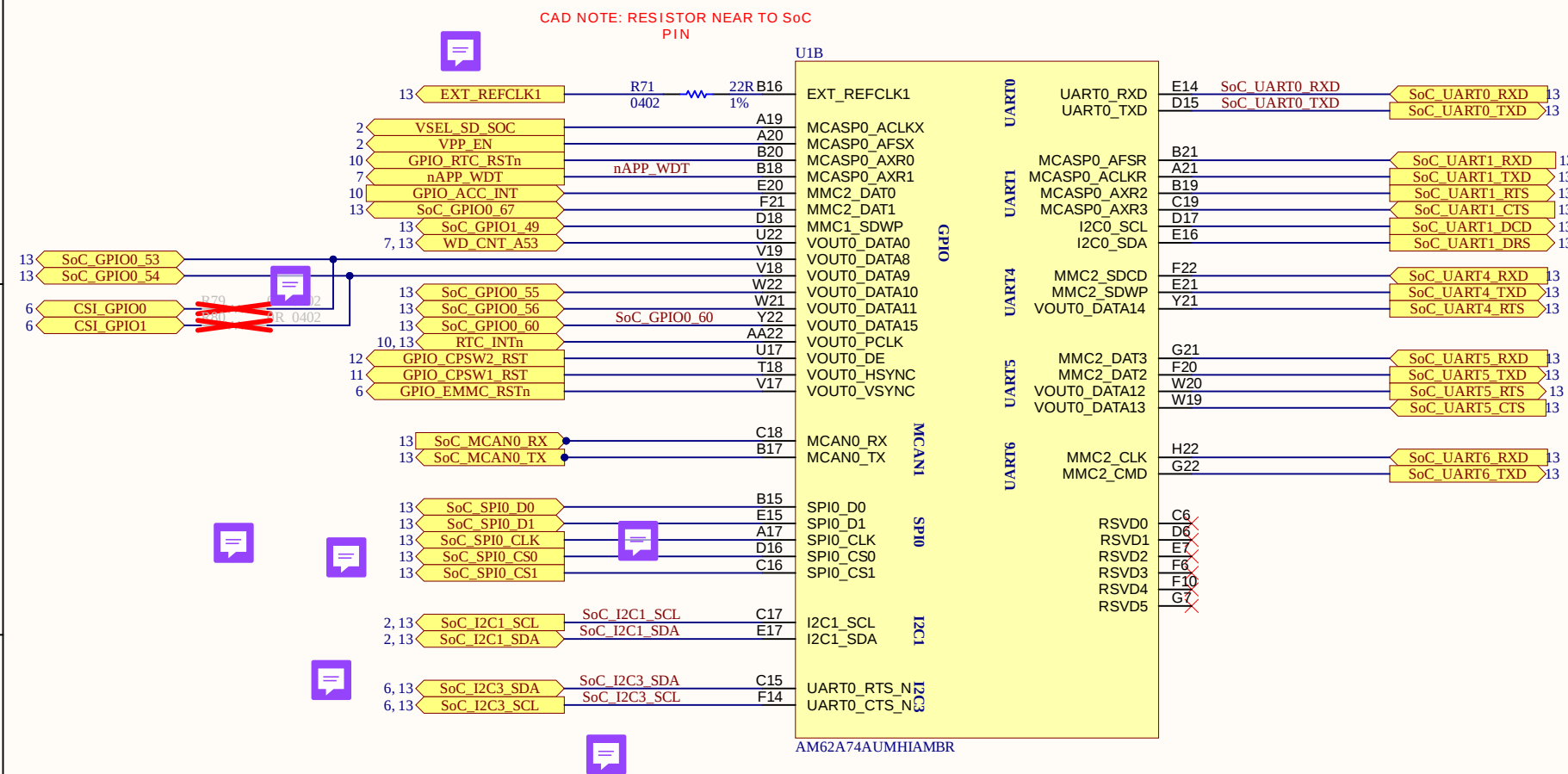
CLOCK BUFFER



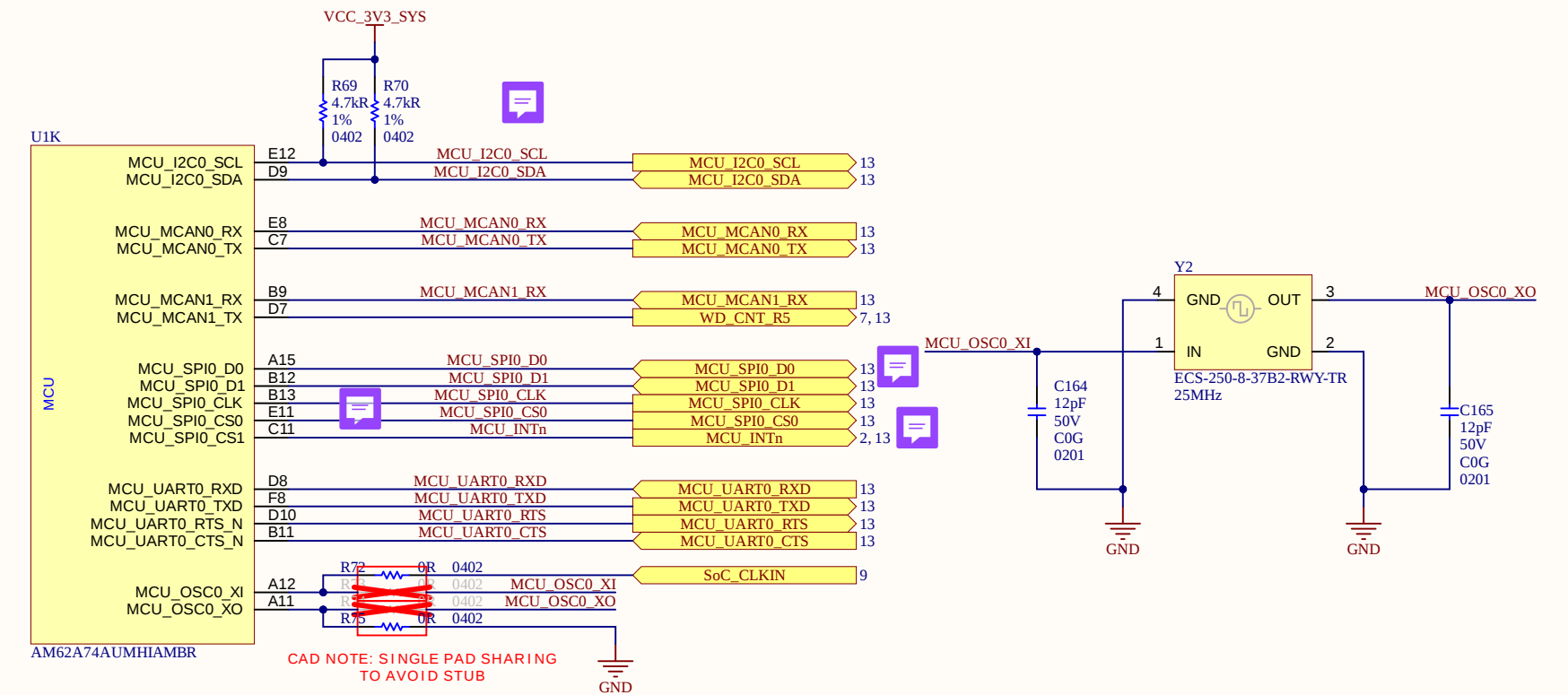
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Project :	SoM-AM62A7x			Revision : R1.0
Sheet Name :	CLOCK BUFFER			Page : 9 OF 13
Variant :	Prototype			Size : C
Status :	Preliminary			
NOTE :	*			

PERIPHERAL

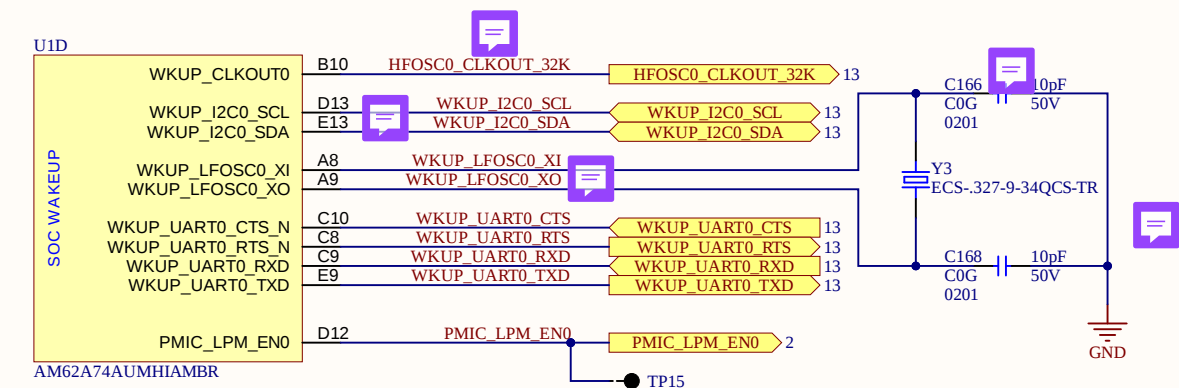
SOC DOMAIN



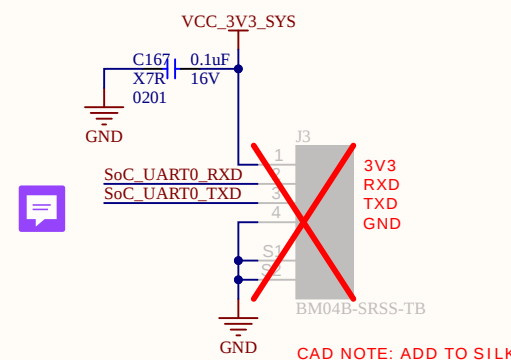
MCU DOMAIN



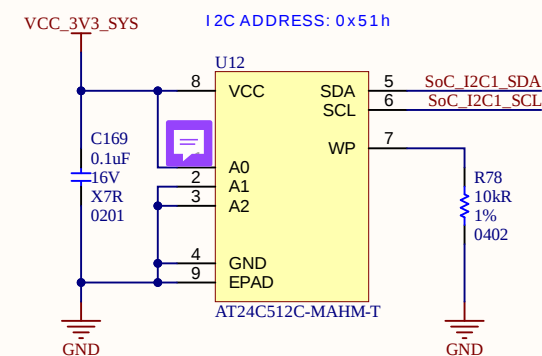
SOC WAKEUP DOMAIN



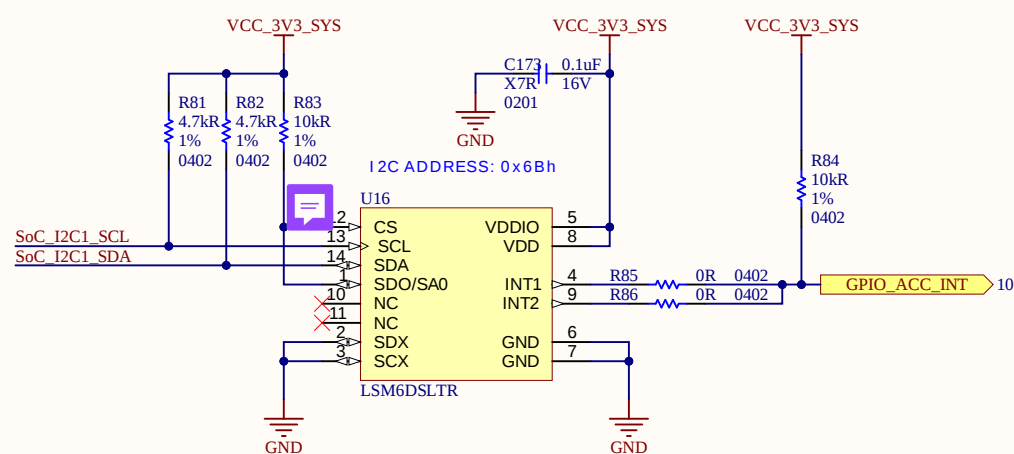
SOC UART LOG



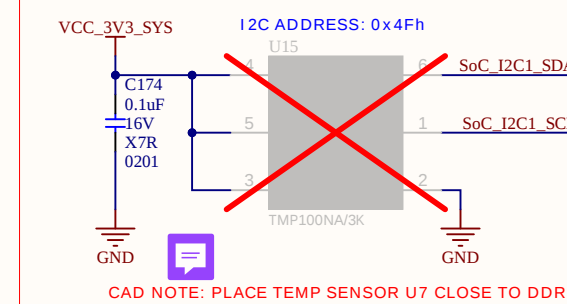
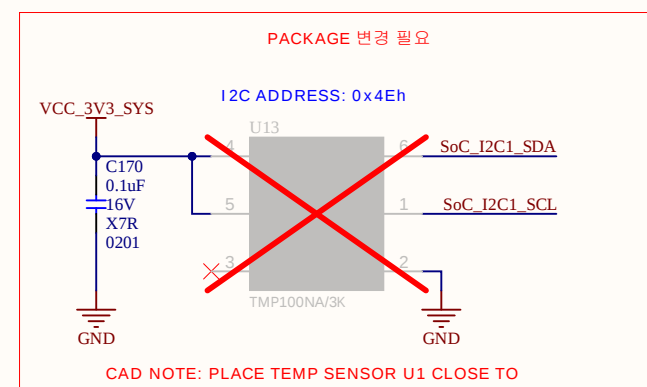
BOARD ID EEPROM (I2C1)



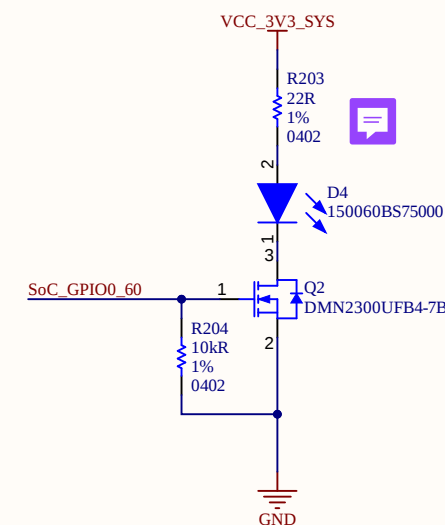
IMU SENSOR (I2C1)



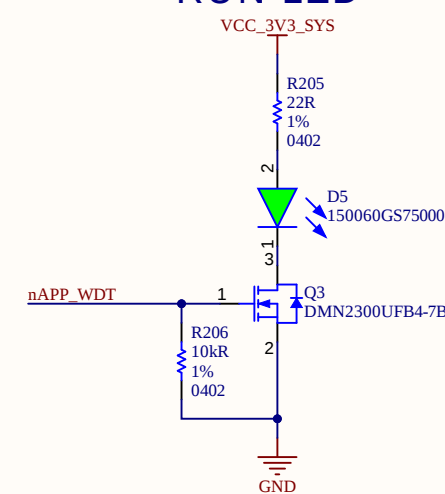
TEMPERATURE SENSORS (I2C1)



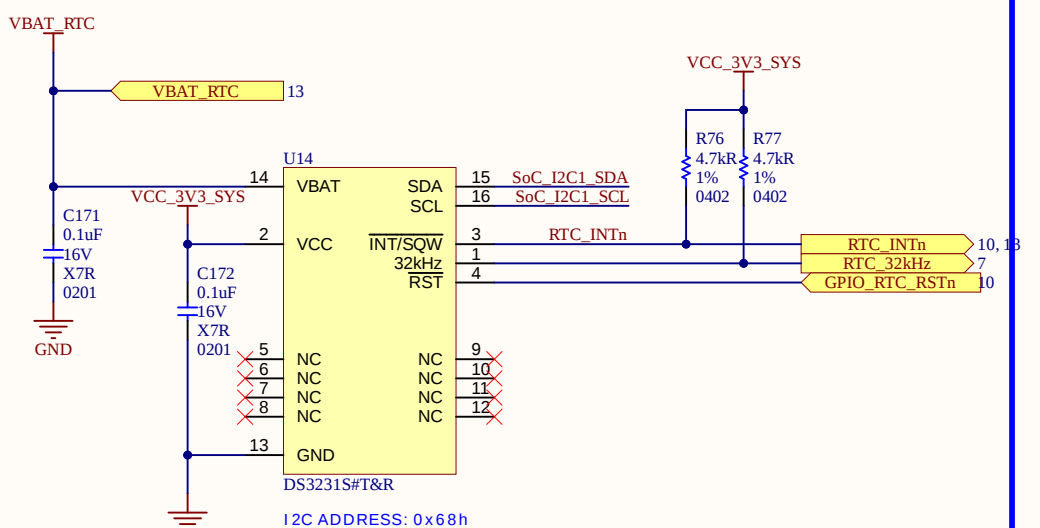
USER LED



RUN LED

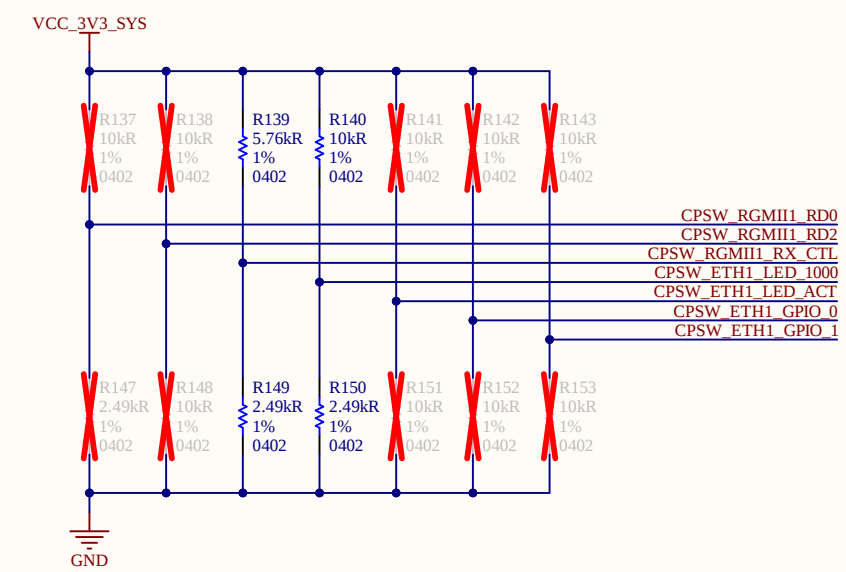
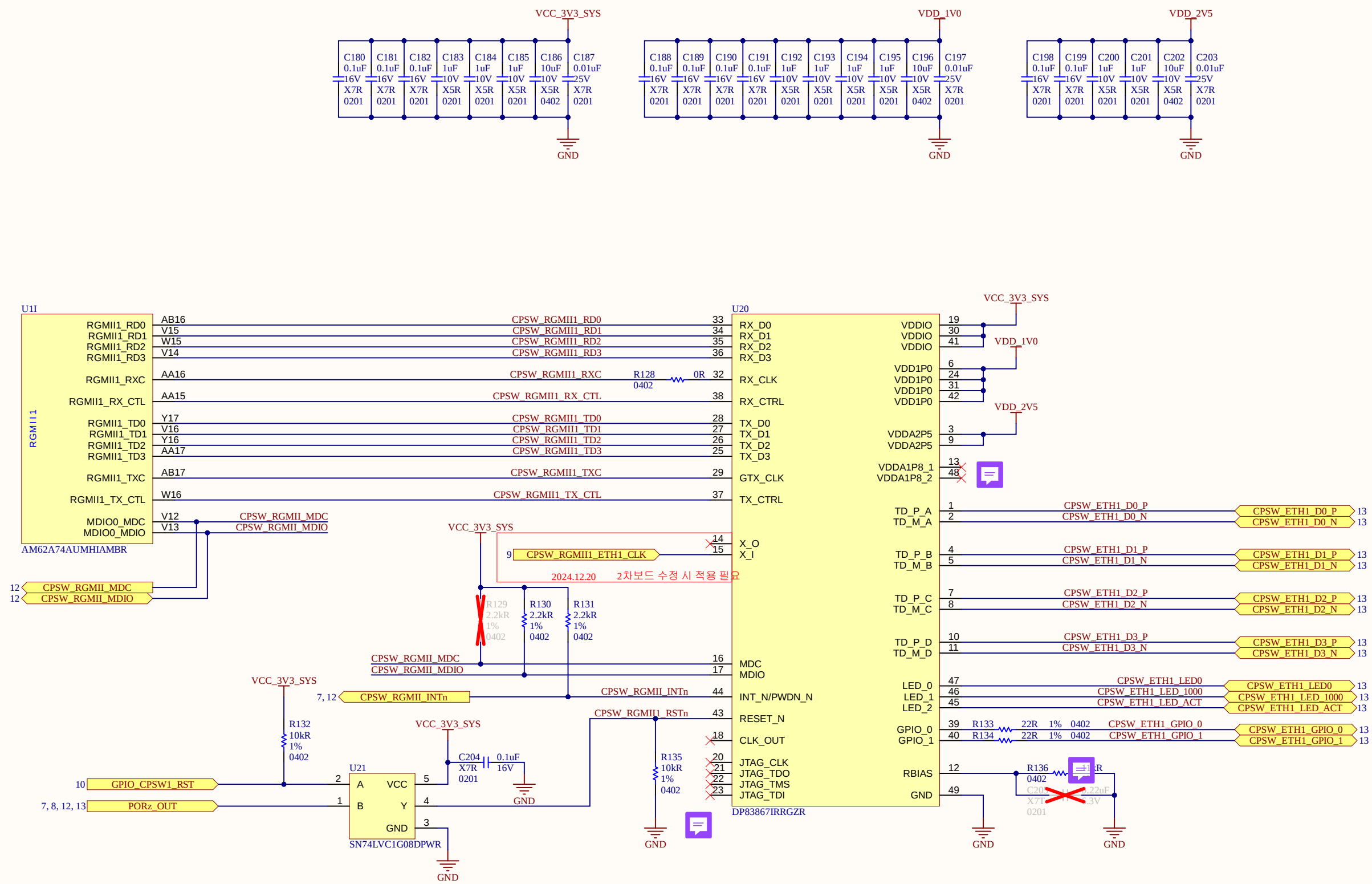


RTC (I2C1)

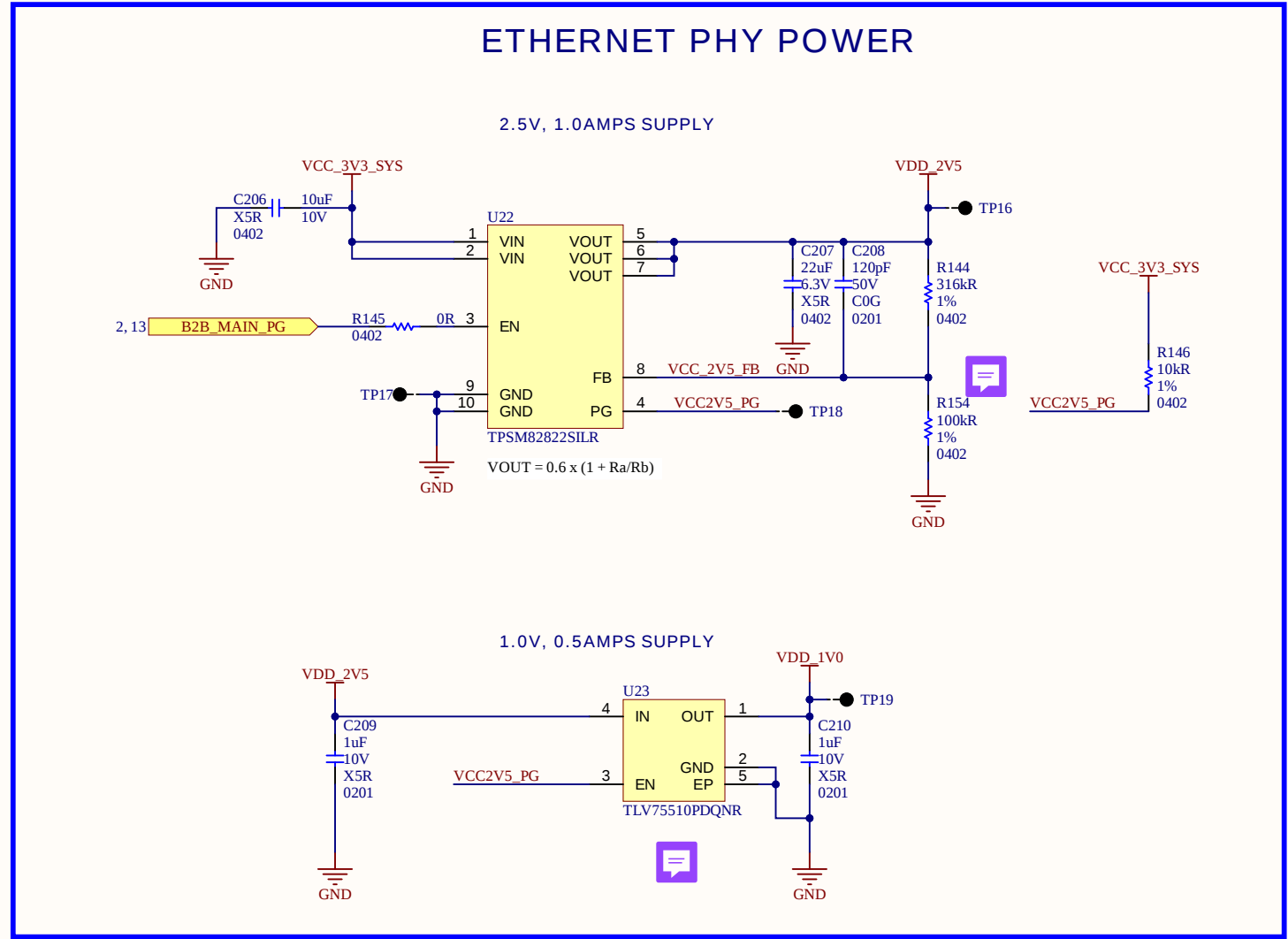


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Project :	SoM-AM62A7x		Revision :
Sheet Name :	PERIPHERAL		R1.0
Variant :	Prototype		Page :
Status :	Preliminary		10 OF 13
NOTE :	*		Size :
			C

CPSW RGMII 1 - PHY

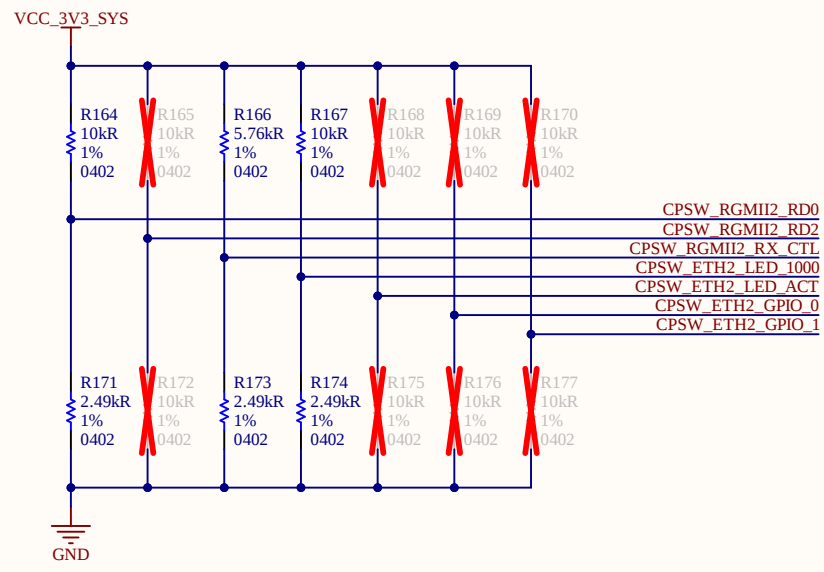
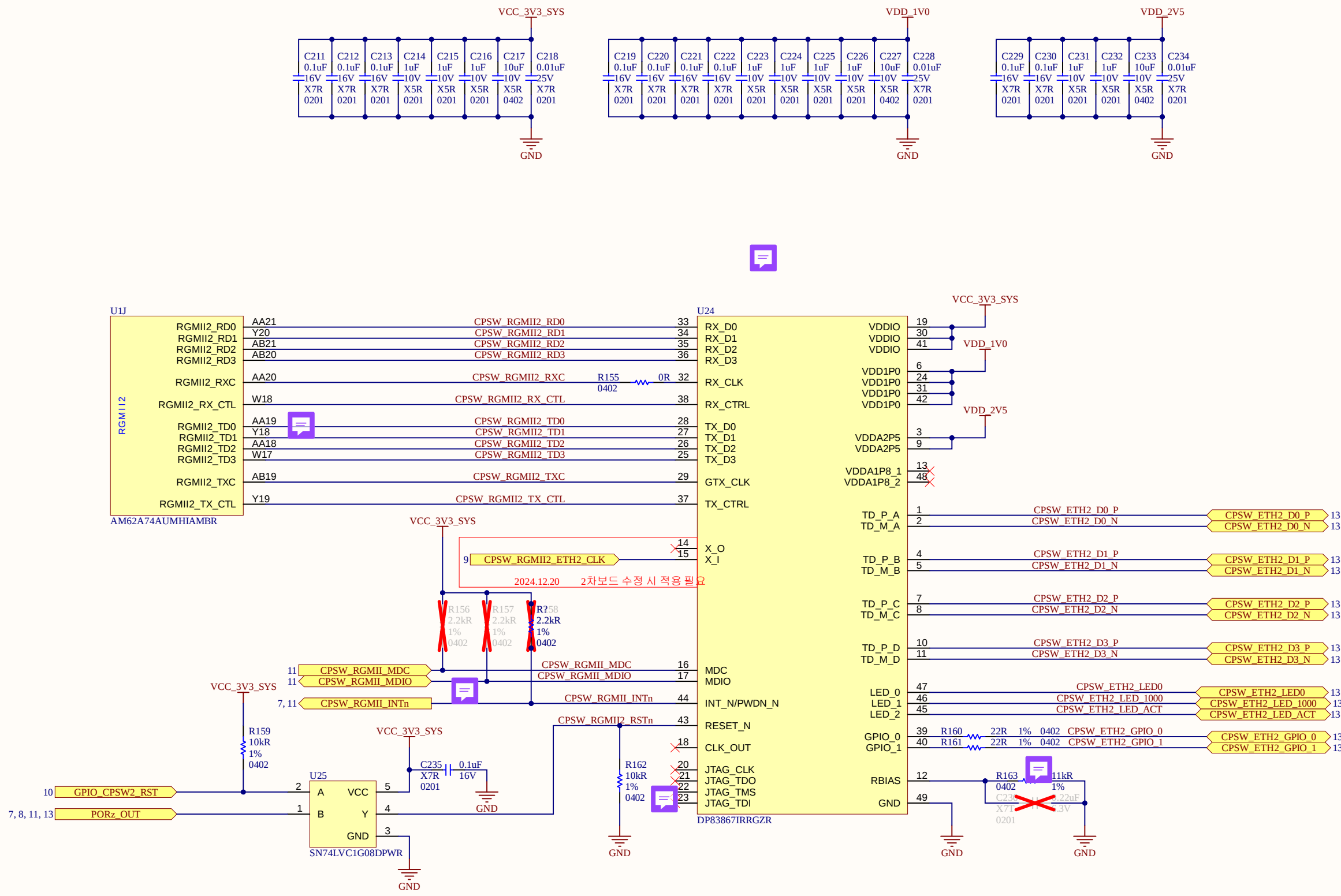


PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns



		Drafted	Checked	Approved
Project :	SoM-AM62A7x			Revision : R1.0
Sheet Name :	CPSW RGMII 1 - PHY			Page : 11 of 13
Variant :	Prototype			Size : C
Status :	Preliminary			
NOTE :				

CPSW RGMII 2 - PHY

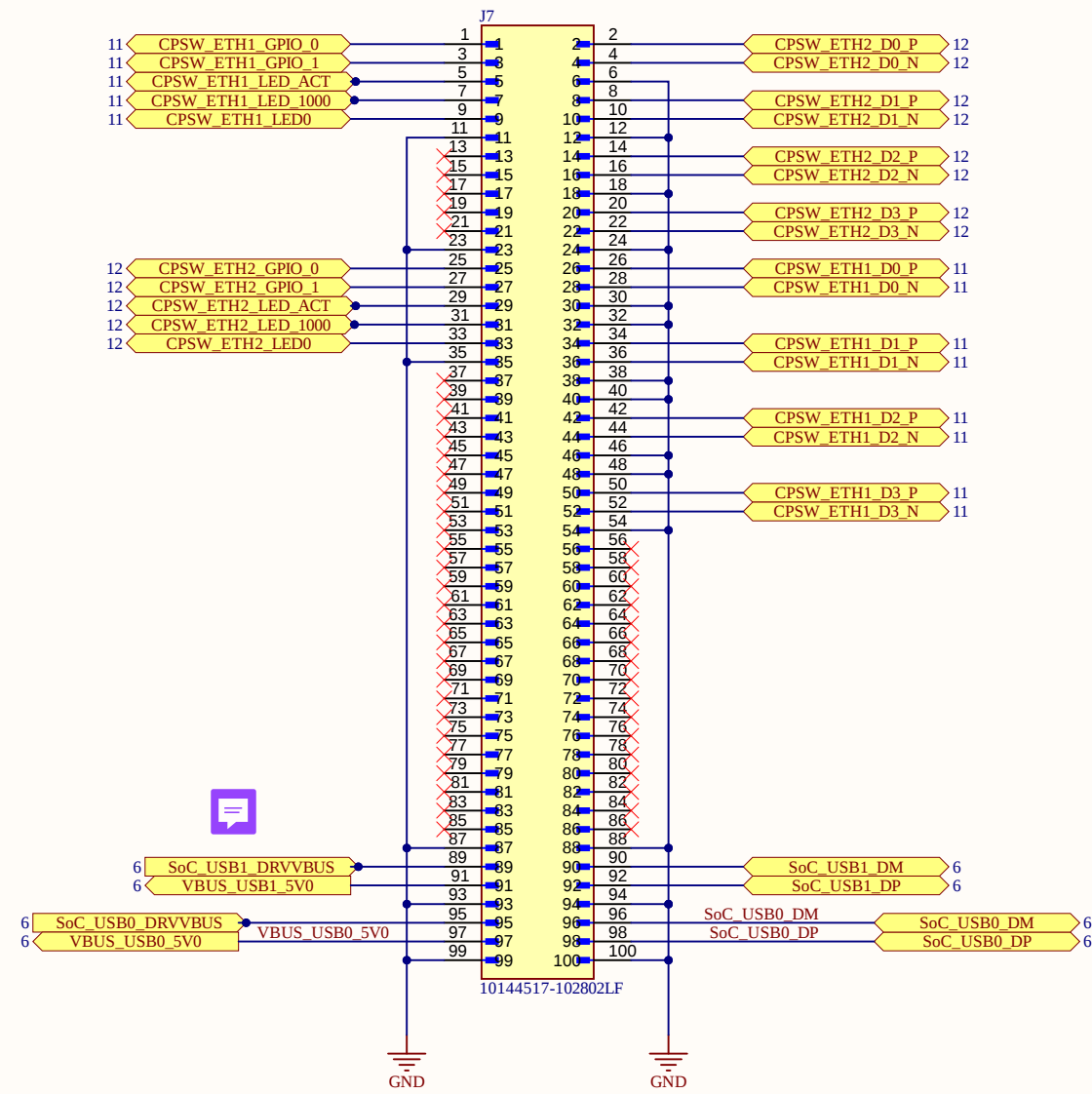
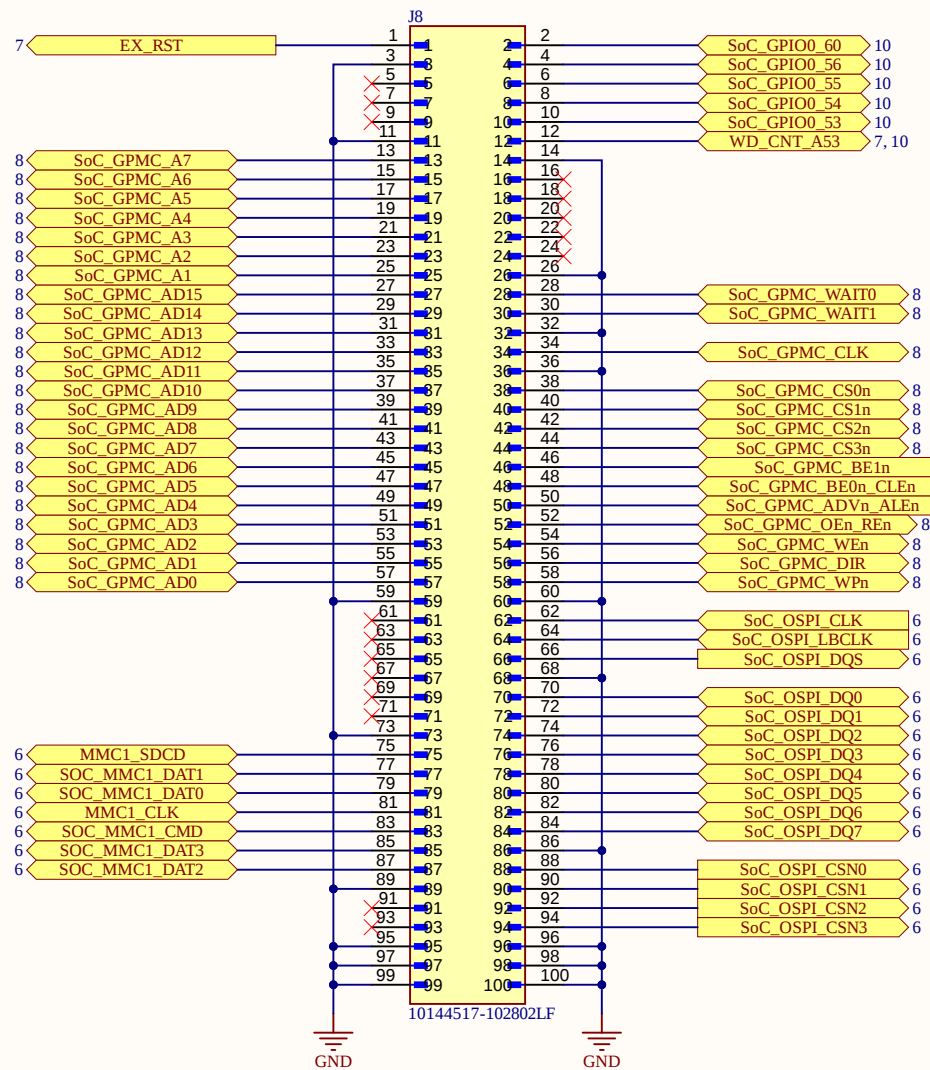
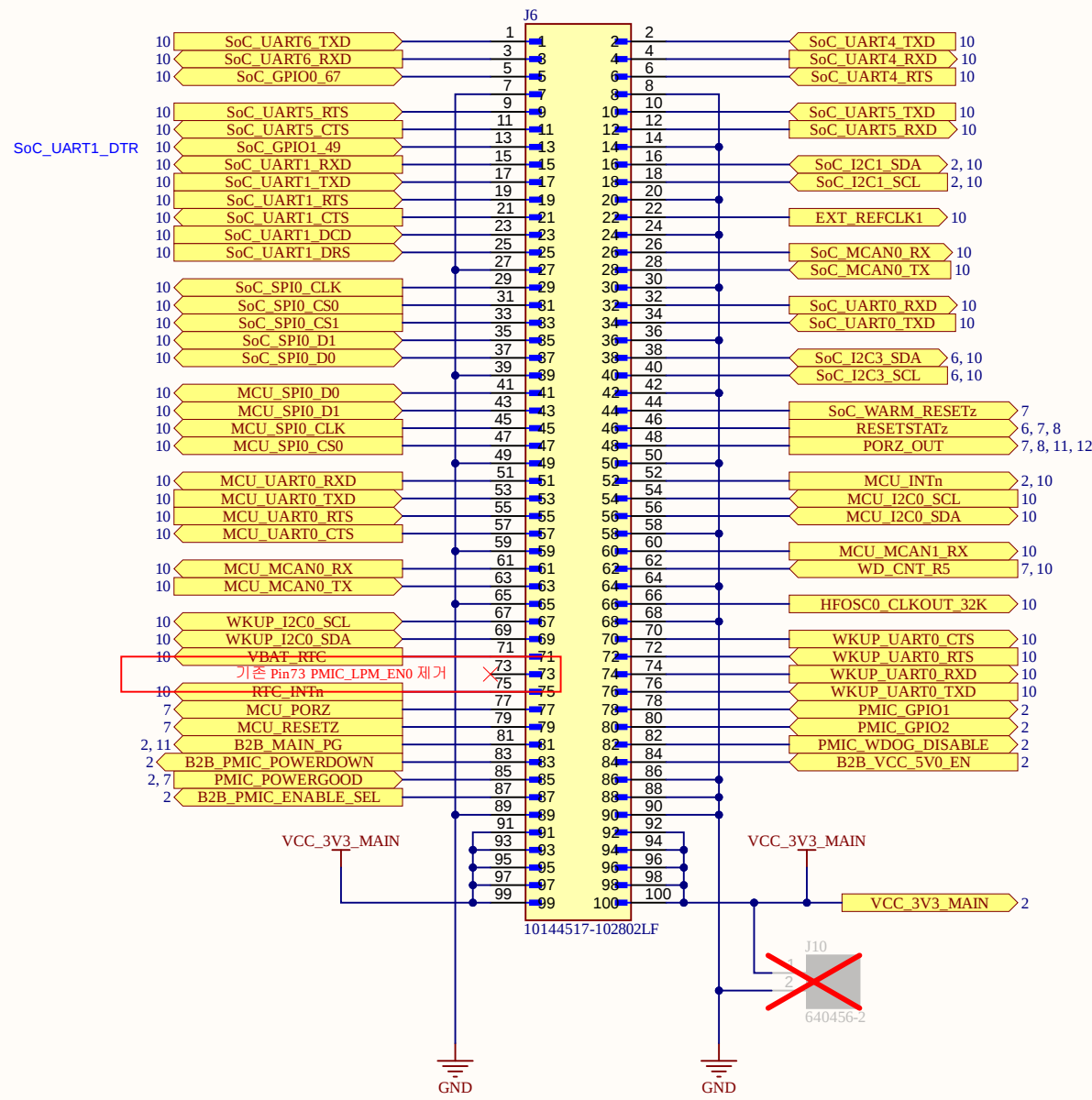


PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

Design Guideline: <https://www.ti.com/lit/an/snla387/snla387.pdf>

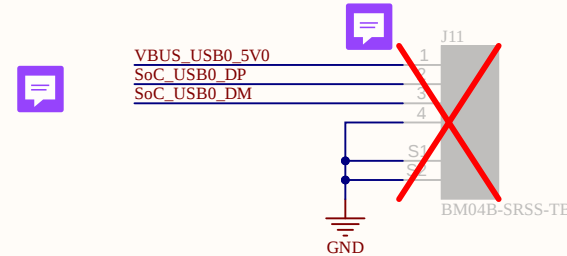
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Sheet Name :	CPSW RGMII 2 - PHY			Page : 12 of 13
Variant :	Prototype			Size : C
Status :	Preliminary			
NOTE :	*			

B2B Connector



USB Interface

INTERNAL USE ONLY
DO NOT POPULATE IN PRODUCTION



		Drafted	Checked	Approved
Project :	SoM-AM62A7x			Revision : R1.0
Sheet Name :	B2B Connector			Page : 13 OF 13
Variant :	Prototype			Size : C
Status :	Preliminary			
NOTE :	*			