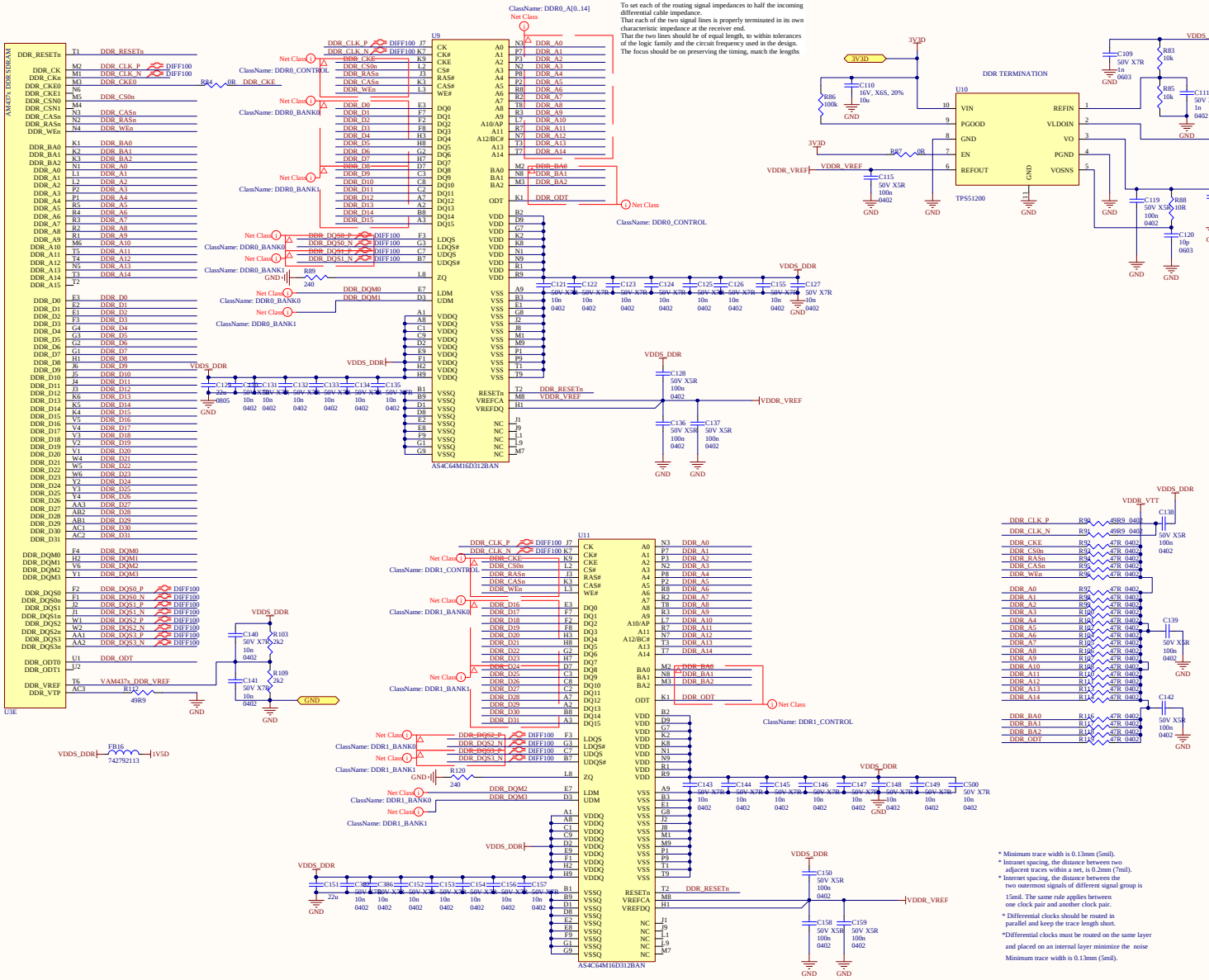
According to Lee Ritchey, a noted industry high-speed PCB design expert, successful differential signaling does not require working to a specific differential impedance. What it does require is:
To set each of the routing signal impedances to half the incoming differential cable impedance.
That each of the two signal lines is properly terminated in its own characteristic impedance at the receiver end.
That the two lines should be of equal length, to within tolerances of the logic family and the circuit frequency used in the design.
The focus should be on preserving the timing, match the lengths



* Minimum trace width is 0.13mm (5mil).
* Intranet spacing, the distance between two adjacent traces within a net, is 0.2mm (7mil).
* Internet spacing, the distance between the two outermost signals of different signal group is 15mil. The same rule applies between one clock pair and another clock pair.
* Differential clocks should be routed in parallel and keep the trace length short.
*Differential clocks must be routed on the same layer and placed on an internal layer minimize the noise Minimum trace width is 0.13mm (5mil).

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