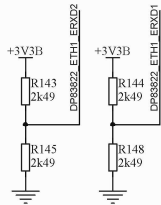


AM335x Ethernet Mac Features

- The general features of the ethernet switch subsystem are:
- Two 10/100/1000 Ethernet ports with GMII, RMII and RGMII interfaces
  - Wire rate switching (802.1d)
  - Non Blocking switch fabric
  - Flexible logical FIFO based packet buffer structure
  - Four priority level QoS support (802.1p)
  - CPPI 3.1 compliant DMA controllers
  - Support for IEEE 1588v2 Clock Synchronization (2008 Annex D and Annex F)
  - Timing FIFO and time stamping logic inside the SS
  - Device Level King (DLK) Support
  - Address Lookup Engine
    - 1024 addresses plus VLANs
    - Wire rate lookup
    - VLAN support
    - Host controlled time-based aging
    - Spanning tree support
    - L2 address lock and L2 filtering support
    - MAC authentication (802.1x)
  - Receive or destination based Multicast and Broadcast limits
    - MAC address blocking
    - Source port locking
    - OTU host accept/deny feature
  - Flow Control Support (802.3x)
  - EtherStats and 802.3stats RMON statistics gathering (shared)
  - Support for external packet dropping engine
  - CPGMAC\_SL transmit to CPGMAC\_SL receive Loopback mode (digital loopback) supported
  - CPGMAC\_SL receive to CPGMAC\_SL transmit Loopback mode (FIFO loopback) supported
  - Maximum frame size 2016 bytes (2020 with VLAN)
  - 4k (2048 x 32) internal CPPI buffer descriptor memory
  - MDIO module for PHY Management
  - Programmable interrupt control with selected interrupt pacing
  - Emulation Support
  - Programmable transmit Inter-Packet Gap (IPG)
  - Reset isolation

Phy Address Strap Option



Strap for MII phy address no other straps to minimize PCB, test can be programmed in SW. Adding both resistors only using mode 4(R143 and R144) gnd connection are DNP

Ethernet eth1

