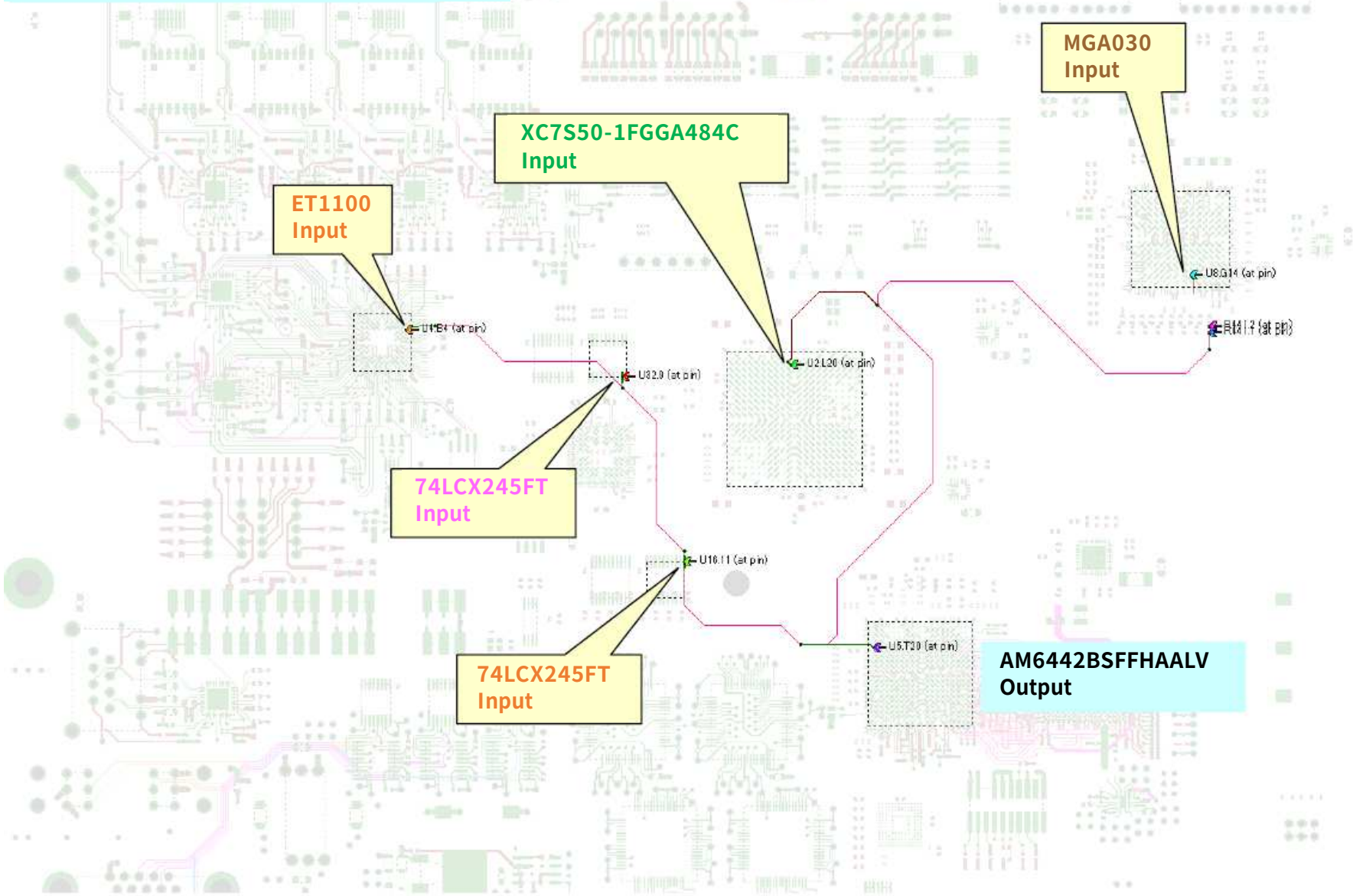
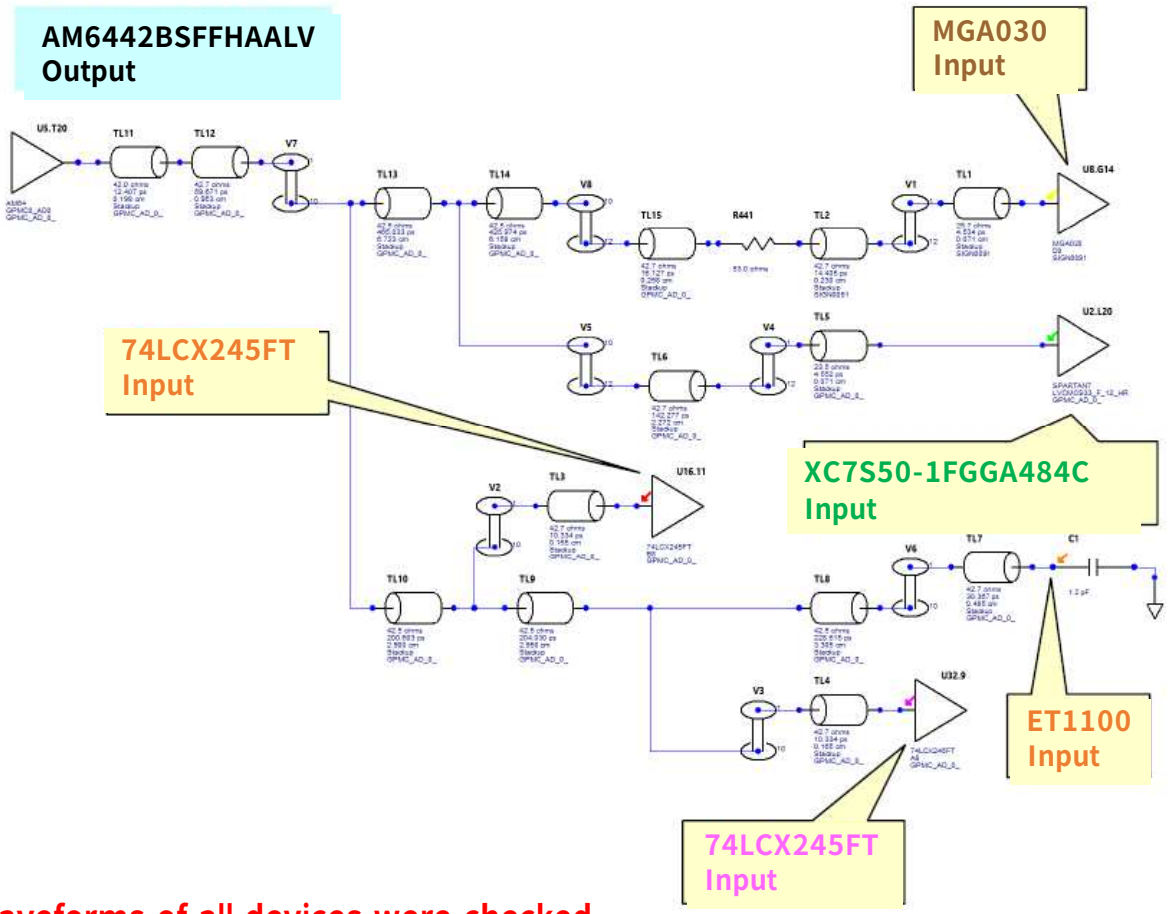
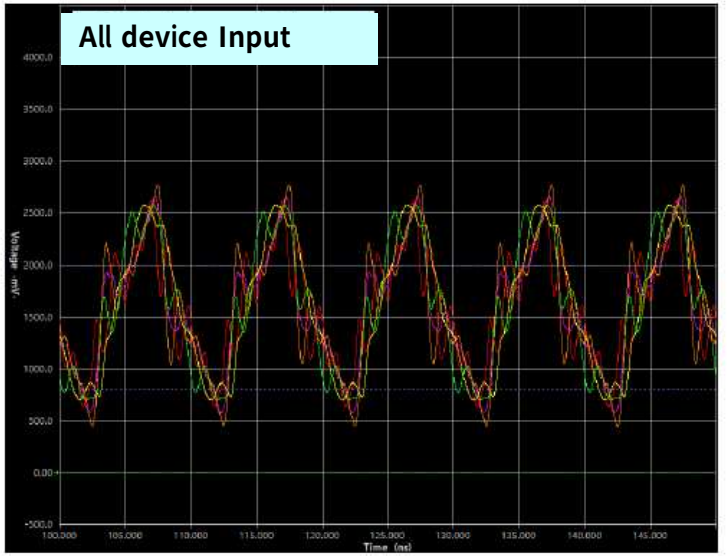
GPMA_AD[0] Tentative wiring diagram

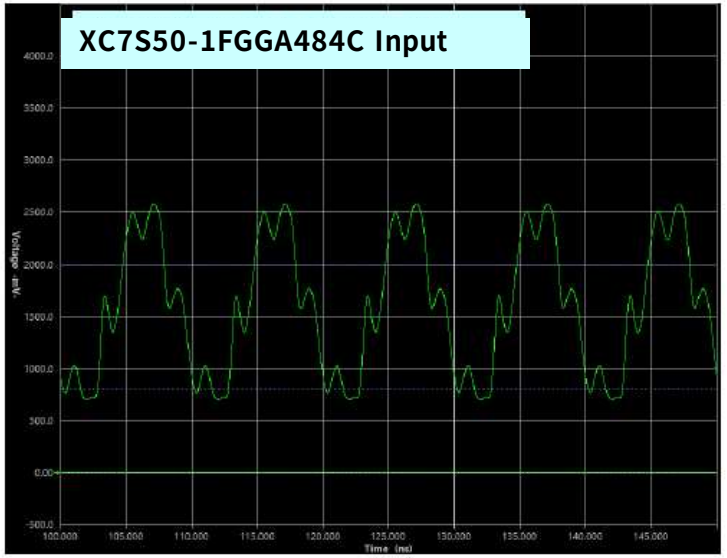


GPMA_AD[0] Topology



Analysis frequency 100MHz

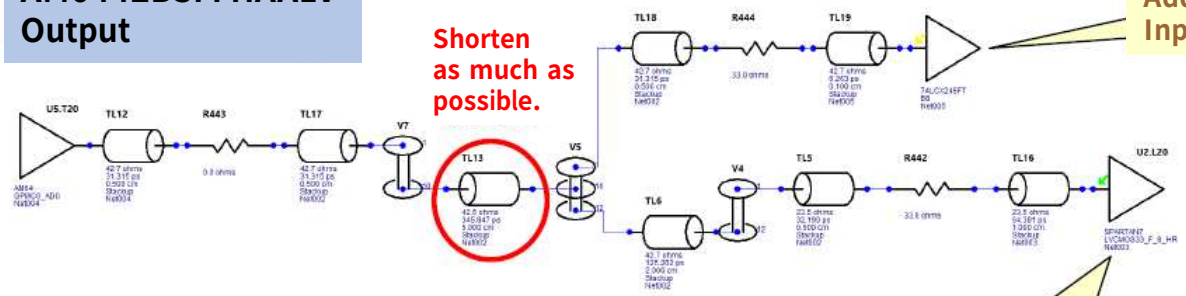




Waveforms of all devices were checked before adjustment, and they are in a very severe condition.

Since the CPU output is a little weak, it is considered to have a Buffer in parallel with the FPGA and to connect to other devices from the Buffer.

AM6442BSFFHAALV Output

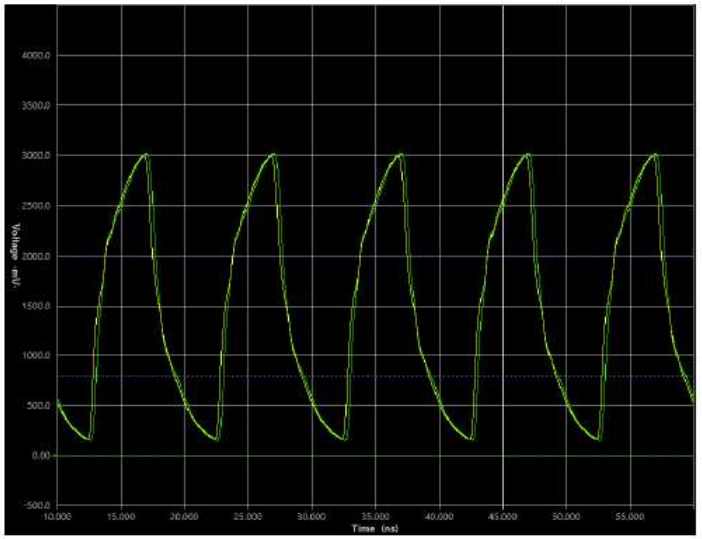


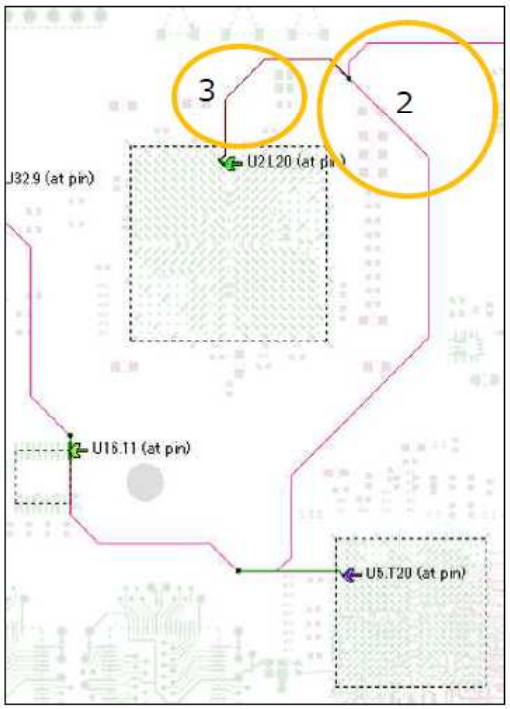
Shorten as much as possible.

Add : 74LCX245FT Input

XC7S50-1FGGA484C Input

Analysis frequency 100MHz





1

1. Move the CPU to the FPGA side as much as possible.
   The topology in the above figure is 90mm between CPU and FPGA, but the shorter the wiring length, the better the waveform quality.
2. Add Buffer + 33Ω in the red circled area.
3. Add 33Ω near the FPGA.