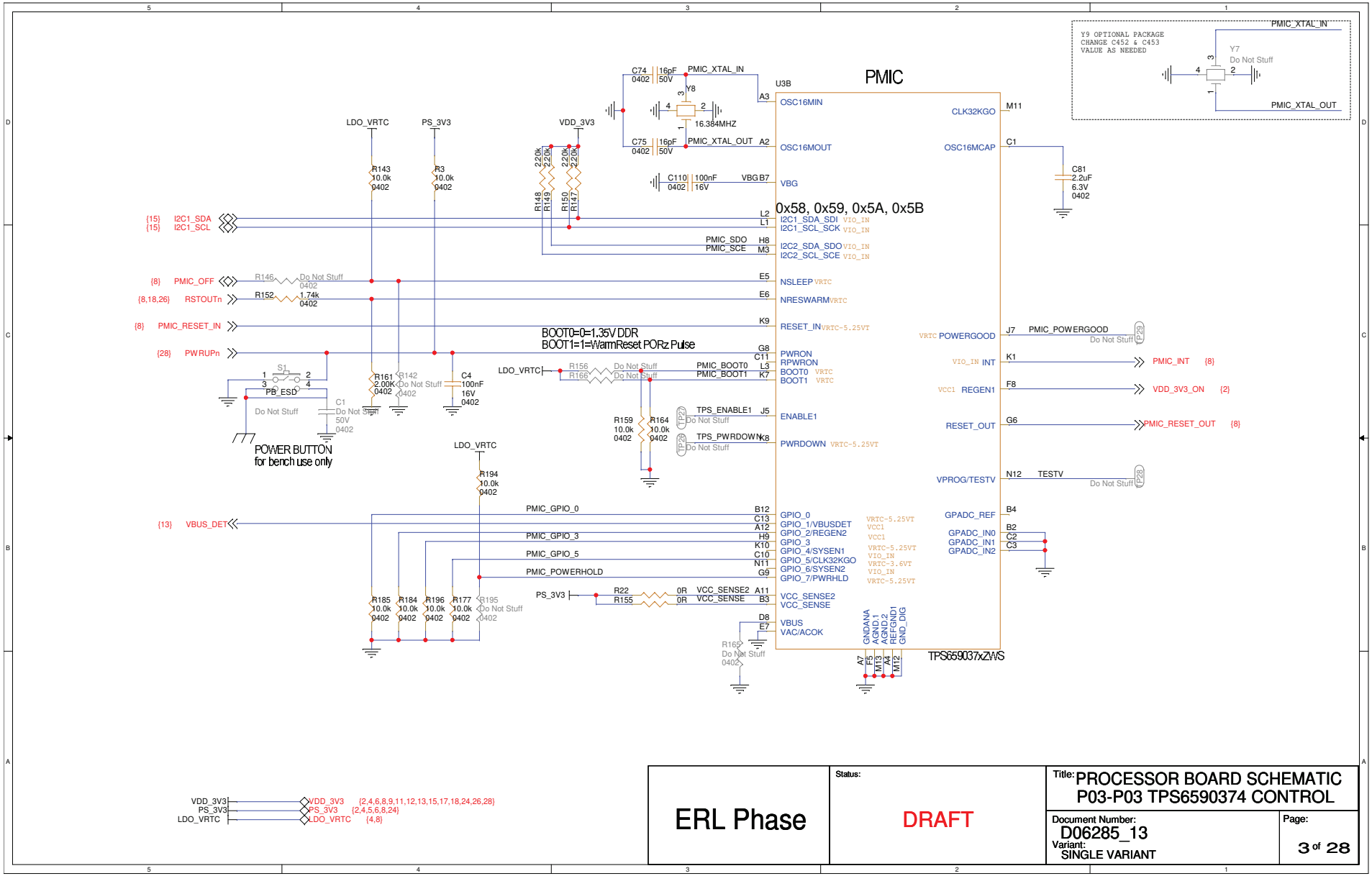
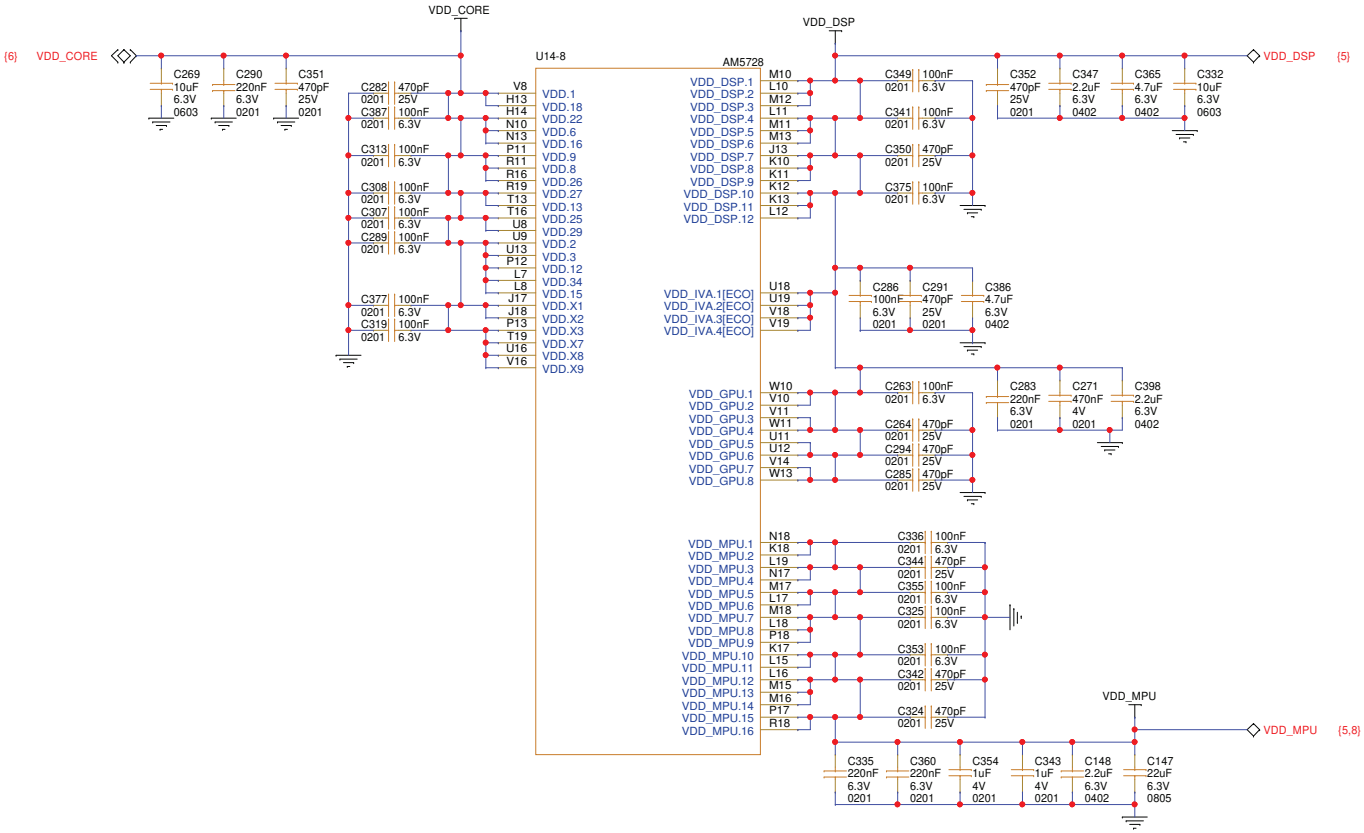
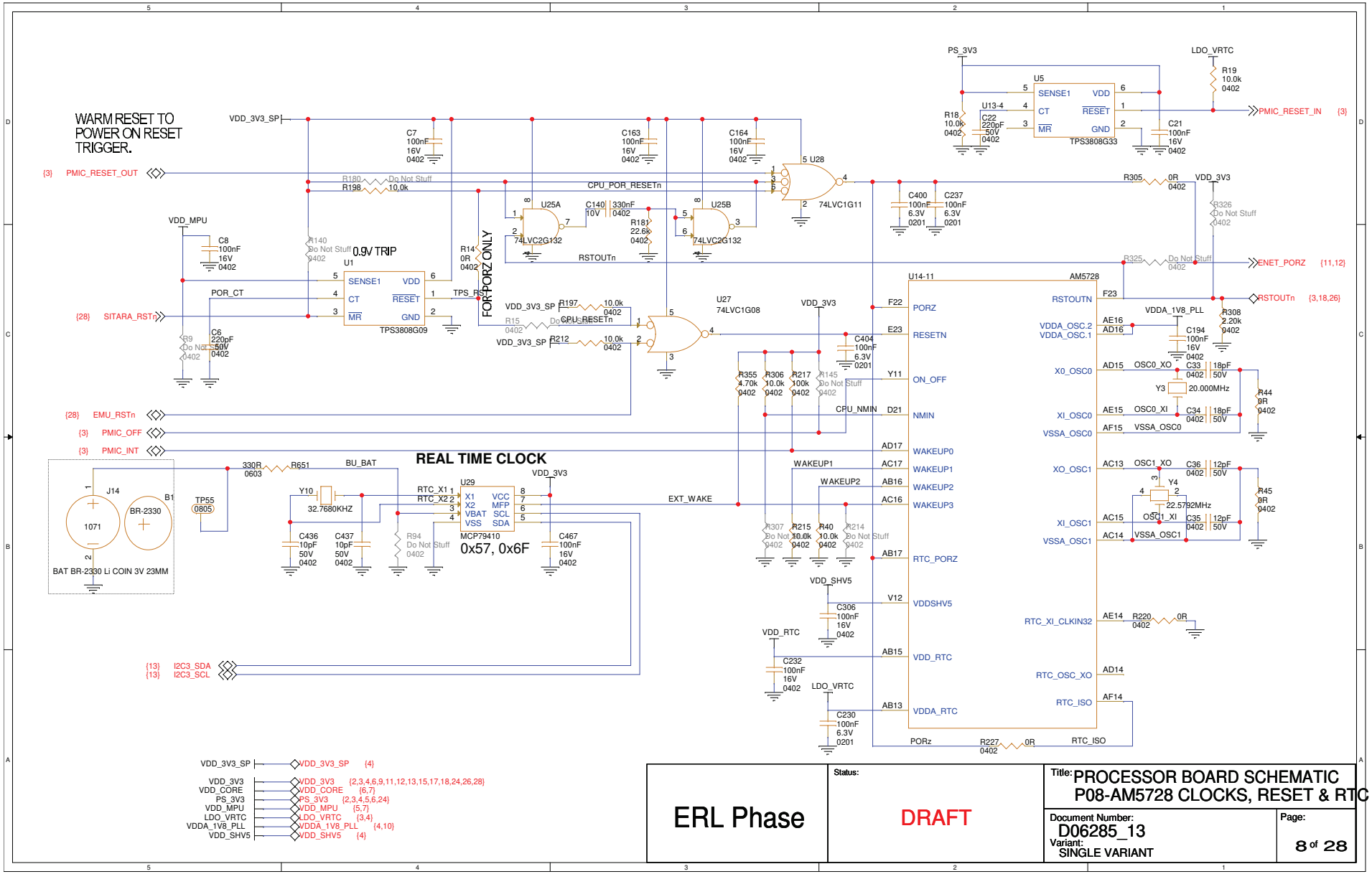


ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P03-P03 TPS6590374 CONTROL	
		Document Number: D06285_13 Variant: SINGLE VARIANT	Page: 3 of 28

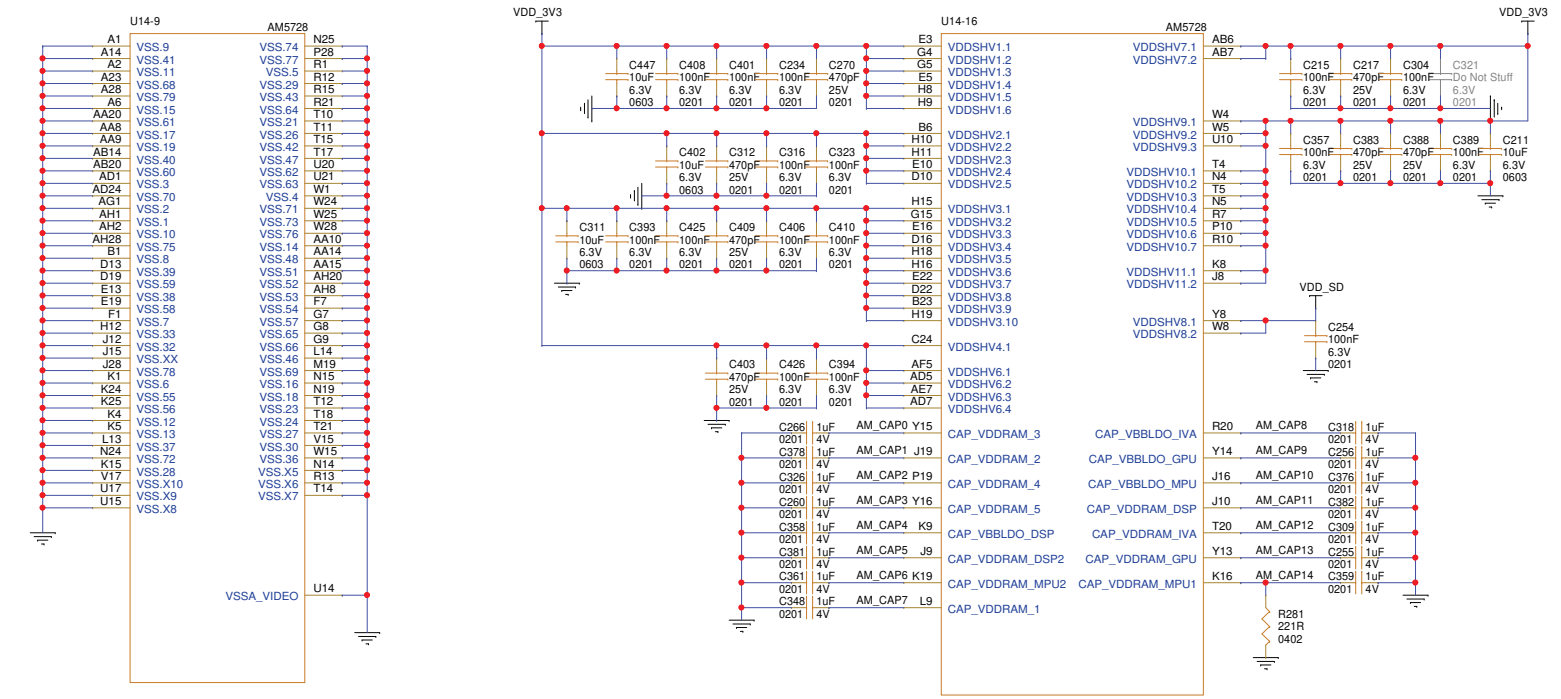


ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P07-AM5728 CORE POWER	
		Document Number: D06285_13 Variant: SINGLE VARIANT	Page: 7 of 28



ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P08-AM5728 CLOCKS, RESET & RTC
		Document Number: D06285_13 Variant: SINGLE VARIANT
		Page: 8 of 28

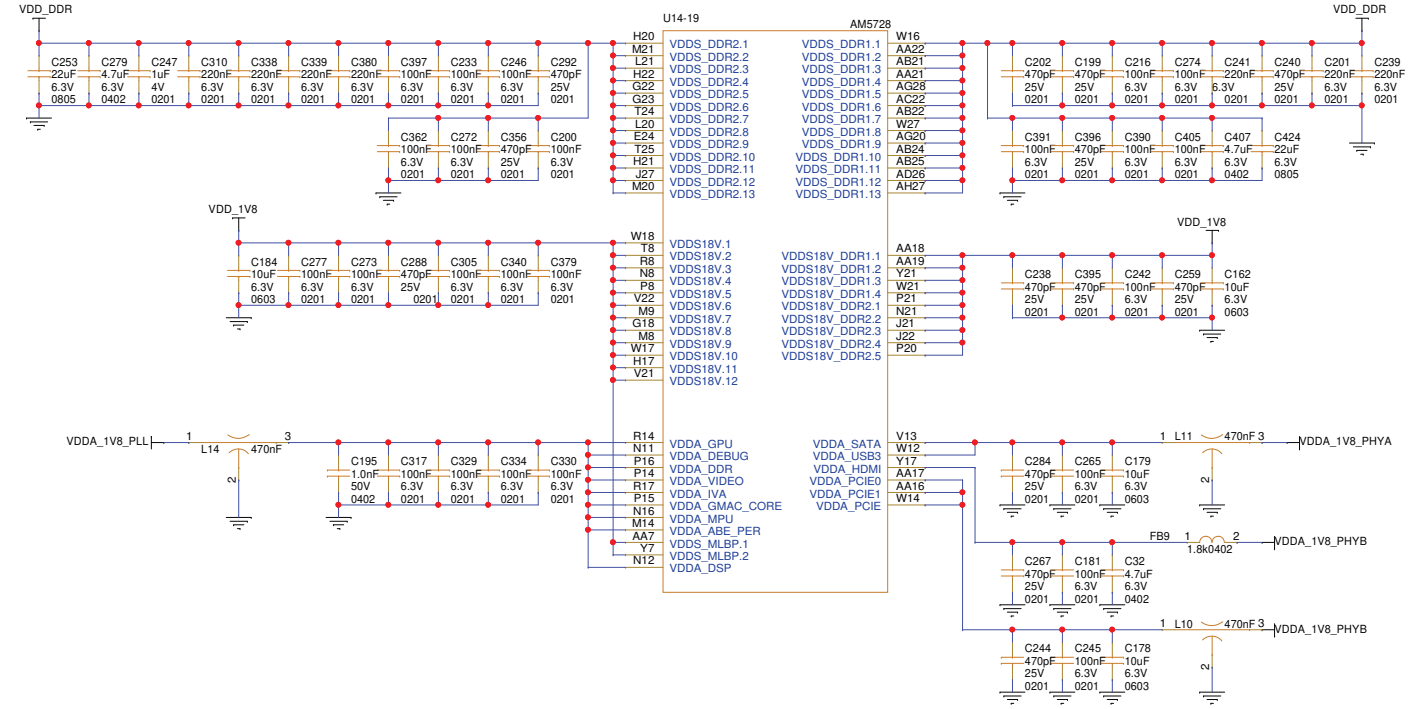
C321 DNP to avoid
mechanical interference



VDD_SD — VDD_SD {4,18}

VDD_3V3 — VDD_3V3 {2,3,4,6,8,11,12,13,15,17,18,24,26,28}

ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P09-AM5728 IO POWER AND GROUND	
		Document Number: D06285_13 Variant: SINGLE VARIANT	Page: 9 of 28



VDD_1V8 {4,6}
VDD_3V3 {2,3,4,6,8,9,11,12,13,15,17,18,24,26,28}
VDD_DDR {5,19,21,22,23,24}
VDDA_1V8_PLL {4,8}
VDDA_1V8_PHYA {4,14}
VDDA_1V8_PHYB {4}

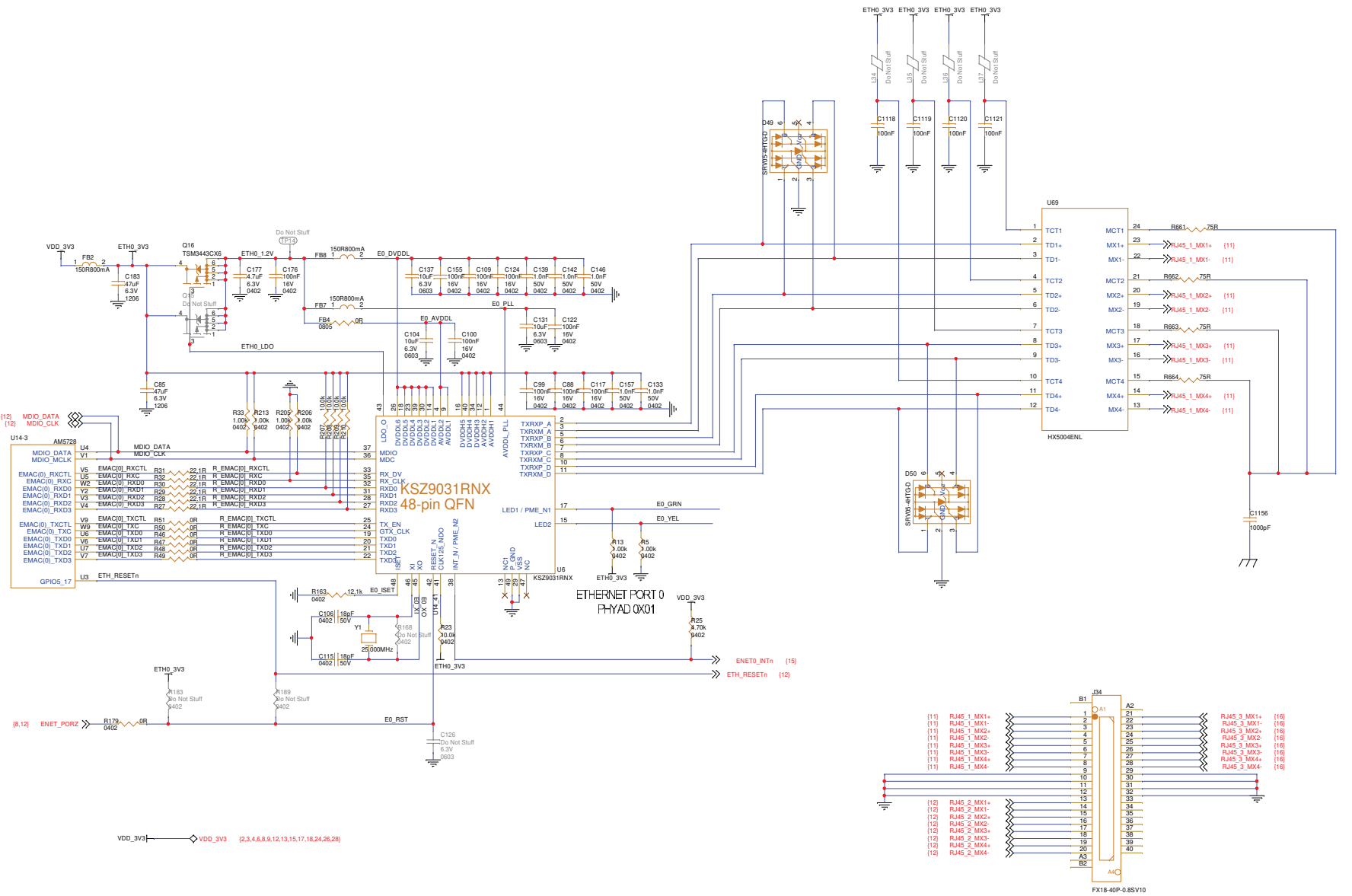
ERL Phase

Status: DRAFT

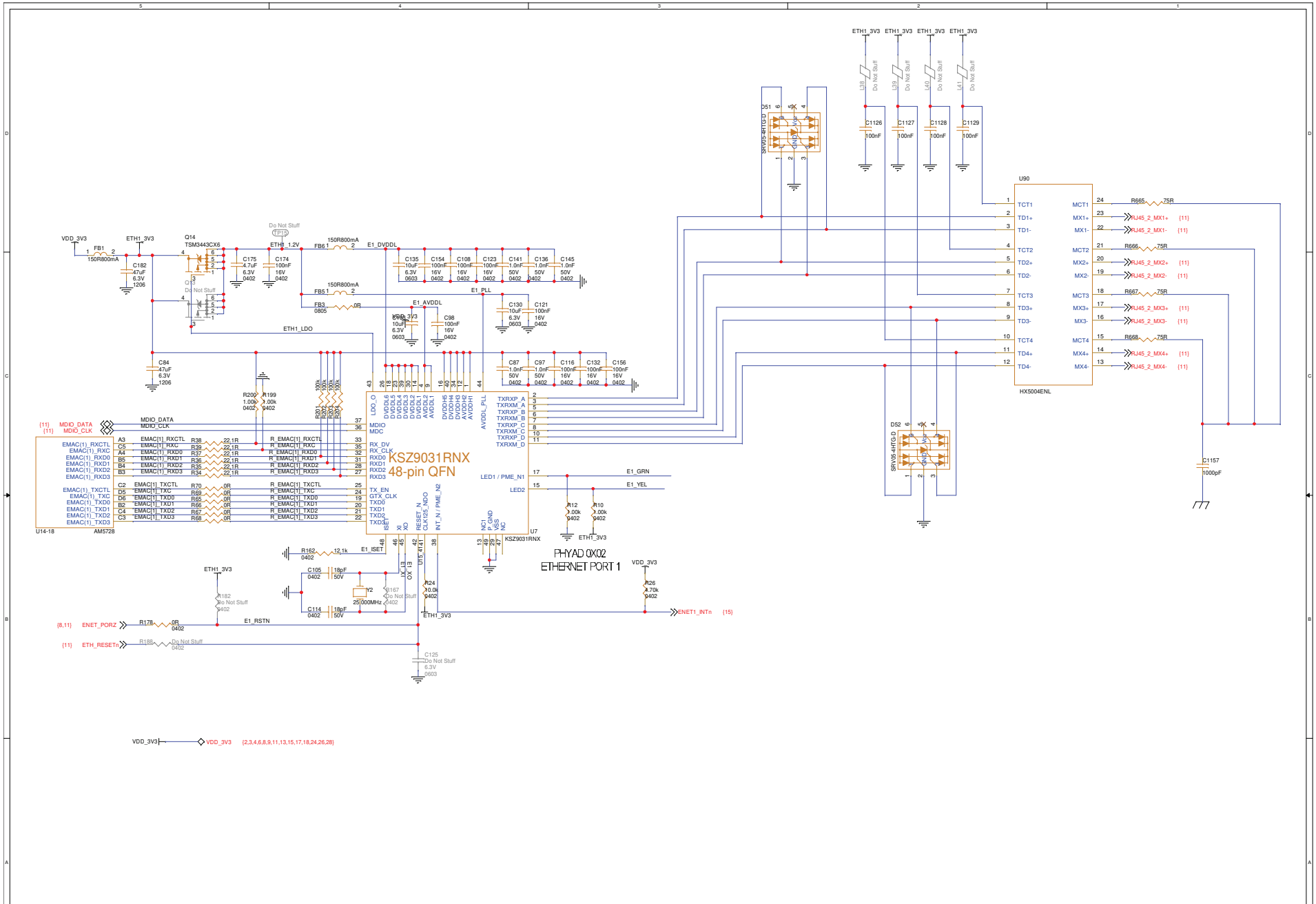
Title: PROCESSOR BOARD SCHEMATIC
P10-AM5728 DDR3 POWER

Document Number: D06285_13
Variant: SINGLE VARIANT

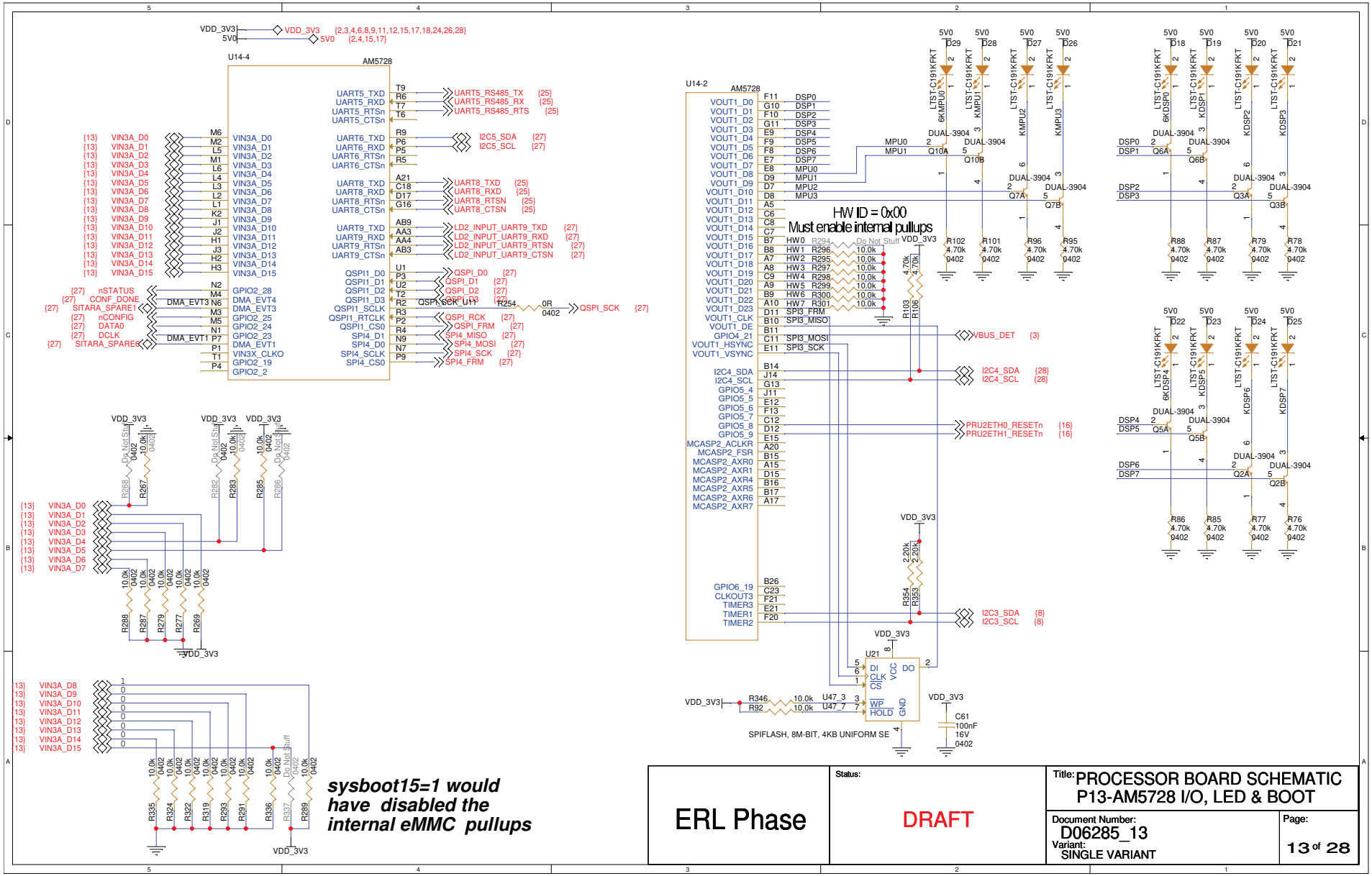
Page: 10 of 28

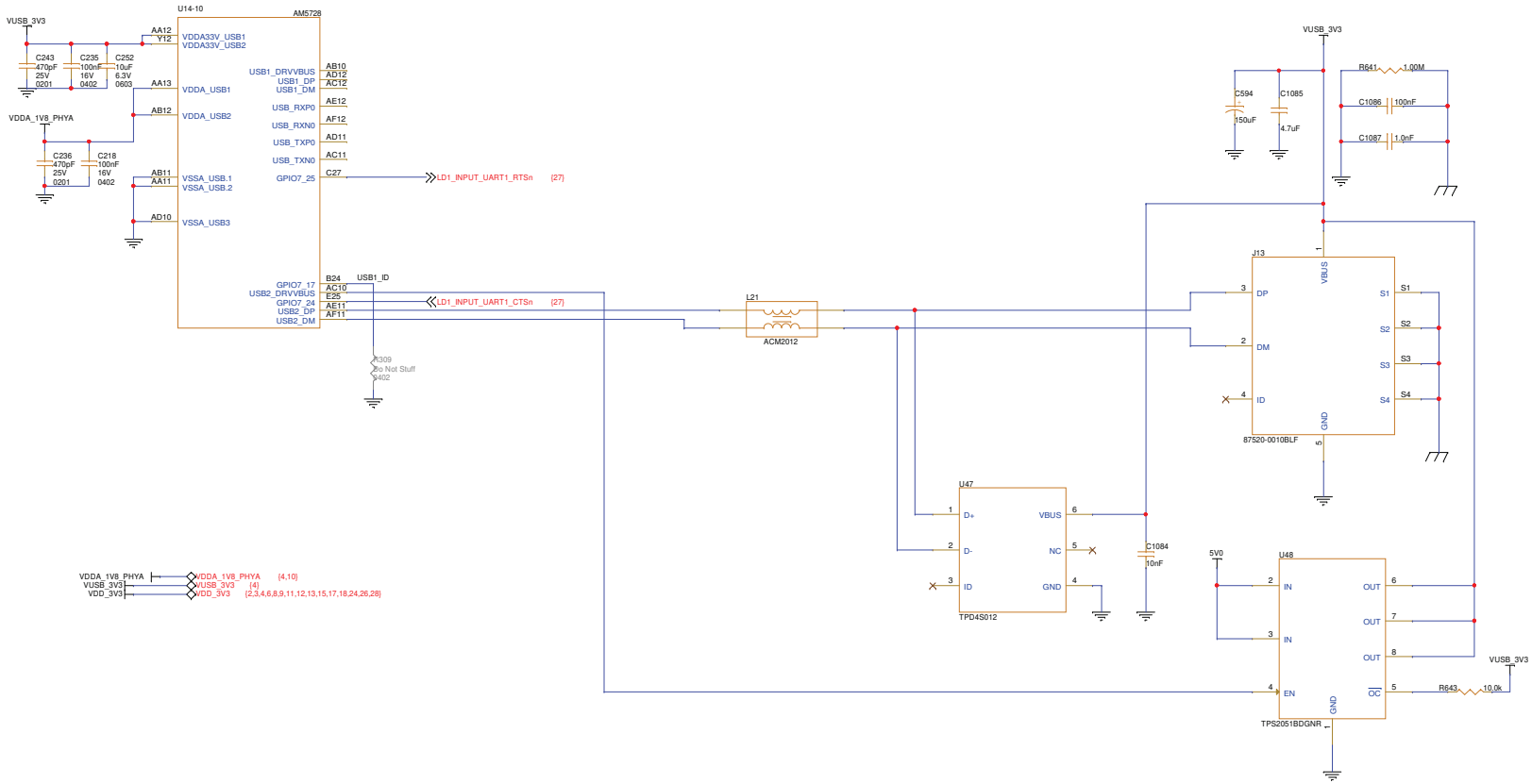


ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P11-AM5728 ETHERNET 1	
		Document Number: D06285_13 Variant: SINGLE VARIANT	Page: 11 of 28

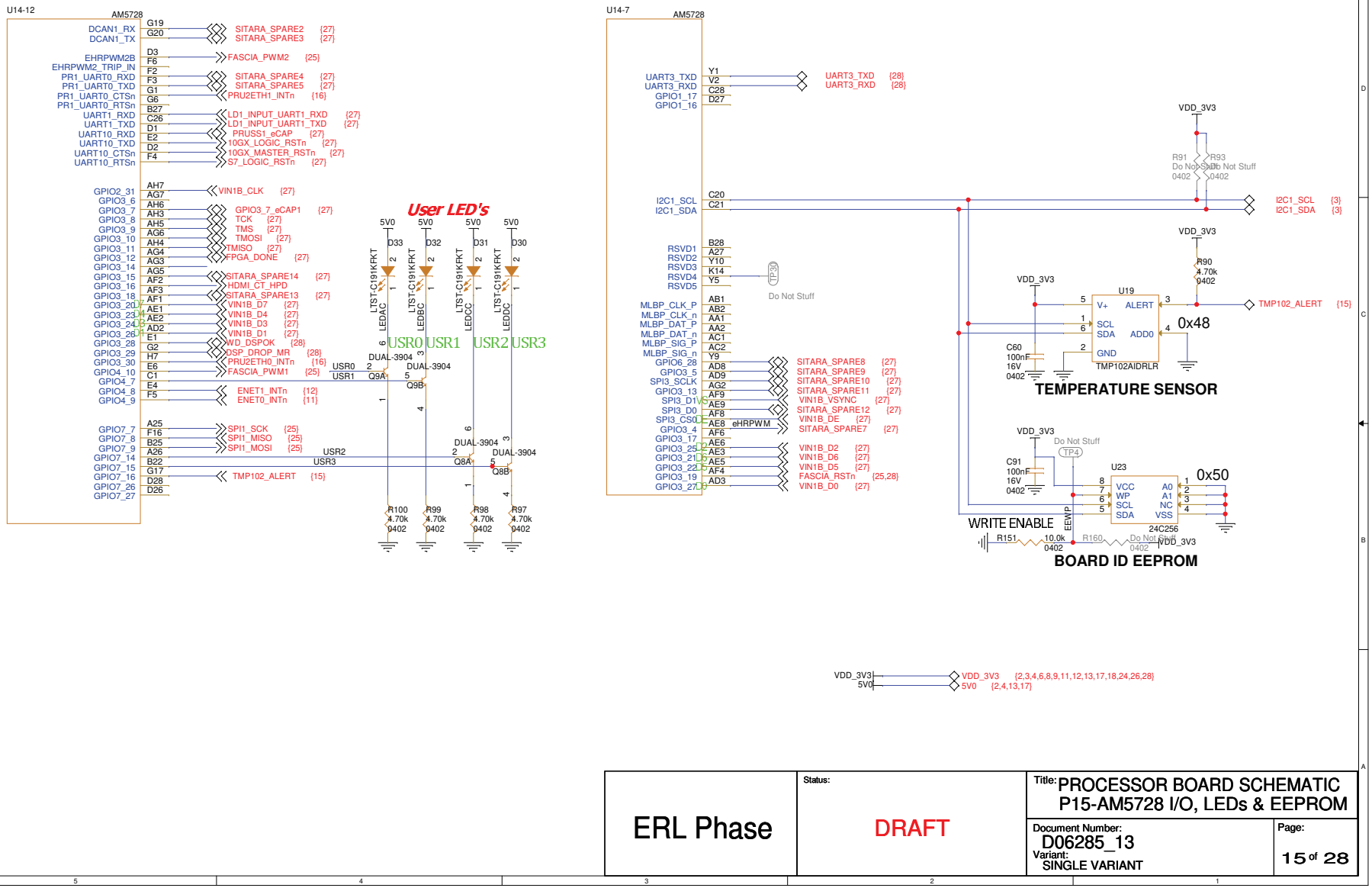


ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P12-AM5728 ETHERNET 2	
		Document Number: D06285_13 Variant: SINGLE VARIANT	Page: 12 of 28

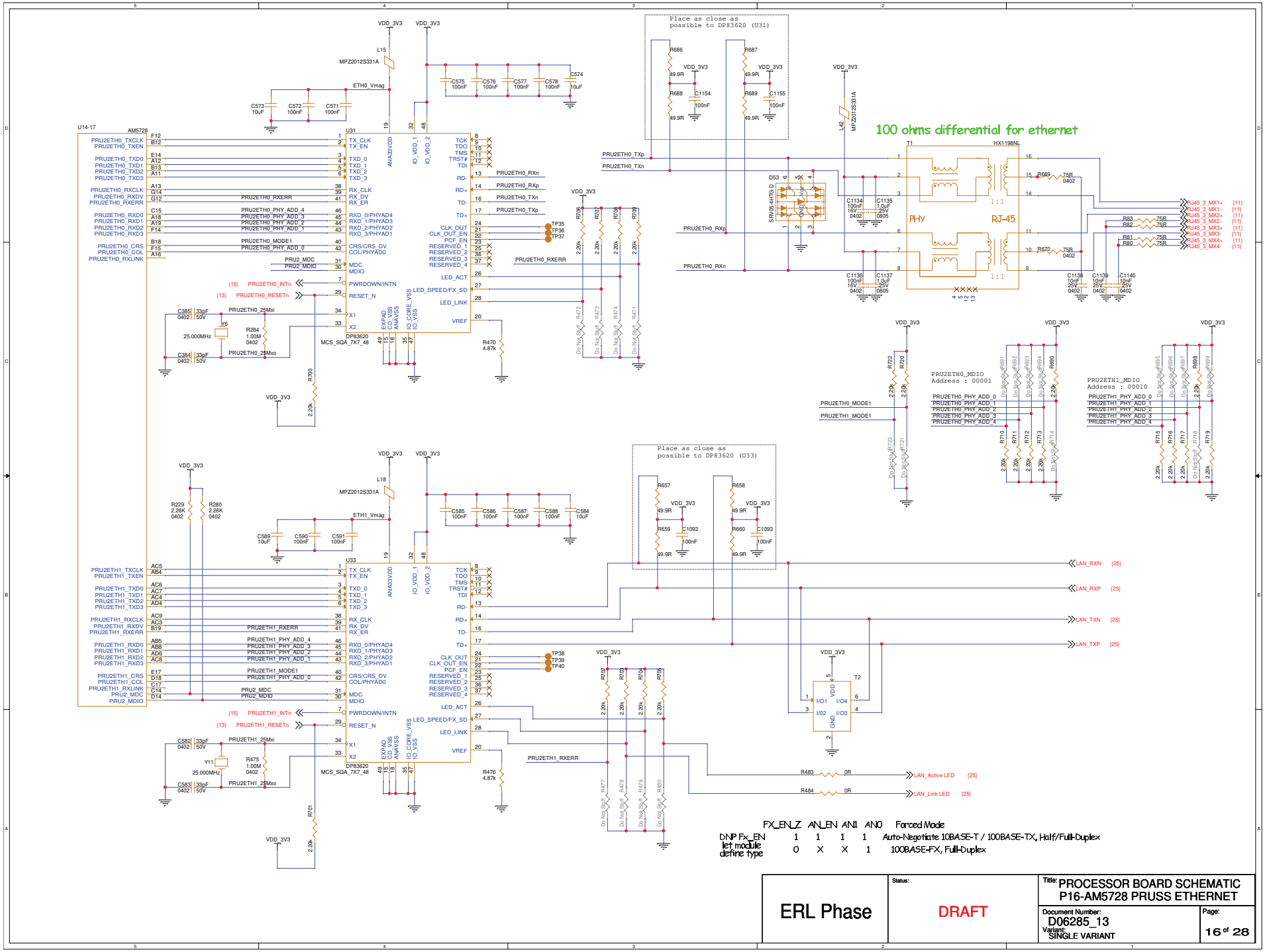

U14-4
AM5728
U14-2
HW ID = 0x00
Must enable internal pullups
sysboot15=1 would have disabled the internal eMMC pullups
SPIFLASH, 8M-BIT, 4KB UNIFORM SE
ERL Phase
Status:
DRAFT
Title: PROCESSOR BOARD SCHEMATIC
P13-AM5728 I/O, LED & BOOT
Document Number:
D06285_13
Variant:
SINGLE VARIANT
Page:
13 of 28

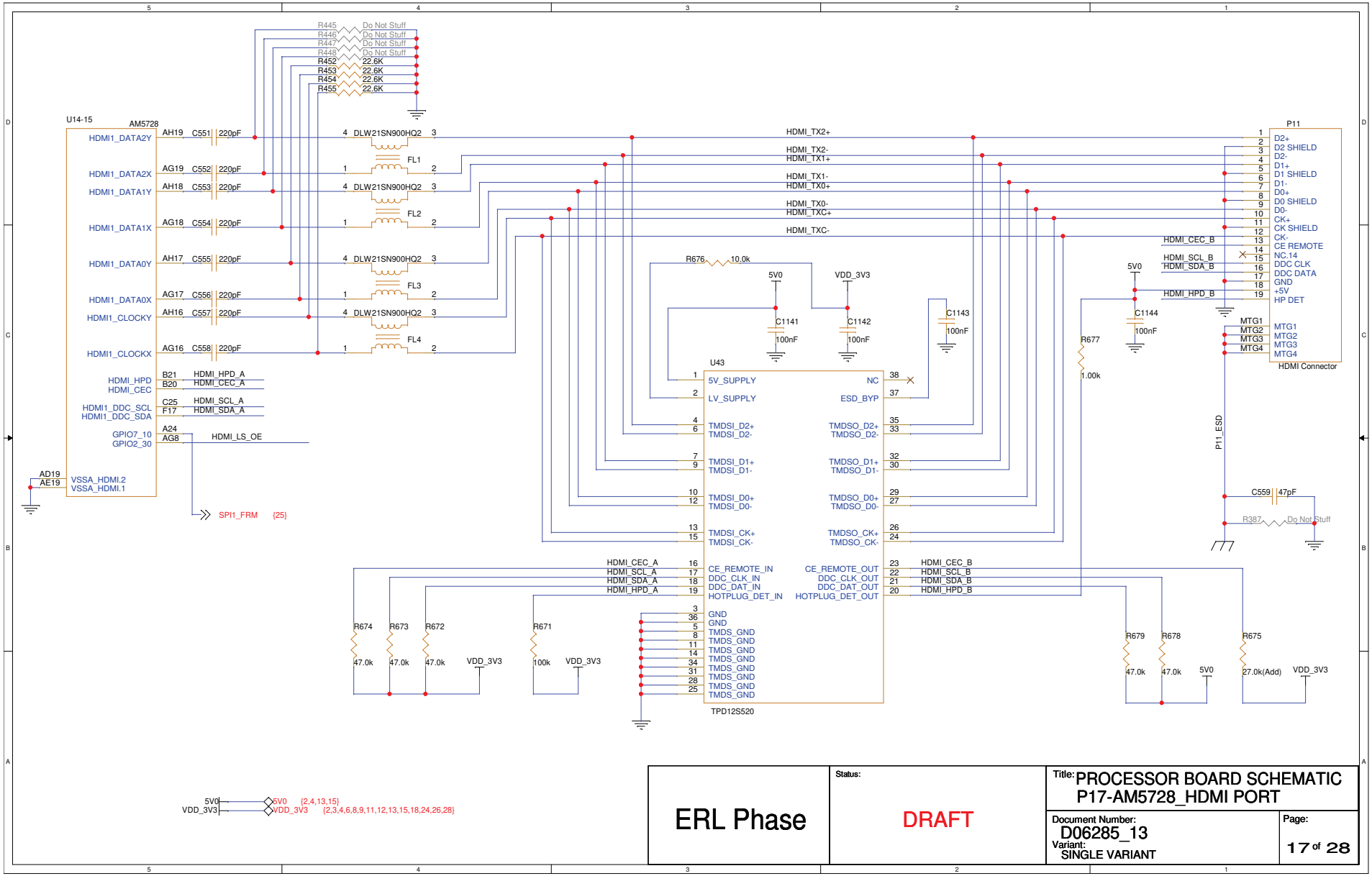


ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P14-AM5728 USB PORTS & HUB	
		Document Number: D06285_13 Variant: SINGLE VARIANT	Page: 14 of 28



ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P15-AM5728 I/O, LEDs & EEPROM	
		Document Number: D06285_13 Variant: SINGLE VARIANT	Page: 15 of 28


100 ohms differential for ethernet
Place as close as possible to DP83620 (U31)
Place as close as possible to DP83620 (U33)
PRU2ETH0_MDIO Address : 00001
PRU2ETH1_MDIO Address : 00010
FX_EN_Z AN_EN AN1 AN0 Forced Mode
DNP Fx_EN let module define type
1 1 1 1 Auto-Negotiate 10BASE-T / 100BASE-TX, Half/Full-Duplex
0 X X 1 100BASE-FX, Full-Duplex
ERL Phase
DRAFT
PROCESSOR BOARD SCHEMATIC
P16-AM5728 PRUSS ETHERNET
D06285_13
SINGLE VARIANT
16 of 28



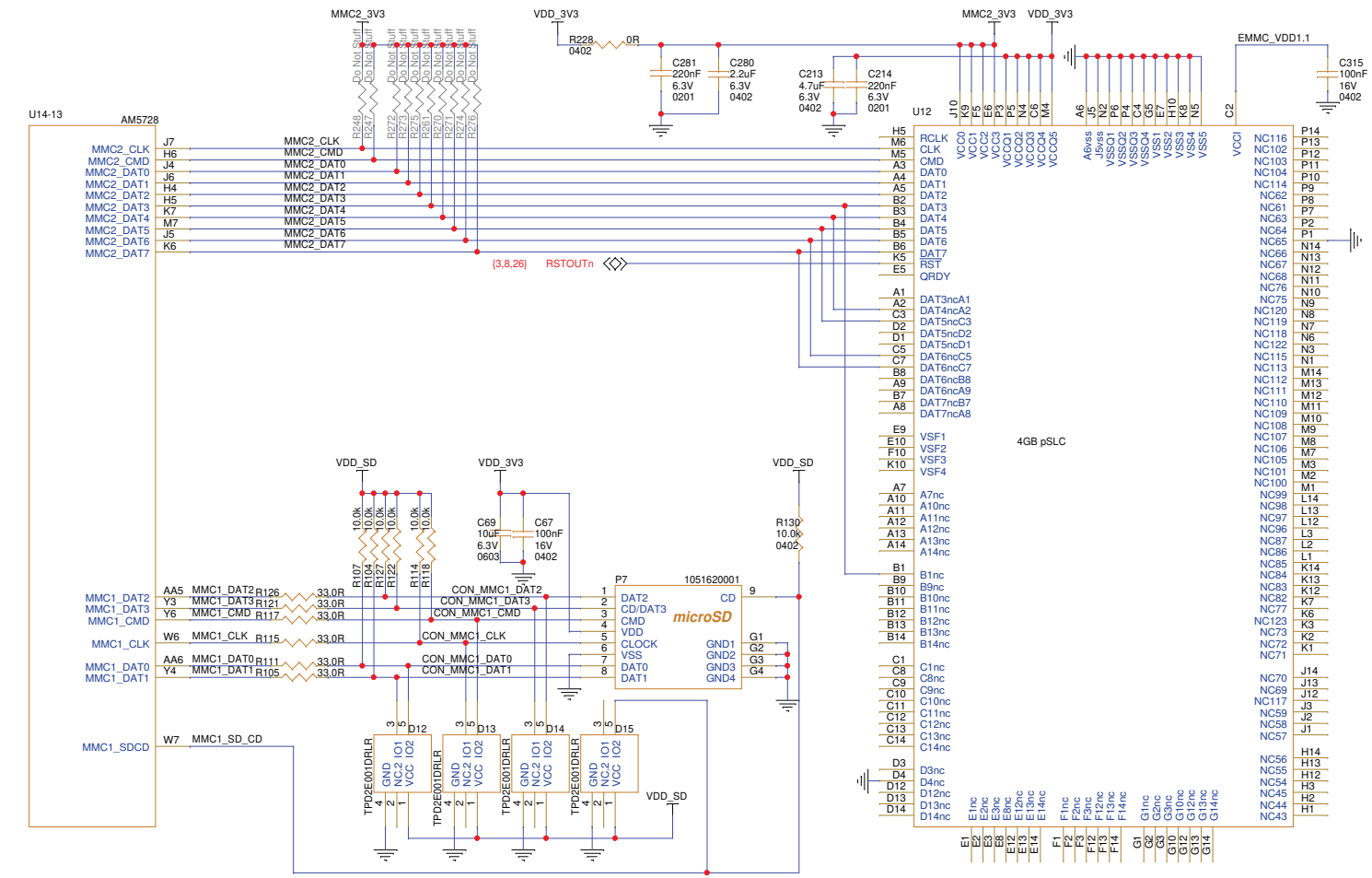
ERL Phase

Status: DRAFT

Title: PROCESSOR BOARD SCHEMATIC
P17-AM5728_HDMI PORT

Document Number: D06285_13
Variant: SINGLE VARIANT

Page: 17 of 28



ERL Phase

Status: DRAFT

Title: PROCESSOR BOARD SCHEMATIC
P18-AM5728 eMMC, MMC3 & uSD

Document Number: D06285_13
Variant: SINGLE VARIANT

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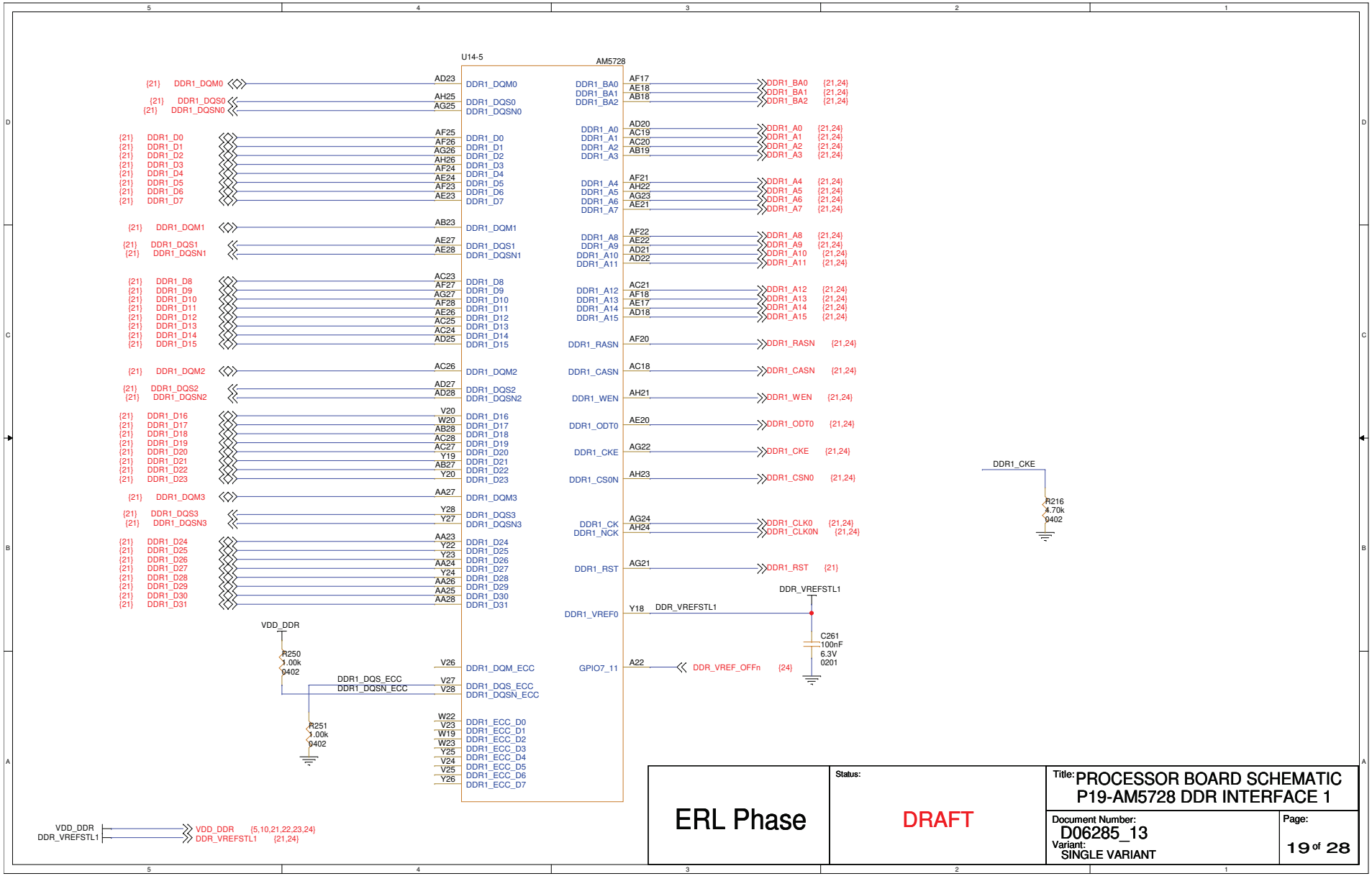
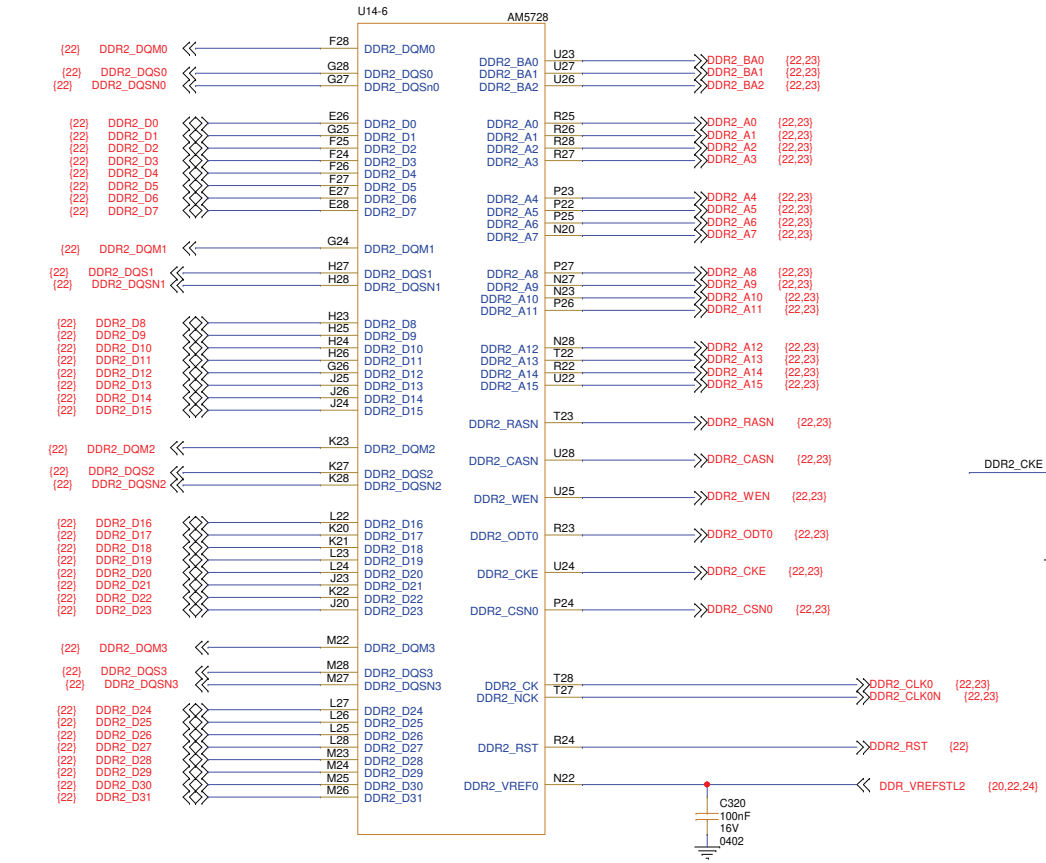
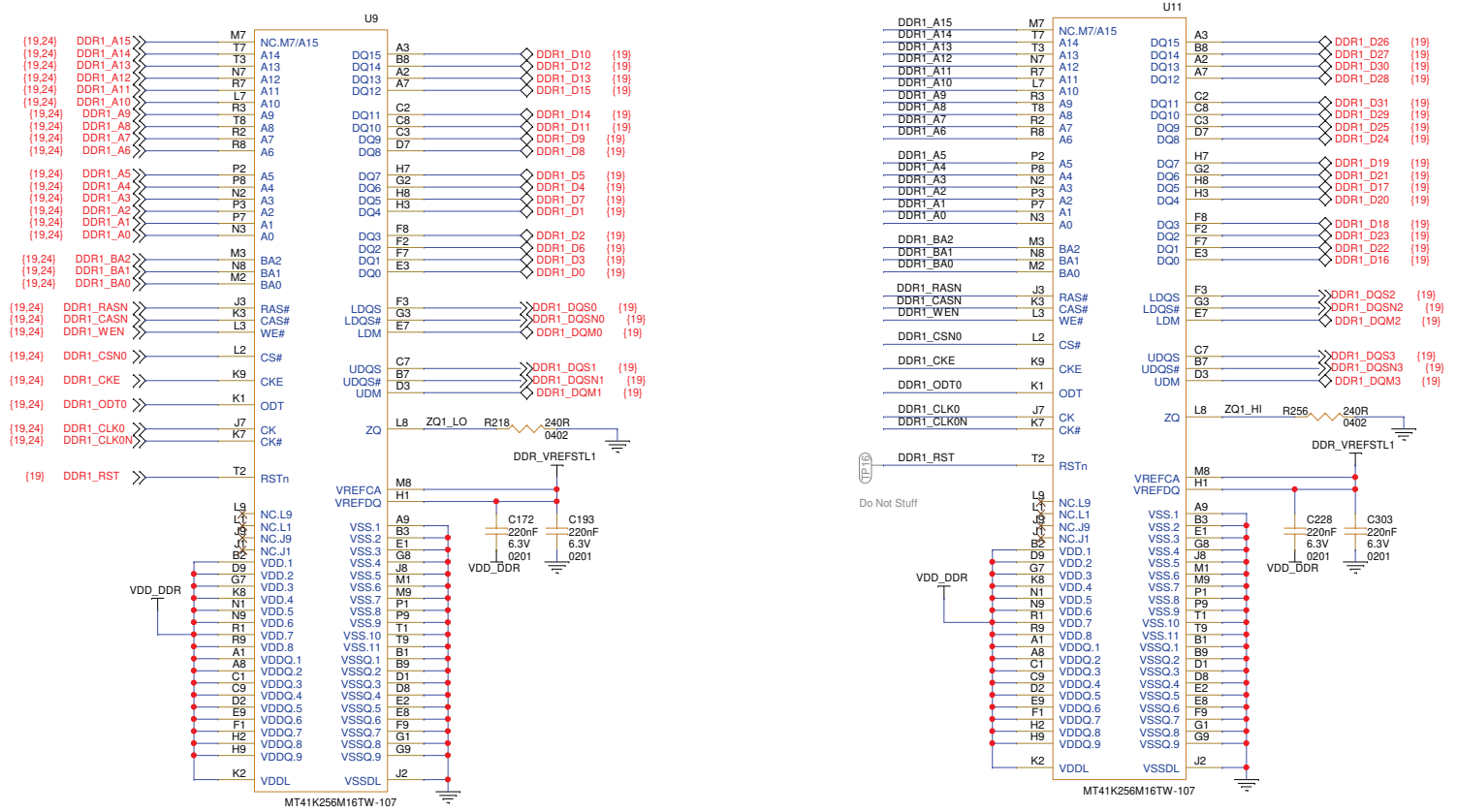

U14-5
AM5728
{21} DDR1_DQM0
{21} DDR1_DQS0
{21} DDR1_DQSN0
{21} DDR1_D0
{21} DDR1_D1
{21} DDR1_D2
{21} DDR1_D3
{21} DDR1_D4
{21} DDR1_D5
{21} DDR1_D6
{21} DDR1_D7
{21} DDR1_DQM1
{21} DDR1_DQS1
{21} DDR1_DQSN1
{21} DDR1_D8
{21} DDR1_D9
{21} DDR1_D10
{21} DDR1_D11
{21} DDR1_D12
{21} DDR1_D13
{21} DDR1_D14
{21} DDR1_D15
{21} DDR1_DQM2
{21} DDR1_DQS2
{21} DDR1_DQSN2
{21} DDR1_D16
{21} DDR1_D17
{21} DDR1_D18
{21} DDR1_D19
{21} DDR1_D20
{21} DDR1_D21
{21} DDR1_D22
{21} DDR1_D23
{21} DDR1_DQM3
{21} DDR1_DQS3
{21} DDR1_DQSN3
{21} DDR1_D24
{21} DDR1_D25
{21} DDR1_D26
{21} DDR1_D27
{21} DDR1_D28
{21} DDR1_D29
{21} DDR1_D30
{21} DDR1_D31
VDD_DDR
R250 1.00k 0402
R251 1.00k 0402
DDR1_DQS_ECC
DDR1_DQSN_ECC
DDR1_BA0
DDR1_BA1
DDR1_BA2
DDR1_A0
DDR1_A1
DDR1_A2
DDR1_A3
DDR1_A4
DDR1_A5
DDR1_A6
DDR1_A7
DDR1_A8
DDR1_A9
DDR1_A10
DDR1_A11
DDR1_A12
DDR1_A13
DDR1_A14
DDR1_A15
DDR1_RASN
DDR1_CASN
DDR1_WEN
DDR1_ODT0
DDR1_CKE
DDR1_CS0N
DDR1_CK
DDR1_NCK
DDR1_RST
DDR1_VREF0
GPIO7_11
DDR_VREF_OFFn {24}
DDR_VREFSTL1
C261 100nF 6.3V 0201
DDR1_CKE
R216 4.70k 0402
VDD_DDR {5,10,21,22,23,24}
DDR_VREFSTL1 {21,24}
ERL Phase
Status:
DRAFT
Title: PROCESSOR BOARD SCHEMATIC
P19-AM5728 DDR INTERFACE 1
Document Number: D06285_13
Variant: SINGLE VARIANT
Page: 19 of 28



ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P20-AM5728 DDR INTERFACE 2
		Document Number: D06285_13 Variant: SINGLE VARIANT
		Page: 20 of 28



VTT {23,24}
DDR_VREFSTL1 {19,24}
VDD_DDR {5,10,19,22,23,24}

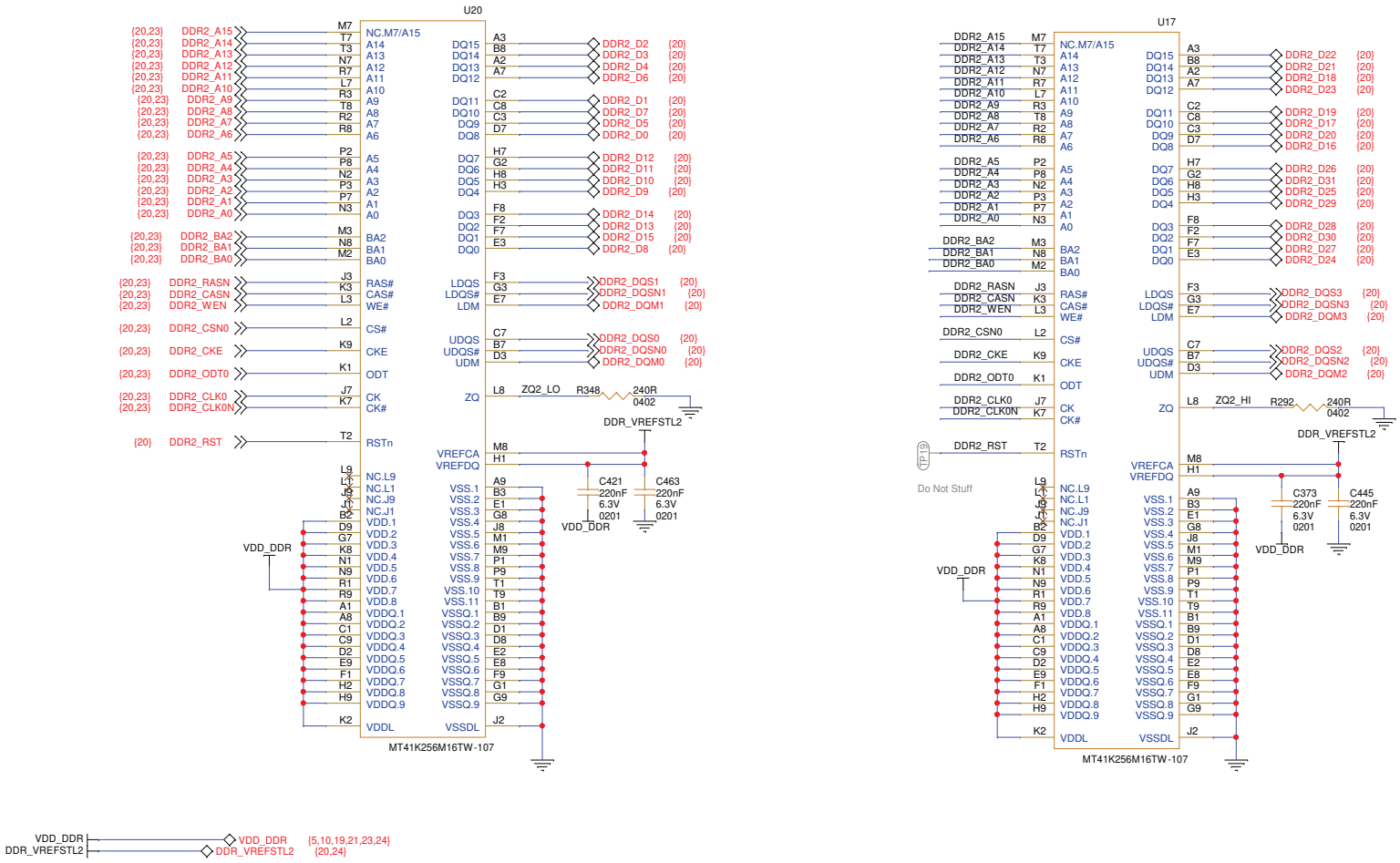
ERL Phase

Status: DRAFT

Title: PROCESSOR BOARD SCHEMATIC
P21-DDR3 BANK 1

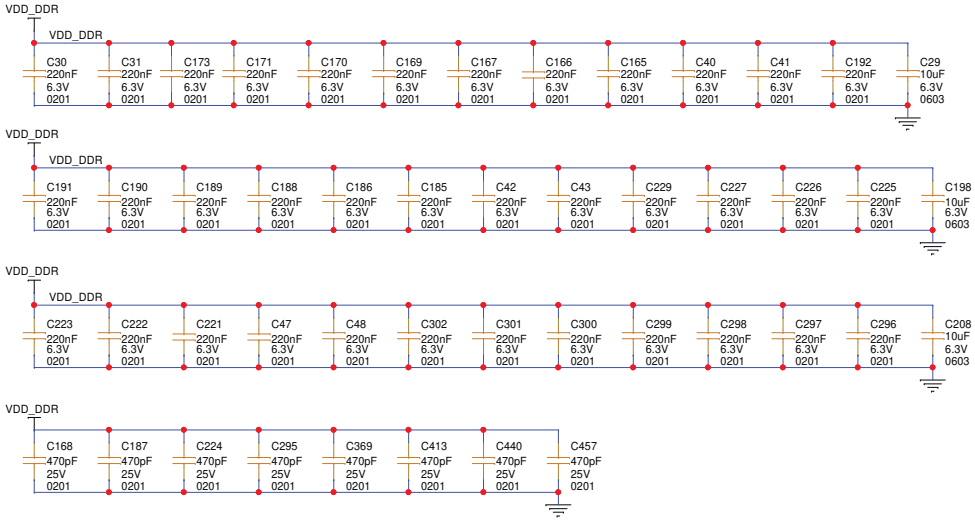
Document Number: D06285_13
Variant: SINGLE VARIANT

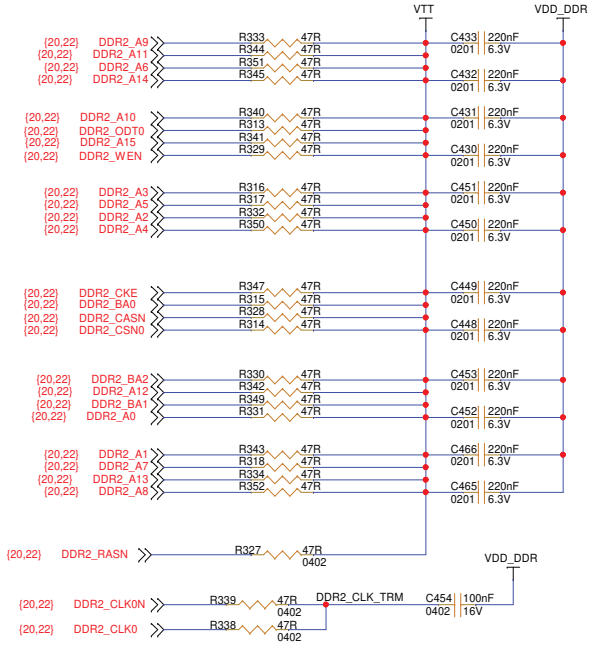
Page: 21 of 28



VDD_DDR — VDD_DDR {5,10,19,21,23,24}
DDR_VREFSTL2 — DDR_VREFSTL2 {20,24}

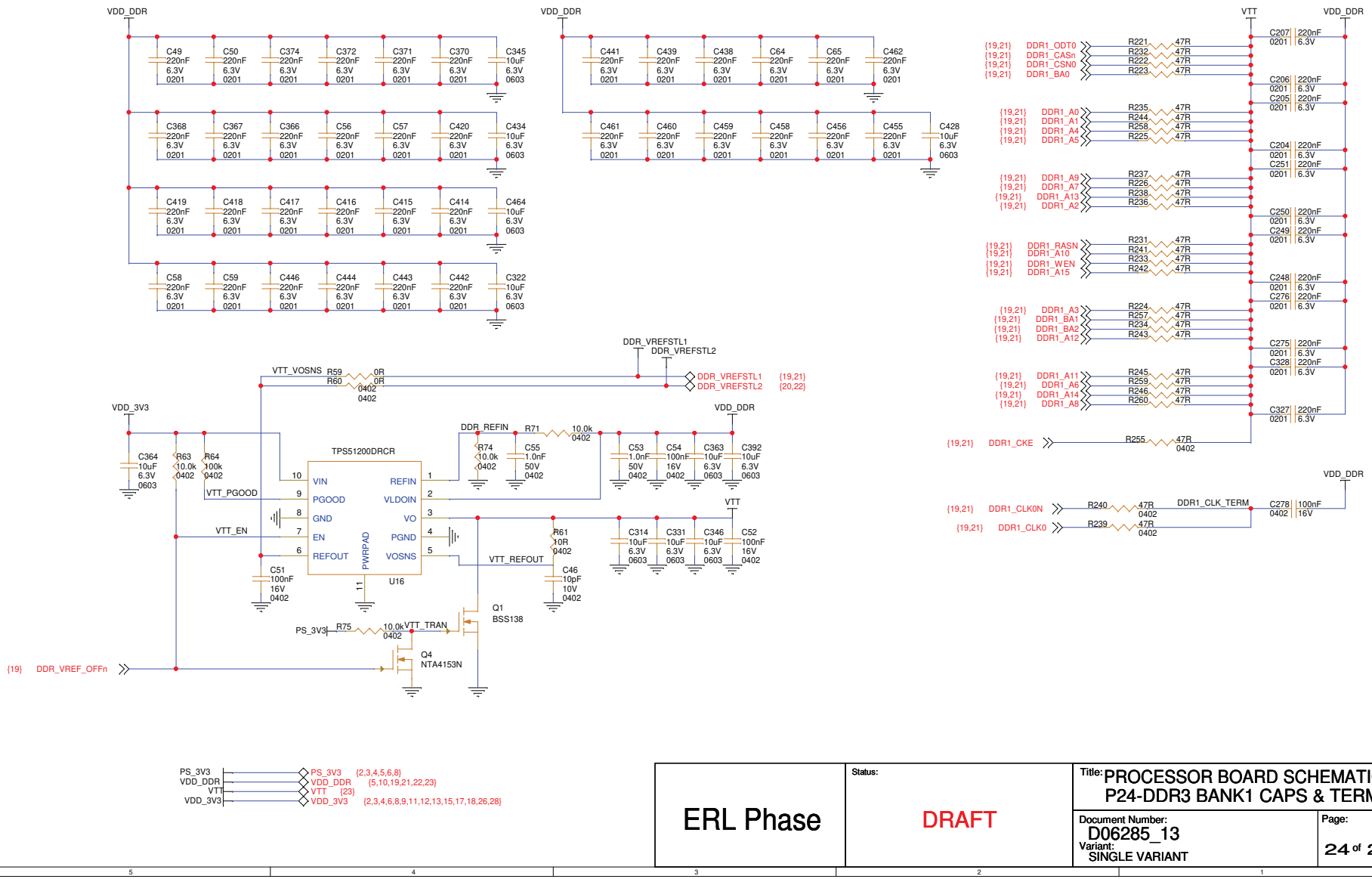
ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P22-DDR3 BANK 2	
		Document Number: D06285_13 Variant: SINGLE VARIANT	Page: 22 of 28







ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P23-DDR3 BANK 2 CAPS & TERM
		Document Number: D06285_13 Variant: SINGLE VARIANT
		Page: 23 of 28



ERL Phase

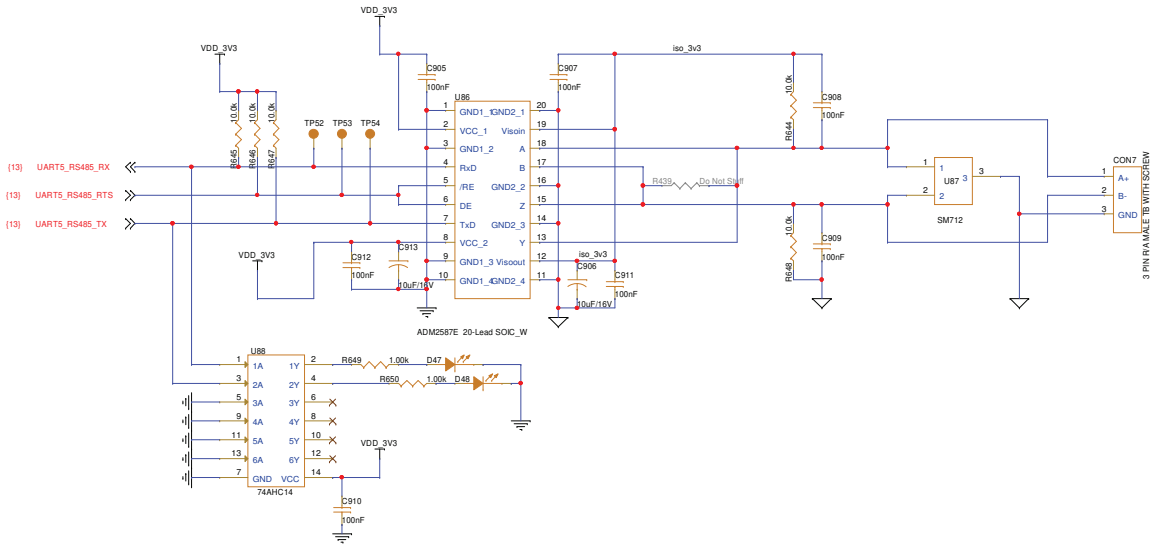
Status: DRAFT

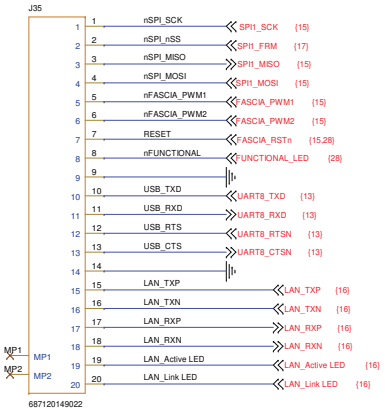
Title: PROCESSOR BOARD SCHEMATIC
P24-DDR3 BANK1 CAPS & TERM

Document Number: D06285_13

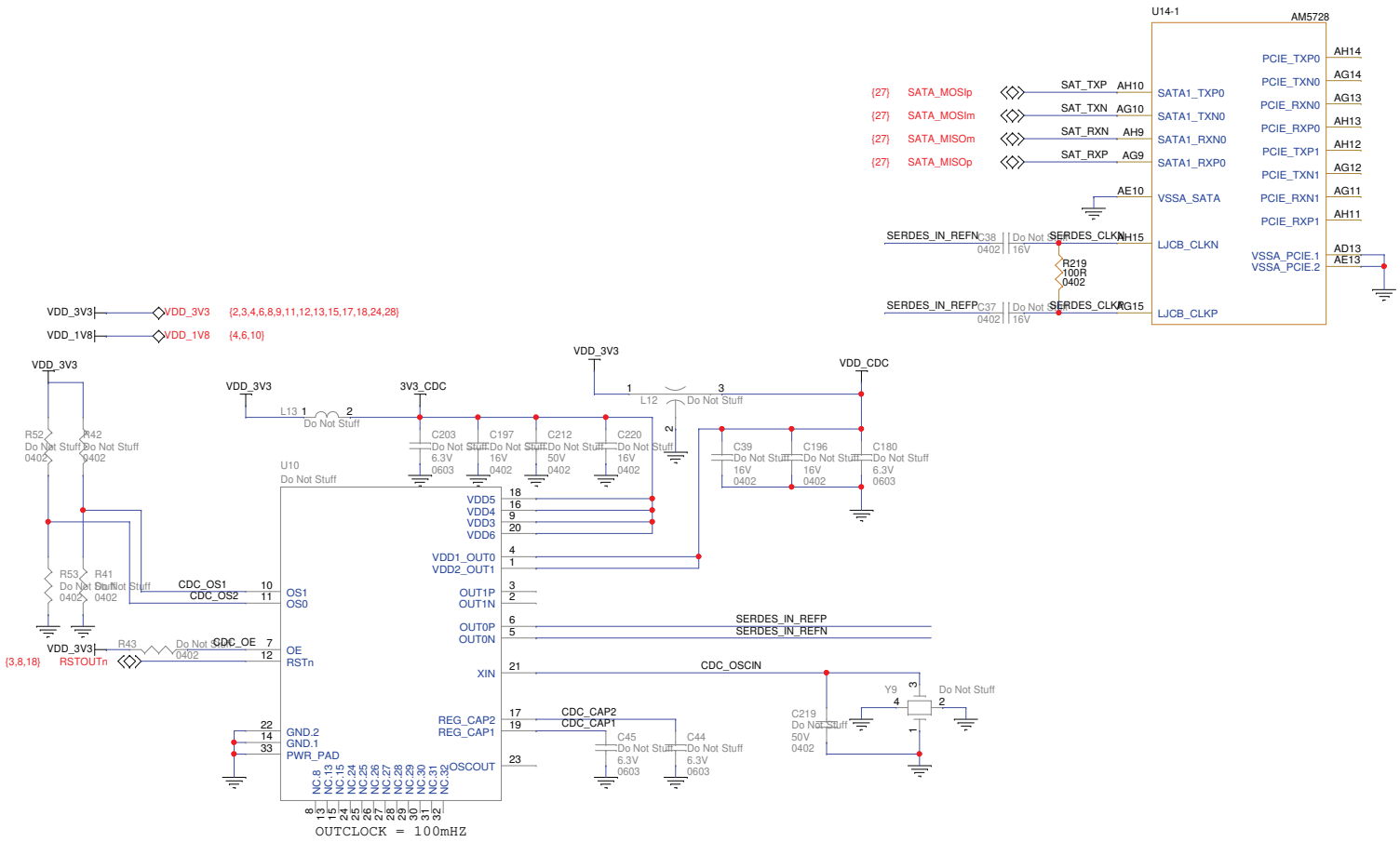
Variant: SINGLE VARIANT

Page: 24 of 28

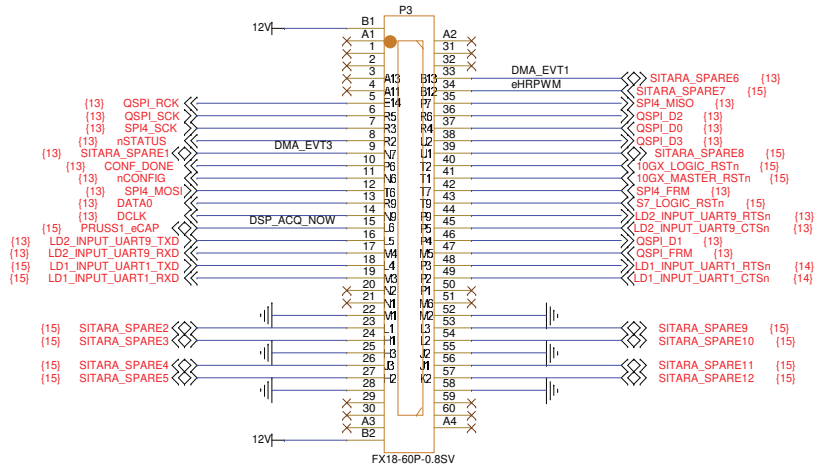


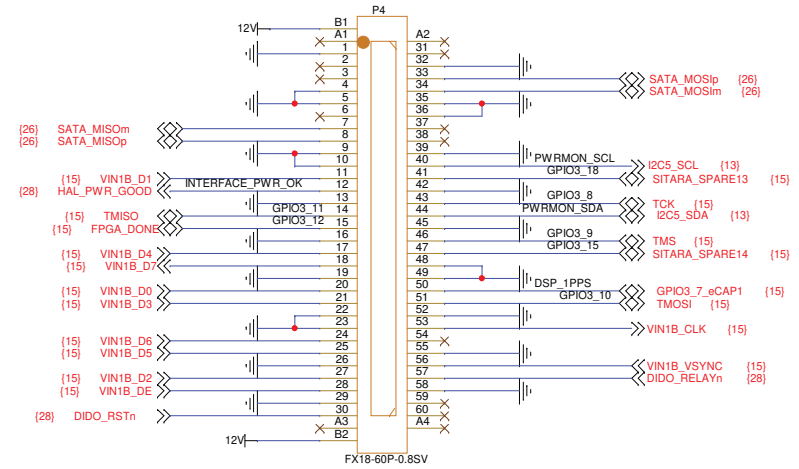


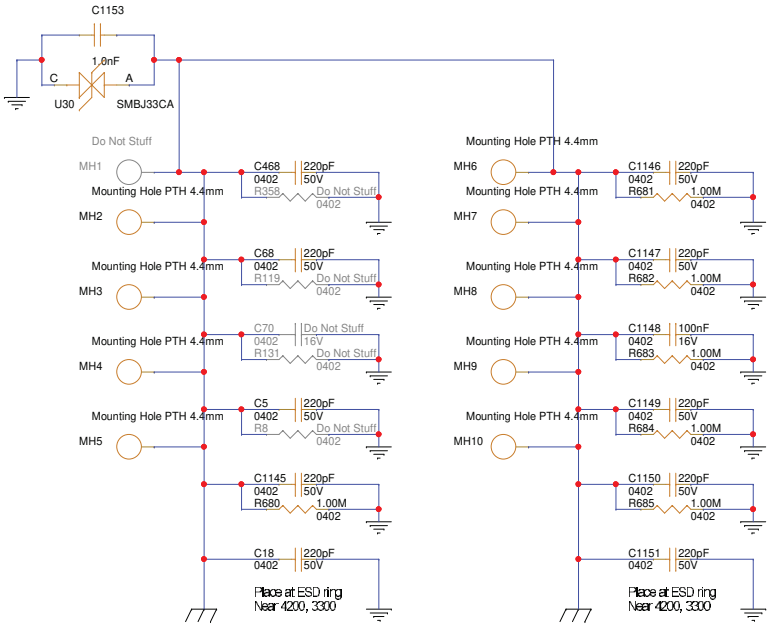
ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P25-RS485 & FASCIA CONNECTOR	
		Document Number: D06285_13 Variant: SINGLE VARIANT	Page: 25 of 28

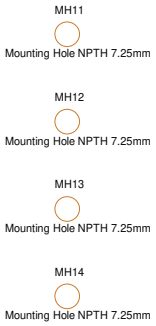


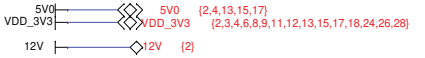
ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P26-PCI, SATA, & SERDES	
		Document Number: D06285_13 Variant: SINGLE VARIANT	Page: 26 of 28

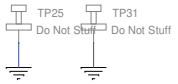




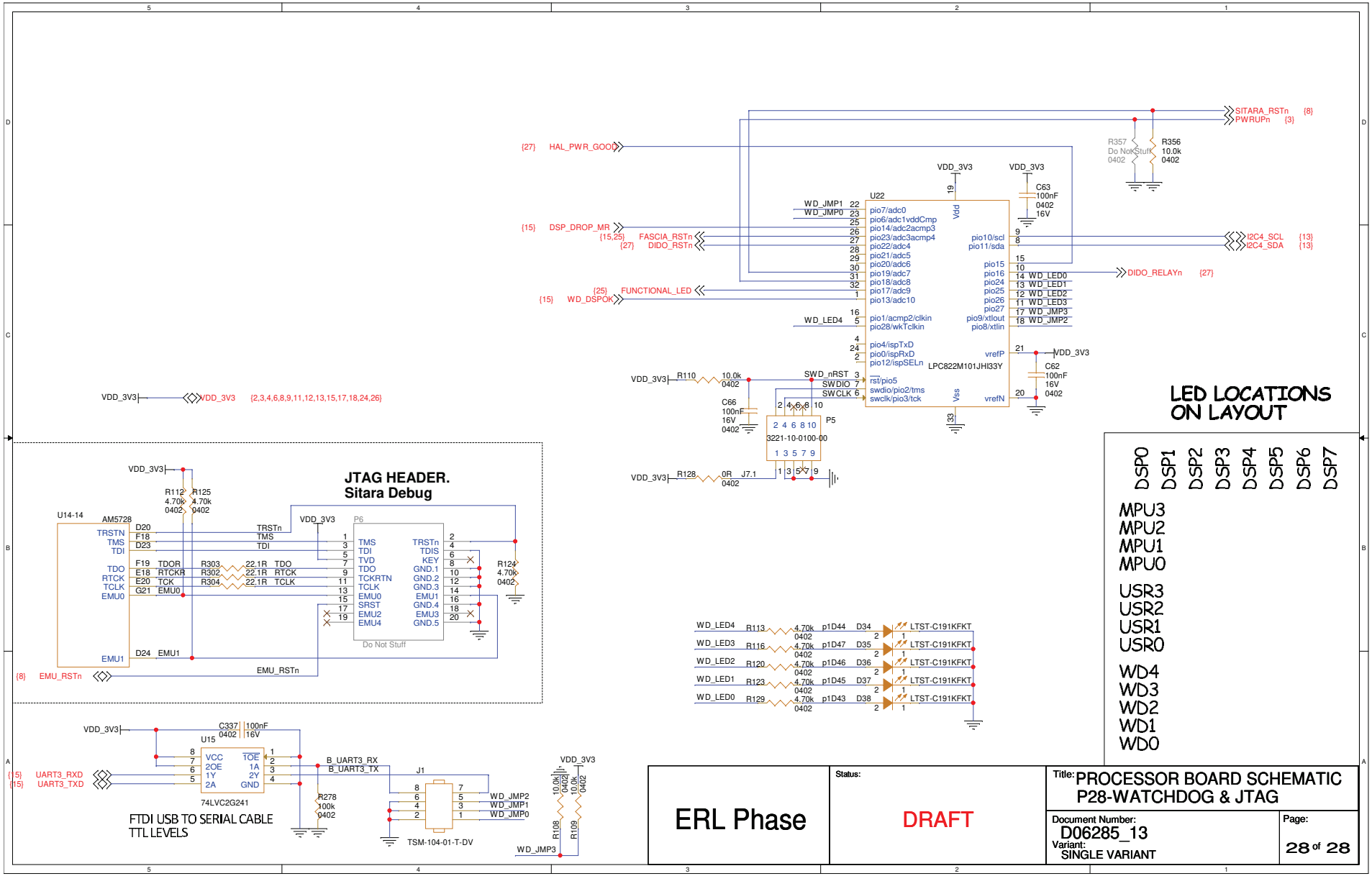








ERL Phase	Status: DRAFT	Title: PROCESSOR BOARD SCHEMATIC P27-EXPANSION HEADERS & MOUNT
		Document Number: D06285_13 Variant: SINGLE VARIANT
		Page: 27 of 28


{27} HAL_PWR_GOOD
SITARA_RSTn {8}
PWRUPn {3}
R357 Do Not Stuff 0402
R356 10.0k 0402
U22
VDD_3V3
C63 100nF 0402 16V
WD_JMP1
WD_JMP0
{15} DSP_DROP_MR
{15,25} FASCIA_RSTn
{27} DIDO_RSTn
I2C4_SCL {13}
I2C4_SDA {13}
DIDO_RELAYn {27}
{25} FUNCTIONAL_LED
{15} WD_DSPOK
WD_LED0
WD_LED1
WD_LED2
WD_LED3
WD_JMP3
WD_JMP2
WD_LED4
LPC822M101JHI33Y
C62 100nF 16V 0402
R110 10.0k 0402
SWD_nRST
SWDIO
SWCLK
C66 100nF 16V 0402
P5
3221-10-0100-00
R128 0R J7.1 0402
VDD_3V3 {2,3,4,6,8,9,11,12,13,15,17,18,24,26}
JTAG HEADER.
Sitara Debug
U14-14
AM5728
TRSTN
TMS
TDI
TDO
RTCK
TCLK
EMU0
EMU1
R112 4.70k 0402
R125 4.70k 0402
R303 22.1R TDO
R302 22.1R RTCK
R304 22.1R TCLK
R124 4.70k 0402
P6
TRSTn
TDIS
KEY
GND.1
GND.2
GND.3
EMU1
GND.4
EMU3
GND.5
Do Not Stuff
EMU_RSTn
{8} EMU_RSTn
WD_LED4 R113 4.70k 0402 p1D44 D34 LTST-C191KFKT
WD_LED3 R116 4.70k 0402 p1D47 D35 LTST-C191KFKT
WD_LED2 R120 4.70k 0402 p1D46 D36 LTST-C191KFKT
WD_LED1 R123 4.70k 0402 p1D45 D37 LTST-C191KFKT
WD_LED0 R129 4.70k 0402 p1D43 D38 LTST-C191KFKT
LED LOCATIONS ON LAYOUT
DSP0 DSP1 DSP2 DSP3 DSP4 DSP5 DSP6 DSP7
MPU3 MPU2 MPU1 MPU0
USR3 USR2 USR1 USR0
WD4 WD3 WD2 WD1 WD0
C337 100nF 0402 16V
U15
74LVC2G241
{15} UART3_RXD
{15} UART3_TXD
B_UART3_RX
B_UART3_TX
R278 100k 0402
J1
TSM-104-01-T-DV
FTDI USB TO SERIAL CABLE
TTL LEVELS
R108 10.0k 0402
R109 10.0k 0402
ERL Phase
Status:
DRAFT
Title: PROCESSOR BOARD SCHEMATIC
P28-WATCHDOG & JTAG
Document Number:
D06285_13
Variant:
SINGLE VARIANT
Page:
28 of 28