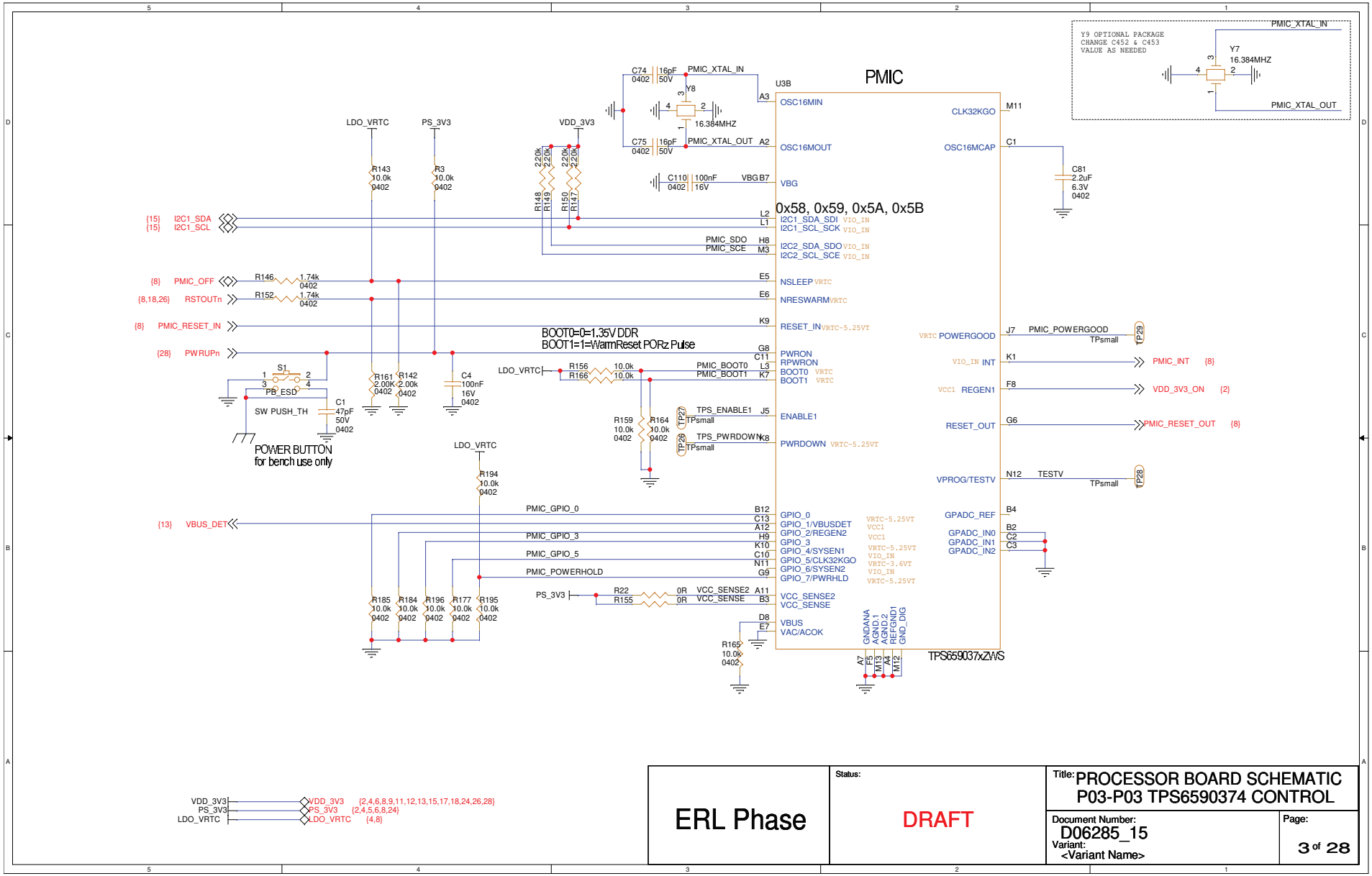
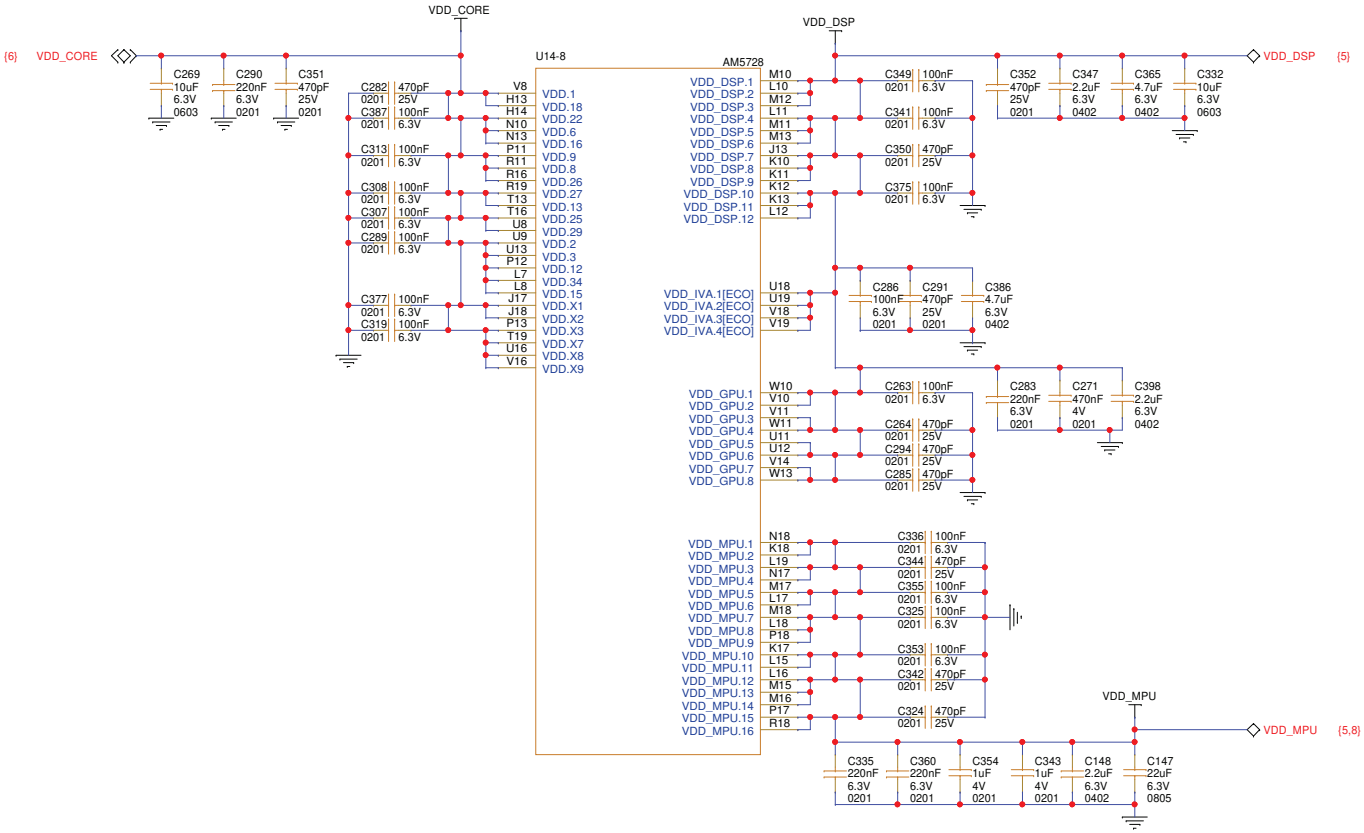
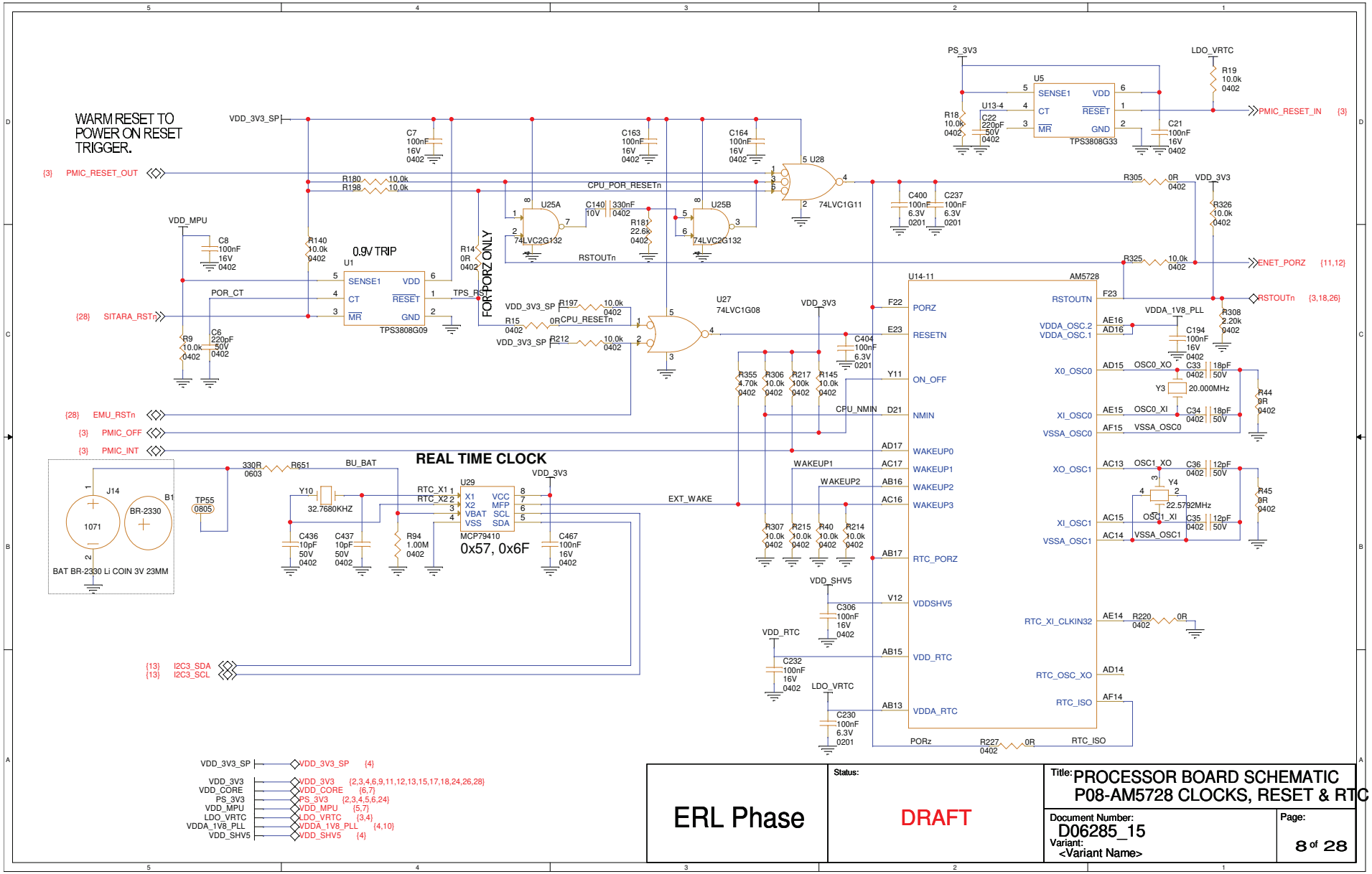
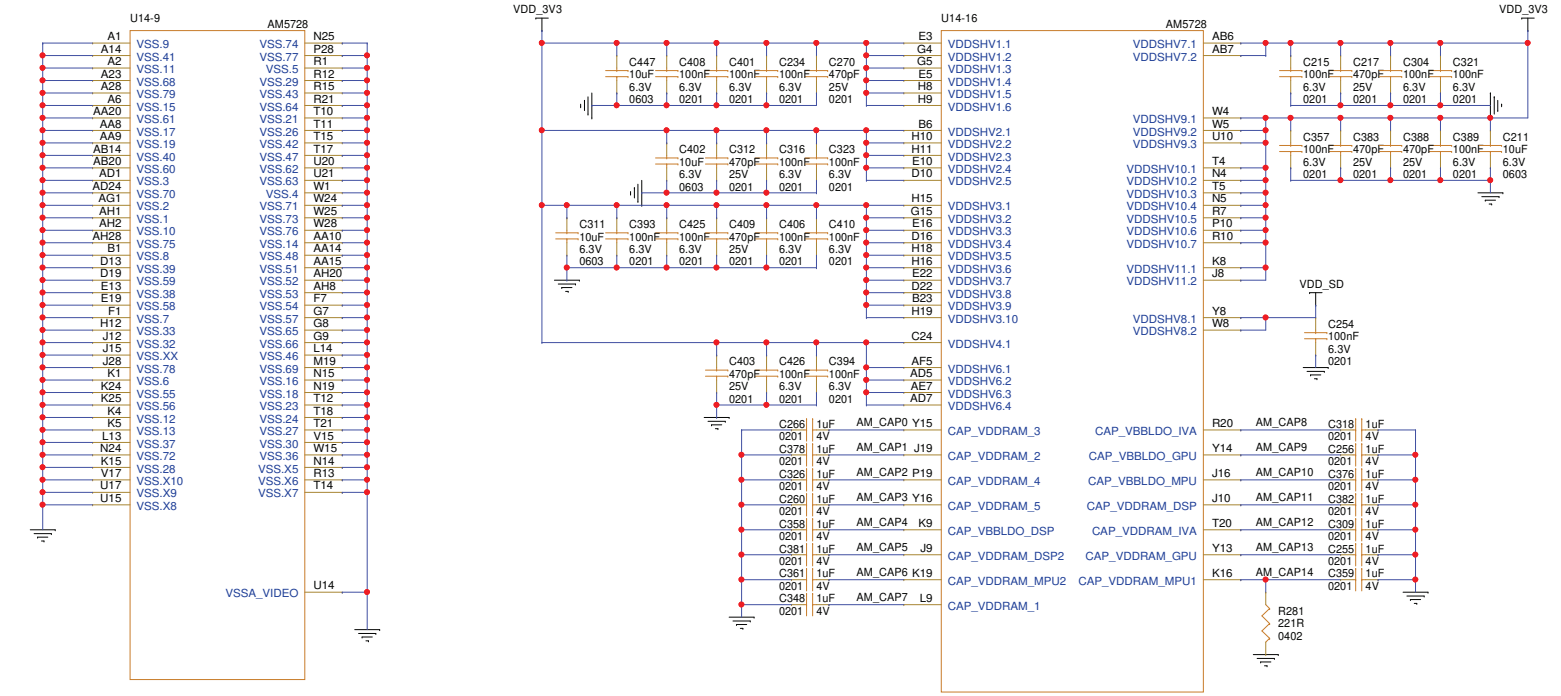

PMIC
U3B
0x58, 0x59, 0x5A, 0x5B
BOOT0=0=1.35V DDR
BOOT1=1=WarmReset PORz Pulse
POWER BUTTON
for bench use only
Y9 OPTIONAL PACKAGE
CHANGE C452 & C453
VALUE AS NEEDED
Y7
16.384MHZ
Y8
16.384MHZ
PMIC_XTAL_IN
PMIC_XTAL_OUT
LDO_VRTC
PS_3V3
VDD_3V3
OSC16MIN
OSC16MOUT
VBG
CLK32KGO
OSC16MCAP
I2C1_SDA_SDI
I2C1_SCL_SCK
I2C2_SDA_SDO
I2C2_SCL_SCE
NSLEEP
NRESWARM
RESET_IN
PWRON
RPWRON
BOOT0
BOOT1
ENABLE1
PWRDOWN
POWERGOOD
INT
REGEN1
RESET_OUT
VPROG/TESTV
GPIO_0
GPIO_1/VBUSDET
GPIO_2/REGEN2
GPIO_3
GPIO_4/SYSEN1
GPIO_5/CLK32KGO
GPIO_6/SYSEN2
GPIO_7/PWRHLD
VCC_SENSE2
VCC_SENSE
VBUS
VAC/ACOK
GPADC_REF
GPADC_IN0
GPADC_IN1
GPADC_IN2
GNDANA
AGND_1
AGND_2
REFGND1
GND_DIG
TPS659037xZWS
PMIC_POWERGOOD
PMIC_INT
VDD_3V3_ON
PMIC_RESET_OUT
TESTV
PMIC_BOOT0
PMIC_BOOT1
TPS_ENABLE1
TPS_PWRDOWN
PMIC_GPIO_0
PMIC_GPIO_3
PMIC_GPIO_5
PMIC_POWERHOLD
VBUS_DET
I2C1_SDA
I2C1_SCL
PMIC_OFF
RSTOUTn
PMIC_RESET_IN
PWRUPn
PMIC_SDO
PMIC_SCE
SW PUSH_TH
PB_ESD
R143 10.0k 0402
R3 10.0k 0402
R146 1.74k 0402
R152 1.74k 0402
R161 2.00k 0402
R142 2.00k 0402
C4 100nF 16V 0402
C1 47pF 50V 0402
C74 16pF 50V 0402
C75 16pF 50V 0402
C110 100nF 16V 0402
C81 2.2uF 6.3V 0402
R148 220k 0402
R149 220k 0402
R150 220k 0402
R147 220k 0402
R156 10.0k 0402
R166 10.0k 0402
R159 10.0k 0402
R164 10.0k 0402
R194 10.0k 0402
R185 10.0k 0402
R184 10.0k 0402
R196 10.0k 0402
R177 10.0k 0402
R195 10.0k 0402
R165 10.0k 0402
R22 0R 0402
R155 0R 0402
TP27 TPsmall
TP29 TPsmall
TP29 TPsmall
TP28 TPsmall
J7 PMIC_POWERGOOD
J5
K8
K1
F8
G6
N12 TESTV
B4
B2
C2
C3
VDD_3V3 {2,4,6,8,9,11,12,13,15,17,18,24,26,28}
PS_3V3 {2,4,5,6,8,24}
LDO_VRTC {4,8}
ERL Phase
Status:
DRAFT
Title: PROCESSOR BOARD SCHEMATIC
P03-P03 TPS6590374 CONTROL
Document Number:
D06285_15
Variant:
<Variant Name>
Page:
3 of 28




| | | |
|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC P07-AM5728 CORE POWER |
| | | Document Number: D06285_15 Variant: <Variant Name> |
| | | Page: 7 of 28 |


WARM RESET TO POWER ON RESET TRIGGER.
REAL TIME CLOCK
0.9V TRIP
FOR PORZ ONLY
BAT BR-2330 Li COIN 3V 23MM
MCP79410
0x57, 0x6F
TPS3808G09
TPS3808G33
74LVC1G11
74LVC2G132
74LVC1G08
AM5728
PMIC_RESET_IN
PMIC_RESET_OUT
ENET_PORZ
RSTOUTn
SITARA_RSTn
EMU_RSTn
PMIC_OFF
PMIC_INT
I2C3_SDA
I2C3_SCL
EXT_WAKE
CPU_POR_RESETn
RSTOUTn
PORz
VDD_3V3_SP
VDD_3V3
VDD_CORE
PS_3V3
VDD_MPU
LDO_VRTC
VDDA_1V8_PLL
VDD_SHV5
VDD_RTC
VDDA_RTC
Status:
DRAFT
ERL Phase
Title: PROCESSOR BOARD SCHEMATIC
P08-AM5728 CLOCKS, RESET & RTC
Document Number:
D06285_15
Variant:
<Variant Name>
Page:
8 of 28

C321 DNP to avoid
mechanical interference




VDD_SD — VDD_SD {4,18}

VDD_3V3 — VDD_3V3 {2,3,4,6,8,11,12,13,15,17,18,24,26,28}

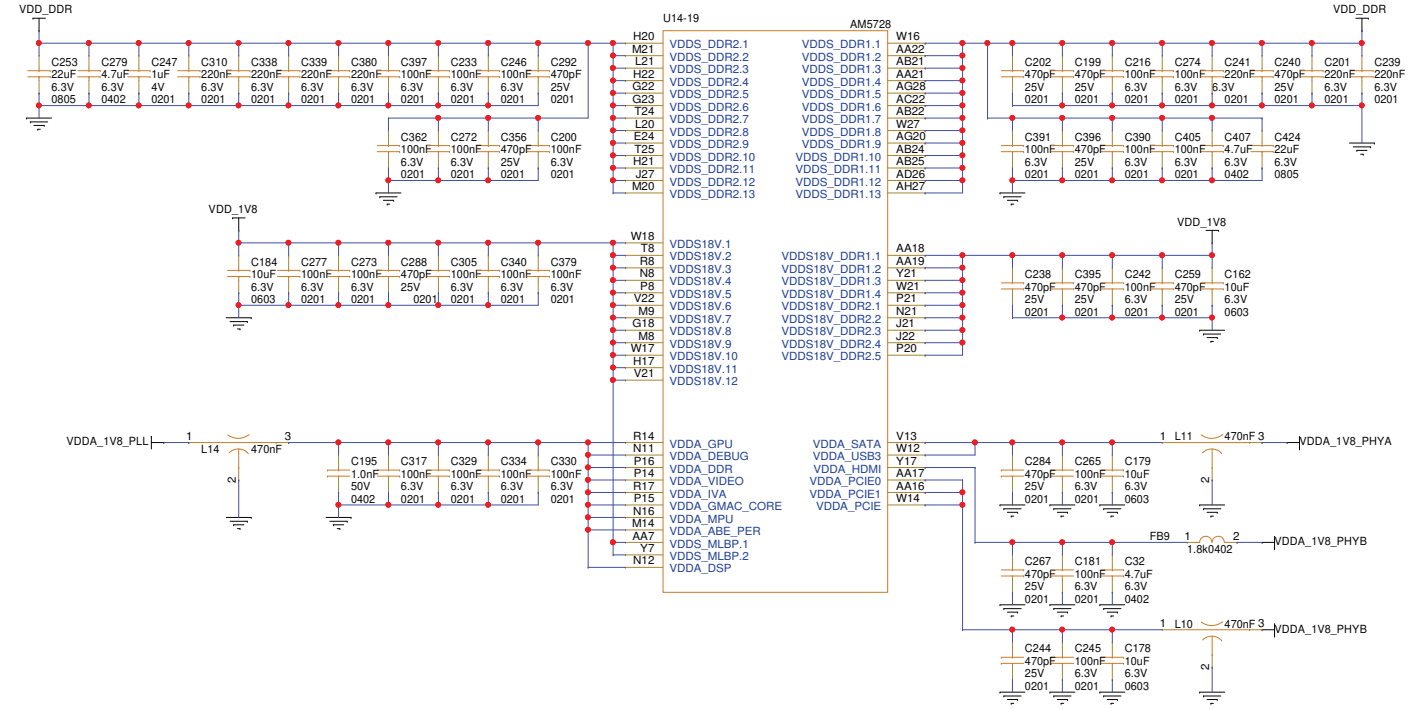
ERL Phase

Status: DRAFT

Title: PROCESSOR BOARD SCHEMATIC
P09-AM5728 IO POWER AND GROUND

Document Number: D06285_15
Variant: <Variant Name>

Page: 9 of 28




| | |
|---|---|
| VDD_1V8 | VDD_1V8 {4,6} |
| VDD_3V3 | VDD_3V3 {2,3,4,6,8,9,11,12,13,15,17,18,24,26,28} |
| VDD_DDR | VDD_DDR {5,19,21,22,23,24} |
| VDDA_1V8_PLL | VDDA_1V8_PLL {4,8} |
| VDDA_1V8_PHYA | VDDA_1V8_PHYA {4,14} |
| VDDA_1V8_PHYB | VDDA_1V8_PHYB {4} |

ERL Phase

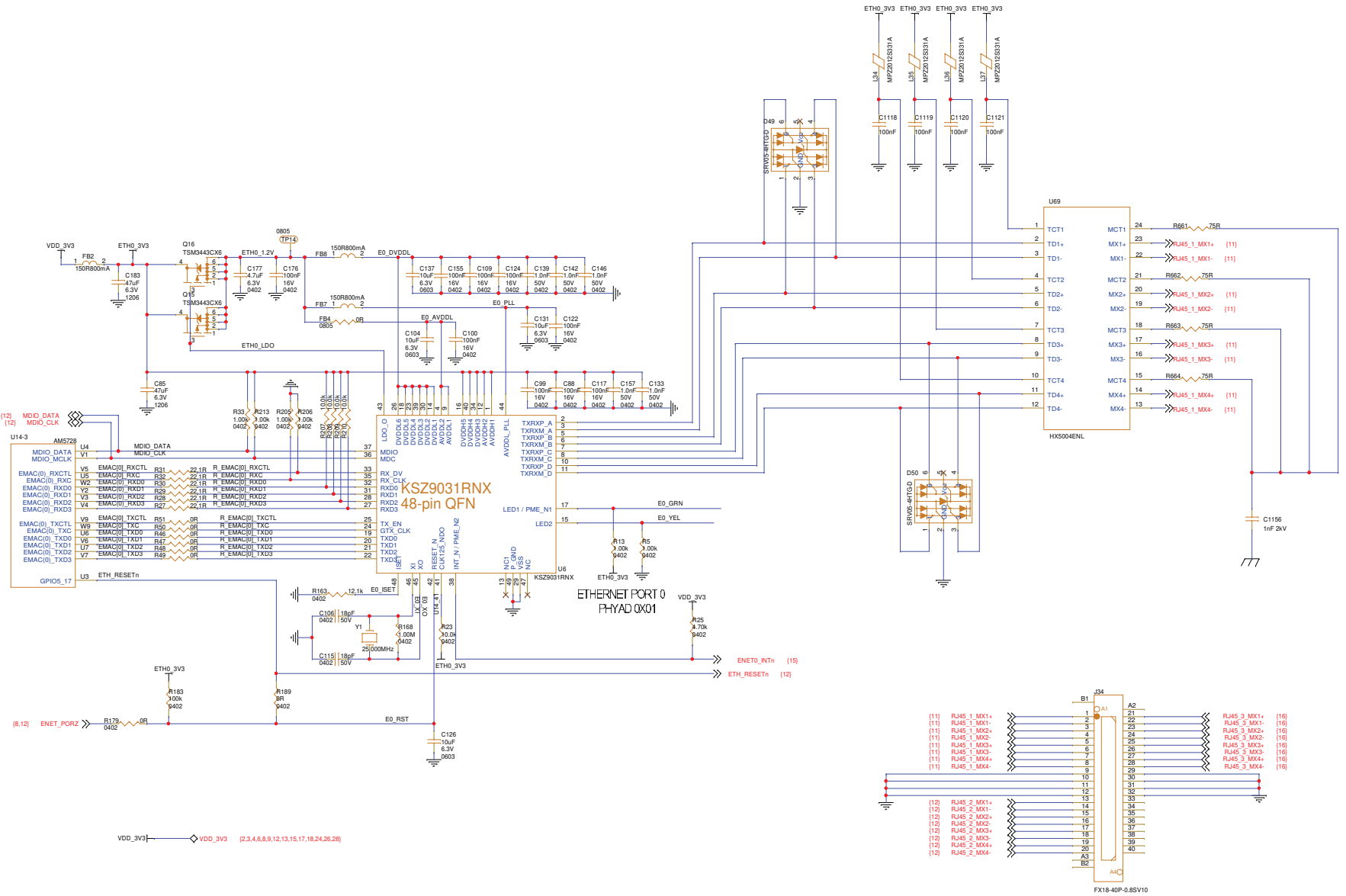
Status: DRAFT

Title: PROCESSOR BOARD SCHEMATIC
P10-AM5728 DDR3 POWER

Document Number: D06285_15

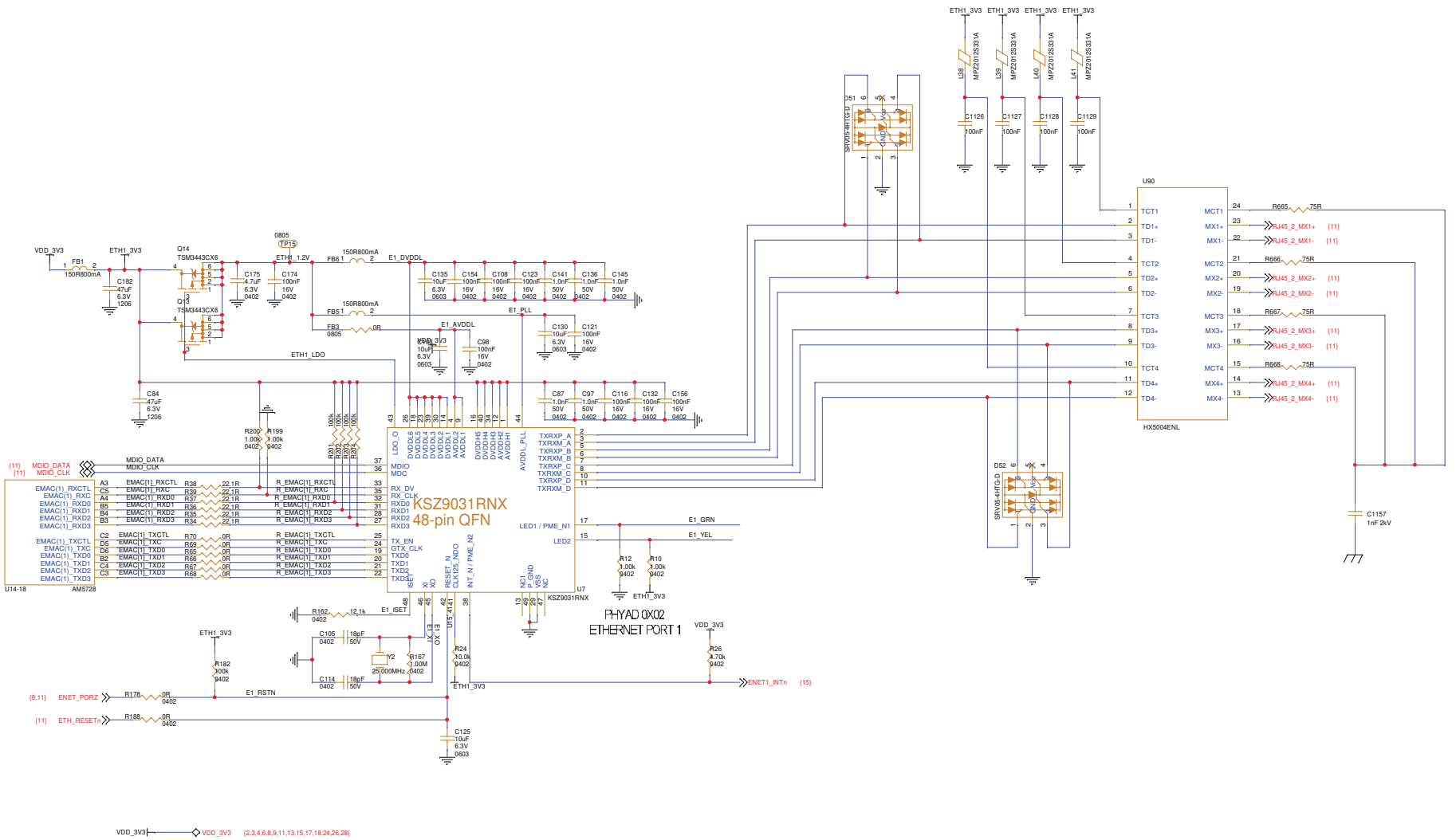
Variant: <Variant Name>

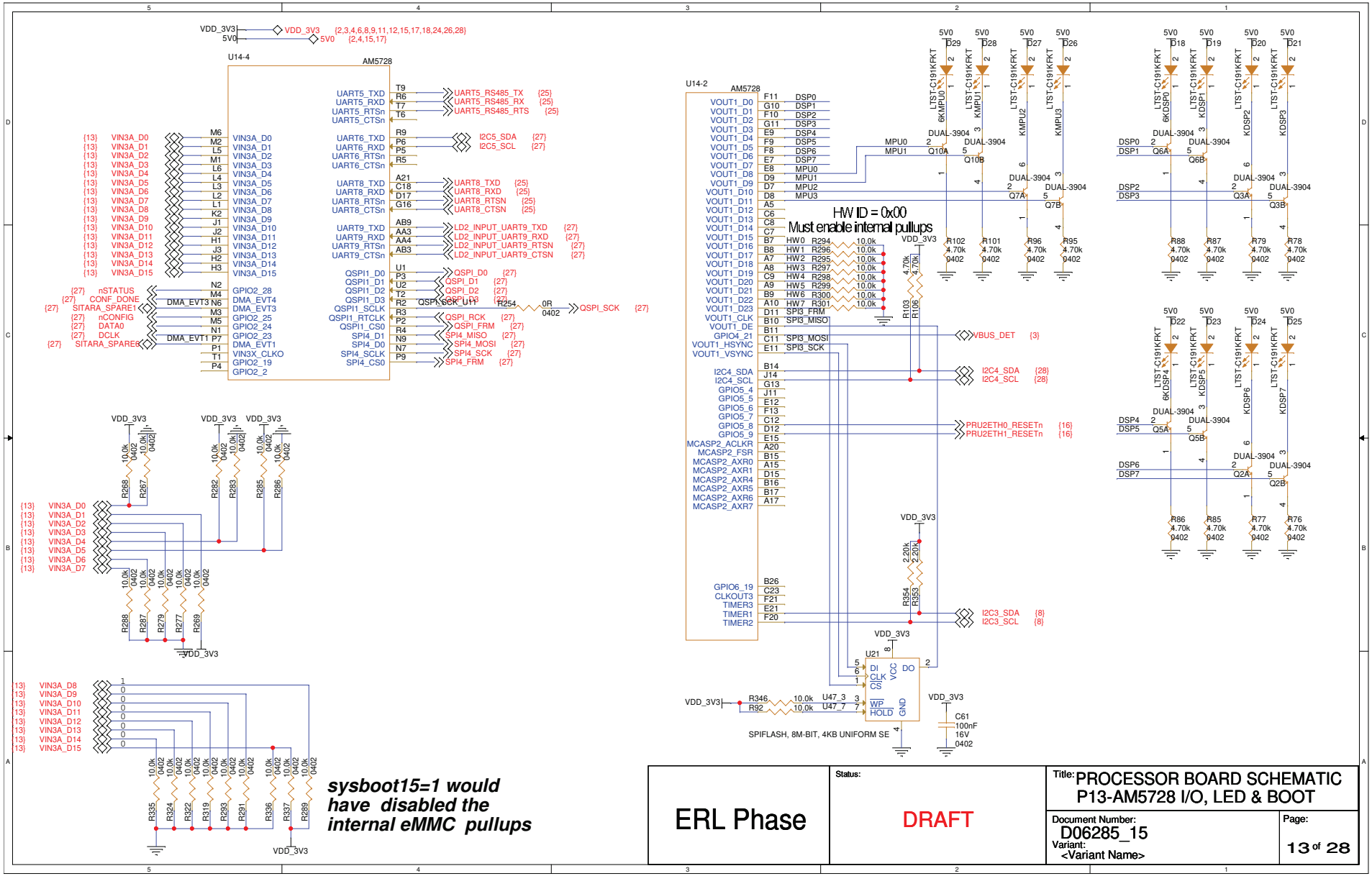
Page: 10 of 28



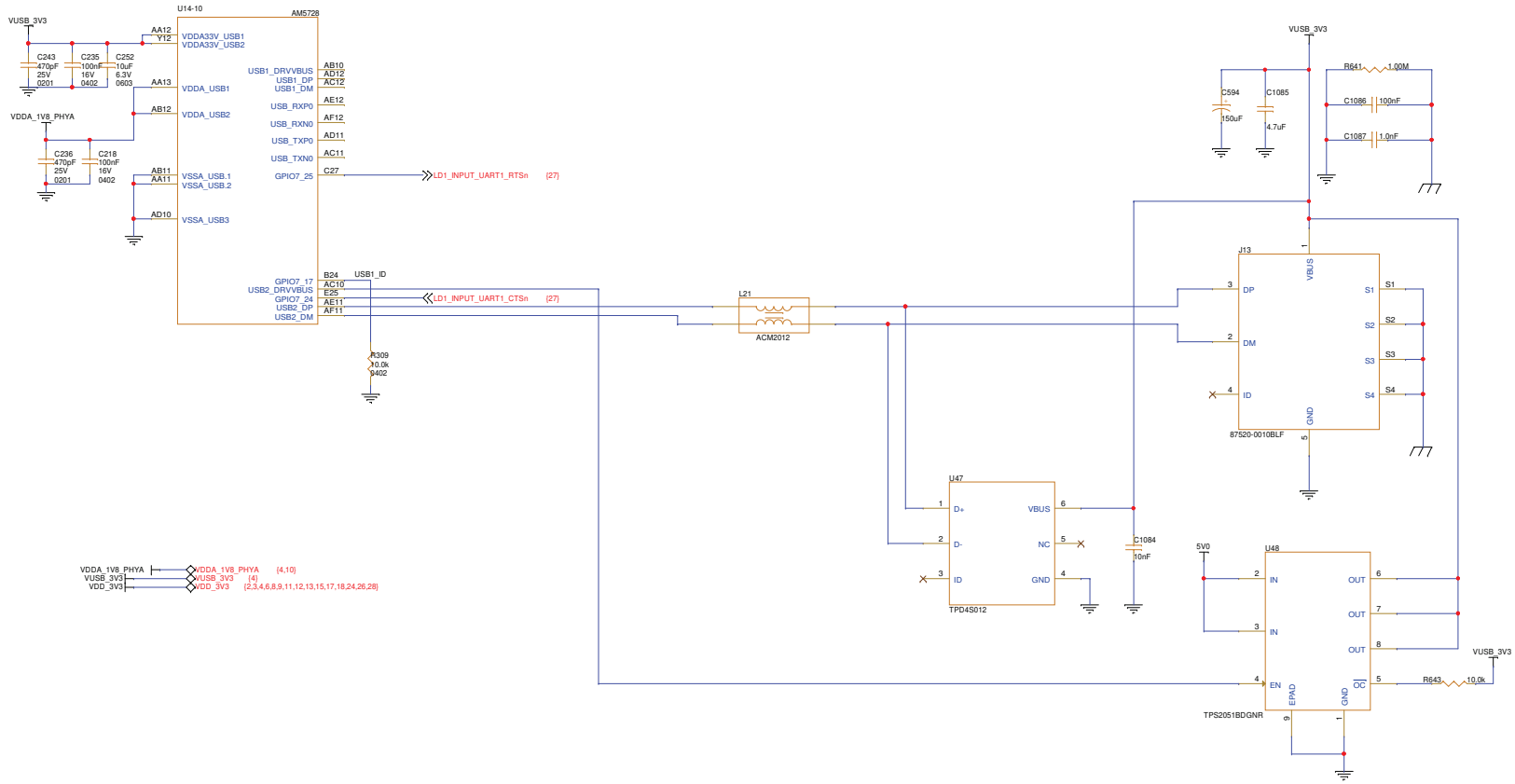

Ethernet signals are connected directly to the Hirose connector without an RJ45.
These signals are intended for board-to-board communication between the processor board and the communication board.

| | | | |
|---|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC P11-AM5728 ETHERNET 1 | |
| | | Document Number: D06285_15 Variant: <Variant Name> | Page: 11 of 28 |

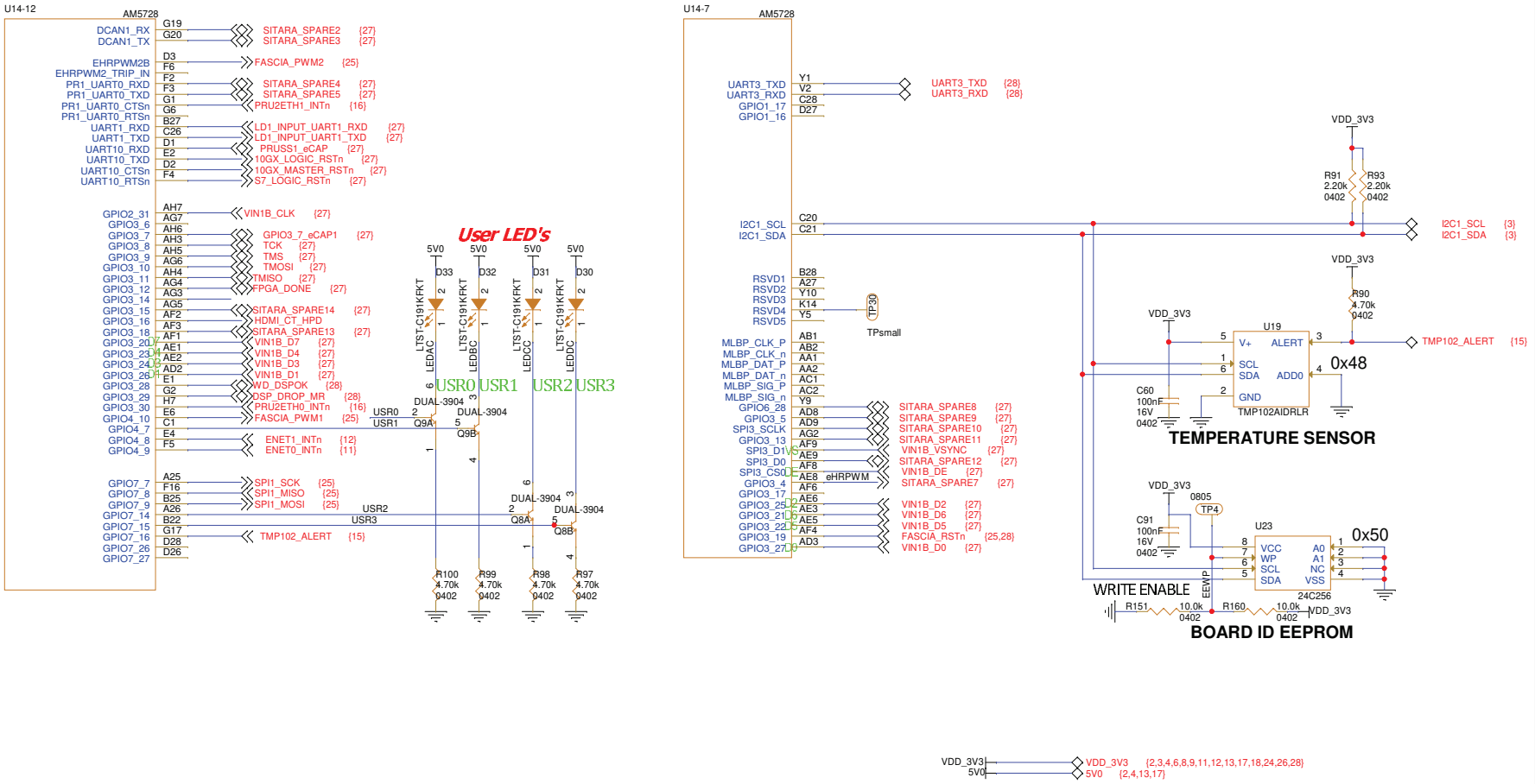

KSZ9031RNX
48-pin QFN
PHYAD 0X02
ETHERNET PORT 1
HX5004ENL
AM5728
KSZ9031RNX
ERL Phase
DRAFT
PROCESSOR BOARD SCHEMATIC
P12-AM5728 ETHERNET 2
D06285_15
<Variant Name>
12 of 28



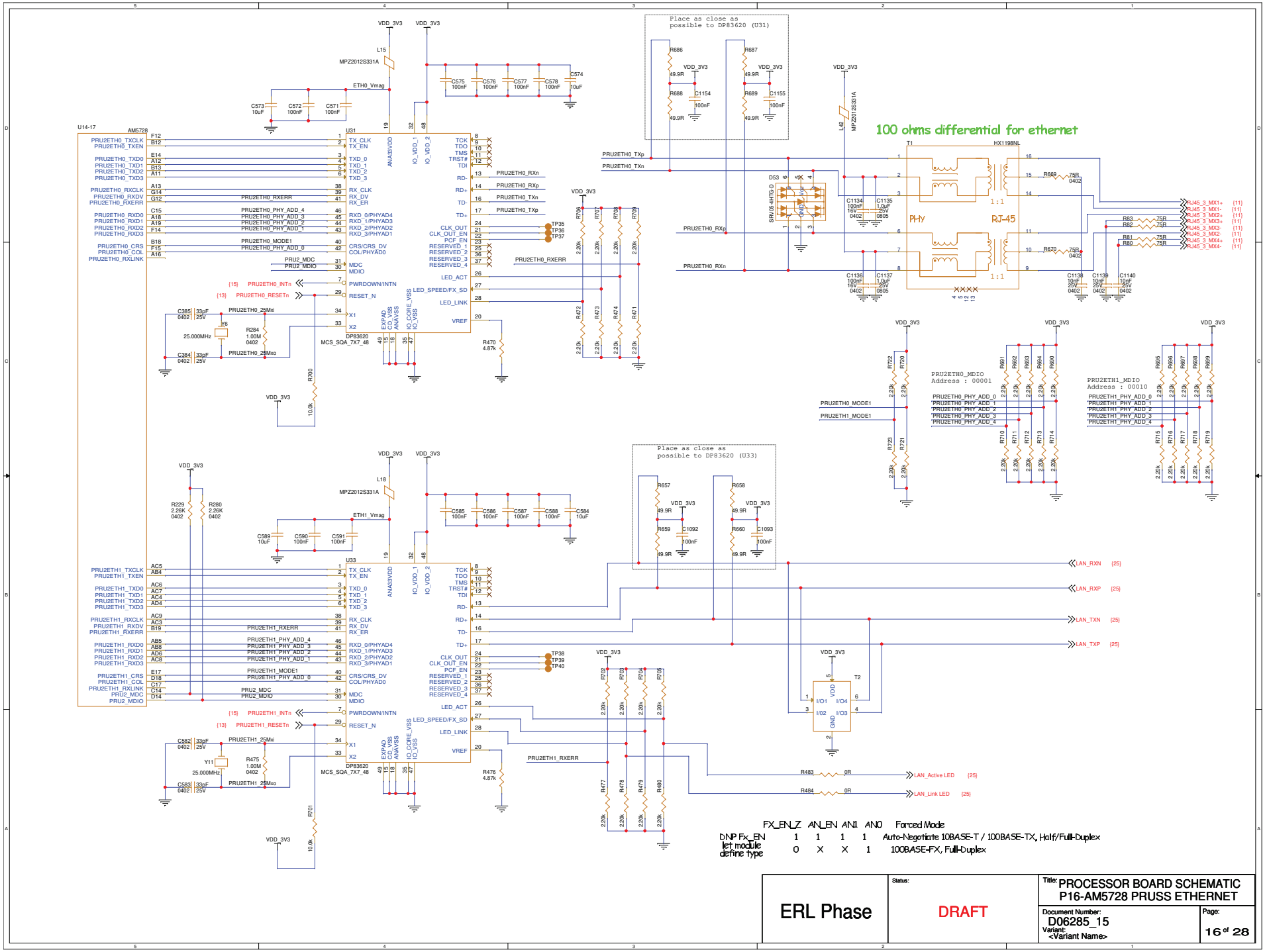

| | | |
|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC<br>P13-AM5728 I/O, LED & BOOT |
| | Document Number: D06285_15<br>Variant: <Variant Name> | Page: 13 of 28 |

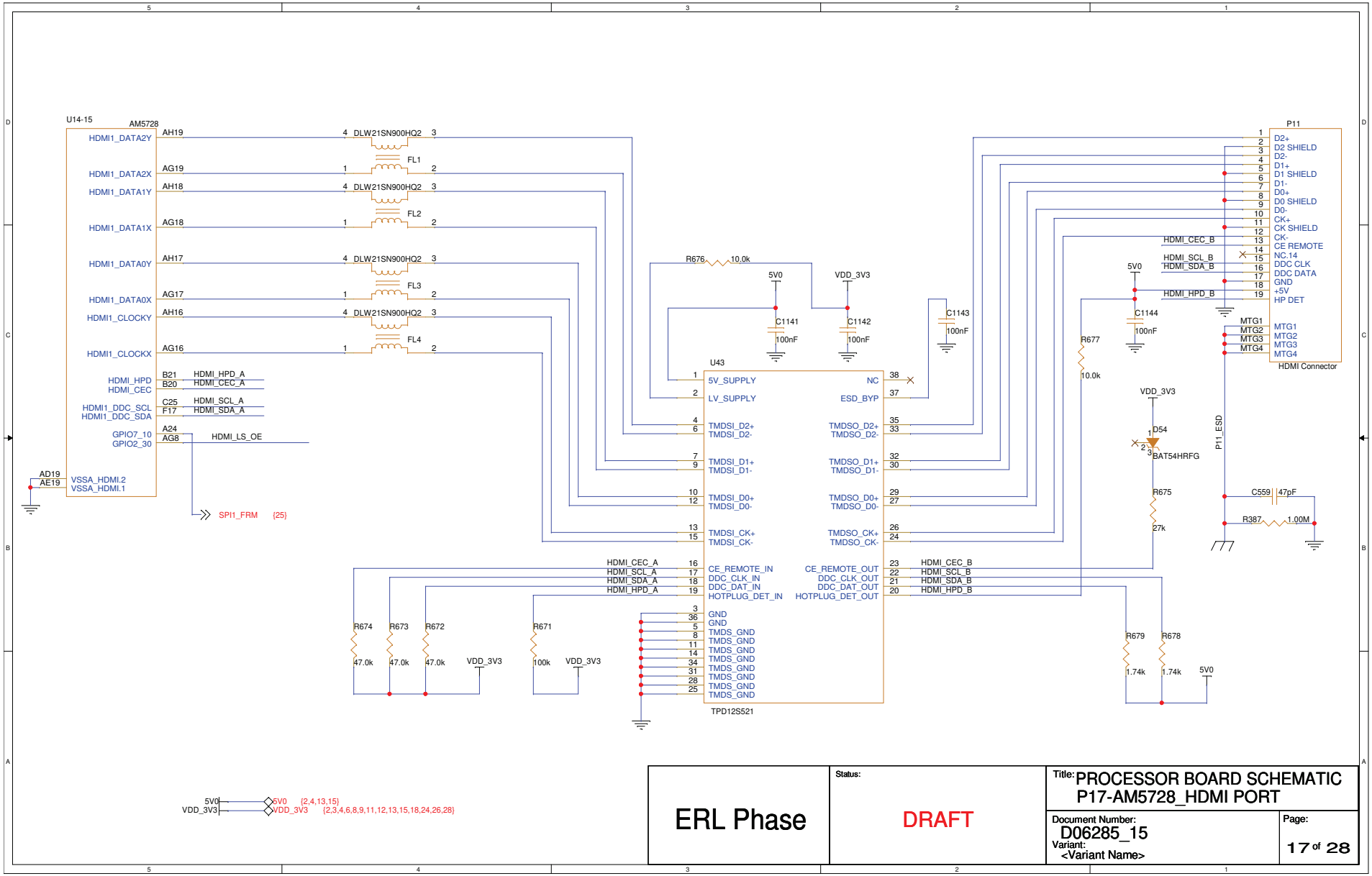



| | | | |
|---|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC<br>P14-AM5728 USB PORTS & HUB | |
| | | Document Number: D06285_15<br>Variant: <Variant Name> | Page: 14 of 28 |

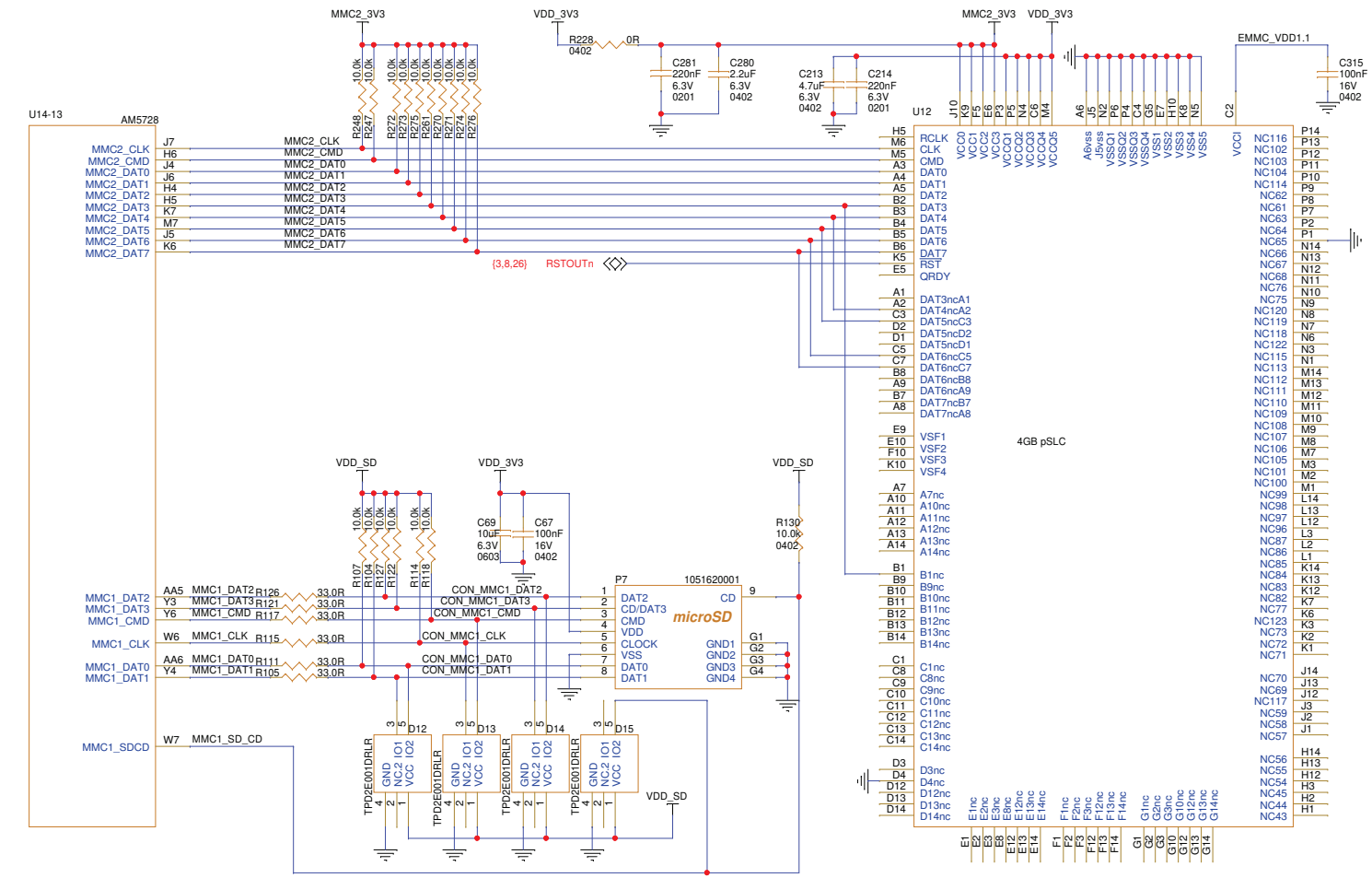



| | | | |
|---|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC P15-AM5728 I/O, LEDs & EEPROM | |
| | | Document Number: D06285_15<br>Variant: <Variant Name> | Page: 15 of 28 |


100 ohms differential for ethernet
Place as close as possible to DP83620 (U31)
Place as close as possible to DP83620 (U33)
PRU2ETH0_MDIO Address : 00001
PRU2ETH1_MDIO Address : 00010
PHY
RJ-45
FX_EN_Z AN_EN AN1 AN0 Forced Mode
DNP Fx_EN let module define type
1 1 1 1 Auto-Negotiate 10BASE-T / 100BASE-TX, Half/Full-Duplex
0 X X 1 100BASE-FX, Full-Duplex
ERL Phase
DRAFT
PROCESSOR BOARD SCHEMATIC
P16-AM5728 PRUSS ETHERNET
D06285_15
<Variant Name>
16 of 28




| | | | |
|---|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC<br>P17-AM5728_HDMI PORT | |
| | | Document Number: D06285_15<br>Variant: <Variant Name> | Page: 17 of 28 |



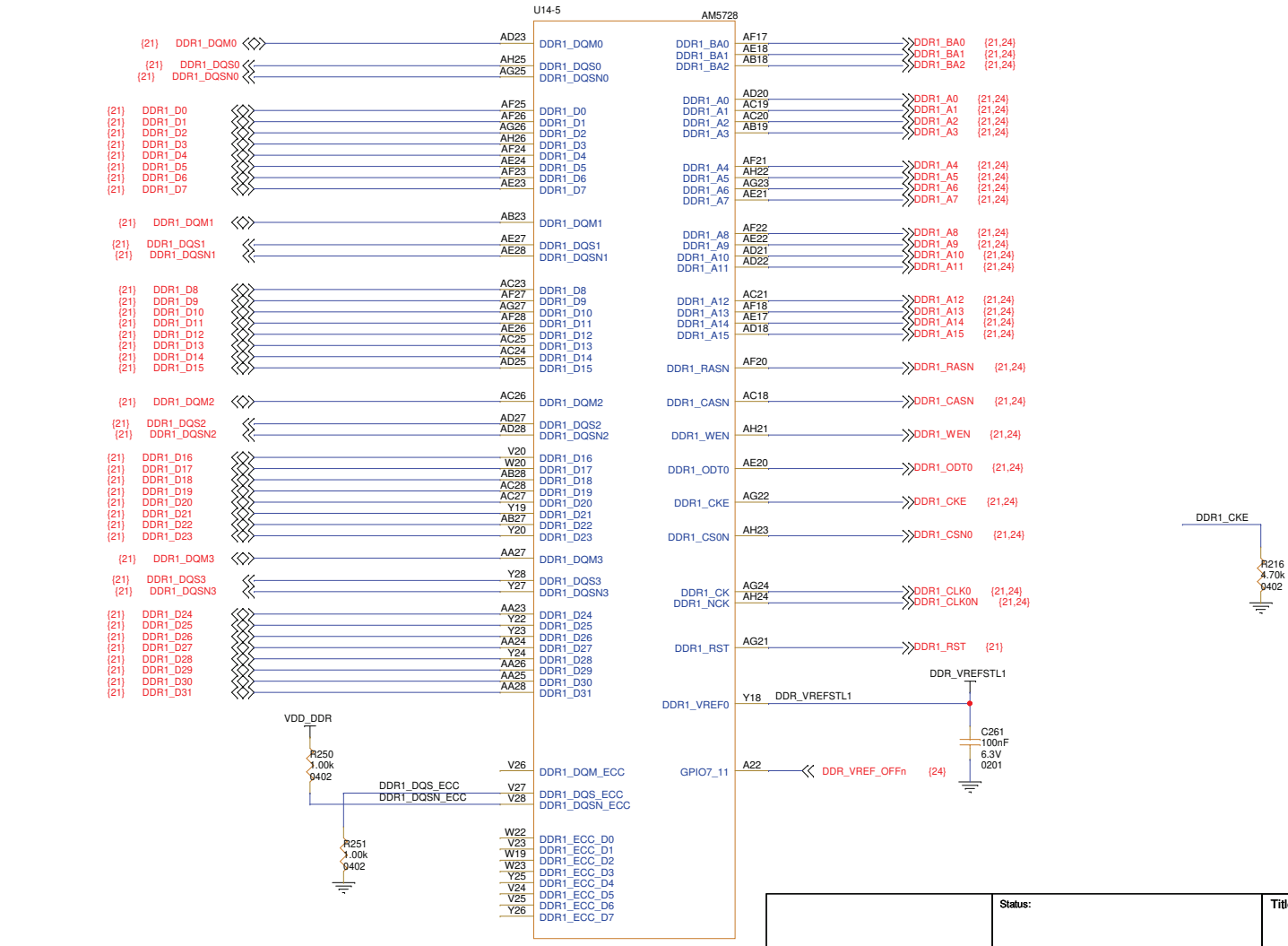

ERL Phase

Status: DRAFT

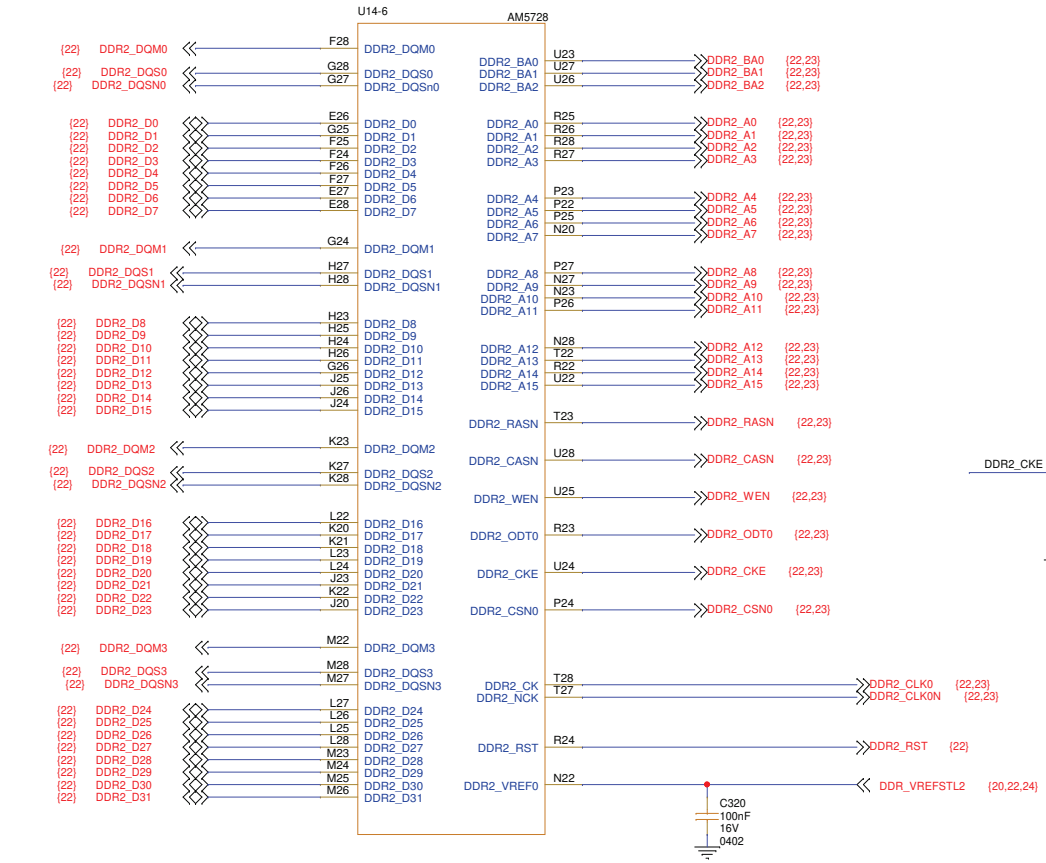
Title: PROCESSOR BOARD SCHEMATIC
P18-AM5728 eMMC, MMC3 & uSD

Document Number: D06285_15
Variant: <Variant Name>

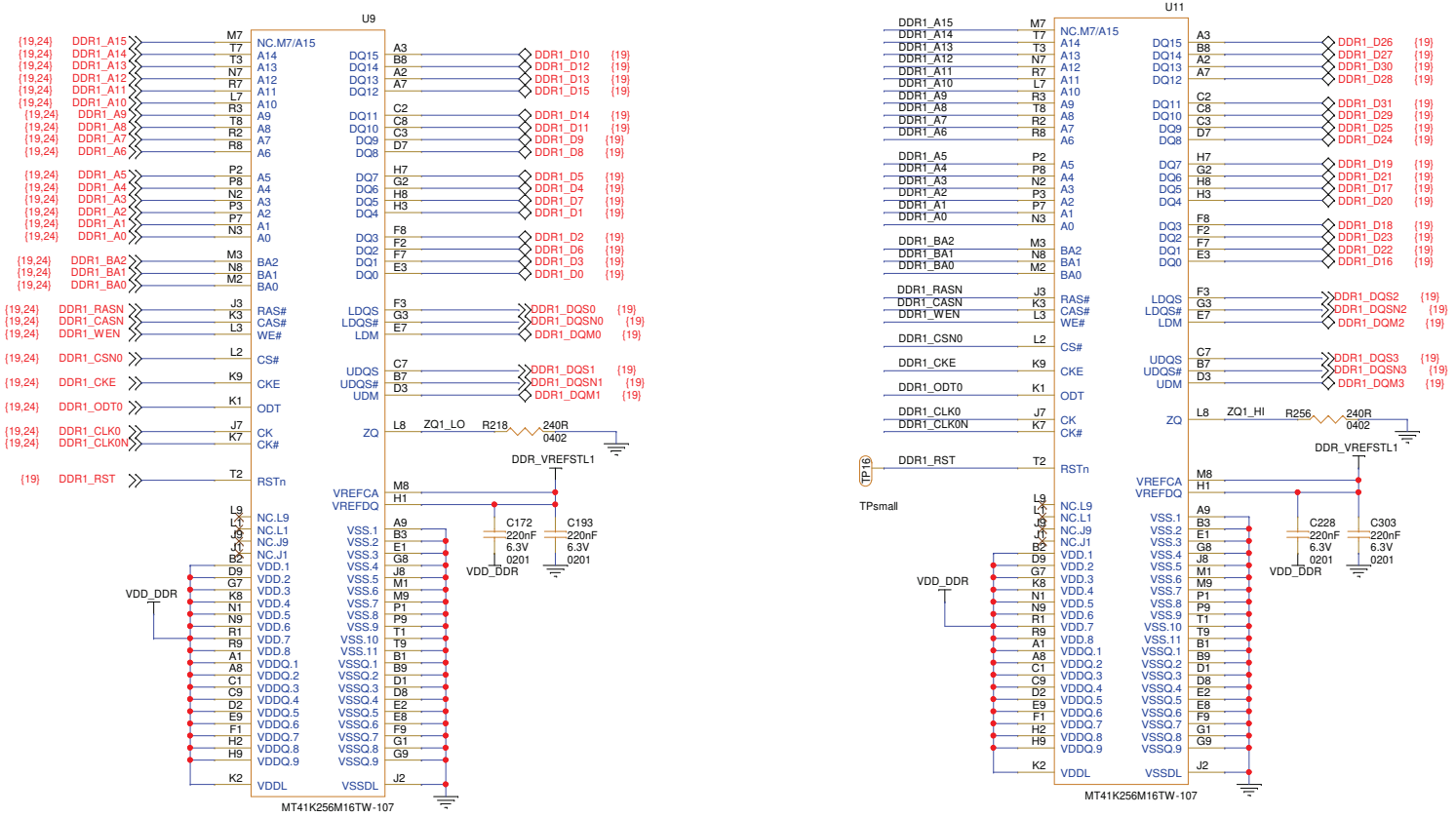
Page: 18 of 28

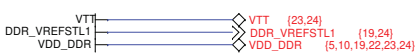



| | | | |
|---|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC P19-AM5728 DDR INTERFACE 1 | |
| | | Document Number: D06285_15 Variant: <Variant Name> | Page: 19 of 28 |

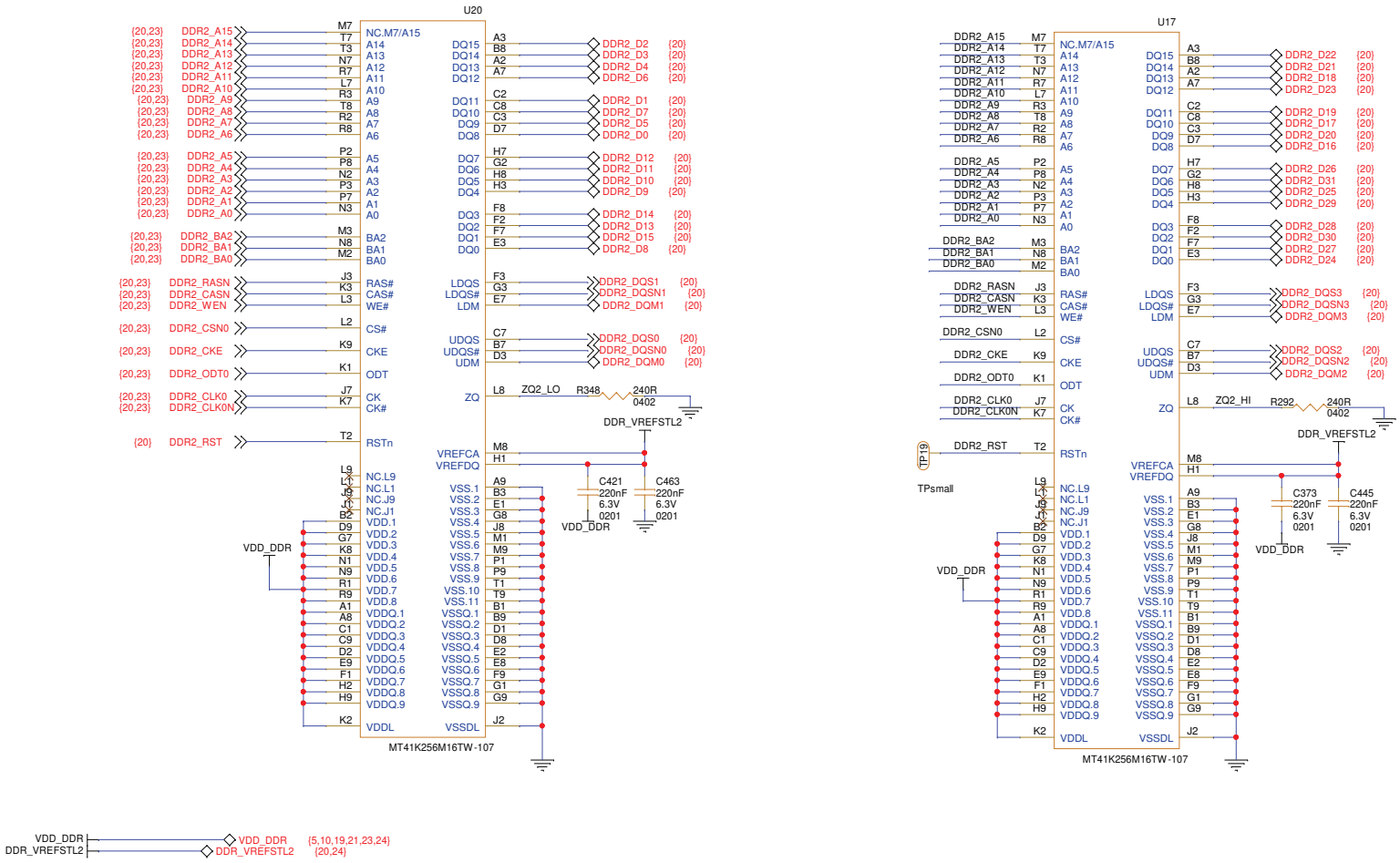



| | | |
|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC<br>P20-AM5728 DDR INTERFACE 2 |
| | | Document Number: D06285_15<br>Variant: <Variant Name> |
| | | Page: 20 of 28 |



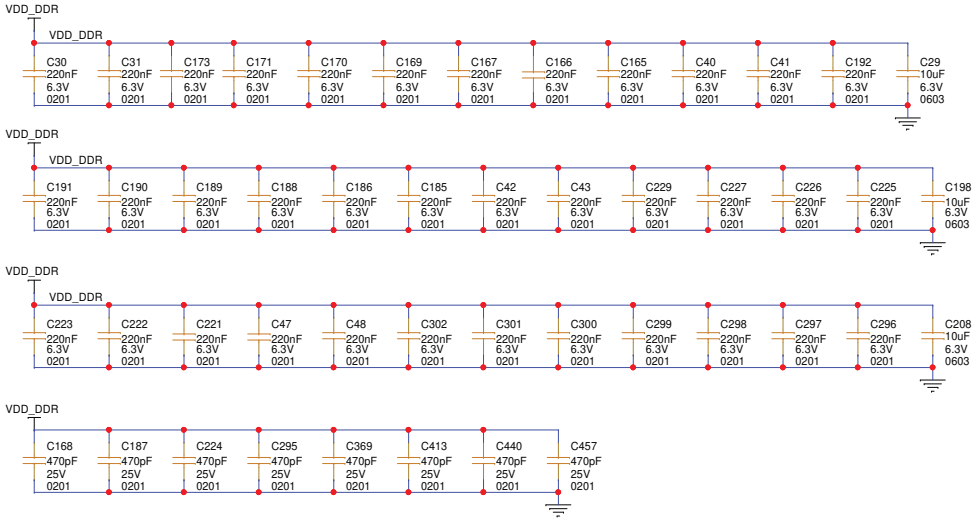



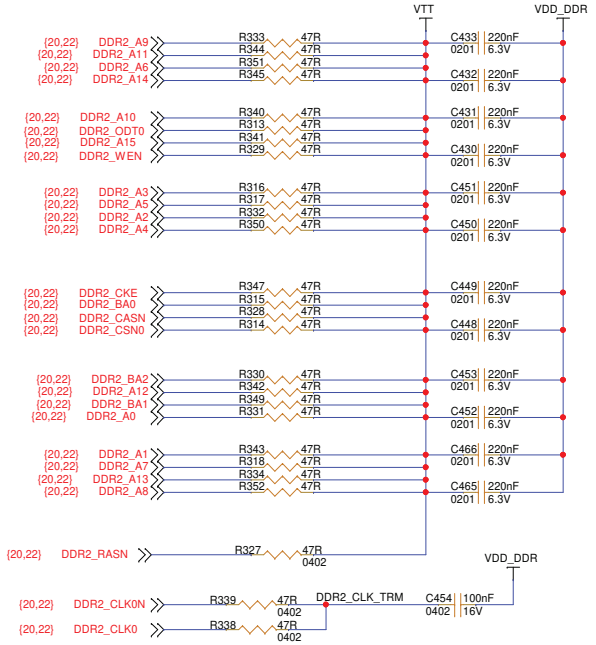

| | | | |
|---|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC P21-DDR3 BANK 1 | |
| | | Document Number: D06285_15<br>Variant: <Variant Name> | Page: 21 of 28 |




VDD_DDR — VDD_DDR {5,10,19,21,23,24}
DDR_VREFSTL2 — DDR_VREFSTL2 {20,24}

| | | |
|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC P22-DDR3 BANK 2 |
| | | Document Number: D06285_15 Variant: <Variant Name> |
| | | Page: 22 of 28 |

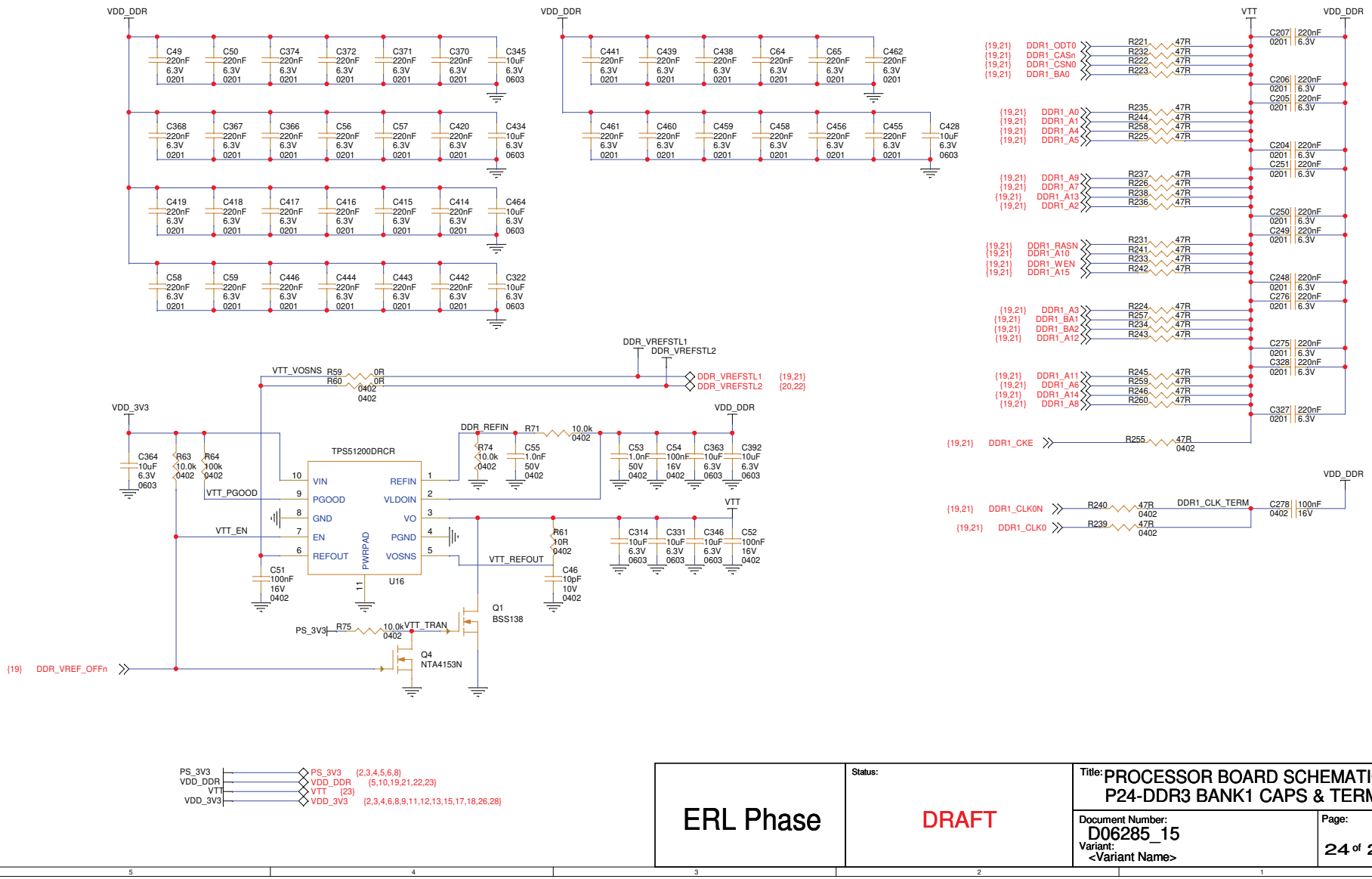






| | | |
|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC<br>P23-DDR3 BANK 2 CAPS & TERM |
| | | Document Number: D06285_15<br>Variant: <Variant Name> |
| | | Page: 23 of 28 |




ERL Phase

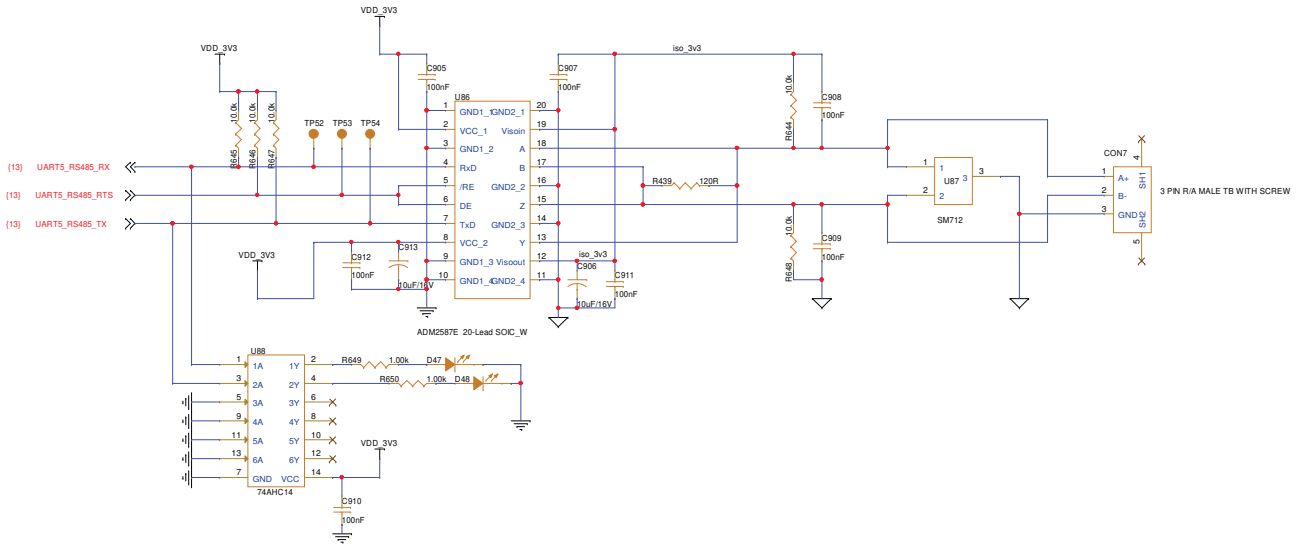
Status: DRAFT

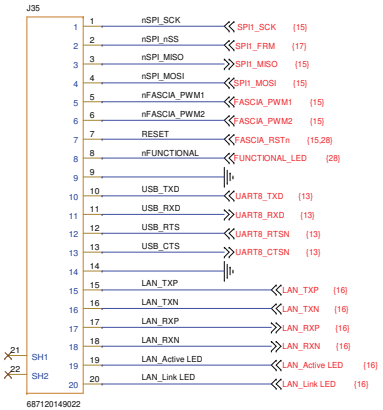
Title: PROCESSOR BOARD SCHEMATIC
P24-DDR3 BANK1 CAPS & TERM

Document Number: D06285_15

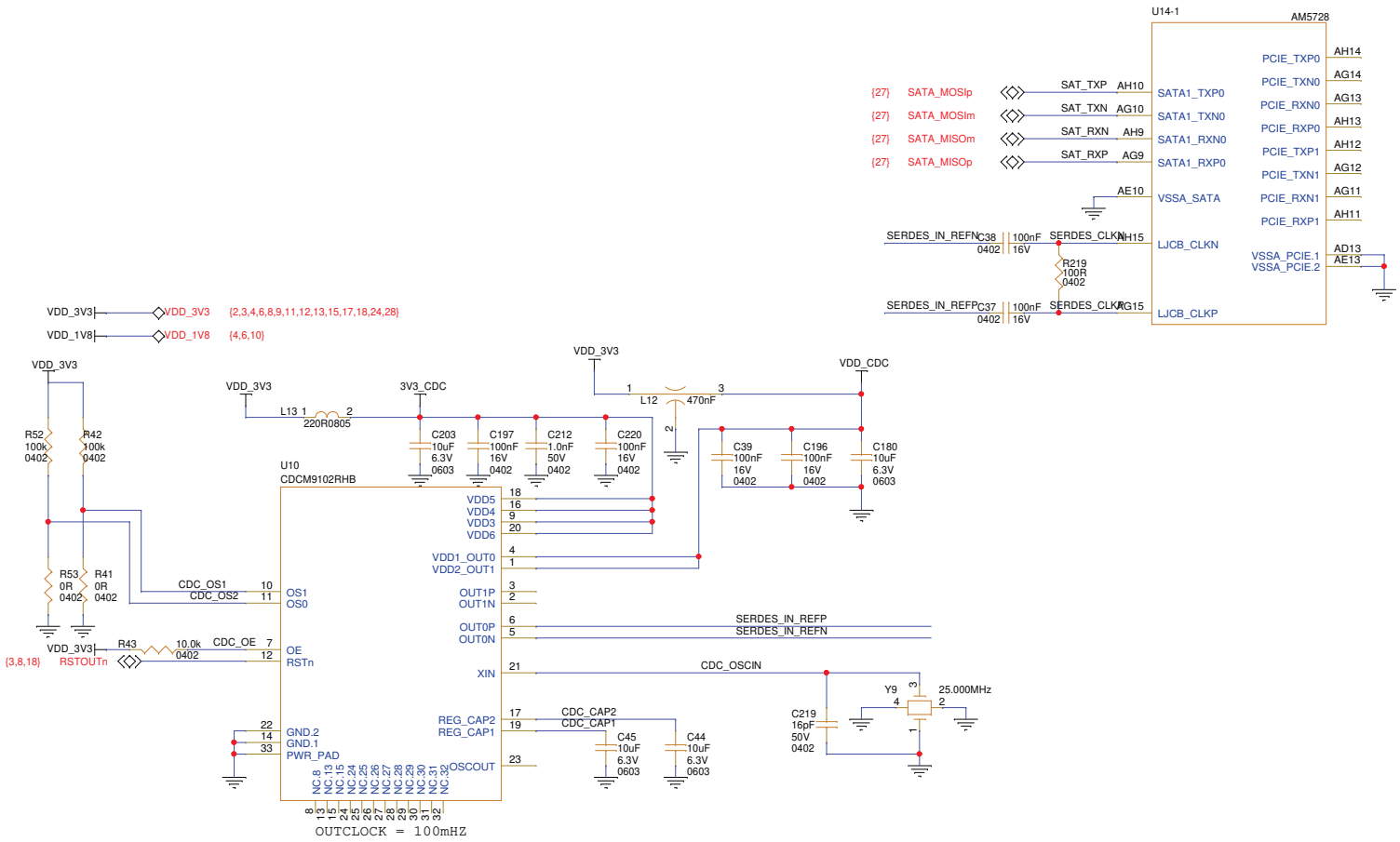
Variant: <Variant Name>

Page: 24 of 28

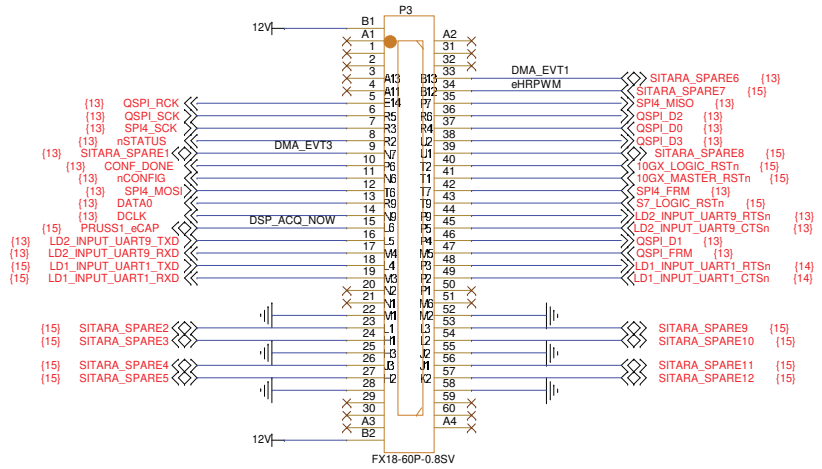


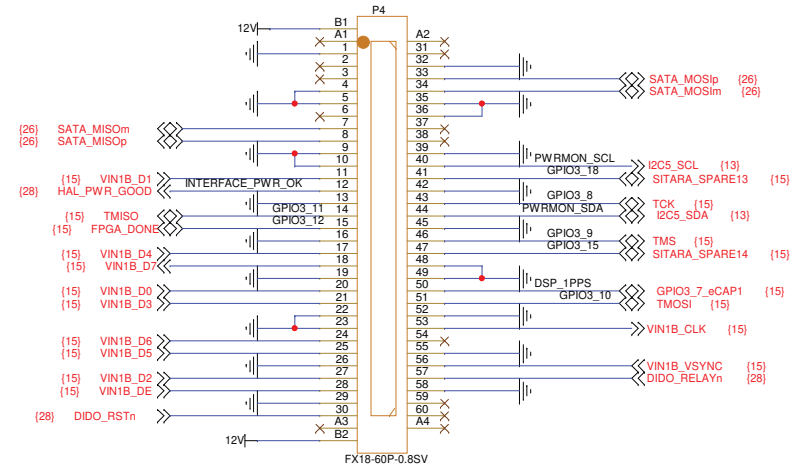



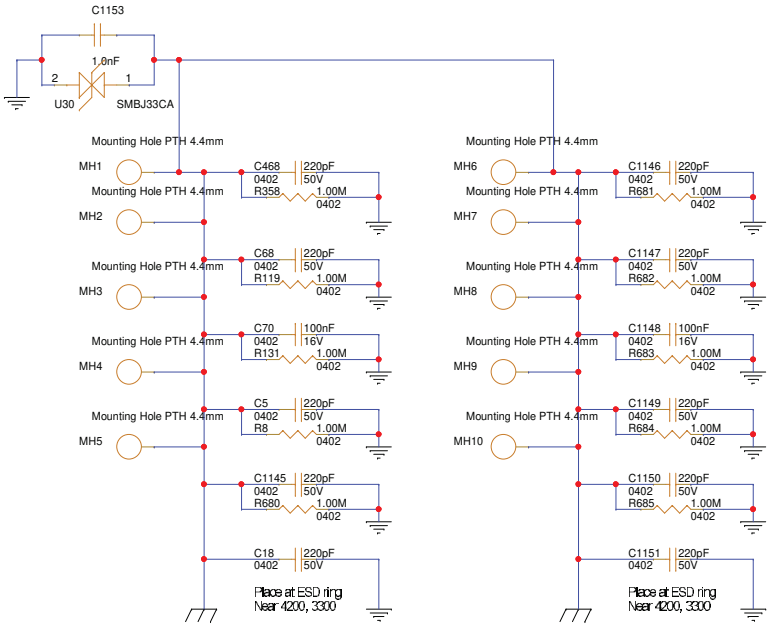

| | | | |
|---|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC<br>P25-RS485 & FASCIA CONNECTOR | |
| | | Document Number: D06285_15<br>Variant: <Variant Name> | Page: 25 of 28 |

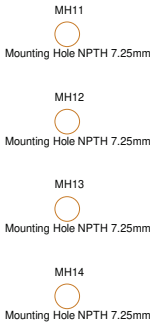


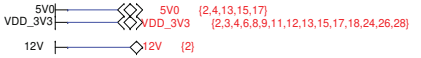

| | | | |
|---|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC P26-PCI, SATA, & SERDES | |
| | | Document Number: D06285_15 Variant: <Variant Name> | Page: 26 of 28 |

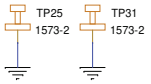


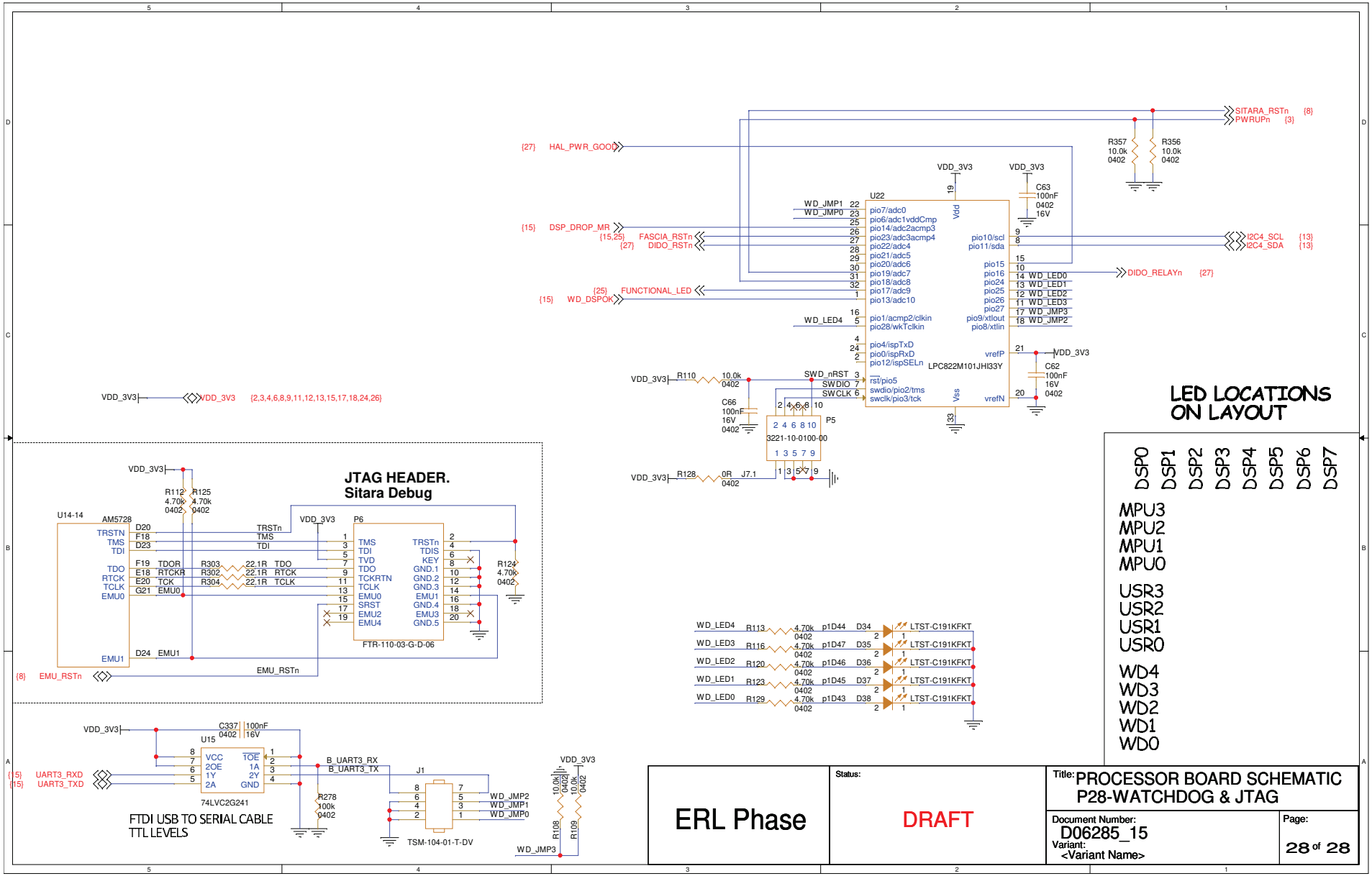




| | | | |
|---|---|---|---|
| ERL Phase | Status: DRAFT | Title: PROCESSOR BOARD SCHEMATIC P27-EXPANSION HEADERS & MOUNT | |
| | | Document Number: D06285_15 Variant: <Variant Name> | Page: 27 of 28 |


{27} HAL_PWR_GOOD
SITARA_RSTn {8}
PWRUPn {3}
R357 10.0k 0402
R356 10.0k 0402
VDD_3V3
U22
C63 100nF 0402 16V
WD_JMP1
WD_JMP0
{15} DSP_DROP_MR
{15,25} FASCIA_RSTn
{27} DIDO_RSTn
{25} FUNCTIONAL_LED
{15} WD_DSPOK
WD_LED4
pio7/adc0
pio6/adc1vddCmp
pio14/adc2acmp3
pio23/adc3acmp4
pio22/adc4
pio21/adc5
pio20/adc6
pio19/adc7
pio18/adc8
pio17/adc9
pio13/adc10
pio1/acmp2/clkin
pio28/wkTclkin
pio4/ispTxD
pio0/ispRxD
pio12/ispSELn
pio10/scl
pio11/sda
I2C4_SCL {13}
I2C4_SDA {13}
pio15
pio16
pio24
pio25
pio26
pio27
pio9/xtlout
pio8/xtlin
WD_LED0
WD_LED1
WD_LED2
WD_LED3
WD_JMP3
WD_JMP2
DIDO_RELAYn {27}
vrefP
vrefN
LPC822M101JHI33Y
Vdd
Vss
VDD_3V3 R110 10.0k 0402
SWD_nRST
SWDIO
SWCLK
rst/pio5
swdio/pio2/tms
swclk/pio3/tck
C66 100nF 16V 0402
P5
3221-10-0100-00
VDD_3V3 R128 0R 0402 J7.1
VDD_3V3 VDD_3V3 {2,3,4,6,8,9,11,12,13,15,17,18,24,26}
JTAG HEADER.
Sitara Debug
U14-14
AM5728
TRSTN
TMS
TDI
TDO
RTCK
TCLK
EMU0
EMU1
R112 4.70k 0402
R125 4.70k 0402
R303 22.1R TDO
R302 22.1R RTCK
R304 22.1R TCLK
R124 4.70k 0402
P6
TRSTn
TDIS
KEY
GND.1
GND.2
GND.3
GND.4
GND.5
EMU2
EMU3
EMU4
FTR-110-03-G-D-06
EMU_RSTn
{8} EMU_RSTn
WD_LED4 R113 4.70k 0402 p1D44 D34 LTST-C191KFKT
WD_LED3 R116 4.70k 0402 p1D47 D35 LTST-C191KFKT
WD_LED2 R120 4.70k 0402 p1D46 D36 LTST-C191KFKT
WD_LED1 R123 4.70k 0402 p1D45 D37 LTST-C191KFKT
WD_LED0 R129 4.70k 0402 p1D43 D38 LTST-C191KFKT
LED LOCATIONS ON LAYOUT
DSP0 DSP1 DSP2 DSP3 DSP4 DSP5 DSP6 DSP7
MPU3 MPU2 MPU1 MPU0
USR3 USR2 USR1 USR0
WD4 WD3 WD2 WD1 WD0
VDD_3V3 C337 100nF 0402 16V
U15
74LVC2G241
{15} UART3_RXD
{15} UART3_TXD
B_UART3_RX
B_UART3_TX
R278 100k 0402
J1
TSM-104-01-T-DV
WD_JMP2
WD_JMP1
WD_JMP0
WD_JMP3
R108 10.0k 0402
R109 10.0k 0402
FTDI USB TO SERIAL CABLE
TTL LEVELS
ERL Phase
Status:
DRAFT
Title: PROCESSOR BOARD SCHEMATIC
P28-WATCHDOG & JTAG
Document Number:
D06285_15
Variant:
<Variant Name>
Page:
28 of 28