TI Analog Solutions for Keystone II Family of SOCs

Compute and Consumer Electronics
Analog Systems Marketing

Overview

- Keystone II family overview and system details
- Power solutions for SOC Core and Aux rails
- Power sequencing solutions
- Clocks
- High speed solutions for PCIe, SAS, SATA, Ethernet
- Hot swap controllers, Current / Power Monitors and Temperature Sensors
- General purpose analog (ESD protection, Logic, etc)

Keystone II Family Overview and System Level Details

Keystone II SOCs Overview

Purpose-built servers

4 ARM A15
8 C66xDSP

4 ARM A15
2 C66xDSP

High performance computing
Media processing
Video analytics
Advanced video (H.265)
Gaming
Virtual Desktop Infrastructure
Radar

And many more…

Embedded enterprise

4 ARM A15
1 C66xDSP

1ARM A15
1 C66xDSP

Enterprise video
Digital video recording
Video analytics
Industrial imaging
Industrial control
Voice gateways
Avionics

And many more…

Power networking

4 ARM A15

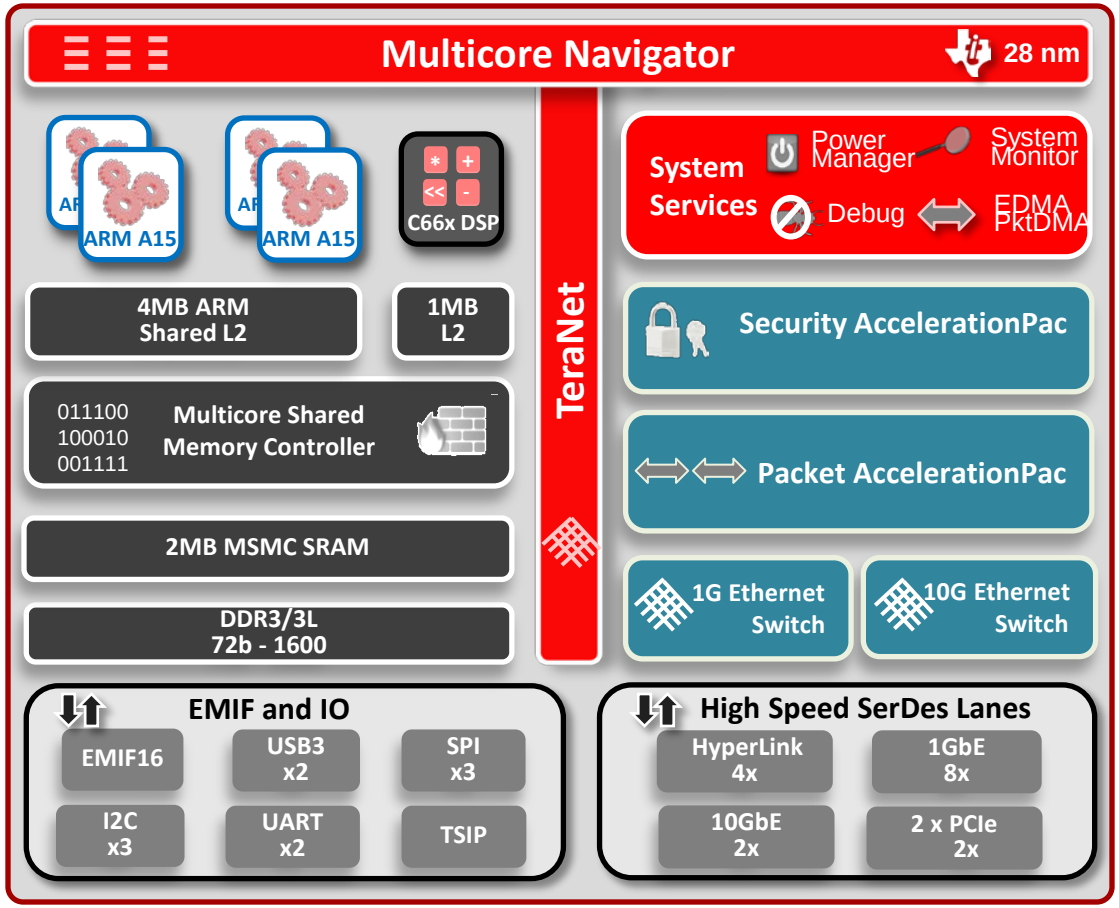
2 ARM A15

Cloud infrastructure
Networking control plane
Routers
Switches
Wireless transport
Wireless core network
Industrial sensor networks

And many more…

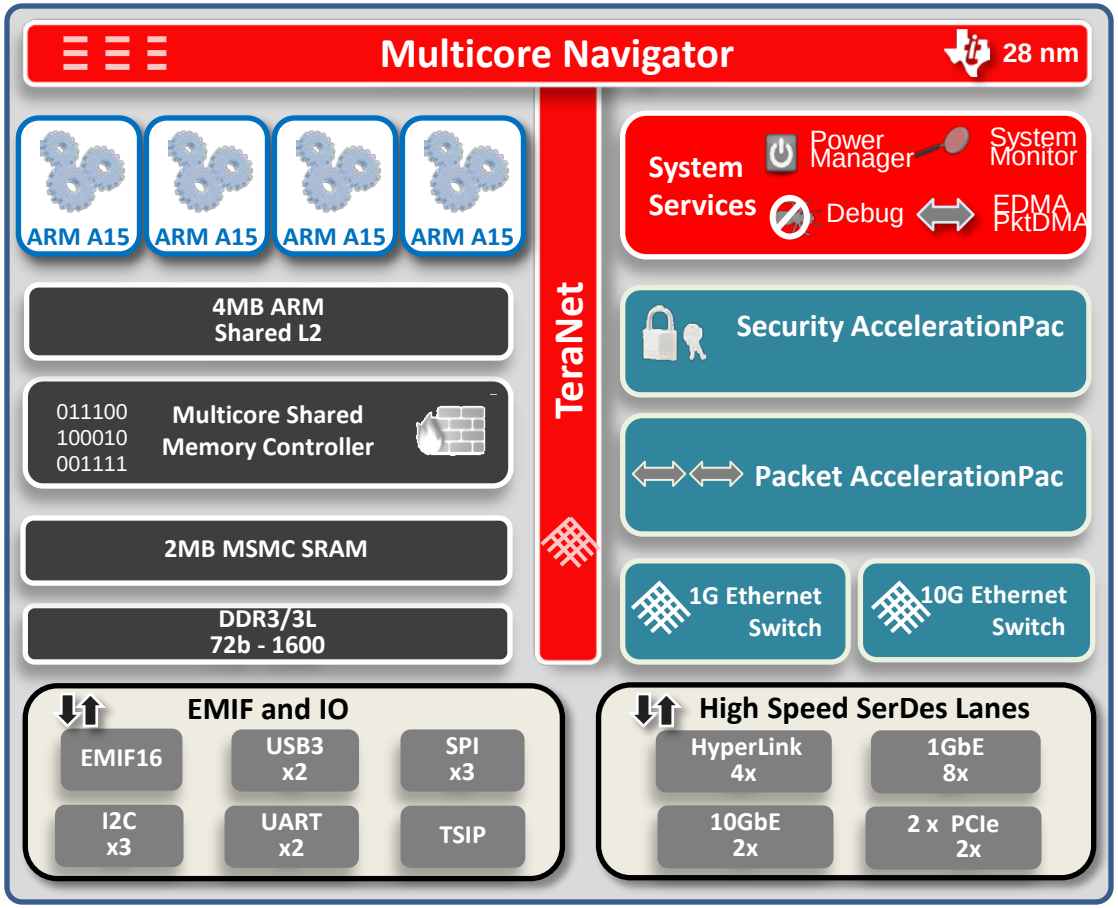
66AK2E05

- **Cores & Memory**
  - 1x C66x DSP up to 1.4GHz
  - 4x ARM Cortex A15 up to 1.4GHz
  - 6MB on chip memory w/ECC
  - 72 bit DDR3/3L w/ECC, 8GB addressable memory
- **Multicore Infrastructure**
  - Navigator with 16k queues, 3200 MIPS
  - 2.2 Tbps Network on Chip
  - 2.8 Tbps Shared Memory Controller
- **Switches**
  - 1GbE: 8 external port switch
  - 10GbE: 2 external port switch
- **Network, Transport**
  - 1.5 Mpps @ full wire-rate
  - Crypto: 4.8 Gbps, IPsec, SRTP
  - Accelerate layer 2,3 and transport
- **Connectivity – 98Gbps**
  - HyperLink(50), PCIe(20), 10GbE(20), 1GbE(8)
- **Power Optimized**
  - 8.6W typical use case at 55C for K2E05
- **Packaging:** 27mm x 27mm



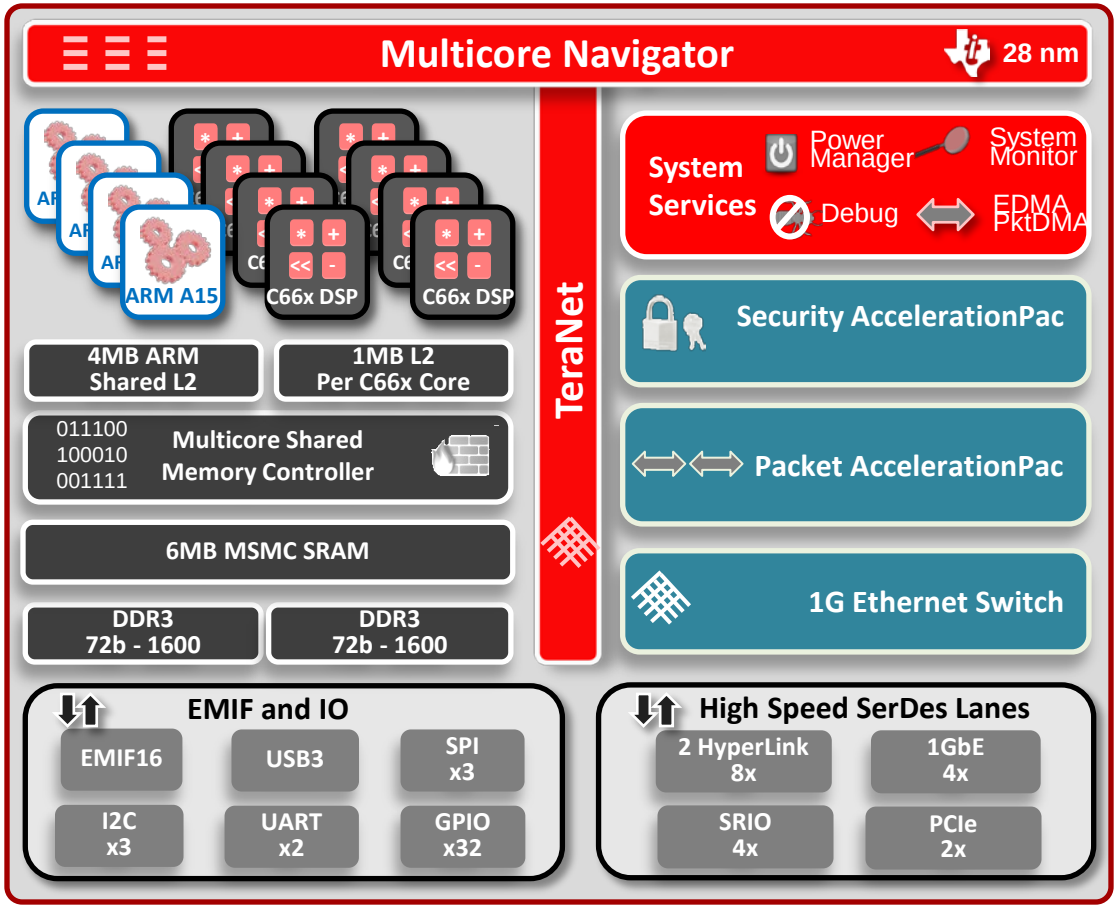
AM5K2E04/02

- **Cores & Memory**
  - 4x/2x Cortex A15 1.25GHz – 1.4GHz
  - 6MB on chip memory w/ECC
  - 72 bit DDR3/3L w/ECC, 8GB addressable memory
- **Multicore Infrastructure**
  - Navigator with 16k queues, 3200 MIPS
  - 2.2 Tbps Network on Chip
  - 2.8 Tbps Shared Memory Controller
- **Switches**
  - 1GbE: 8 external port switch
  - 10GbE: 2 external port switch **(only in AM5K2E04)**
- **Network, Transport**
  - 1.5 Mpps @ full wire-rate
  - Crypto: 4.8 Gbps, IPsec, SRTP
  - Accelerate layer 2,3 and transport
- **Connectivity – 94Gbps**
  - HyperLink(50), PCIe(20), 10GbE(20), 1GbE(4)
- **Power Optimized**
  - 8.1W typical use case at 55C for K2E04
- **Packaging**: 27mm x 27mm

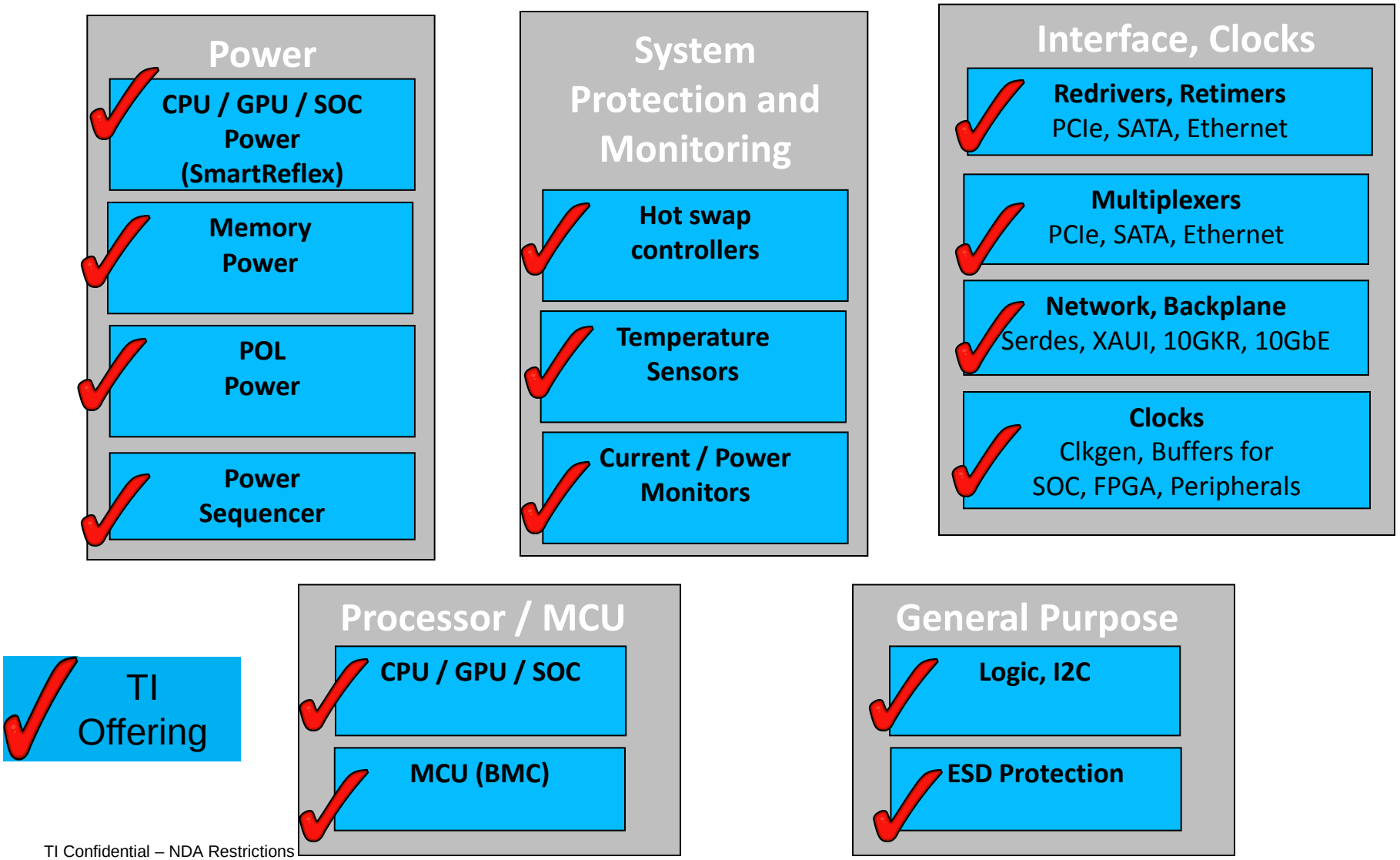


66AK2H12

- **Cores & Memory**
  - 8x C66x DSP up to 1.2GHz
  - 4x ARM Cortex A15 up to 1.4GHz
  - 18MB on chip memory w/ECC
  - 2 x 72 bit DDR3 w/ECC, 10GB addressable memory
- **Multicore Infrastructure**
  - Navigator with 16k queues, 3200 MIPS
  - 2.2 Tbps Network on Chip
  - 2.8 Tbps Shared Memory Controller
- **Switches**
  - 1GbE: 4 external port switch
- **Network, Transport**
  - 1.5 Mpps @ full wire-rate
  - Crypto: 6.4 Gbps, IPsec, SRTP
  - Accelerate layer 2,3 and transport
- **Connectivity – 134Gbps**
  - HyperLink(100), PCIe(10), SRIO(20), 1GbE(4)
- **Packaging:** 40mm x 40mm



What is On a Keystone II SOC Board?



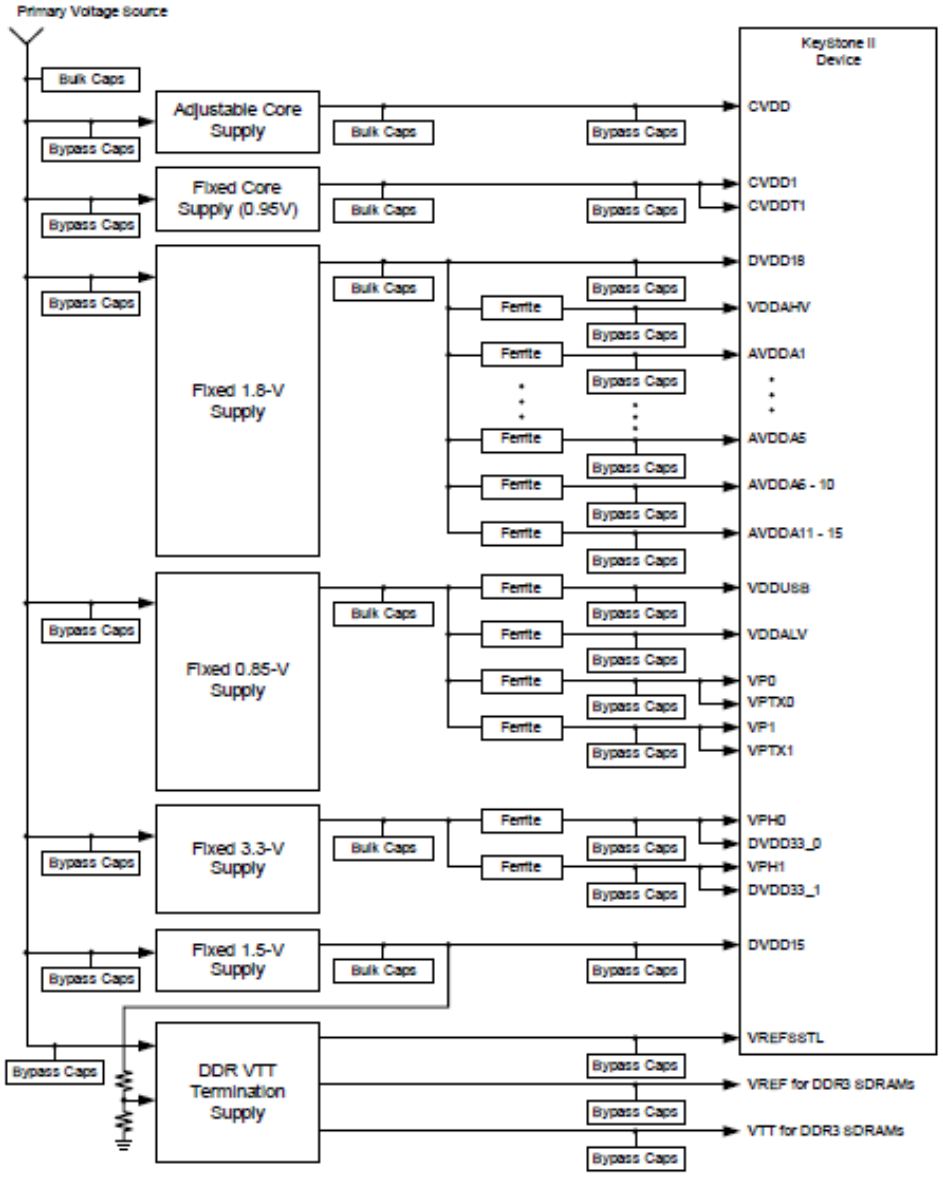
Power Solutions for

SOC Core and Aux Rails

www.ti.com/power

Keystone 2 Power Rails

- 6 rails provide the basic power requirements for all Keystone II devices
  - CVDD
  - CVDD1
  - 0.85V
  - 3.3V
  - 1.8V
  - 1.5V



Power for K2H

K2H12/14 Power Recommendations

Supply	VIN=12V – Quad SOC Implementation	VIN = 12V Single SOC Implementation
CVDD (AVS)	4x TPS53353/5 (up to 20A/30A)) + 4x LM10011	V/I/T Telemetry: TPS544C25 (VM) + LM10011 or TPS544C20 (DCAP2) + LM10011
CVDD1 (0.95V)	TPS53353	TPS54620/2
DVDD15* (1.5V) & VTT (0.75V)	2x TPS53353 + 2x TPS51200	TPS54325/6 + TPS51200
DVDD18** & VDDAHV (1.8V)	TPS53318	TPS54040
DVDD33**	TPS53318	TPS54040
VDDALV (0.85V)	TPS53318	TPS54225

* DVDD will need up to 1A additional for each attached memory device. (5 devices max supported)
** This 1.8V supply will normally be shared among other LVCMOS devices. Similarly the 3.3V supply for USB will normally be shared with other devices on the board.

TPS53318/19/53/55

8A/14A/20A/30A Sync Buck Converter with Eco-Mode™

Features

- V_{IN}: 4.5V to 18V
- V_{OUT}: 0.6V to 5.5V
- 0.8% (typ) 0.6V Reference
- D-CAP™ Mode - 100ns Transient Response
- Built-in LDO
- Dedicated EN Input and Power Good Output
- 8 Selectable Frequency Setting
- 1/2/4/8ms Selectable Internal Softstart
- OVP/UVP/OTP with Programmable OCP
- Supports Pre-Biased Start-Up

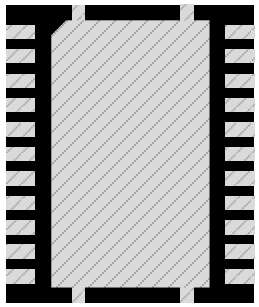
Benefits

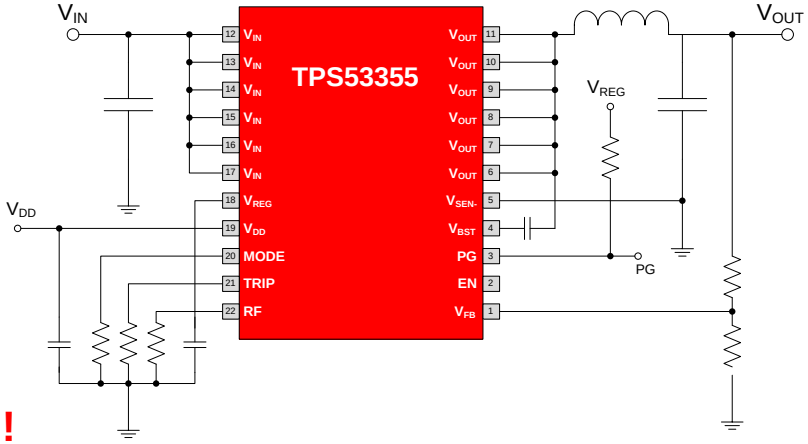
- Directly convert from 12V
- Supports the most common rail voltages
- Improves accuracy at point of load
- No loop compensation and save output caps
- No external bias voltage required
- Applications requiring sequencing
- Efficiency and cost optimization
- Sequential start-up to reduce in-rush current
- Load is fully protected
- Soft start-up over pre-biased output

Applications

- Servers
- Storage
- Embedded PCs, POS Terminals
- Switches, Routers

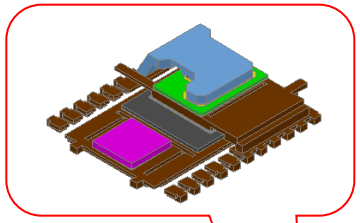
DQT - (PSON 22)
6mm x 5mm
Top View

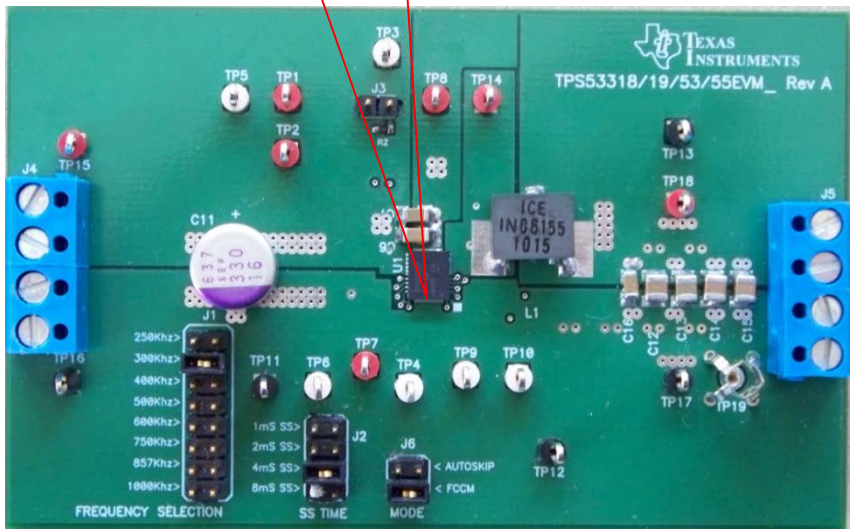


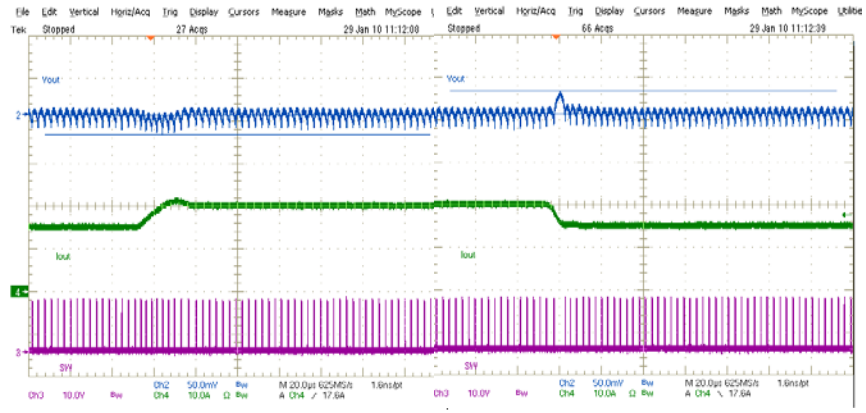


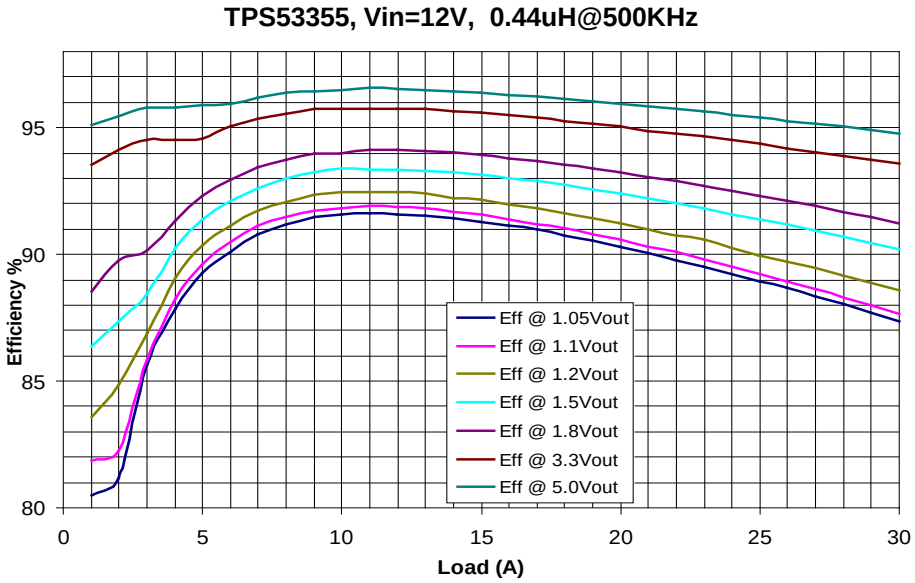
Pin to Pin Compatible!!!

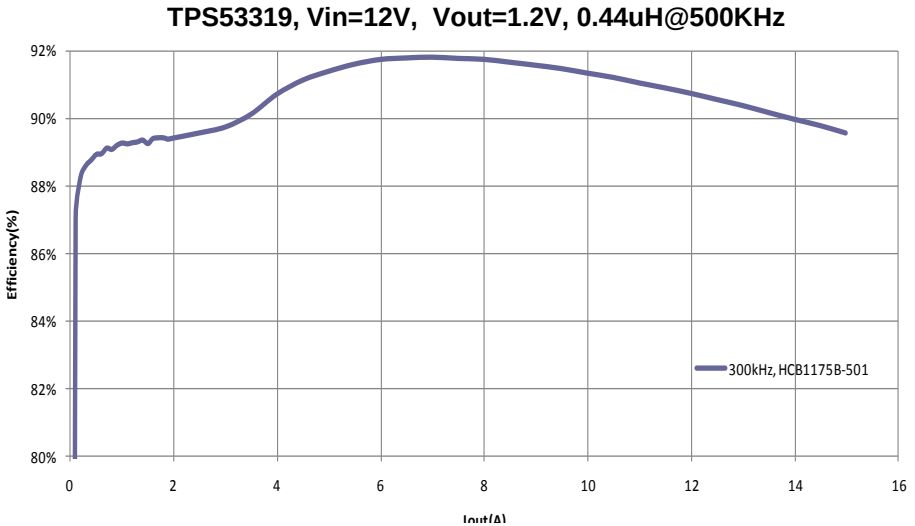
8A~30A Series Integrated FETs Switcher











Top 10 Reasons To Use TPS53318/19/53/55

- Best in class efficiency
- Save output caps, least BOM cost
- Insensitive to output capacitor type@value
- Easy design, no compensation
- Single rail input
- Small quiescent current and high efficiency
- Support Light Load, seamless DCM/CCM transition
- Upgrade designs from discrete controller TPS53219 with the same external components
- Fully protected: OVP/UVP/OTP and thermal and Rds,on compensated OCP with tight tolerance
- Pin to Pin compatible: 30A@TPS53355, 20A@TPS53353, 14A@ TPS53319 and 8A@TPS53318

Top Avatar (TPS544B25/C25)

4.5-18V 20A/30A Voltage Mode SWIFT with PMBus programmability and Voltage, Current and Temperature Telemetry

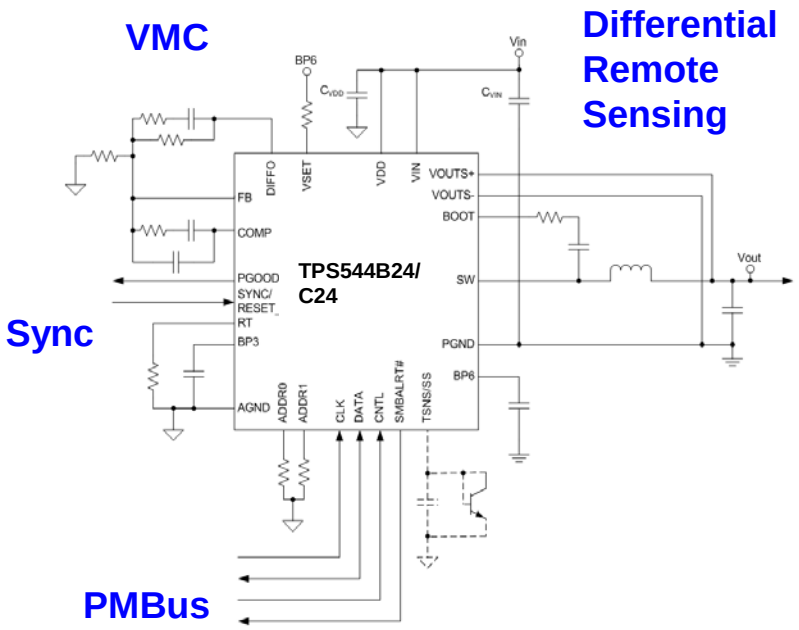
Samples: Now
RTM: 1Q2015

Features

- 4.5V to 18Vin, Vo 0.5 to 5.5 volts
- Programmable VOUT, AVS and Margining through PMBus
- Reference Voltage with 0.5% Accuracy from -40C to 125C junction temperature range
- Integrated NexFETs with senseFET Technology
- MOSFET Rds(on): HS/LS=5.5/2.0mohm
- Voltage Mode Control (VMC) with Input Feedforward
- Programmable Frequency 200kHz to 1MHz
- External Frequency Synchronization
- PMBus Interface
  - I, V, T Accurate Sensing
  - Programmable UVLO, Soft-start/stop, PGOOD
  - Programmable Thermally Compensated OCP, Output Over/Under Voltage and Overtemperature Protection and Fault Response
- Supports Pre-biased Output
- Differential Remote Sensing
- On Chip NVM
- 40-Pin 5x7 QFN Package

Applications

- Switchers/Routers/Wireless Infrastructure
- Cloud Computing/Server/Storage



TPS544B20/C20

4.5V to 18V Input, 20A/ 30A SWIFT™ Step-Down Converter with PMBus™

NEW!

Features

- Integrated 4.5/2mΩ NexFET™ Power Stage
- Programmable Settings and Configuration via PMBus Interface
- Adjustable Voltage via PMBus Interface
- Monitoring/Telemetry via PMBus Interface
- 0.6V to 5.5V Output with 0.5% Vref Accuracy
- D-CAP™/D-CAP2™ Mode Control Topology
- Differential Remote Sensing
- 250kHz to 1MHz Adjustable Frequency
- 5x7x1mm QFN Package

Benefits

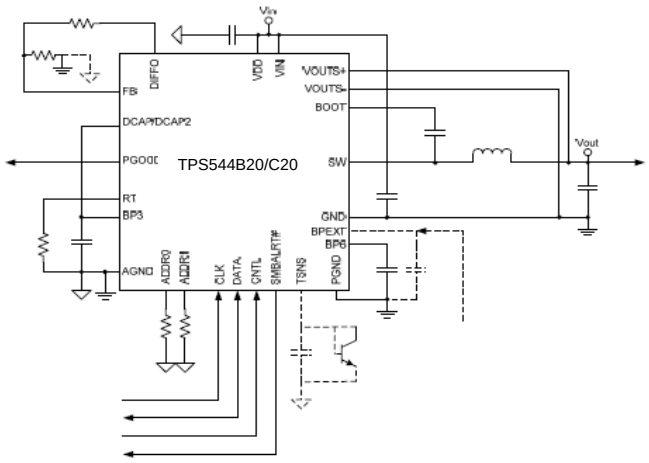
- >90% Efficiency at 12Vin/1.8Vout/30A @ 500KHz
- Set Over-Current & P-Good/UV/OV/OT Levels; UVLO; Soft-Start; Fault Responses; Ton/off Delays
- Trim Output Voltage & Control Margin Up/Down
- Accurately Sense Current, Voltage, & Temperature
- Ideal for Powering Advanced Processors
- No Loop Compensation with Cout Flexibility
- Accurate Voltage Over Long Routing Distances
- Optimize Design for High Efficiency or Small Size
- High Power Density Less than 200mm² total Area

Applications

- Cloud Computing, Server, Data Storage
- Wired and Wireless Infrastructure Equipment
- High Speed Switches & Routers
- Industrial Automated Test Equipment
- Point-of-Load Power for High-Current DSPs, FPGAs, and ASICs

Pin Compatible

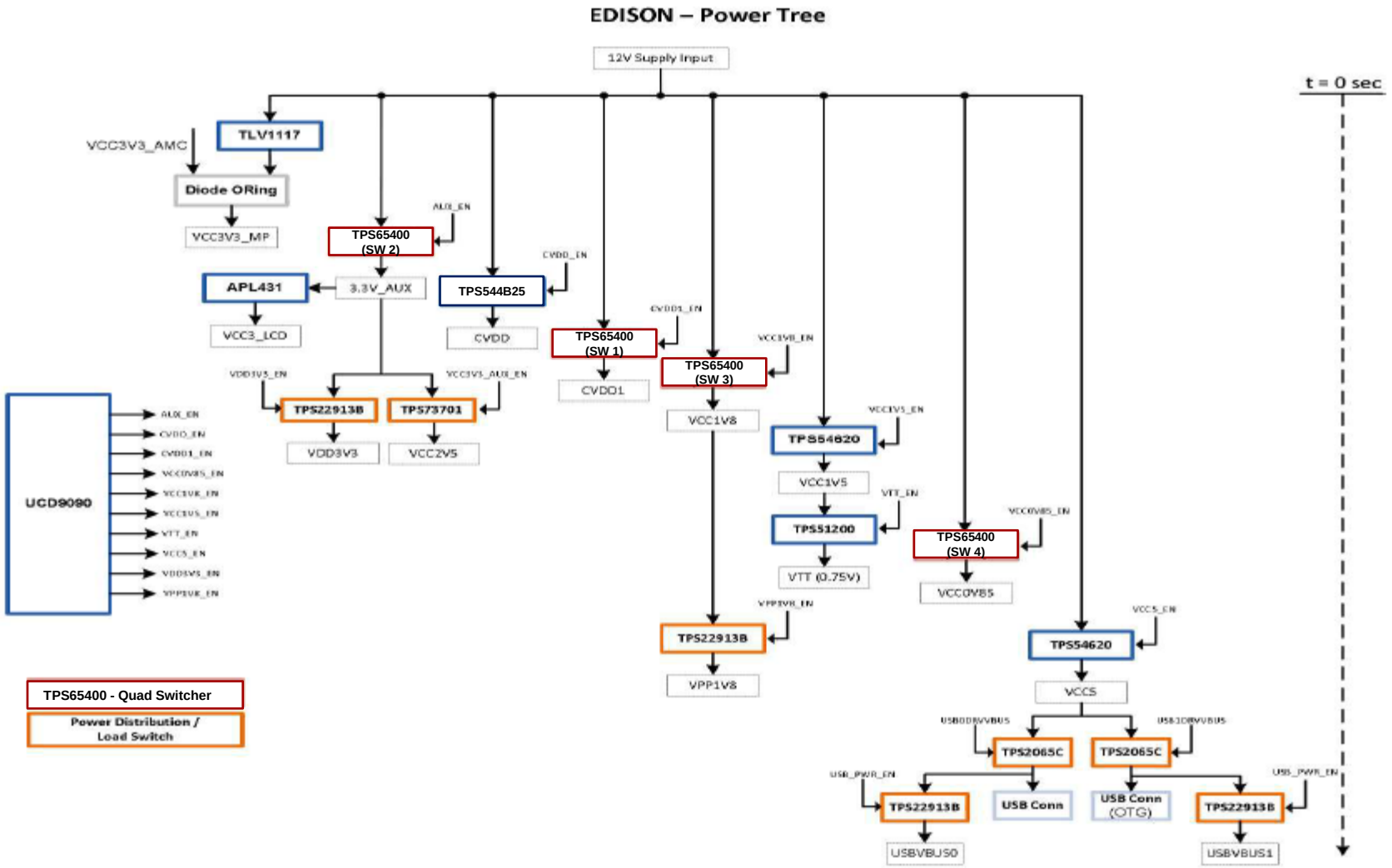
Device	Iout
TPS544B20	20-A
TPS544C20	30-A



Texas Instruments

Power for K2E

K2E05/02 Power Tree



K2E05/02 Power Recommendations

Supply	VIN = 12V Single SOC Implementation
CVDD (AVS)	TPS544B25
CVDD1 (0.95V)	TPS65400 (Sw 1)
DVDD15* (1.5V) & VTT (0.75V)	TPS54620 + TPS51200
DVDD18** & VDDAHV (1.8V)	TPS65400 (Sw 2)
DVDD33**	TPS65400 (Sw 3)
VDDALV (0.85V)	TPS65400 (Sw 4)

TPS544B25 is the identical catalog version of TPS544B24 on EVM

TPS54620

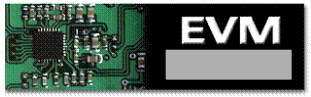
4.5V to 17V Input 6-A Synchronous Step Down SWIFT ™ DCDC Converter

Features

- Integrated Monolithic 26mΩ High Side and 19mΩ Low Side MOSFETs
- 200KHz to 1.6MHz Adjustable Switching Frequency
- 0.8V Reference with 1% Accuracy over Temperature
- Synchronizes to External Clock
- Integrated Tracking Function
- 3.5 x 3.5mm 14 pin QFN Package

Applications

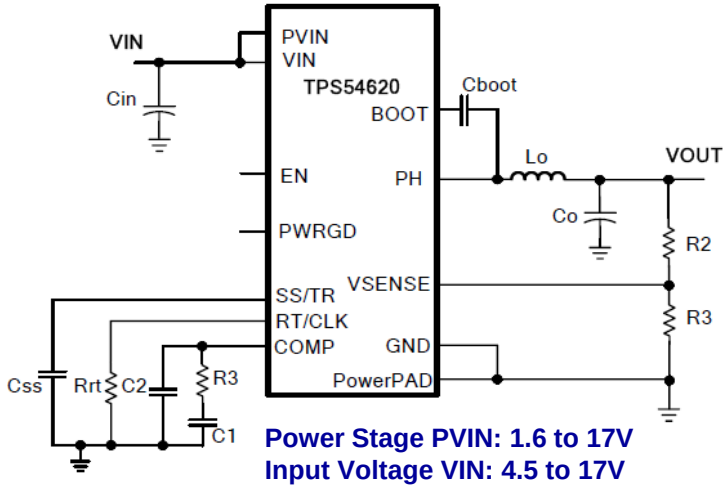
- Broadband, Networking & Communication Infrastructure
- Servers and Work Stations
- Compact PCI / PCI Express / PXI Express Applications



TPS54620EVM-374

Benefits

- 95% Peak Efficiency; Optimized for Low Output Voltages
- High Frequency Supports Small Output Inductor and Capacitor Size
- Ideal for Powering New Deep Sub-Micron DSPs, FPGAs, and ASICs
- Eliminates Beat Noise for Sensitive Applications
- Easily Implement Sequencing Schemes
- 60% Smaller Package than other 12V / 6A Converters with Integrated FETs



Power Stage PVIN: 1.6 to 17V
Input Voltage VIN: 4.5 to 17V

TPS51200

3A Source-Sink DDR Termination Regulator

Features

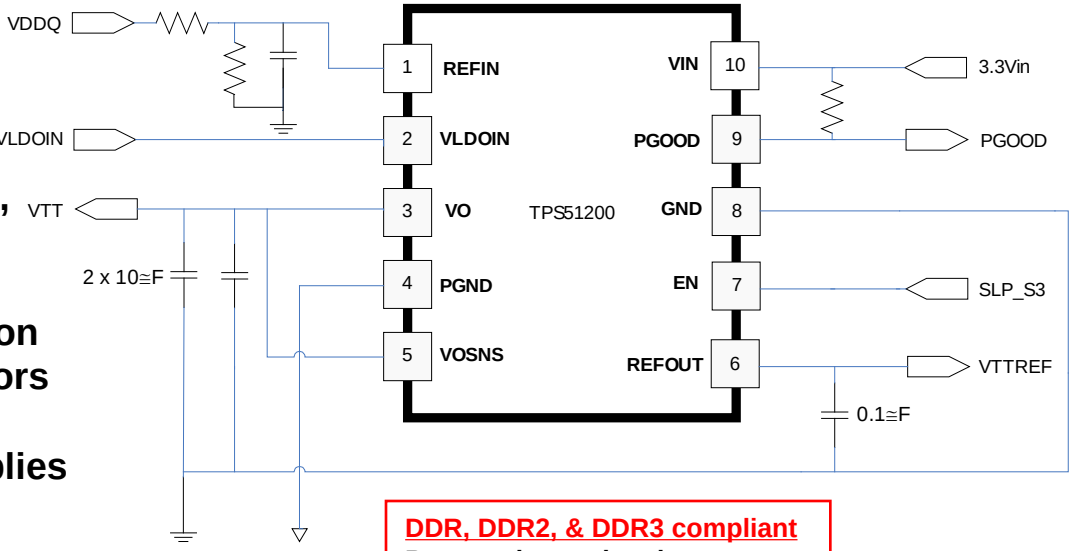
- Requires only 20uF of ceramic output capacitance
- Direct interface to S3 and sensing of S5 control signals
- Supports high-Z in S3 and soft-off in S5
- LDO input can be reduced to 1.2V
- SS, UVLO, OCL and thermal shutdown
- Enable input and Power Good output
- 10-pin SON package

Benefits

- Lower cost and size than competing parts requiring 600uF or more of electrolytic capacitance
- Ease of use
- Fewer external components and lower cost
- Lower power dissipation
- System protection
- Controlled turn-on and monitored output regulation
- Enables small form factor designs

Applications

- DDR, DDR2, DDR3, and low-power DDR3/DDR4 VTT Memory Termination
- Graphics Processors
- Core Supplies
- Chipset/RAM supplies as low as 0.5V



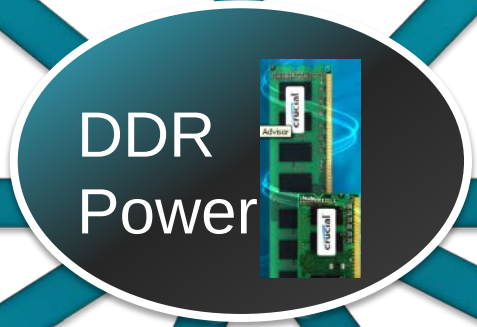
Low VIN Requirement
2.375V to 3.5V

PGOOD Output
Open drain Output to indicate VTT is within regulation

VTTREF sink and source
+/- 10mA

DDR, DDR2, & DDR3 compliant
Post package trimming to meet any DDR3 V_{TT} tolerance spec

DDR Memory Power Solutions



Highest-current LDO
3.3VIN – 3A
VTT
DDR2/DDR3/DDR3L/LPDDR3
TPS51200

Simplest LDO
5VIN - 3A
VTT
DDR2
TPS51100

Smallest LDO
Most Price Competitive
3.3V/5VIN - 2A
VTT
DDR3/DDR3L/LPDDR3
TPS51206

PWM + LDO
Most optimized for bulk caps
VDDQ and VTT
DDR3/DDR3L/LPDDR3
TPS51216

6A iFET
Highest-current/efficiency
VTT
DDR3/DDR3L/LPDDR3
TPS53317

PWM + LDO
Highest Power Density
Lowest BOM cost
VDDQ and VTT
DDR3/DDR3L/LPDDR3
TPS51916

PWM + LDO
Industrial temp range
VDDQ and VTT
DDR2/DDR3/DDR3L
TPS59116

8A/10A iFET
Industrial temp range
VDDQ
DDR2/DDR3/DDR3L/LPDDR3
TPS51362/7

PWM + LDO
Highest volume
Most Flexible
VDDQ and VTT
DDR2/DDR3/DDR3L
TPS51116

Power Sequencing for Keystone II

- There are 2 acceptable power up sequences for Keystone II devices outlined below.

Core Voltages Before I/O Voltages

K2E

1. CVDD
2. CVDD1, VDDAHV, AVDDAx, DVDD18
3. DVDD15
4. VDDALV, VDDUSBx, USBxVP, USBxVPTX
5. USBxDVDD33

K2H

1. CVDD
2. CVDD1, CVDDT1, VDDAHV, AVDDAx, DVDD18
3. DVDD15
4. VDDALV, VDDUSB, VP, VPTX
5. DVDD33

I/O Voltages before Core Voltages

K2E

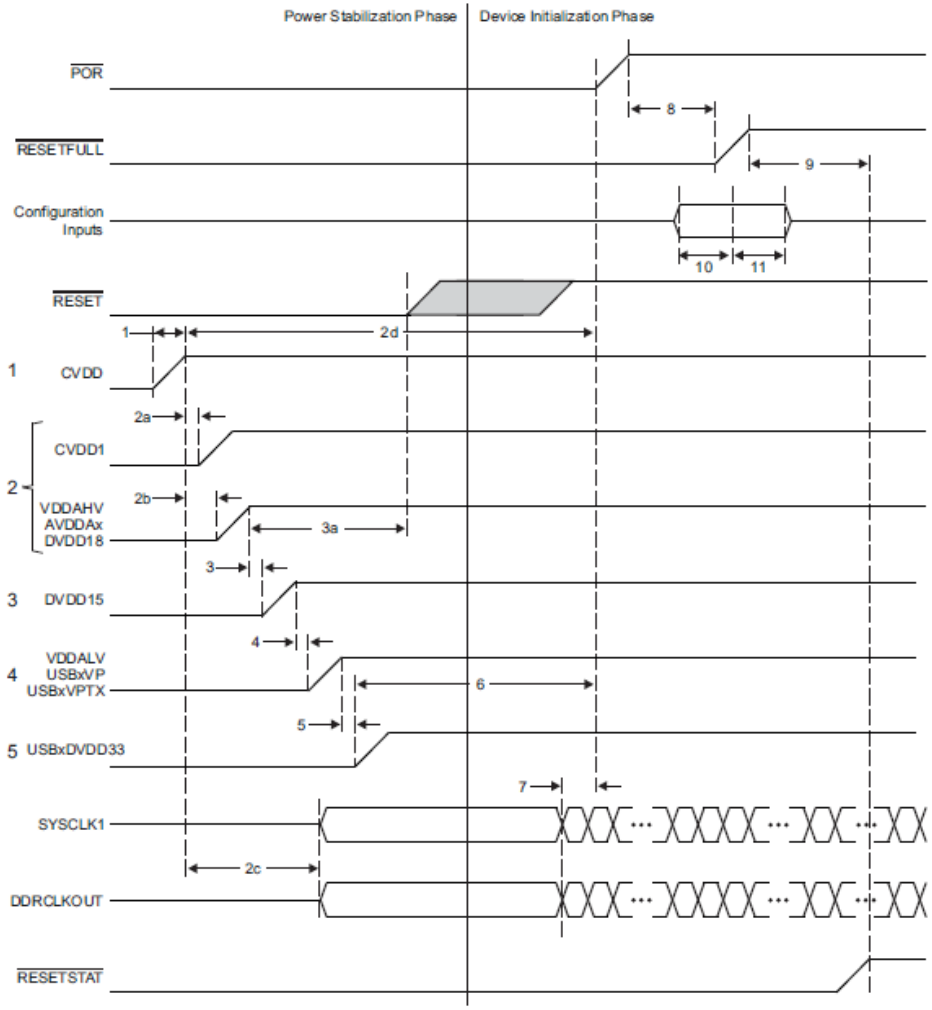
1. VDDAHV, AVDDAx, DVDD18
2. CVDD
3. CVDD1
4. DVDD15
5. VDDALV, VDDUSBx, USBxVP, USBxVPTX
6. USBxDVDD33

K2H

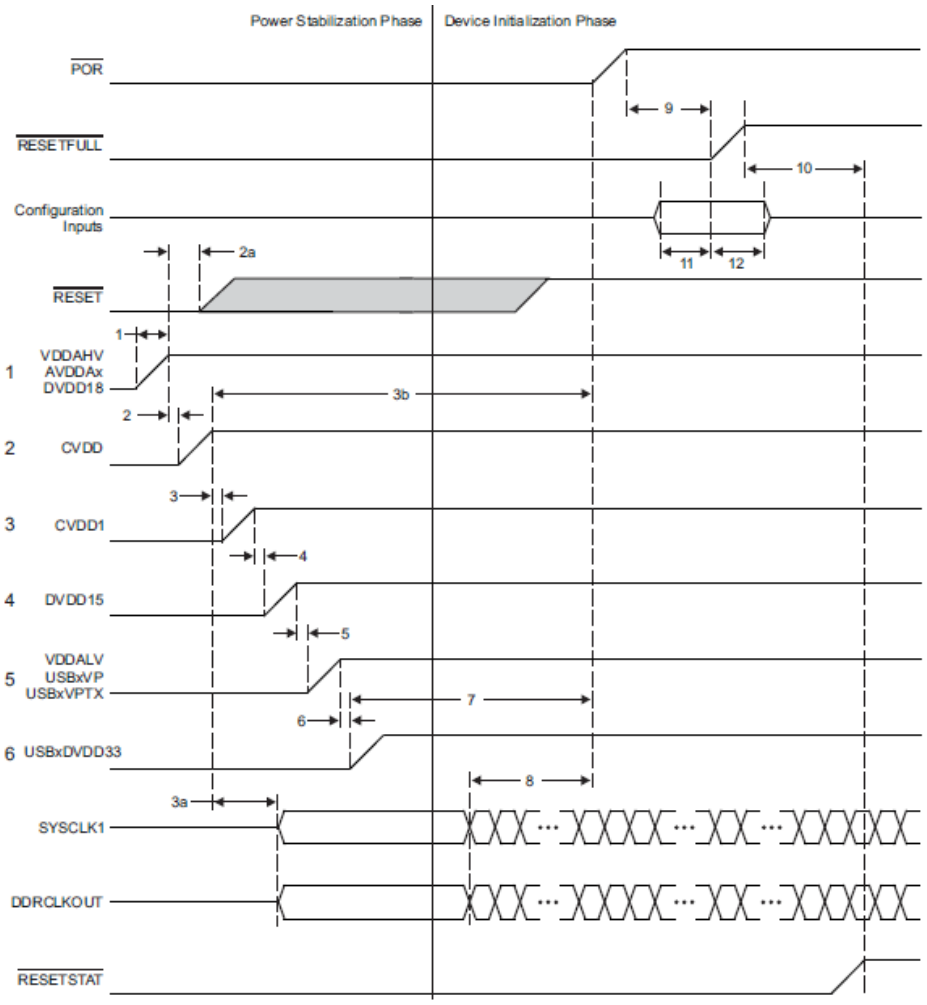
1. VDDAHV, AVDDAx, DVDD18
2. CVDD
3. CVDD1, CVDDT1
4. DVDD15
5. VDDALV, VDDUSB, VP, VPTX
6. DVDD33

Power Sequencing – Timing Diagrams

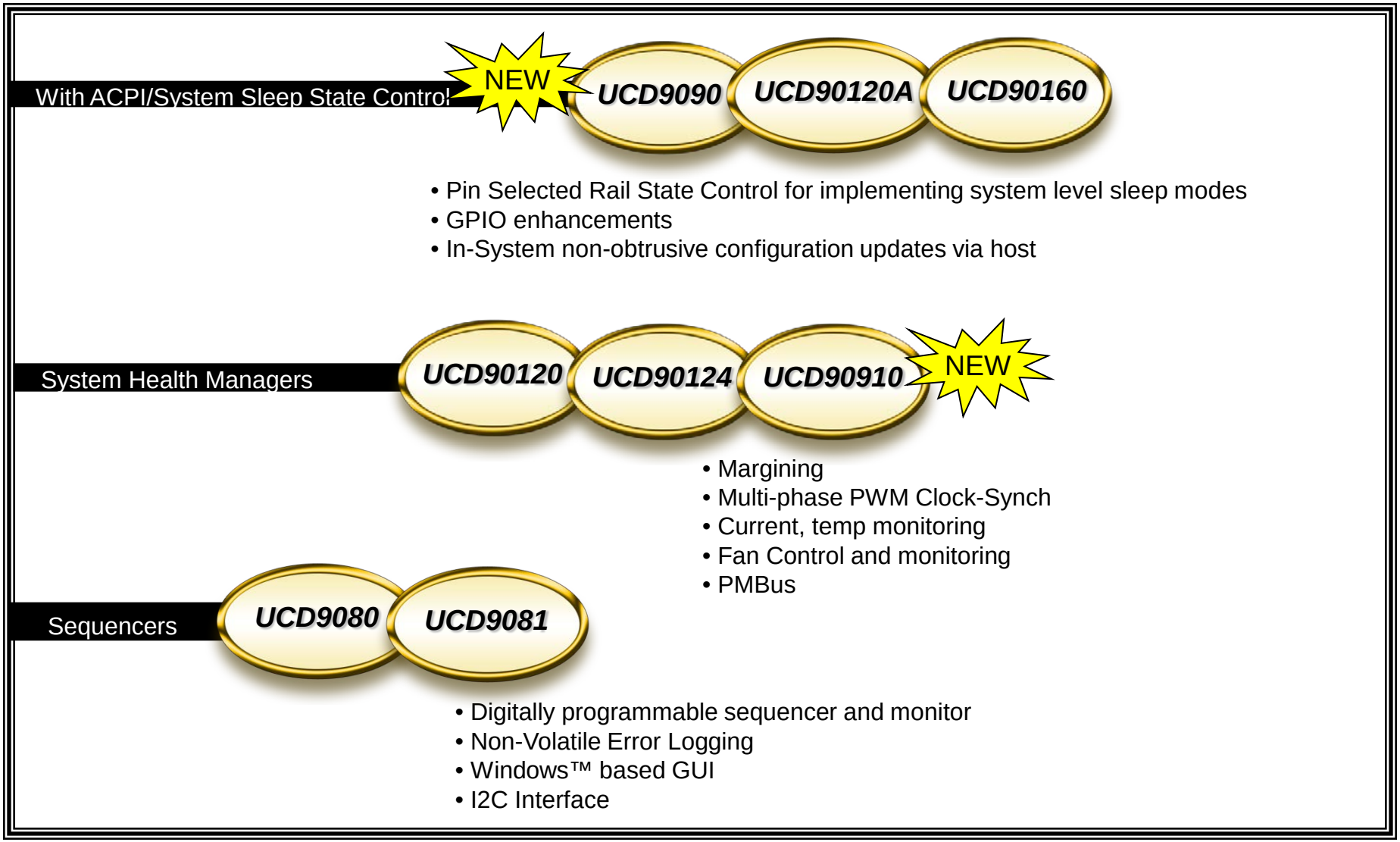
Core Before IO Power Sequencing



IO-Before-Core Power Sequencing



Power Sequencer/System Health Managers



Sequencer Portfolio Selection Guide

	UCD90160	UCD90120	UCD90120A	UCD90124	UCD9090	UCD90910	UCD9081
# Rails Sequenced	16	12	12	12	10	10	8
# of Monitor Inputs	16	13	13	13	11	13	8
ADC Ref Accuracy	0.5% Internal	0.5% Internal	0.5% Internal	0.5% Internal	0.5% Int ot Ext	0.5% Internal	External
Voltage Margining*	10	10	10	10	10	10	
Fan Control*	N/A	N/A	N/A	4	N/A	10	N/A
Multi-phase PWM clock outputs*	8	N/A	8	8	8	8	N/A
ACPI Sleep State Control	Yes	No	Yes	No	Yes	No	No
Current and Temp Monitor Scaling	No	Yes	Yes	Yes	Yes	Yes	No
NV Fault Logs	8	16	TBD	10	15	20	8
Other NV Logging	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	N/A
Max GPI/GPO*	8/16	8/12	8/12	8/12	8/10	8/10	0/4
Internal Temp Sensor	Yes	Yes	Yes	Yes	Yes	Yes	No
Communication and Programming I/F	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	I2C
Watchdog Timer	Yes	Yes	Yes	Yes	Yes	Yes	No
Package Type (size)	64-pin QFN(9x9)	64-pin QFN(9x9)	64-pin QFN(9x9)	64-pin QFN (9x9)	48-pin QFN (7x7)	64-pin QFN (9x9)	32-pin QFN (5x5)
Availability	Production	Production	Production	Production	Production	Production	Production

* Table shows the max number of each feature supported by each device. For example, the UCD90124 has 12 PWM pins used as any combination of margining, PWM, fan control, or GPIO up to the max listed. See data sheets for details.

UCD9090: 10-Rail Sequencer and System Health Monitor with ACPI System Sleep State Control

Features

- **Sequence, Monitor, and Margin up** to 10 Rails
- Independent Turn and Turn off dependencies
- Dependencies on time, parent rails, GPIs, and I2C commands
- Flexible GPIO configuration with BOOLEAN Logic capability
- 11 ADC Inputs with user settable scale factors for detecting voltage (OV/UV), current(OC/UC), or temp faults
- 6 optional comparators for fault response in < 80 us
- Respond to faults by configuring retries, shutdown delays, re- sequencing and groups of rails to shutdown
- **Non-Volatile fault and peak logging**
- Simultaneously **margin/trim** up to 10 rails using PWM outputs and I2C commands
- Up to 8 multi-phase PWM clock outputs
- Easy-to-use **Fusion Digital Power Designer GUI**
- JTAG and PMBus interfaces provide flexible options for in-system host communication and configuration
- **Pin Selected Sleep State control for use with ACPI or similar system power specifications**

Applications

- Server/Storage Systems
- Communication Infrastructure
- Industrial/ATE
- Embedded Computing

Benefits

- Flexibility sequencing requirements supports most possible sequencing scenarios
- Detect power supply warnings and faults and store to non-volatile memory for failure analysis
- Monitor voltage, current and temp in actual system units to eliminate host software scaling
- Closed-Loop Margining for corner testing of power supplies allows designers to identify possible system reliability issues
- Multi-phase PWM outputs eliminate need for separate chip to synch switch mode power supplies
- ACPI sleep state control allows host to shut down rails that are not in use and conserve system power
- TI's ***Fusion Digital Power GUI*** eliminates need to write code