TI Analog Solutions for Keystone II Family of SOCs

Compute and Consumer Electronics
Analog Systems Marketing

Overview

- Keystone II family overview and system details
- Power solutions for SOC Core and Aux rails
- Power sequencing solutions
- Clocks
- High speed solutions for PCIe, SAS, SATA, Ethernet
- Hot swap controllers, Current / Power Monitors and Temperature Sensors
- General purpose analog (ESD protection, Logic, etc)

Keystone II Family Overview and System Level Details

Keystone II SOCs Overview

Purpose-built servers

4 ARM A15
8 C66xDSP

4 ARM A15
2 C66xDSP

High performance computing
Media processing
Video analytics
Advanced video (H.265)
Gaming
Virtual Desktop Infrastructure
Radar

And many more…

Embedded enterprise

4 ARM A15
1 C66xDSP

1ARM A15
1 C66xDSP

Enterprise video
Digital video recording
Video analytics
Industrial imaging
Industrial control
Voice gateways
Avionics

And many more…

Power networking

4 ARM A15

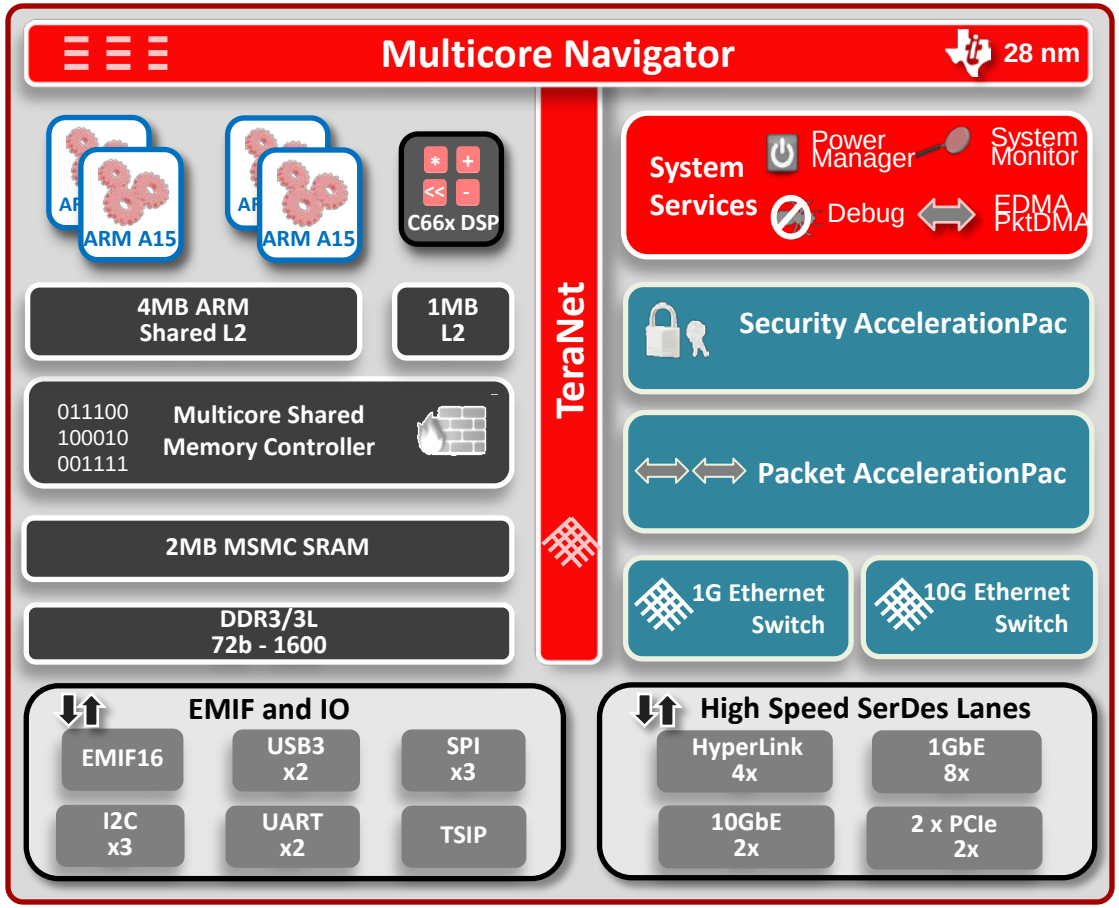
2 ARM A15

Cloud infrastructure
Networking control plane
Routers
Switches
Wireless transport
Wireless core network
Industrial sensor networks

And many more…

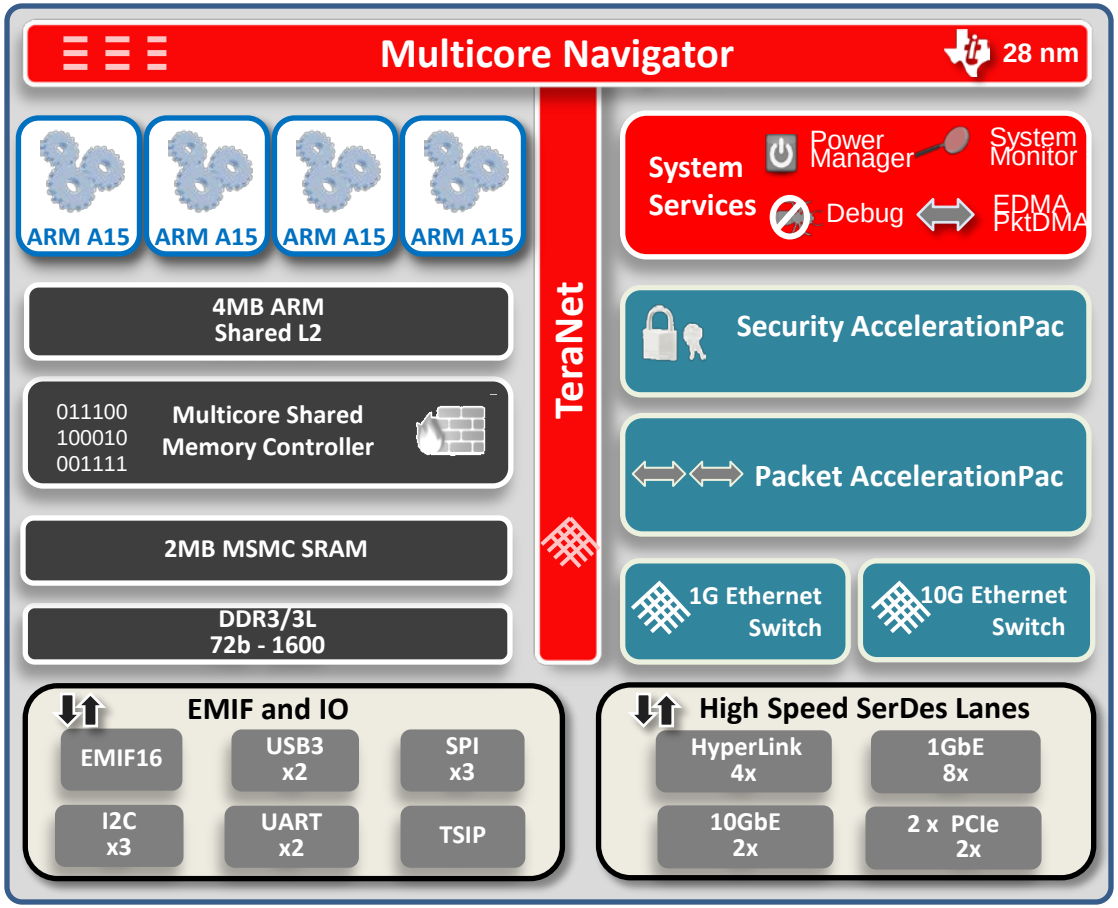
66AK2E05

- **Cores & Memory**
  - 1x C66x DSP up to 1.4GHz
  - 4x ARM Cortex A15 up to 1.4GHz
  - 6MB on chip memory w/ECC
  - 72 bit DDR3/3L w/ECC, 8GB addressable memory
- **Multicore Infrastructure**
  - Navigator with 16k queues, 3200 MIPS
  - 2.2 Tbps Network on Chip
  - 2.8 Tbps Shared Memory Controller
- **Switches**
  - 1GbE: 8 external port switch
  - 10GbE: 2 external port switch
- **Network, Transport**
  - 1.5 Mpps @ full wire-rate
  - Crypto: 4.8 Gbps, IPsec, SRTP
  - Accelerate layer 2,3 and transport
- **Connectivity – 98Gbps**
  - HyperLink(50), PCIe(20), 10GbE(20), 1GbE(8)
- **Power Optimized**
  - 8.6W typical use case at 55C for K2E05
- **Packaging:** 27mm x 27mm



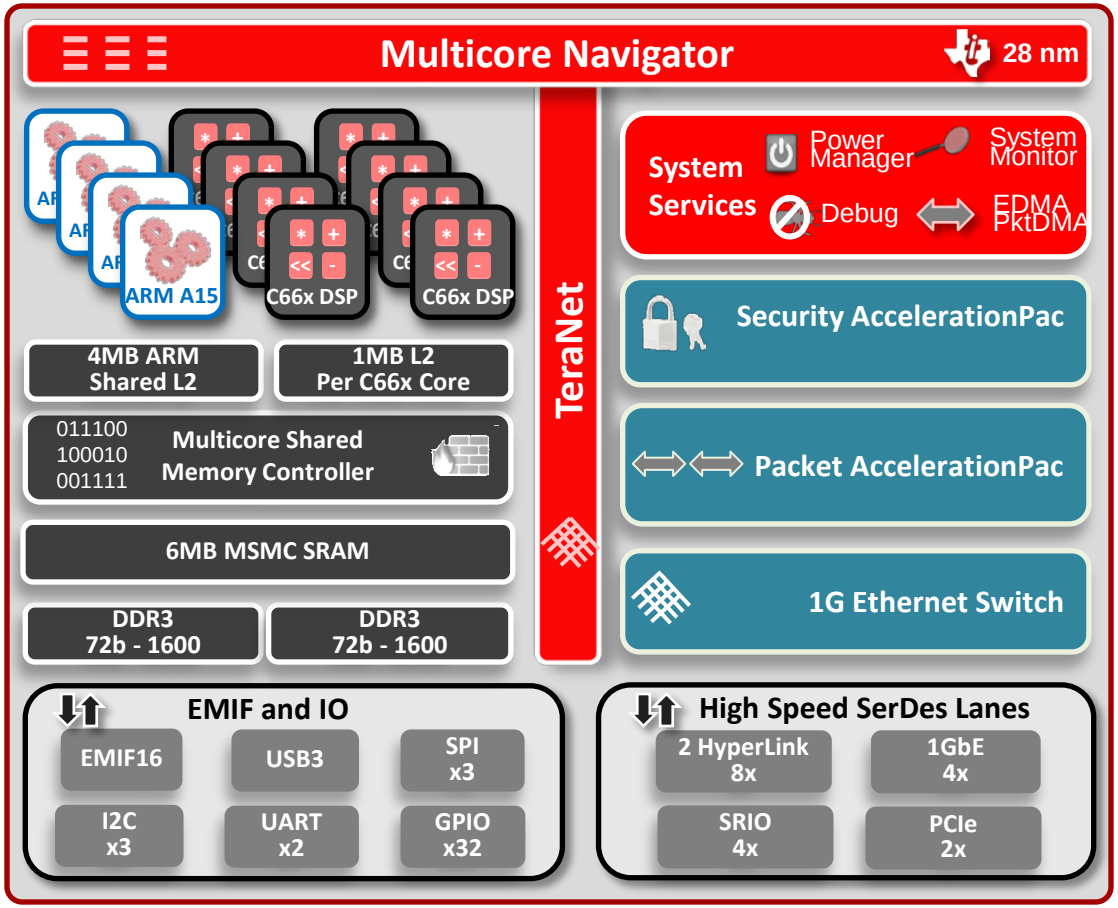
AM5K2E04/02

- **Cores & Memory**
  - 4x/2x Cortex A15 1.25GHz – 1.4GHz
  - 6MB on chip memory w/ECC
  - 72 bit DDR3/3L w/ECC, 8GB addressable memory
- **Multicore Infrastructure**
  - Navigator with 16k queues, 3200 MIPS
  - 2.2 Tbps Network on Chip
  - 2.8 Tbps Shared Memory Controller
- **Switches**
  - 1GbE: 8 external port switch
  - 10GbE: 2 external port switch **(only in AM5K2E04)**
- **Network, Transport**
  - 1.5 Mpps @ full wire-rate
  - Crypto: 4.8 Gbps, IPsec, SRTP
  - Accelerate layer 2,3 and transport
- **Connectivity – 94Gbps**
  - HyperLink(50), PCIe(20), 10GbE(20), 1GbE(4)
- **Power Optimized**
  - 8.1W typical use case at 55C for K2E04
- **Packaging**: 27mm x 27mm

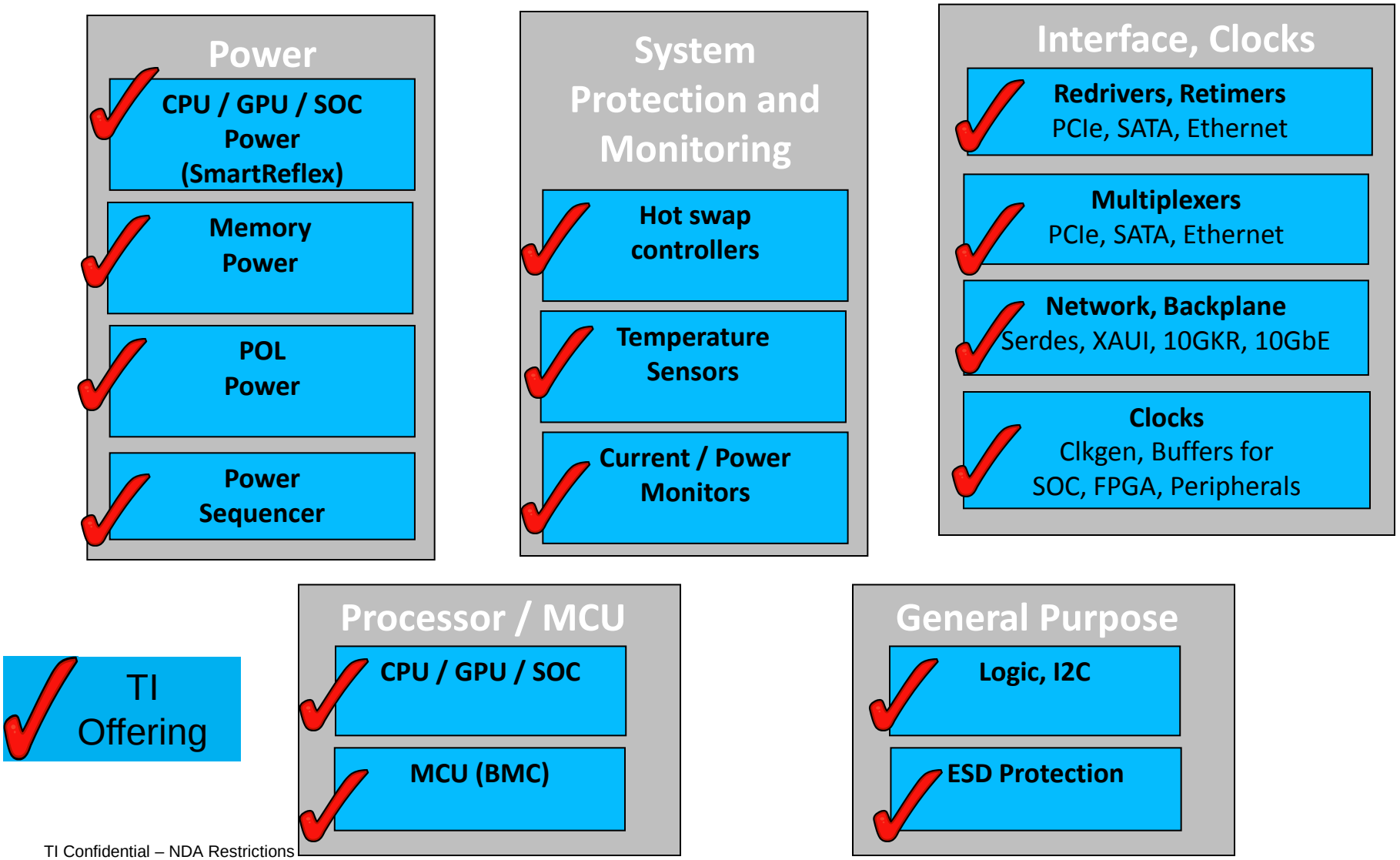


66AK2H12

- **Cores & Memory**
  - 8x C66x DSP up to 1.2GHz
  - 4x ARM Cortex A15 up to 1.4GHz
  - 18MB on chip memory w/ECC
  - 2 x 72 bit DDR3 w/ECC, 10GB addressable memory
- **Multicore Infrastructure**
  - Navigator with 16k queues, 3200 MIPS
  - 2.2 Tbps Network on Chip
  - 2.8 Tbps Shared Memory Controller
- **Switches**
  - 1GbE: 4 external port switch
- **Network, Transport**
  - 1.5 Mpps @ full wire-rate
  - Crypto: 6.4 Gbps, IPsec, SRTP
  - Accelerate layer 2,3 and transport
- **Connectivity – 134Gbps**
  - HyperLink(100), PCIe(10), SRIO(20), 1GbE(4)
- **Packaging:** 40mm x 40mm



What is On a Keystone II SOC Board?



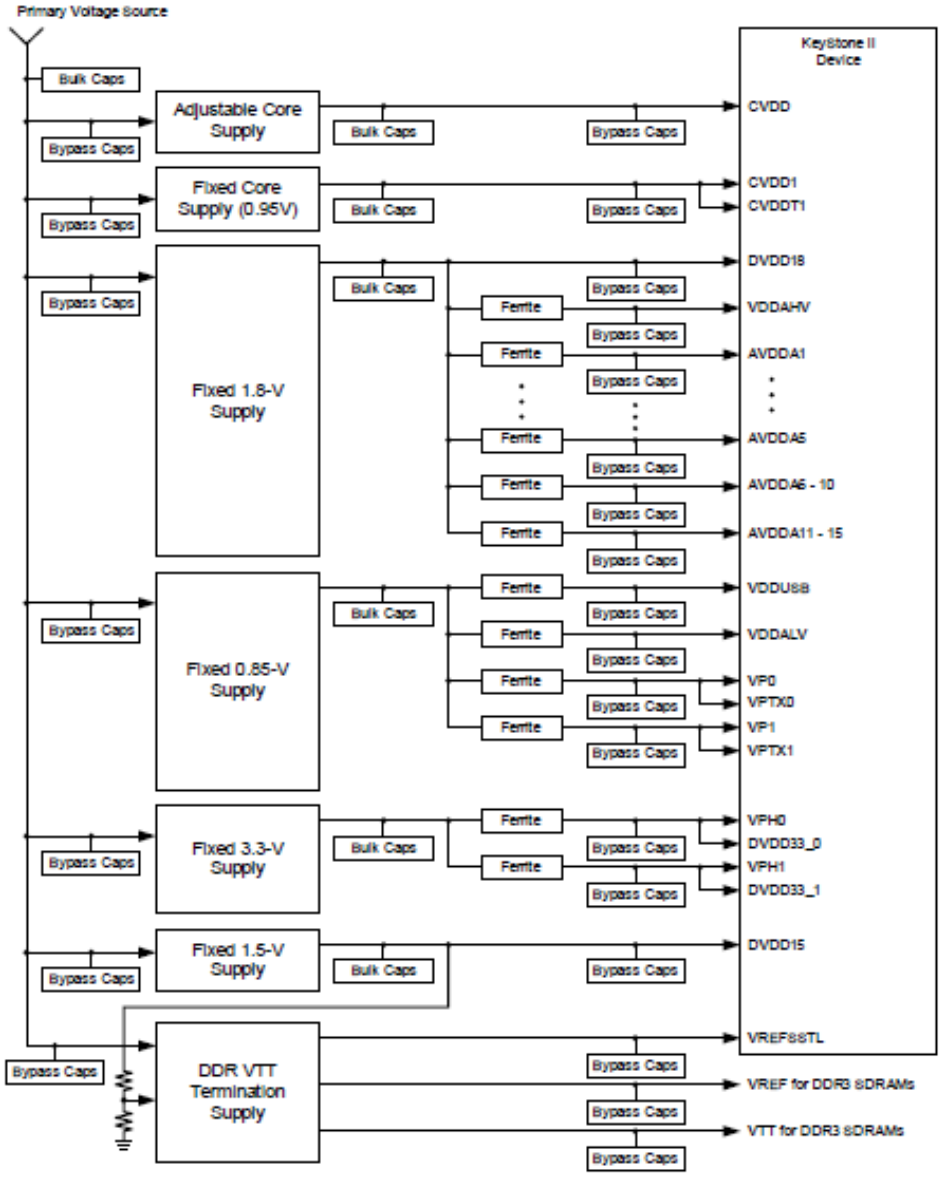
Power Solutions for

SOC Core and Aux Rails

www.ti.com/power

Keystone 2 Power Rails

- 6 rails provide the basic power requirements for all Keystone II devices
  - CVDD
  - CVDD1
  - 0.85V
  - 3.3V
  - 1.8V
  - 1.5V



Power for K2H

K2H12/14 Power Recommendations

Supply	VIN=12V – Quad SOC Implementation	VIN = 12V Single SOC Implementation
CVDD (AVS)	4x TPS53353/5 (up to 20A/30A)) + 4x LM10011	V/I/T Telemetry: TPS544C25 (VM) + LM10011 or TPS544C20 (DCAP2) + LM10011
CVDD1 (0.95V)	TPS53353	TPS54620/2
DVDD15* (1.5V) & VTT (0.75V)	2x TPS53353 + 2x TPS51200	TPS54325/6 + TPS51200
DVDD18** & VDDAHV (1.8V)	TPS53318	TPS54040
DVDD33**	TPS53318	TPS54040
VDDALV (0.85V)	TPS53318	TPS54225

* DVDD will need up to 1A additional for each attached memory device. (5 devices max supported)
** This 1.8V supply will normally be shared among other LVCMOS devices. Similarly the 3.3V supply for USB will normally be shared with other devices on the board.

TPS53318/19/53/55

8A/14A/20A/30A Sync Buck Converter with Eco-Mode™

Features

- V_{IN}: 4.5V to 18V
- V_{OUT}: 0.6V to 5.5V
- 0.8% (typ) 0.6V Reference
- D-CAP™ Mode - 100ns Transient Response
- Built-in LDO
- Dedicated EN Input and Power Good Output
- 8 Selectable Frequency Setting
- 1/2/4/8ms Selectable Internal Softstart
- OVP/UVP/OTP with Programmable OCP
- Supports Pre-Biased Start-Up

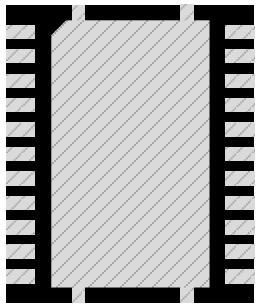
Benefits

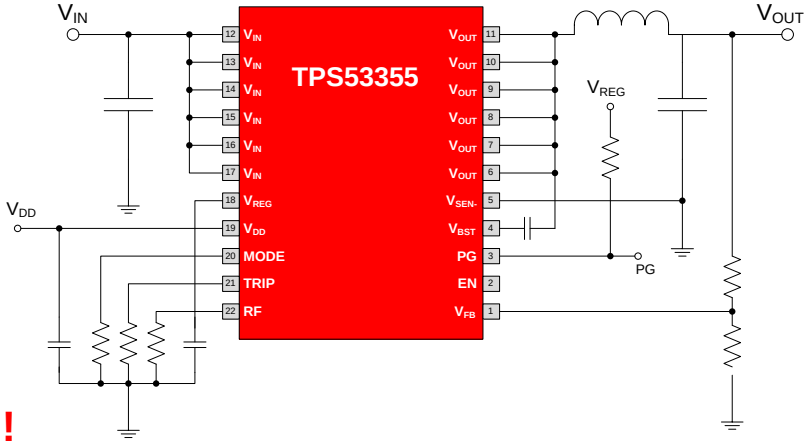
- Directly convert from 12V
- Supports the most common rail voltages
- Improves accuracy at point of load
- No loop compensation and save output caps
- No external bias voltage required
- Applications requiring sequencing
- Efficiency and cost optimization
- Sequential start-up to reduce in-rush current
- Load is fully protected
- Soft start-up over pre-biased output

Applications

- Servers
- Storage
- Embedded PCs, POS Terminals
- Switches, Routers

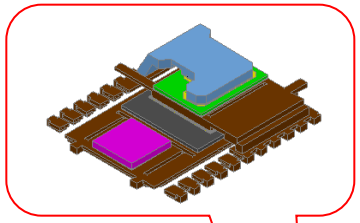
DQT - (PSON 22)
6mm x 5mm
Top View

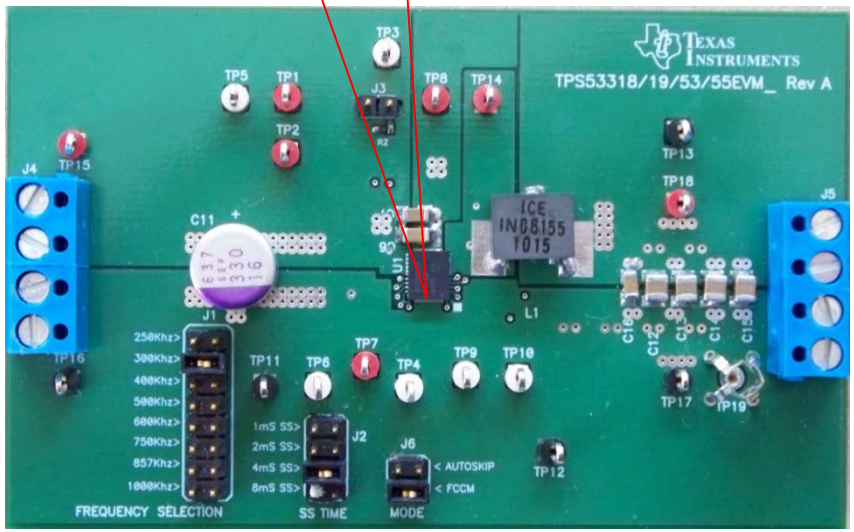


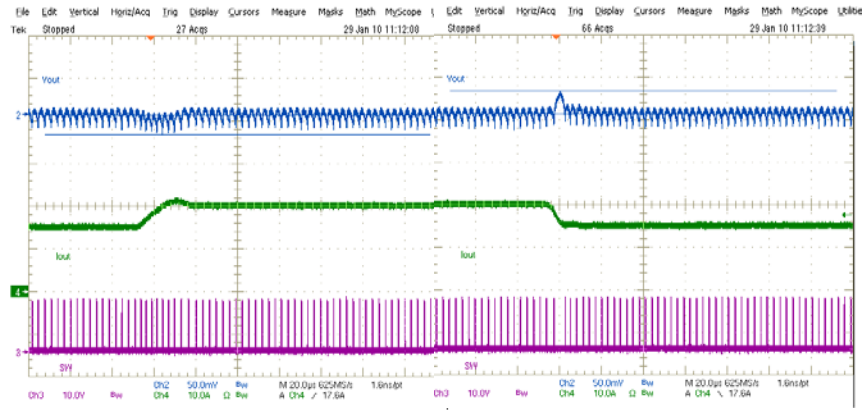


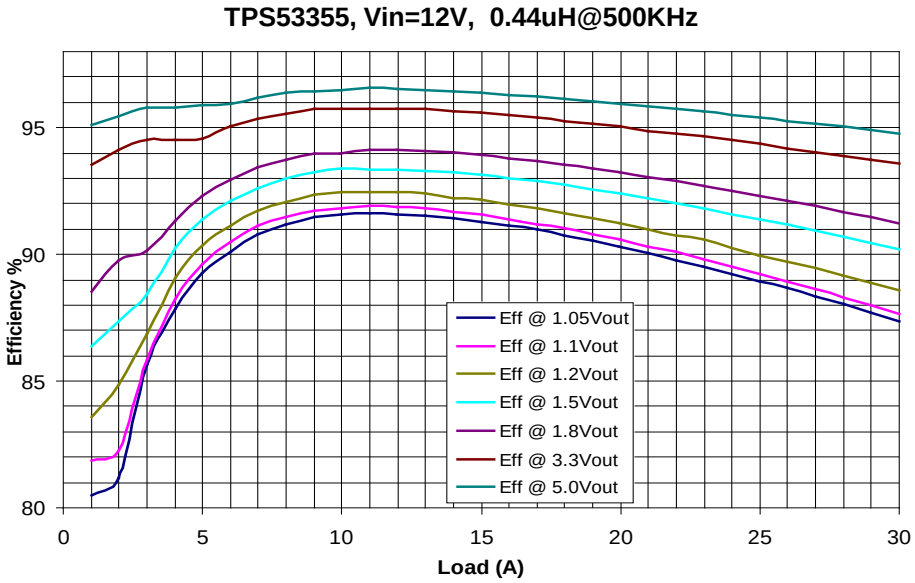
Pin to Pin Compatible!!!

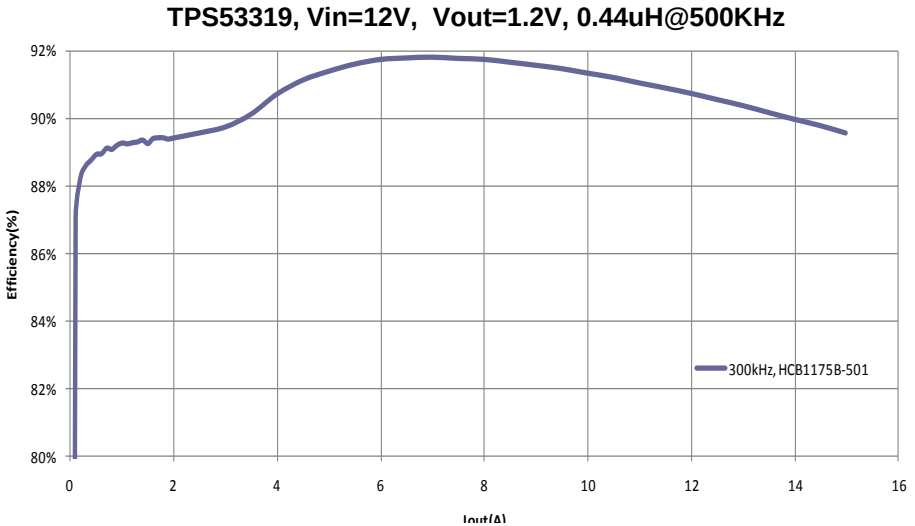
8A~30A Series Integrated FETs Switcher











Top 10 Reasons To Use TPS53318/19/53/55

- Best in class efficiency
- Save output caps, least BOM cost
- Insensitive to output capacitor type@value
- Easy design, no compensation
- Single rail input
- Small quiescent current and high efficiency
- Support Light Load, seamless DCM/CCM transition
- Upgrade designs from discrete controller TPS53219 with the same external components
- Fully protected: OVP/UVP/OTP and thermal and Rds,on compensated OCP with tight tolerance
- Pin to Pin compatible: 30A@TPS53355, 20A@TPS53353, 14A@ TPS53319 and 8A@TPS53318

Top Avatar (TPS544B25/C25)

4.5-18V 20A/30A Voltage Mode SWIFT with PMBus programmability and Voltage, Current and Temperature Telemetry

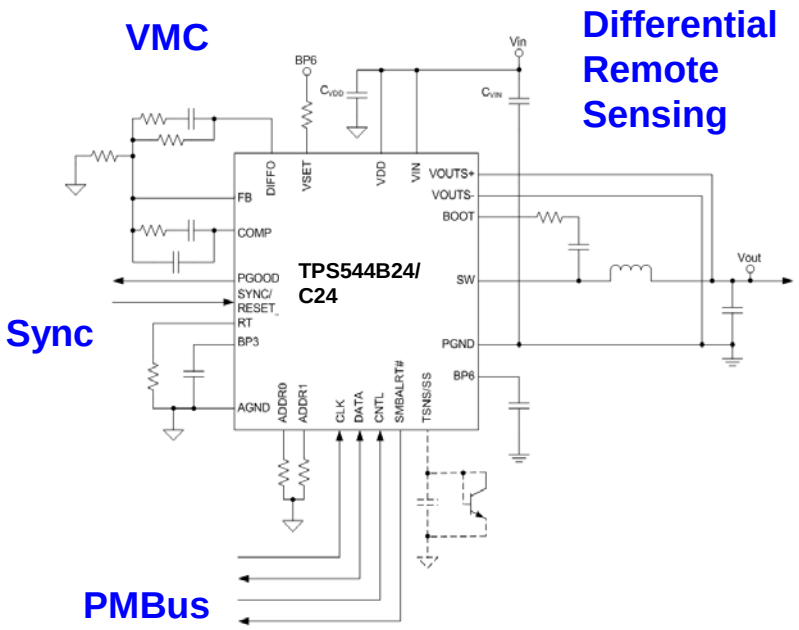
Samples: Now
RTM: 1Q2015

Features

- 4.5V to 18Vin, Vo 0.5 to 5.5 volts
- Programmable VOUT, AVS and Margining through PMBus
- Reference Voltage with 0.5% Accuracy from -40C to 125C junction temperature range
- Integrated NexFETs with senseFET Technology
- MOSFET Rds(on): HS/LS=5.5/2.0mohm
- Voltage Mode Control (VMC) with Input Feedforward
- Programmable Frequency 200kHz to 1MHz
- External Frequency Synchronization
- PMBus Interface
  - I, V, T Accurate Sensing
  - Programmable UVLO, Soft-start/stop, PGOOD
  - Programmable Thermally Compensated OCP, Output Over/Under Voltage and Overtemperature Protection and Fault Response
- Supports Pre-biased Output
- Differential Remote Sensing
- On Chip NVM
- 40-Pin 5x7 QFN Package

Applications

- Switchers/Routers/Wireless Infrastructure
- Cloud Computing/Server/Storage



TPS544B20/C20

4.5V to 18V Input, 20A/ 30A SWIFT™ Step-Down Converter with PMBus™

NEW!

Features

- Integrated 4.5/2mΩ NexFET™ Power Stage
- Programmable Settings and Configuration via PMBus Interface
- Adjustable Voltage via PMBus Interface
- Monitoring/Telemetry via PMBus Interface
- 0.6V to 5.5V Output with 0.5% Vref Accuracy
- D-CAP™/D-CAP2™ Mode Control Topology
- Differential Remote Sensing
- 250kHz to 1MHz Adjustable Frequency
- 5x7x1mm QFN Package

Benefits

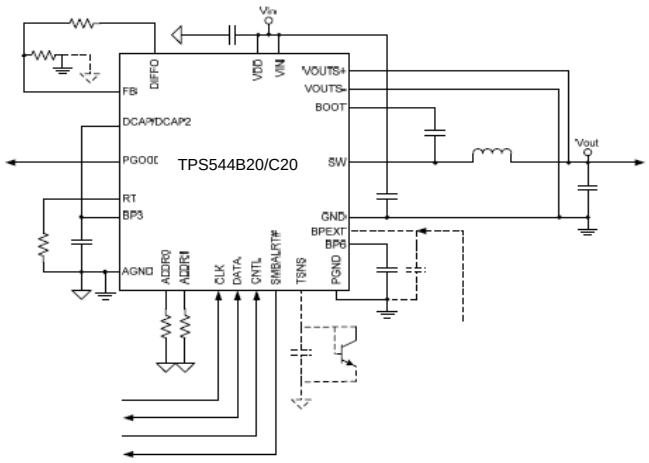
- >90% Efficiency at 12Vin/1.8Vout/30A @ 500KHz
- Set Over-Current & P-Good/UV/OV/OT Levels; UVLO; Soft-Start; Fault Responses; Ton/off Delays
- Trim Output Voltage & Control Margin Up/Down
- Accurately Sense Current, Voltage, & Temperature
- Ideal for Powering Advanced Processors
- No Loop Compensation with Cout Flexibility
- Accurate Voltage Over Long Routing Distances
- Optimize Design for High Efficiency or Small Size
- High Power Density Less than 200mm² total Area

Applications

- Cloud Computing, Server, Data Storage
- Wired and Wireless Infrastructure Equipment
- High Speed Switches & Routers
- Industrial Automated Test Equipment
- Point-of-Load Power for High-Current DSPs, FPGAs, and ASICs

Pin Compatible

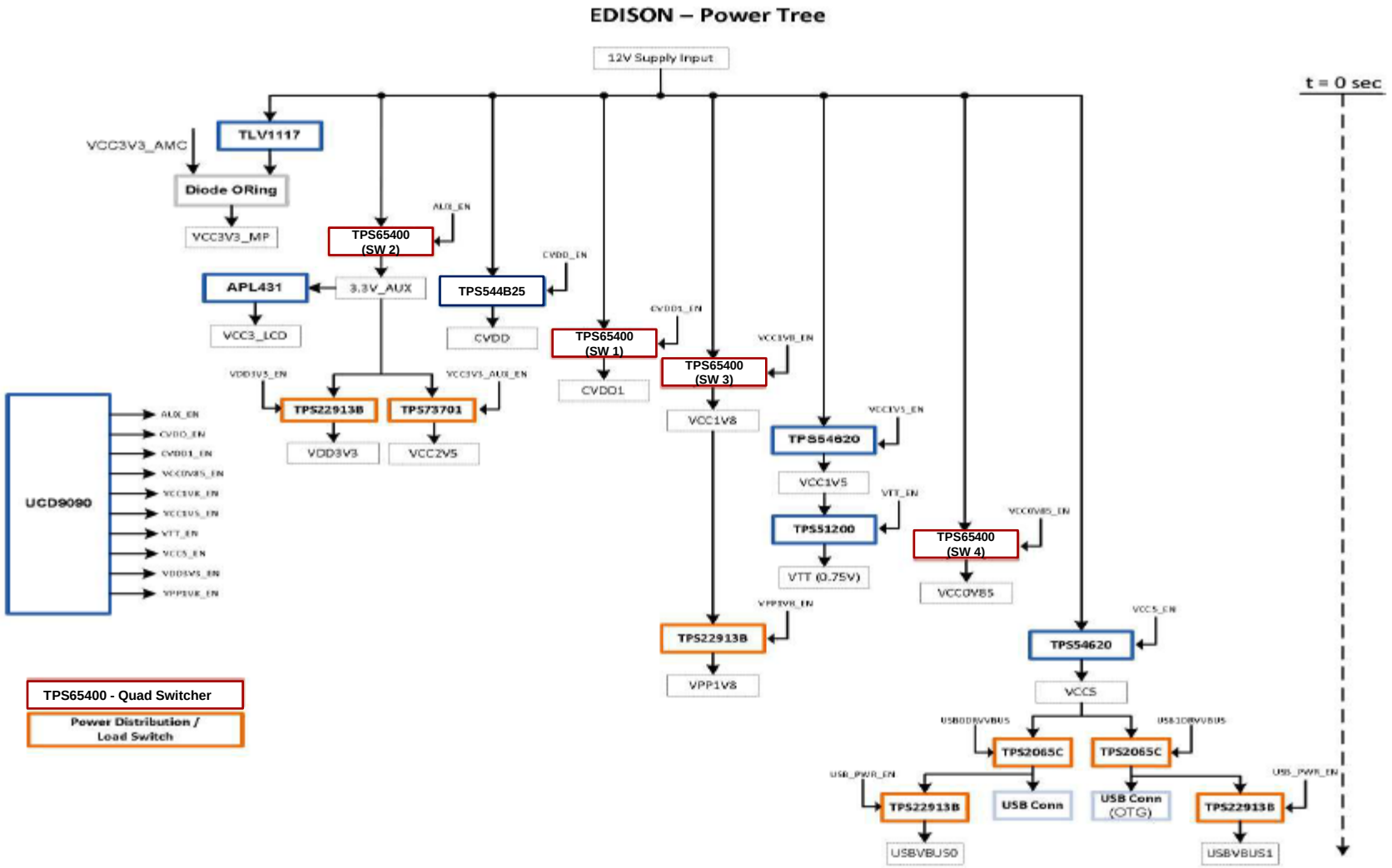
Device	Iout
TPS544B20	20-A
TPS544C20	30-A



Texas Instruments

Power for K2E

K2E05/02 Power Tree



K2E05/02 Power Recommendations

Supply	VIN = 12V Single SOC Implementation
CVDD (AVS)	TPS544B25
CVDD1 (0.95V)	TPS65400 (Sw 1)
DVDD15* (1.5V) & VTT (0.75V)	TPS54620 + TPS51200
DVDD18** & VDDAHV (1.8V)	TPS65400 (Sw 2)
DVDD33**	TPS65400 (Sw 3)
VDDALV (0.85V)	TPS65400 (Sw 4)

TPS544B25 is the identical catalog version of TPS544B24 on EVM

TPS54620

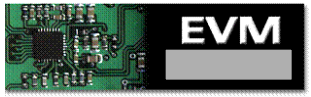
4.5V to 17V Input 6-A Synchronous Step Down SWIFT ™ DCDC Converter

Features

- Integrated Monolithic 26mΩ High Side and 19mΩ Low Side MOSFETs
- 200KHz to 1.6MHz Adjustable Switching Frequency
- 0.8V Reference with 1% Accuracy over Temperature
- Synchronizes to External Clock
- Integrated Tracking Function
- 3.5 x 3.5mm 14 pin QFN Package

Applications

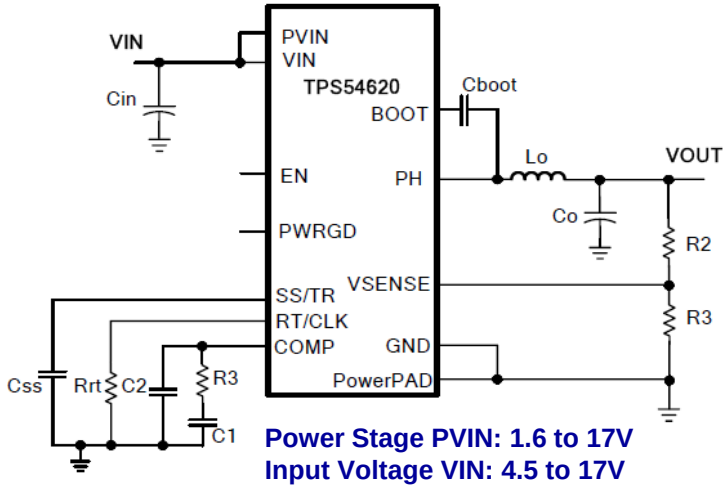
- Broadband, Networking & Communication Infrastructure
- Servers and Work Stations
- Compact PCI / PCI Express / PXI Express Applications



TPS54620EVM-374

Benefits

- 95% Peak Efficiency; Optimized for Low Output Voltages
- High Frequency Supports Small Output Inductor and Capacitor Size
- Ideal for Powering New Deep Sub-Micron DSPs, FPGAs, and ASICs
- Eliminates Beat Noise for Sensitive Applications
- Easily Implement Sequencing Schemes
- 60% Smaller Package than other 12V / 6A Converters with Integrated FETs



Power Stage PVIN: 1.6 to 17V
Input Voltage VIN: 4.5 to 17V

TPS51200

3A Source-Sink DDR Termination Regulator

Features

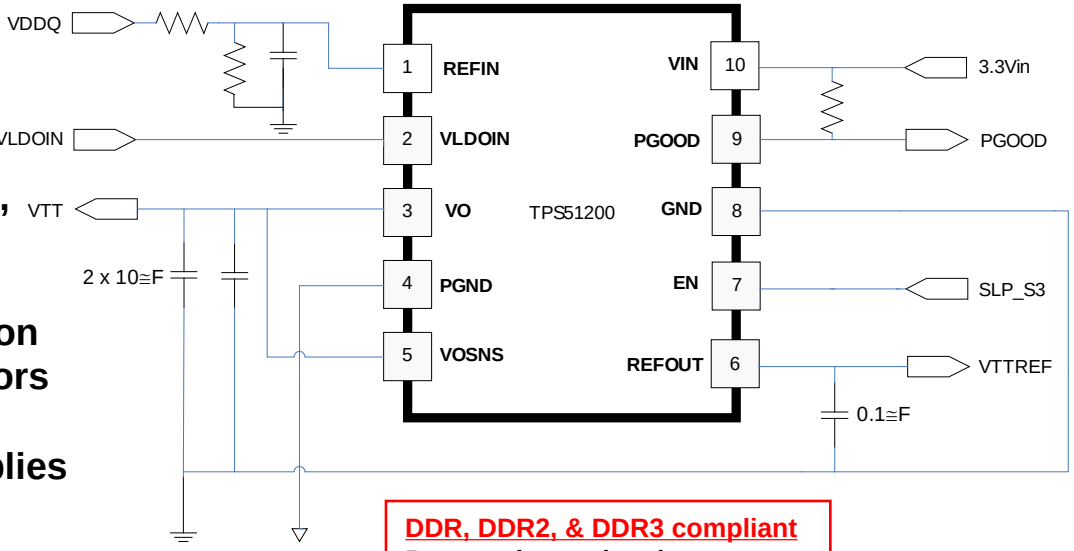
- Requires only 20uF of ceramic output capacitance
- Direct interface to S3 and sensing of S5 control signals
- Supports high-Z in S3 and soft-off in S5
- LDO input can be reduced to 1.2V
- SS, UVLO, OCL and thermal shutdown
- Enable input and Power Good output
- 10-pin SON package

Benefits

- Lower cost and size than competing parts requiring 600uF or more of electrolytic capacitance
- Ease of use
- Fewer external components and lower cost
- Lower power dissipation
- System protection
- Controlled turn-on and monitored output regulation
- Enables small form factor designs

Applications

- DDR, DDR2, DDR3, and low-power DDR3/DDR4 VTT Memory Termination
- Graphics Processors
- Core Supplies
- Chipset/RAM supplies as low as 0.5V



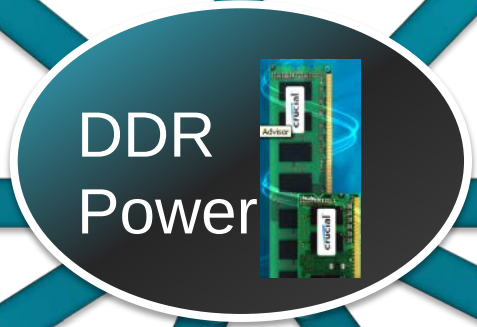
Low VIN Requirement
2.375V to 3.5V

PGOOD Output
Open drain Output to indicate VTT is within regulation

VTTREF sink and source
+/- 10mA

DDR, DDR2, & DDR3 compliant
Post package trimming to meet any DDR3 V_{TT} tolerance spec

DDR Memory Power Solutions



Highest-current LDO
3.3VIN – 3A
VTT
DDR2/DDR3/DDR3L/LPDDR3
TPS51200

Simplest LDO
5VIN - 3A
VTT
DDR2
TPS51100

Smallest LDO
Most Price Competitive
3.3V/5VIN - 2A
VTT
DDR3/DDR3L/LPDDR3
TPS51206

PWM + LDO
Most optimized for bulk caps
VDDQ and VTT
DDR3/DDR3L/LPDDR3
TPS51216

6A iFET
Highest-current/efficiency
VTT
DDR3/DDR3L/LPDDR3
TPS53317

PWM + LDO
Highest Power Density
Lowest BOM cost
VDDQ and VTT
DDR3/DDR3L/LPDDR3
TPS51916

PWM + LDO
Industrial temp range
VDDQ and VTT
DDR2/DDR3/DDR3L
TPS59116

8A/10A iFET
Industrial temp range
VDDQ
DDR2/DDR3/DDR3L/LPDDR3
TPS51362/7

PWM + LDO
Highest volume
Most Flexible
VDDQ and VTT
DDR2/DDR3/DDR3L
TPS51116

Power Sequencing for Keystone II

- There are 2 acceptable power up sequences for Keystone II devices outlined below.

Core Voltages Before I/O Voltages

K2E

1. CVDD
2. CVDD1, VDDAHV, AVDDAx, DVDD18
3. DVDD15
4. VDDALV, VDDUSBx, USBxVP, USBxVPTX
5. USBxDVDD33

K2H

1. CVDD
2. CVDD1, CVDDT1, VDDAHV, AVDDAx, DVDD18
3. DVDD15
4. VDDALV, VDDUSB, VP, VPTX
5. DVDD33

I/O Voltages before Core Voltages

K2E

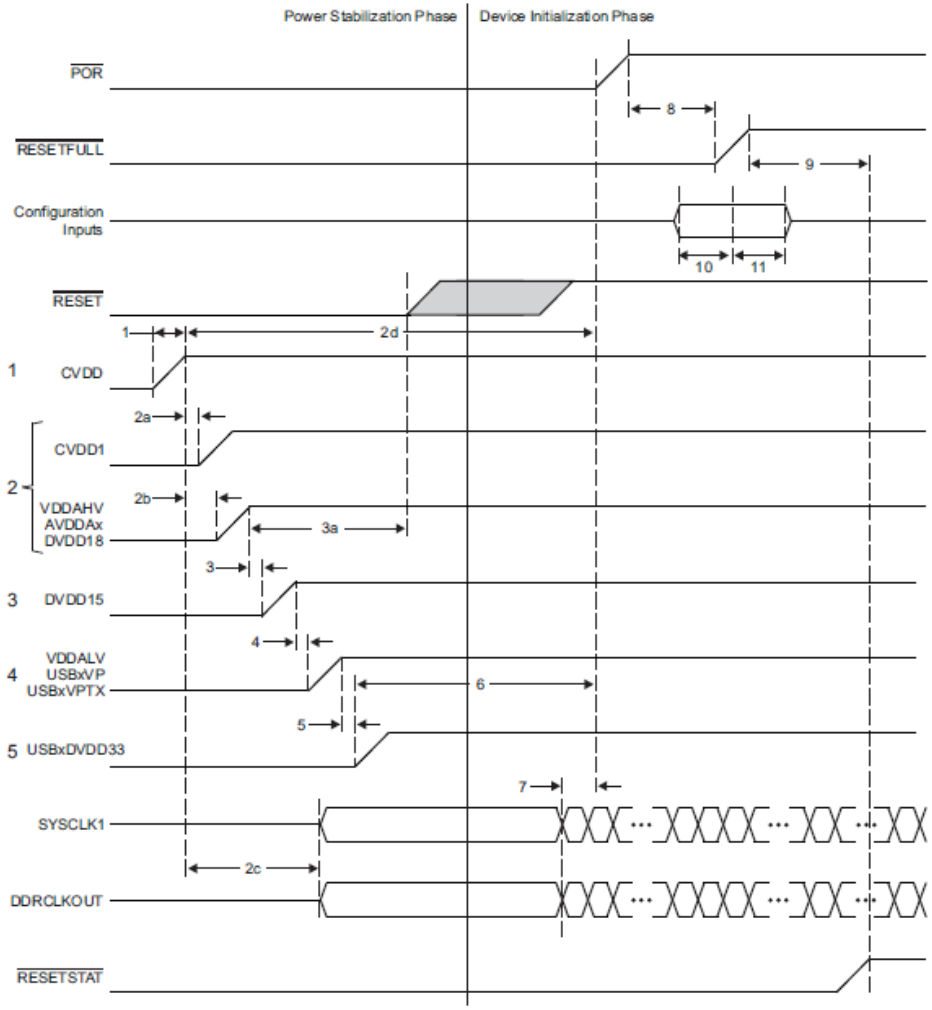
1. VDDAHV, AVDDAx, DVDD18
2. CVDD
3. CVDD1
4. DVDD15
5. VDDALV, VDDUSBx, USBxVP, USBxVPTX
6. USBxDVDD33

K2H

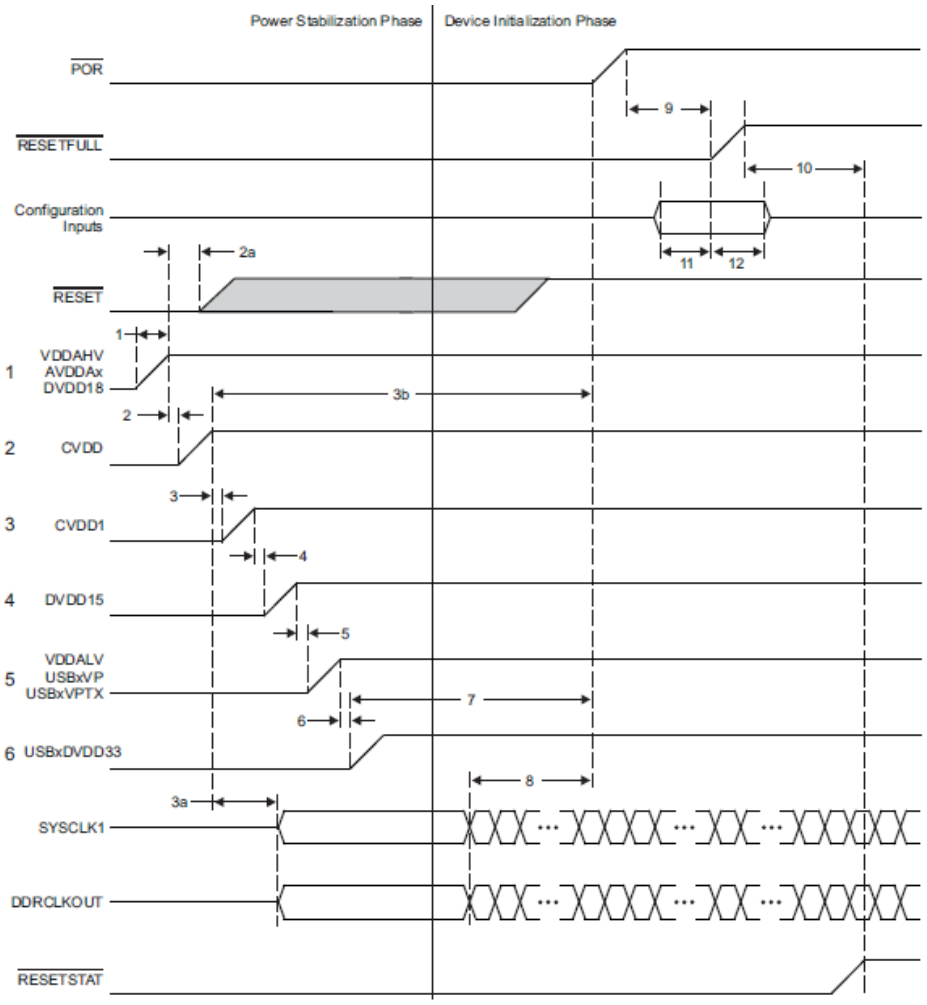
1. VDDAHV, AVDDAx, DVDD18
2. CVDD
3. CVDD1, CVDDT1
4. DVDD15
5. VDDALV, VDDUSB, VP, VPTX
6. DVDD33

Power Sequencing – Timing Diagrams

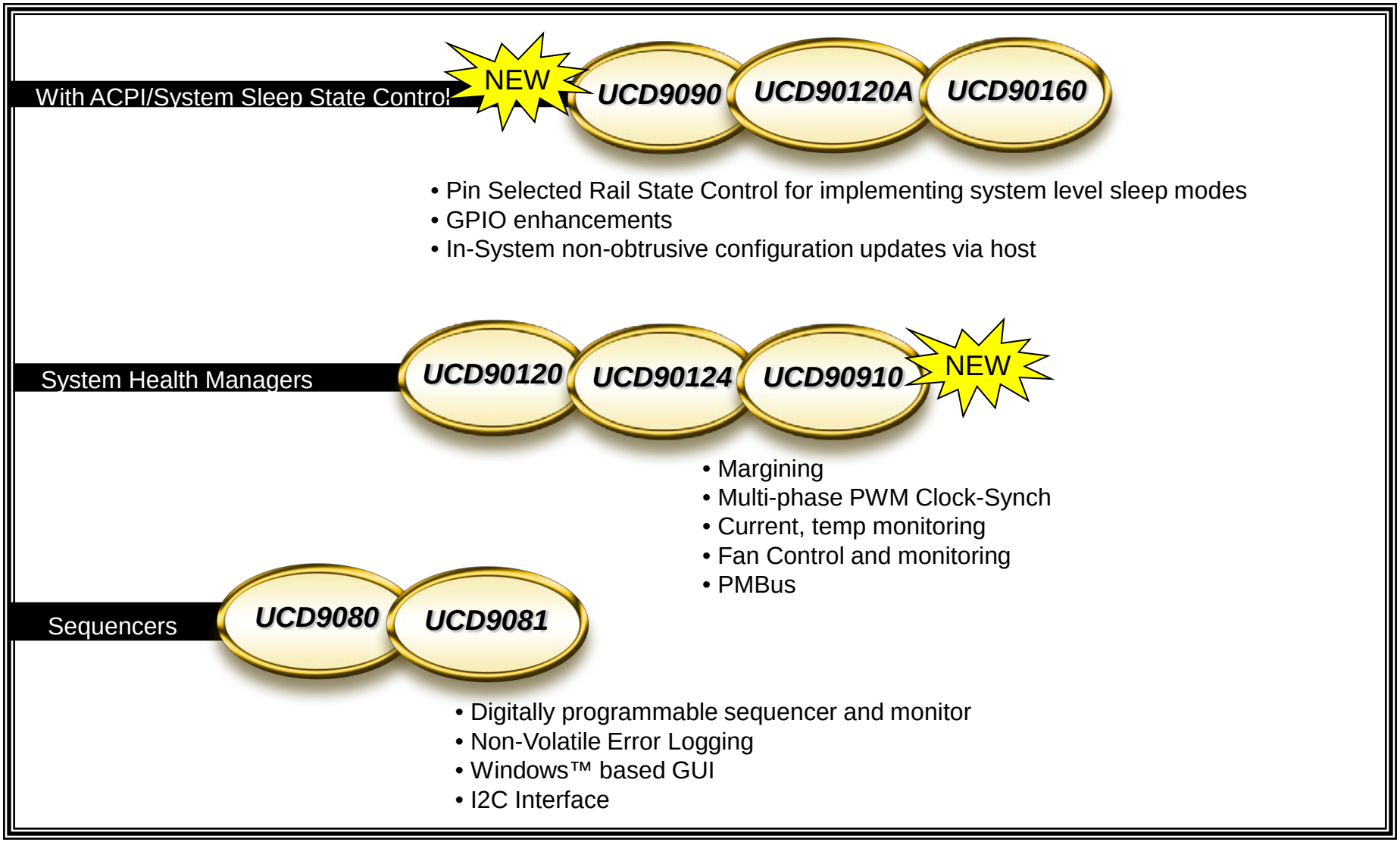
Core Before IO Power Sequencing



IO-Before-Core Power Sequencing



Power Sequencer/System Health Managers



Sequencer Portfolio Selection Guide

	UCD90160	UCD90120	UCD90120A	UCD90124	UCD9090	UCD90910	UCD9081
# Rails Sequenced	16	12	12	12	10	10	8
# of Monitor Inputs	16	13	13	13	11	13	8
ADC Ref Accuracy	0.5% Internal	0.5% Internal	0.5% Internal	0.5% Internal	0.5% Int ot Ext	0.5% Internal	External
Voltage Margining*	10	10	10	10	10	10	
Fan Control*	N/A	N/A	N/A	4	N/A	10	N/A
Multi-phase PWM clock outputs*	8	N/A	8	8	8	8	N/A
ACPI Sleep State Control	Yes	No	Yes	No	Yes	No	No
Current and Temp Monitor Scaling	No	Yes	Yes	Yes	Yes	Yes	No
NV Fault Logs	8	16	TBD	10	15	20	8
Other NV Logging	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	Peaks, Resets, Run-time clock	N/A
Max GPI/GPO*	8/16	8/12	8/12	8/12	8/10	8/10	0/4
Internal Temp Sensor	Yes	Yes	Yes	Yes	Yes	Yes	No
Communication and Programming I/F	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	PMBus/I2C, JTAG	I2C
Watchdog Timer	Yes	Yes	Yes	Yes	Yes	Yes	No
Package Type (size)	64-pin QFN(9x9)	64-pin QFN(9x9)	64-pin QFN(9x9)	64-pin QFN (9x9)	48-pin QFN (7x7)	64-pin QFN (9x9)	32-pin QFN (5x5)
Availability	Production	Production	Production	Production	Production	Production	Production

* Table shows the max number of each feature supported by each device. For example, the UCD90124 has 12 PWM pins used as any combination of margining, PWM, fan control, or GPIO up to the max listed. See data sheets for details.

UCD9090: 10-Rail Sequencer and System Health Monitor with ACPI System Sleep State Control

Features

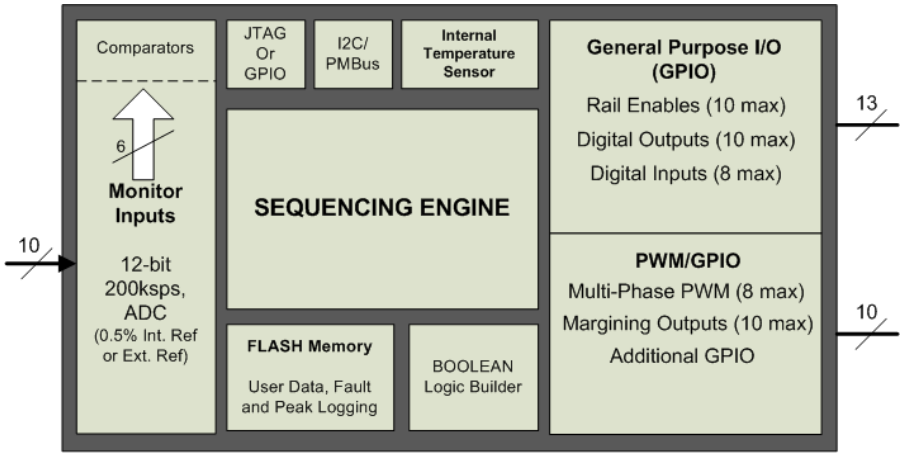
- **Sequence, Monitor, and Margin up** to 10 Rails
- Independent Turn and Turn off dependencies
- Dependencies on time, parent rails, GPIs, and I2C commands
- Flexible GPIO configuration with BOOLEAN Logic capability
- 11 ADC Inputs with user settable scale factors for detecting voltage (OV/UV), current(OC/UC), or temp faults
- 6 optional comparators for fault response in < 80 us
- Respond to faults by configuring retries, shutdown delays, re- sequencing and groups of rails to shutdown
- **Non-Volatile fault and peak logging**
- Simultaneously **margin/trim** up to 10 rails using PWM outputs and I2C commands
- Up to 8 multi-phase PWM clock outputs
- Easy-to-use **Fusion Digital Power Designer GUI**
- JTAG and PMBus interfaces provide flexible options for in-system host communication and configuration
- **Pin Selected Sleep State control for use with ACPI or similar system power specifications**

Applications

- Server/Storage Systems
- Communication Infrastructure
- Industrial/ATE
- Embedded Computing

Benefits

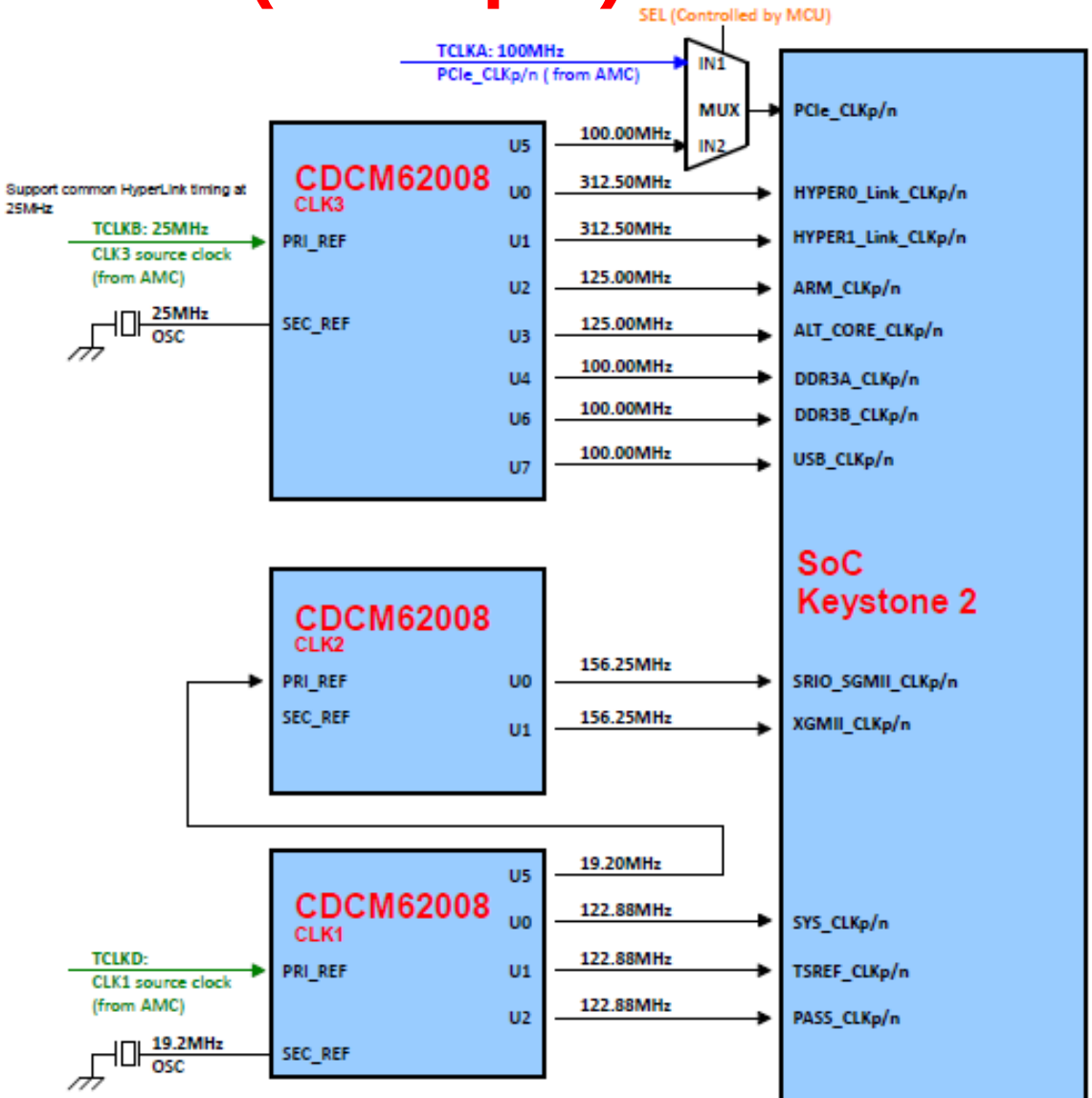
- Flexibility sequencing requirements supports most possible sequencing scenarios
- Detect power supply warnings and faults and store to non-volatile memory for failure analysis
- Monitor voltage, current and temp in actual system units to eliminate host software scaling
- Closed-Loop Margining for corner testing of power supplies allows designers to identify possible system reliability issues
- Multi-phase PWM outputs eliminate need for separate chip to synch switch mode power supplies
- ACPI sleep state control allows host to shut down rails that are not in use and conserve system power
- TI's ***Fusion Digital Power GUI*** eliminates need to write code



Clocks

www.ti.com/clocks

K2H Clock Tree (example)



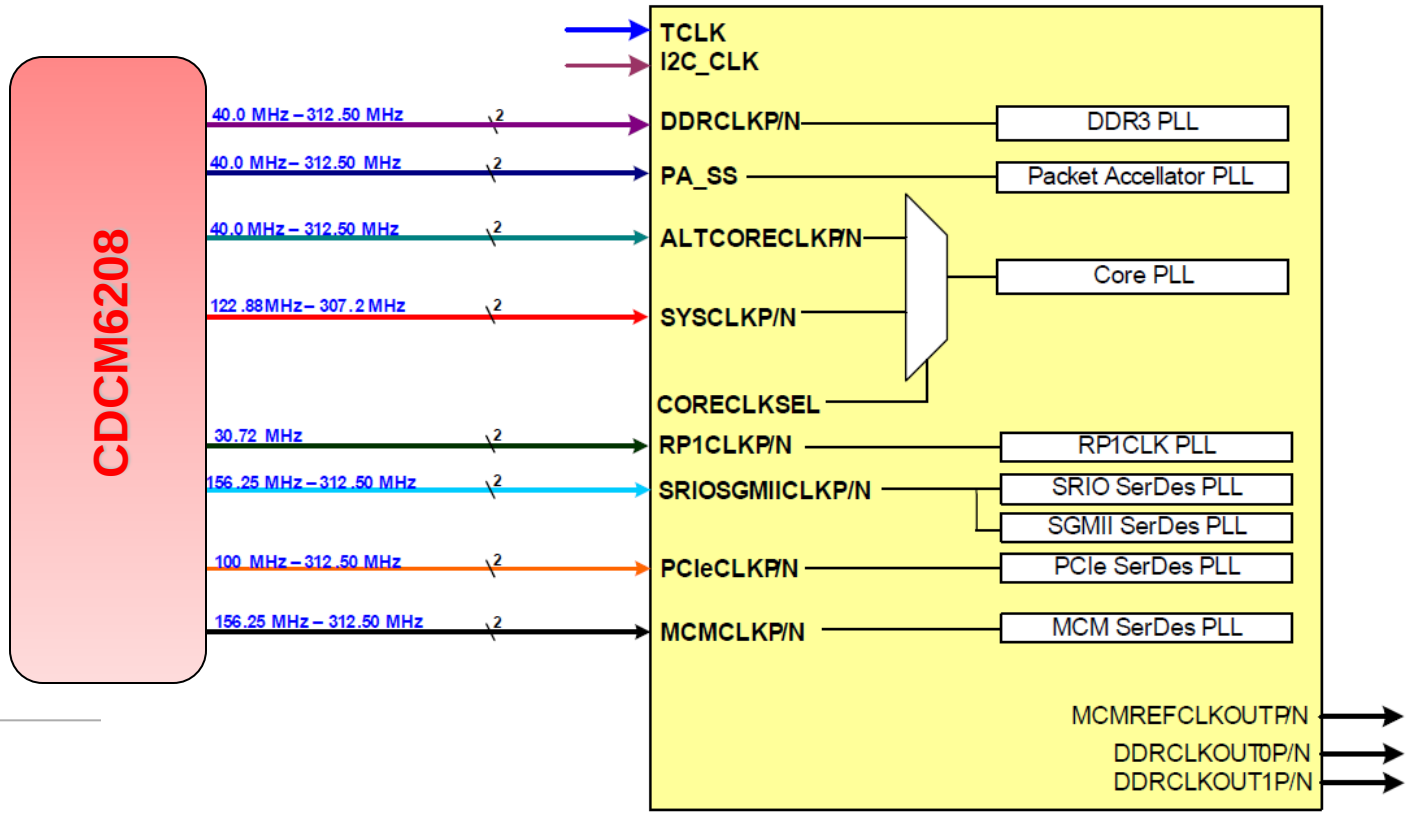
Keystone DSP suggests ....

3.5 Clocking and Clock Trees (Fan out Clock Sources)

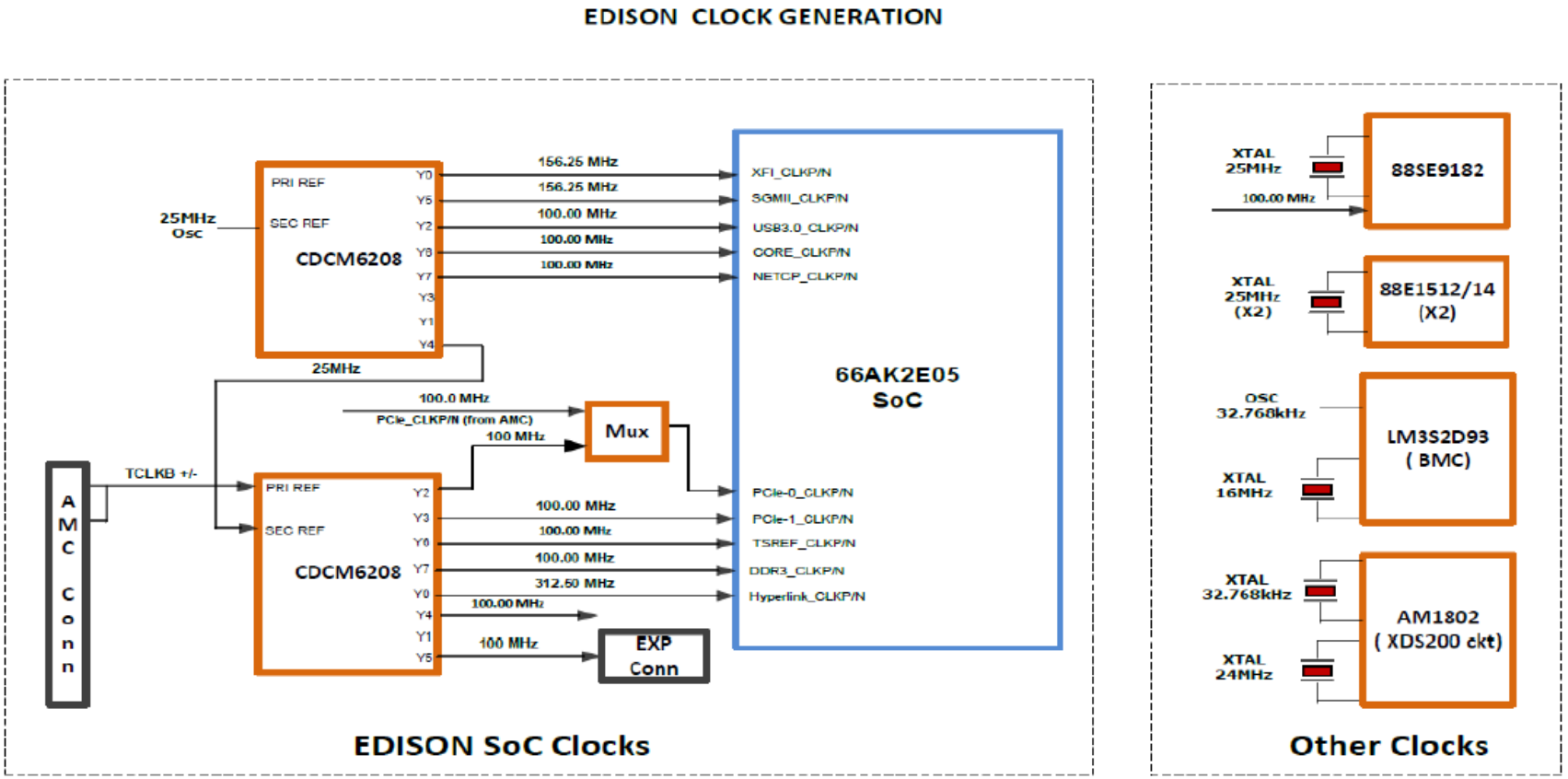
For systems with multiple high performance DSP processors, it is not recommended that a single clock source be used (single output only). Excessive loading, reflections, and noise will impact performance. Instead it is recommended that differential clocking be used which include a differential clock tree.

Texas Instruments has developed a specific line of clock sources to meet the challenging requirements of today's high performance DSPs. In most applications the use of these specific clock sources eliminates the need for external buffers, level translators, external jitter cleaners, or multiple oscillators.

Figure 4 KeyStone DSP Reference Clocks



66AK2E05 SOC Clock Tree

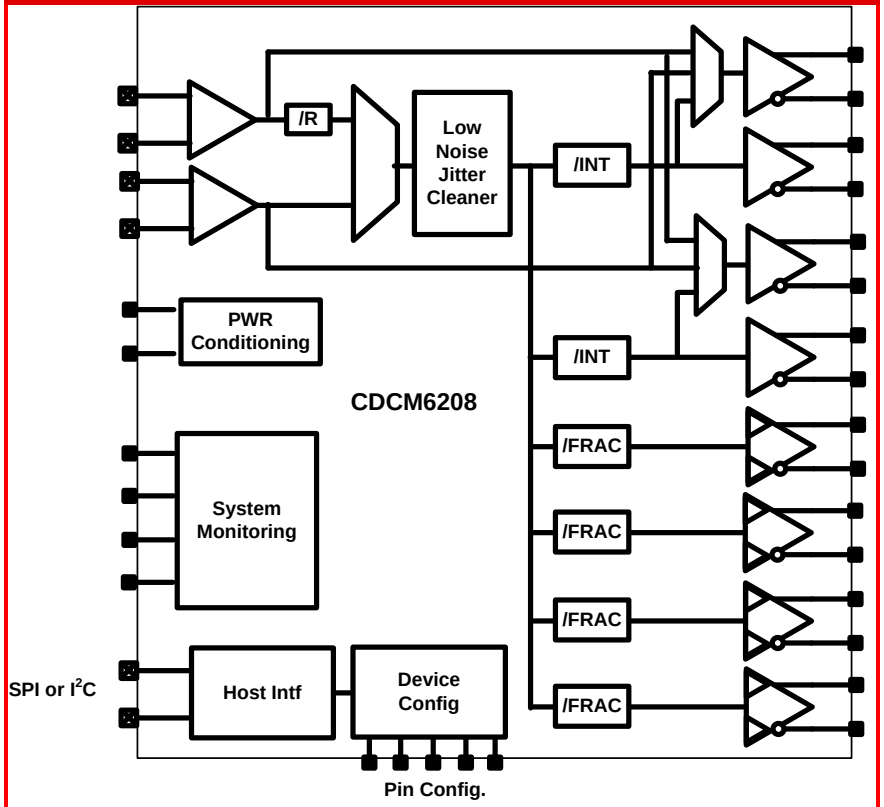


CDCM6208: Low Jitter Clock Generator

Superior Performance with Low Power & Flexible Frequency Planning

Features	
RMS jitter @ 156.25MHz	265 fs (12kHz – 20MHz) 25 MHz Crystal as reference
Max f_{OUT}	800 MHz
Output Format	LVDS, CML, LVPECL, HCSL or LVCMOS
Typical Power Consumption	< 0.5 W (best in the market)
Supply Voltage	1.8 V, 2.5 V and/or 3.3 V Allowing Mixed Supply Voltages
Total Number of Outputs	8 differential outputs. Up to 8 single ended
Input Reference Clocks	Crystal, XO, Single ended or Differential Clock
Multiple Clock Frequencies	4 Fractional dividers 2 Integer dividers
Independent Clock Domains	5

CDCM6208 Block Diagram



Ideal clock for TI-DSPs (Keystone)

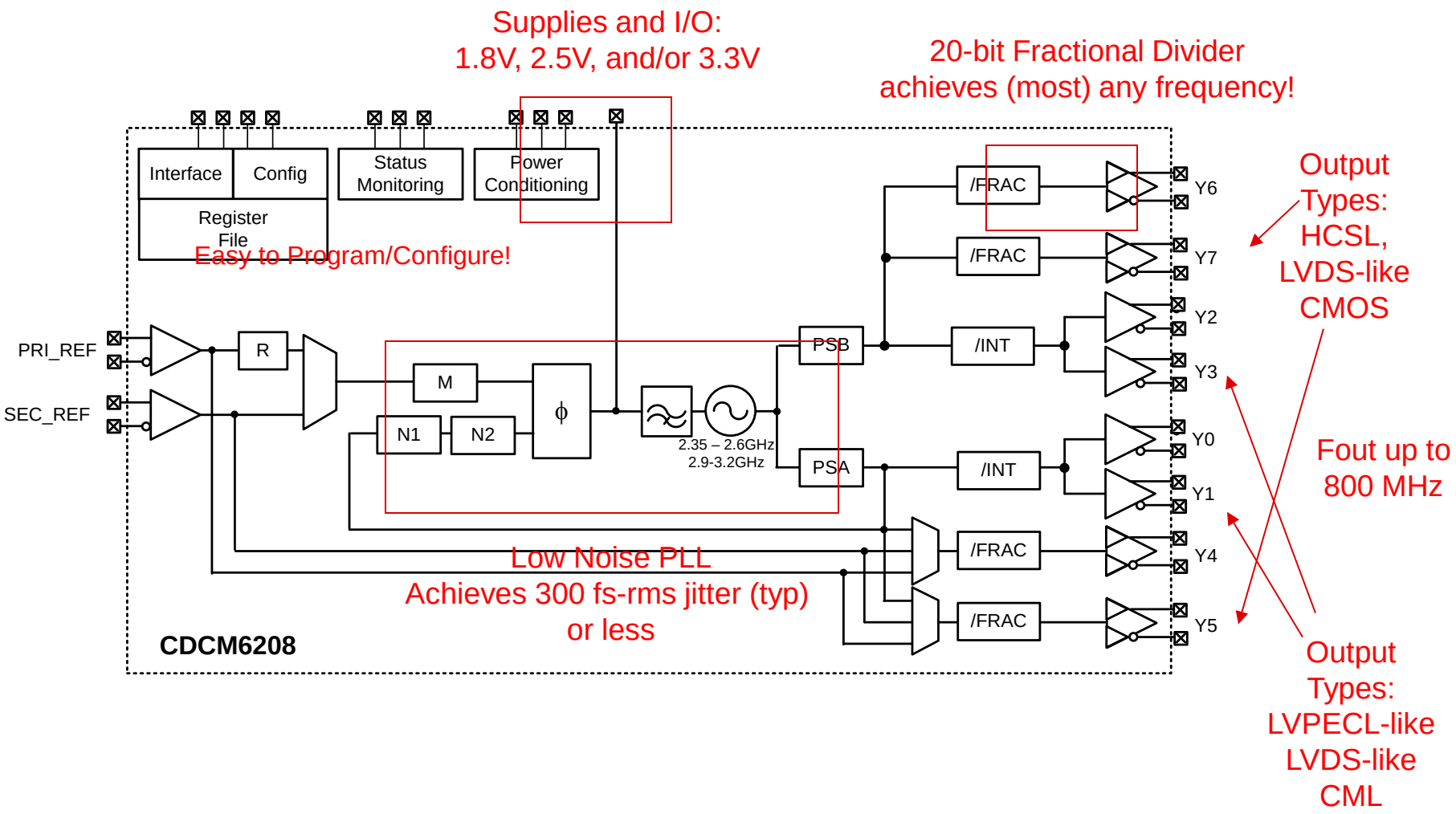
In Production

Jitter Budget Keystone DSP and CDM6208 actuals

integer & fractional output compliant to 10GbE

	Logic (NYQ)*	CDCM6208		Input Jitter spec NYQ (9) *	CDCM6208 measured	Trise / Tfall 3 *	Duty Cycle %	Stability *
SRIO_SGMII_CLKp SRIO_SGMII_CLKn (if SRIO is used)	LJCB or LVDS (1)	LVDS	156.25MHz	4ps RMS 56 ps pk-pk @ 1x10^{-12} BERT [1.875MHz to 20MHz single-pole filter bound] IEEE802.3ae spec page 280	**56ps pk-pk with unbound jitter; 44ps-pk-pk with bounded jitter**	50 – 350 ps2	45 / 55	± 100 PPM
SRIO_SGMII_CLKp SRIO_SGMII_CLKn (SRIO not used)	LJCB or LVDS (1)			8ps RMS 112 ps pk-pk @ 1x10E-12 BER7		50 – 350 ps2	45 / 55	± 100 PPM
PCIe_CLKp PCIe_CLKn	LJCB or LVDS (1)			4ps RMS 56 ps pk-pk		50 – 350 ps2	45 / 55	± 100 PPM
RPI_CLKp RP1_CLKn	LVDS	LVDS or PECL	30.72MHz (0-ppm)	4 ps RMS 56 ps pk-pk	**0.1ps RMS (10k-20M) 12ps pk-pk (DJ unbound)**	50 – 350 ps2	45 / 55	± 100 PPM
MCM_CLKp MCM_CLKn	LJCB or LVDS (1)			8ps RMS 112 ps pk-pk @ 1x10E-12 BER7		50 – 350 ps2	45 / 55	± 100 PPM
ALTCORE_CLKp ALTCORE_CLKn	LJCB or LVDS (1)			100 ps pk-pk		50 – 350 ps2	45 / 55	± 100 PPM
PA_SS_CLKp PA_SS_CLKn	LJCB or LVDS (1)			100 ps pk-pk		50 – 350 ps2	45 / 55	± 100 PPM
SYSCLKp SYSCLKn	LJCB or LVDS (1)	LVDS or PECL	122.88MHz (0-ppm)	2 ps RMS (28 ps pk–pk), period5 [10k-20M]	**0.3ps RMS (10k-20M) 13ps-pp (DJ unbound)**	50 – 350 ps2	45 / 55	± 100 PPM
DDR_CLKp DDR_CLKn	LJCB or LVDS (1)	LVDS	66.67MHz (-0.02ppm or +55 ppm)	2.5% of DDRCLK output period (pk-pk)4 (which is 374ps-pp)	**0.98ps-rms (10k-20M) 32ps-pp DJ (10k-20M)**	50 – 350 ps2	45 / 55	± 100 PPM
FGPA 100MHz	CMOS	CMOS (1.8V, 2.5V or 3.3V)	100MHz (-0.1ppm or -33 ppm)		**1.1ps RMS (10k-20M) 6ps pk-pk DJ (10k-20M)**			± 100 PPM ??

CDCM6208
Block Diagram



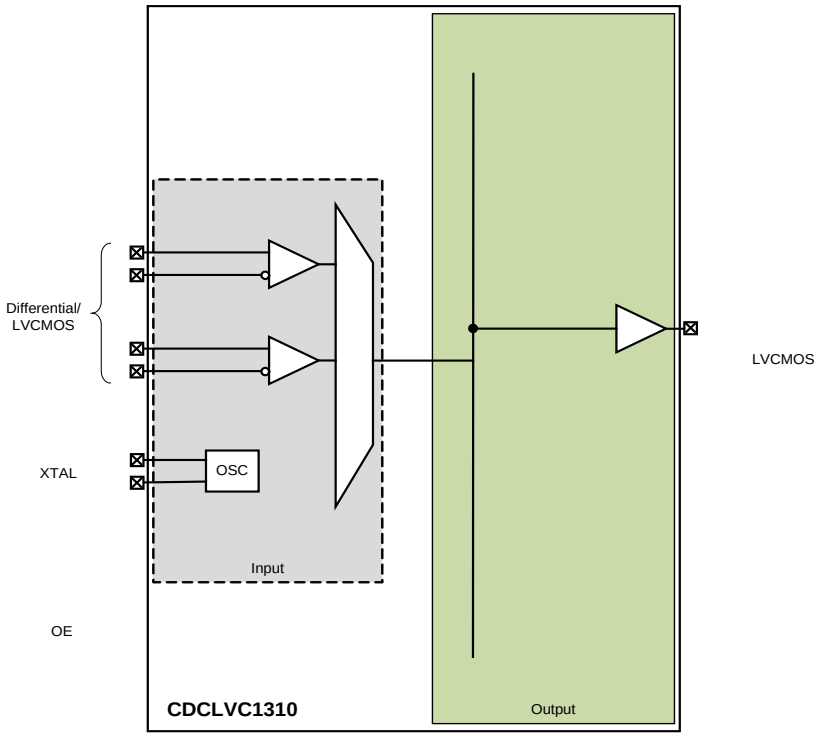
Additional Clock Devices

CDCLVC1310: Low-Noise Clock Buffer

10-Output LVCMOS Buffer / Level Translator

Features	
Additive jitter	25 fs_{RMS} (12k to 20 MHz) @ 156.25 MHz LVPECL
Output Frequency	200MHz
Noise Floor	-169 dBc/Hz (25 MHz Crystal input)
Universal Input Buffers	LVPECL, LVDS, CML, SSTL, HSTL, and LVCMOS input
Crystal Input	8 to 50 MHz
Output Skew	30 ps (typ)
Core Supply Output Supply	3.3 V or 2.5V 3.3 V, 2.5V, 1.8V or 1.5V

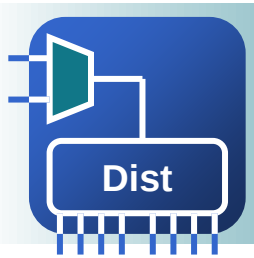
CDCLVC1310 Block Diagram



Low Additive Jitter, Low Power & Level Translation

Clocking for other Peripherals

TI Complete Clock Solution Portfolio



LMK01x00, LMK0030x/10x, CDCLVC1310 – Distribution

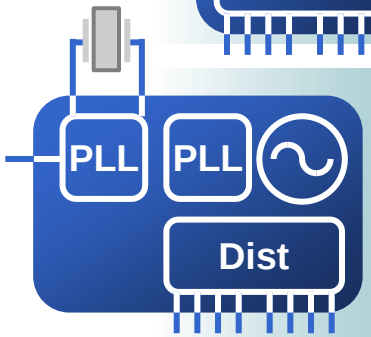
- Lowest additive jitter CLK fanout
- Programmable dividers / delays for flexibility

LMK02000 – Jitter Cleaning / Distribution

- Low noise PLL + external VCXO cleans CLK
- Includes distribution functionality

LMK03x00, CDCM6208 – Clock Generation / Distribution

- Integrates PLL + VCO cleans and/or multiplies CLK
- Includes distribution functionality



LMK04x00 – Jitter Cleaning / Generation / Distribution

- Cascaded PLL + VCO provides low cost jitter cleaning
- Crystal Oscillator can be used for CLK Generation
- Includes all functionality of LMK01000

High Speed Interface (PCIe, USB3, SAS, SATA, Ethernet) and Serdes Solutions

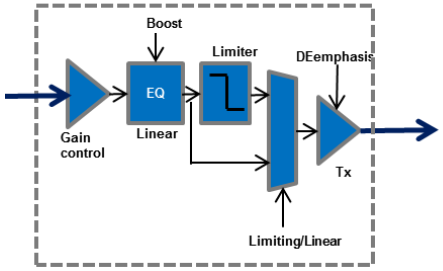
www.ti.com/sigcon

www.ti.com/usb

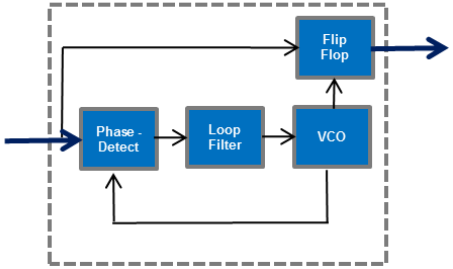
www.ti.com/serdes

3 Development Vectors for 3 Signal Conditioning Problems

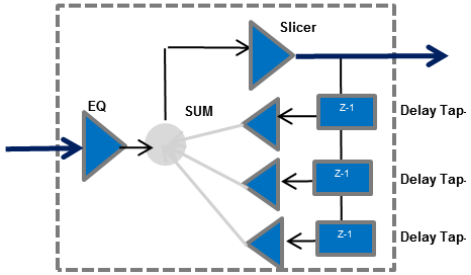
Equalization & De-Emphasis Driver



Clock Data Recovery (CDR)



Decision Feedback EQ (DFE)

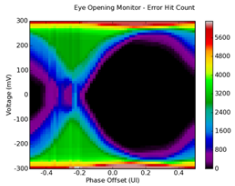


✓ **Insertion Loss**

✓ **Jitter**

✓ **X-Talk, Reflections**

Ease of Use Features

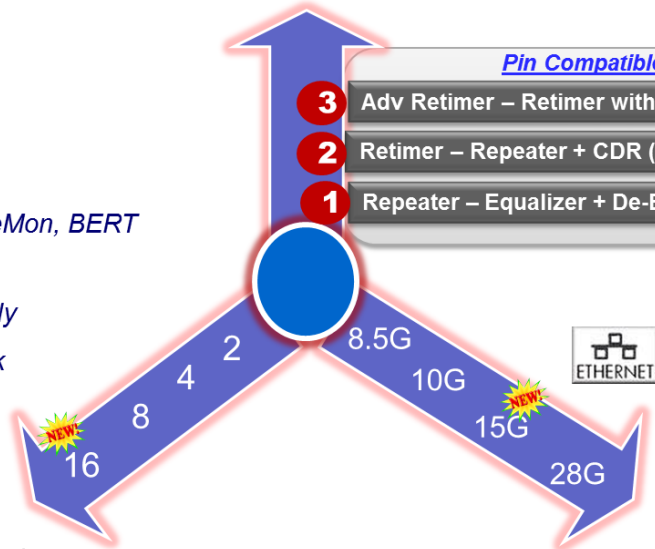


- ✓ *On chip diag – EyeMon, BERT*
- ✓ *Flow-thru package*
- ✓ *Single power supply*
- ✓ *No reference clock*

Signal Conditioning Function

Pin Compatible Upgrade

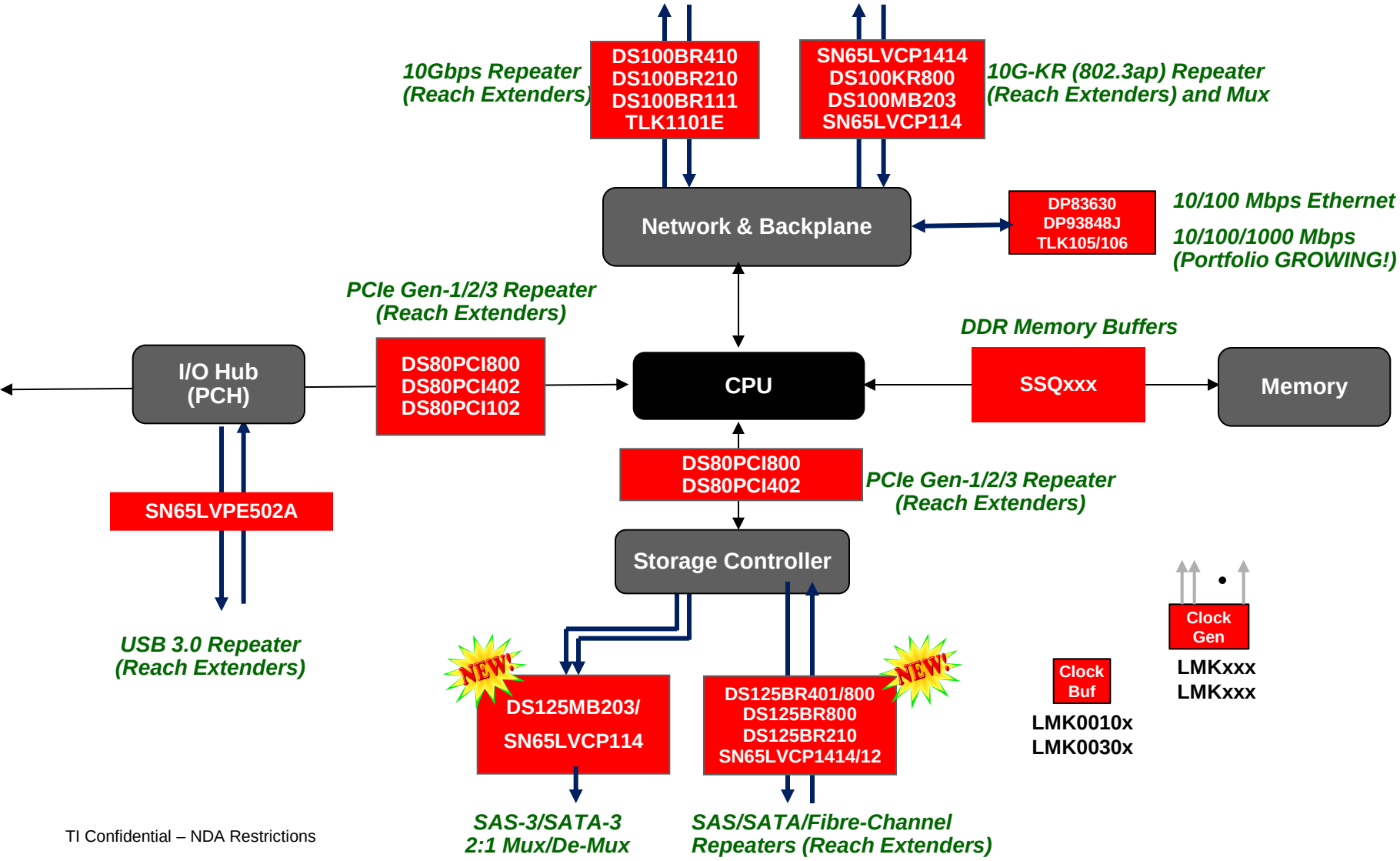
3. Adv Retimer – Retimer with DFE (Decision Feedback EQ)
2. Retimer – Repeater + CDR (Clock-Data-Recovery)
1. Repeater – Equalizer + De-Emphasis Driver



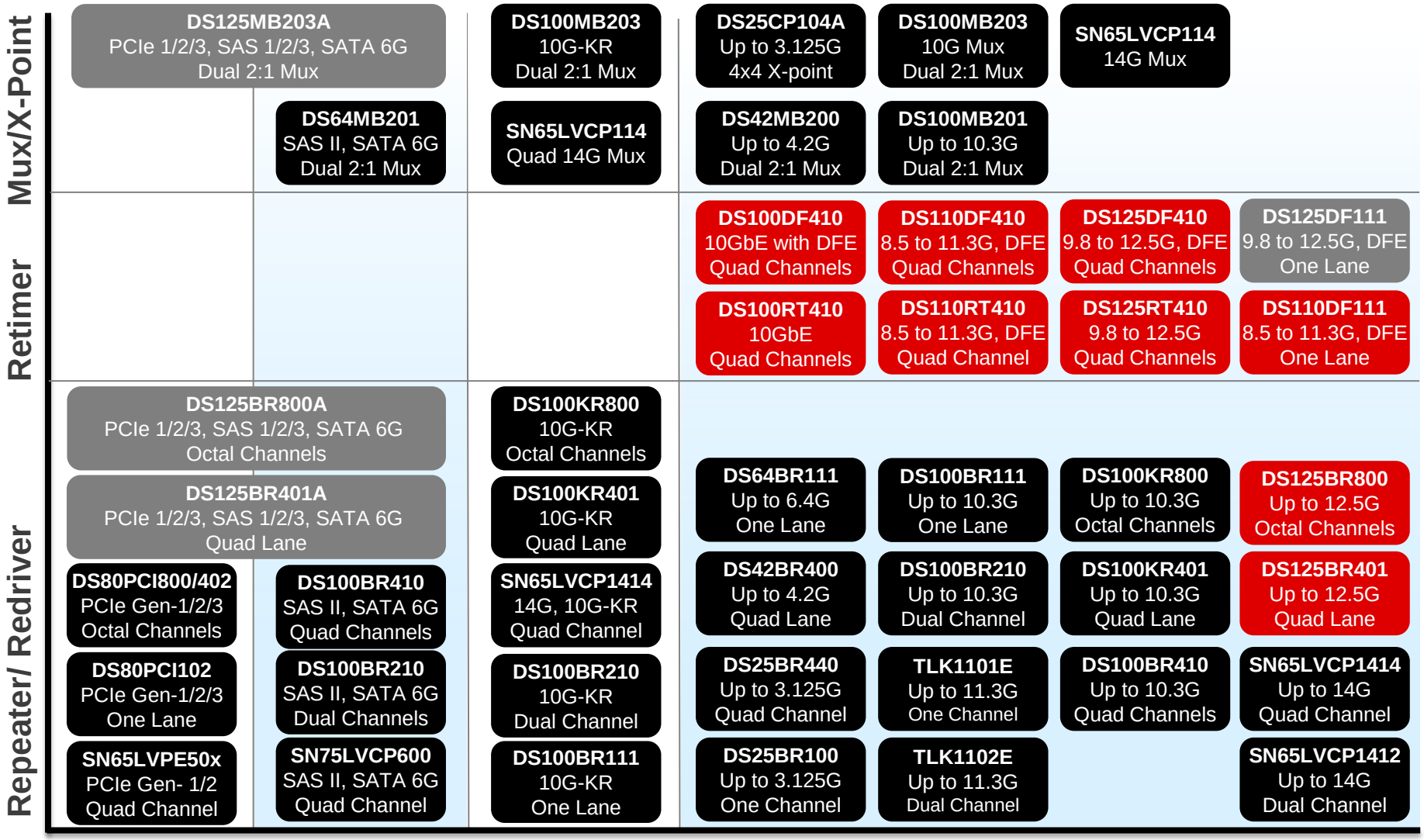
Channel/Port Configuration

Protocol, Data Rate

Interface Solutions for Server, Storage, Network and Backplane



Most Complete SigCon Portfolio in the Industry



(Products Highlighted in RED are New Arrivals, and Dark Grey are Preview Products)

Ethernet PHYs and Link Consolidation Solutions

- Ethernet is interface of choice for Data Centers
  - All 10G PHYs support Backplane (KR) as well as Optical ports
    - TLK10232 (dual) for XAUI (3.125G x 4) to KR / Optical (10G Serial)
    - TLK10034 (quad), TLK10021 (single) also available
  - Broad selection of GbE and 10GbE Redrivers and Muxes
    - DS100BR111/210/410: Single/Dual/Quad Ultra-low power 10G redrivers
    - DS100MB203, SN65LVCP1412/14: 10GbE/10GKR Mux + Redriver
  - Protocol translation and crosspoint ICs for various 10GbE interfaces
    - TLK10134/2 (quad/dual) translate between 10G-KR, RXAUI, XAUI, XLAUI, etc

- Gigabit serial links proliferating within Networking
  - Driving up cost, power consumption, system complexity, time to market
  - 10 Gbps Serial link aggregation can solve this problem
    - TLK10022: Aggregate up to 4 links (up to 2.5G each) into 1 link (up to 10G)
    - TLK10081: Aggregate up to 8 links (up to 1.25G each) into 1 link (up to 10G)

SYSTEM PROTECTION AND MONITORING

WWW.TI.COM/HOTSWAP

WWW.TI.COM/ERROR_P_TEMP

System Protection & Management Focus: Managing Power to Critical Systems

1) Protection

- Inrush Control
- FET Current/Power
- Circuit Breaker

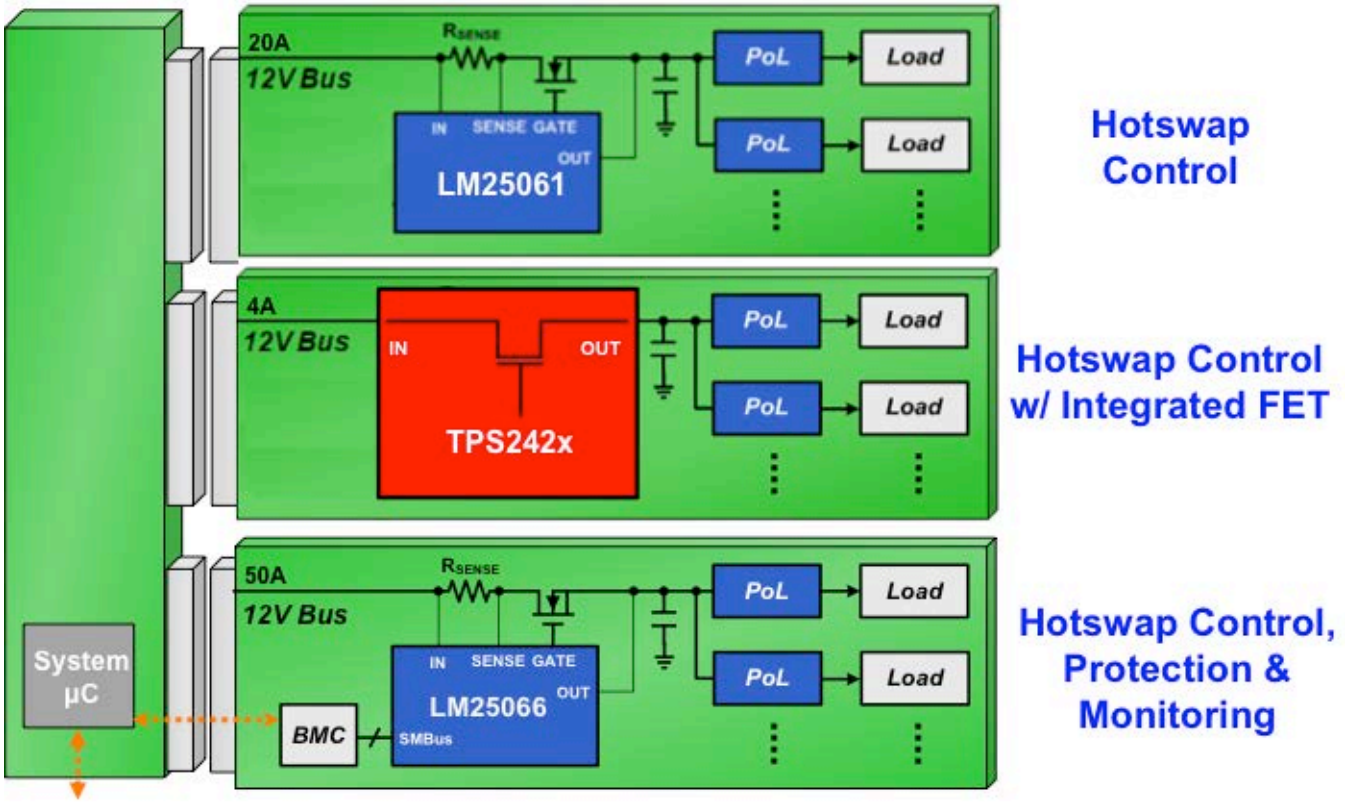
2) Control

- Programmable Limits
- Fault / Warning Levels
- Power Capping

3) Monitoring

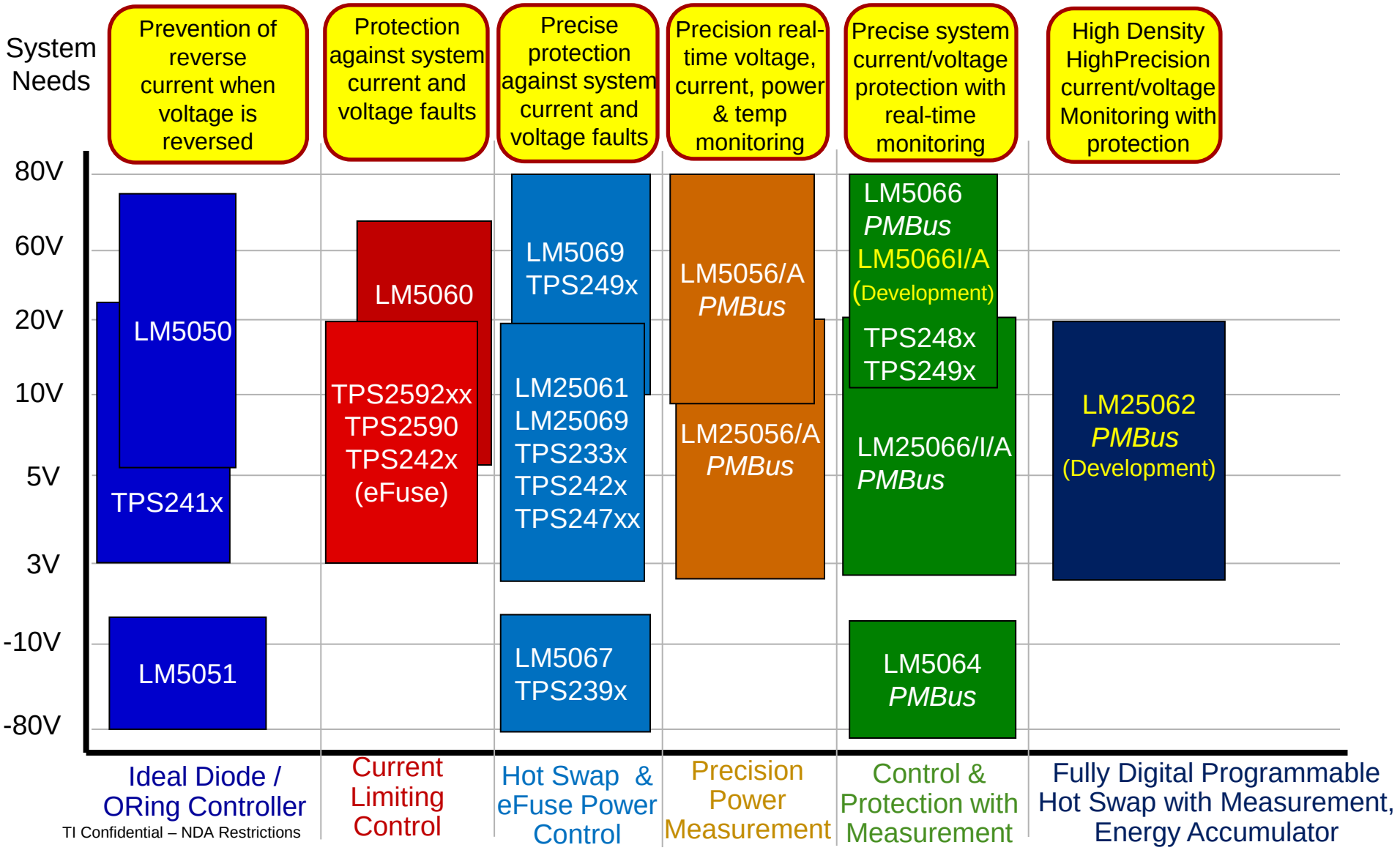
- Power Measurement
- Fault Monitoring
- Digital Interface

Different Degrees of Power System Protection

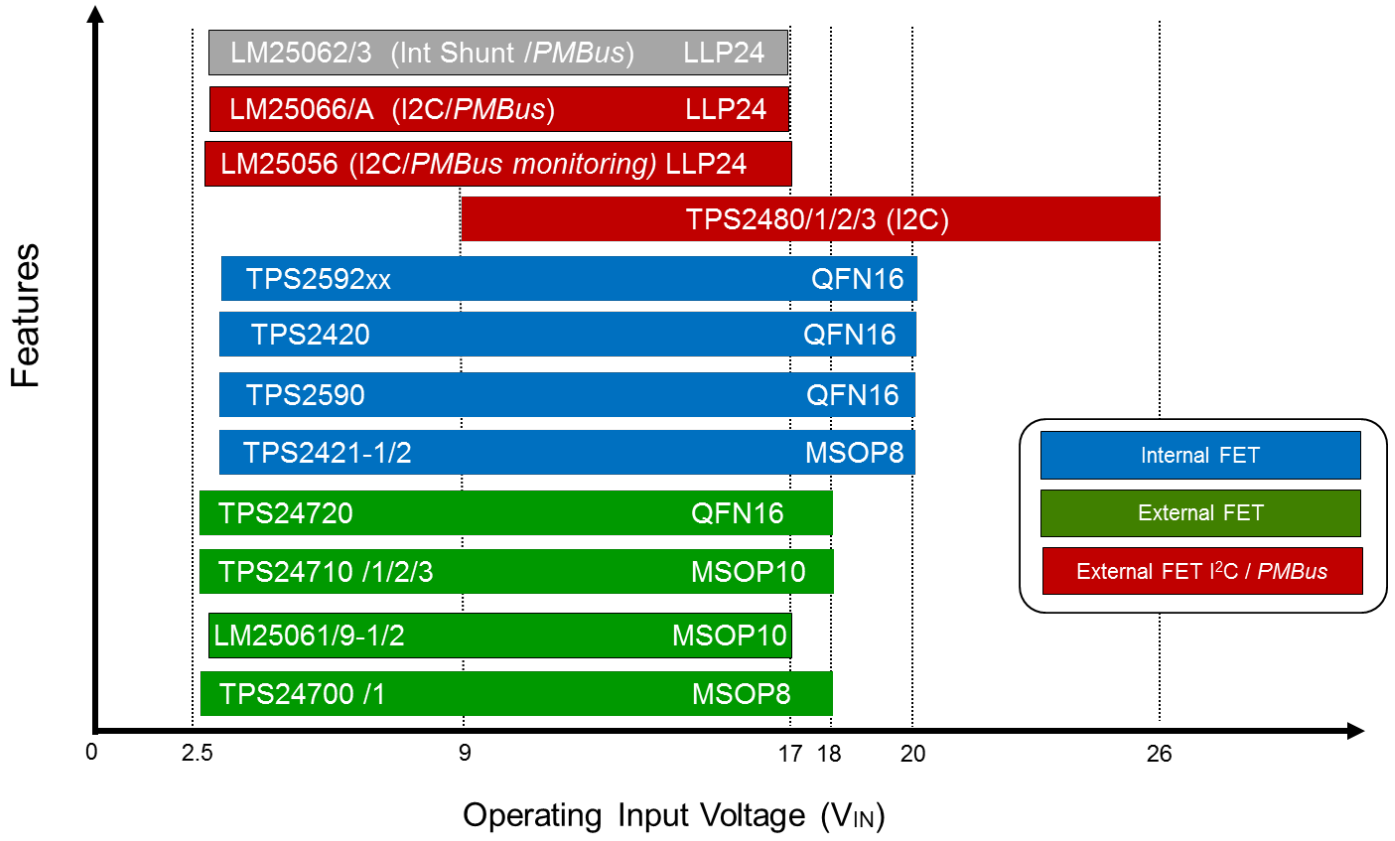


- **Why Protection Is Needed:**
  - **Hot Plug & Turn-On Event:** Large input capacitance on a card draws a large in-rush current when plugged in to backplane or at power up
  - **Fault Conditions:** During a fault condition large currents will flow
- **Device Protects and Isolates Faults:**
  - MOSFET, PoLs, Capacitors, PCB traces, and edge connectors can be damaged by high in-rush or fault currents
  - Prevents backplane supply voltage droop from resetting other line cards

System Protection and Management Portfolio



Protection Circuits for Server Applications



Computing/Storage/ Industrial

- Servers
- PCIe cards
- Micro TCA

Typical Input Voltage: 3V, 5V, 12V, 24V

- **Hot Swap:** LM25061/69, TPS233x, TPS242x, TPS245x, TPS247xx
- **ORing:** LM5050, TPS241x
- **Hot Swap + ORing:** TPS231x/2x/4x/5x/6x, TPS245x, TPS256x
- **Hot Swap + Monitoring:** LM25066/A, TPS2480/81/92/93
- **Power Monitoring IC:** LM25056

Current Monitor: Featured Parts

	Highest Accuracy Digital Power Monitor	Smallest Digital Power Monitor	Triple Channel Digital Current/Voltage Monitor	Current Sensing Comparator
	INA226	**INA231**	**INA3221**	**INA300**
Common Mode Range	0 to 36V	0 to 28V	0 to 26V	0V to 36V
Offset Voltage	10uV (max)	50uV (max)	80uV (max)	500uV (max)
Gain Error	0.1% (max)	0.5% (max)	0.25% (max)	N/A
Supply Range	2.7V to 5.5V	2.7V to 5.5V	2.7V to 5.5V	2.7V to 5.5V
Iq	420uA (max)	420uA (max)	450uA (max)	150uA (max)
Package	MSOP-10 3 x 4.9mm	WCSP 1.68 x 1.43mm	QFN 4 x 4mm	QFN 2 x 2mm

Temp Sensors: Featured Parts

	1.8V Drop-in to Industry Standard LM75	Highest Accuracy w/ Minimal Size & Power	Smallest & Lowest Power
	TMP75B / C	**TMP112**	**TMP103**
Type	Local	Local	Local
Accuracy (max)	+/-1C @ 0C to 70C +/-2C @ -25C to 85C +/-3C @ -40C to 125C	+/-0.5C @ 0C to 60C +/-1C @ -40C to 125C	+/-2C @ -10C to 100C +/-3C @ -40C to 125C
Supply Range	1.4V to 3.6V	1.4V to 3.6V	1.4V to 3.6V
Iq (max)	55uA (75B) 35uA (75C)	10uA	3uA
Package	MSOP - (3 x 4.9mm) SOIC - (4.9 x 6mm)	SOT-563 (1.6 x 1.6 mm)	WCSP (0.8 x 0.8mm)

	1.8V Capable Remote	3Ch. Remote	3Ch Remote w/ Power Monitoring
	TMP451	**TMP423**	**TMP513**
Accuracy (max)	+/-1C @ 0C to 70C +/-2C @ -40C to 125C	+/-1.5C @ 15C to 85C +/-2.5C @ -40C to 125C	+/-1C @ 15C to 85C +/-2.5C @ -40C to 125C
Series Resistance Cancellation	1k Ohm	3k Ohm	3k Ohm
N-Factor Correction	Yes	Yes	Yes
1.8V Capable I2C	Yes	No	No
Supply Range	1.7V to 3.6V	2.7V to 5.5V	3.0V to 26V
Iq (max)	40uA	38uA	1.4mA
Package	MSOP - (3 x 4.9mm) SOIC - (4.9 x 6mm)	SOT-23 (2.9 x 2.8 mm)	QFN (4.0 x 4.0mm) SOIC (9.9 x 6.0mm)

General Purpose Analog (Logic, I2C, ESD Protection, Multiplexers)

www.ti.com/logic

www.ti.com/i2c

www.ti.com/esd

www.yi.com/switches

TI Analog Portfolio:

Most Trusted Supply Chain Partner for Multi-source Products (Standard Linear and Logic)

Delivering the broadest standard linear and logic portfolio with supply continuity

Standard Linear

- Amplifiers and Comparators
- Interface ICs
- Power ICs

Functions

Comparators	Amplifiers
Buffers	Flip-Flop/Latches
Interface	Logic Gates
Linear Regulators	I²C Logic
LDO Regulators	Signal Switches
Buses	JTAG Logic
Voltage Supervisors	Drivers
Timers	Translators

& many more…

Standard Logic

- I²C
- Little Logic
- Voltage Level Translation
- Analog Switch
- Specialty Logic

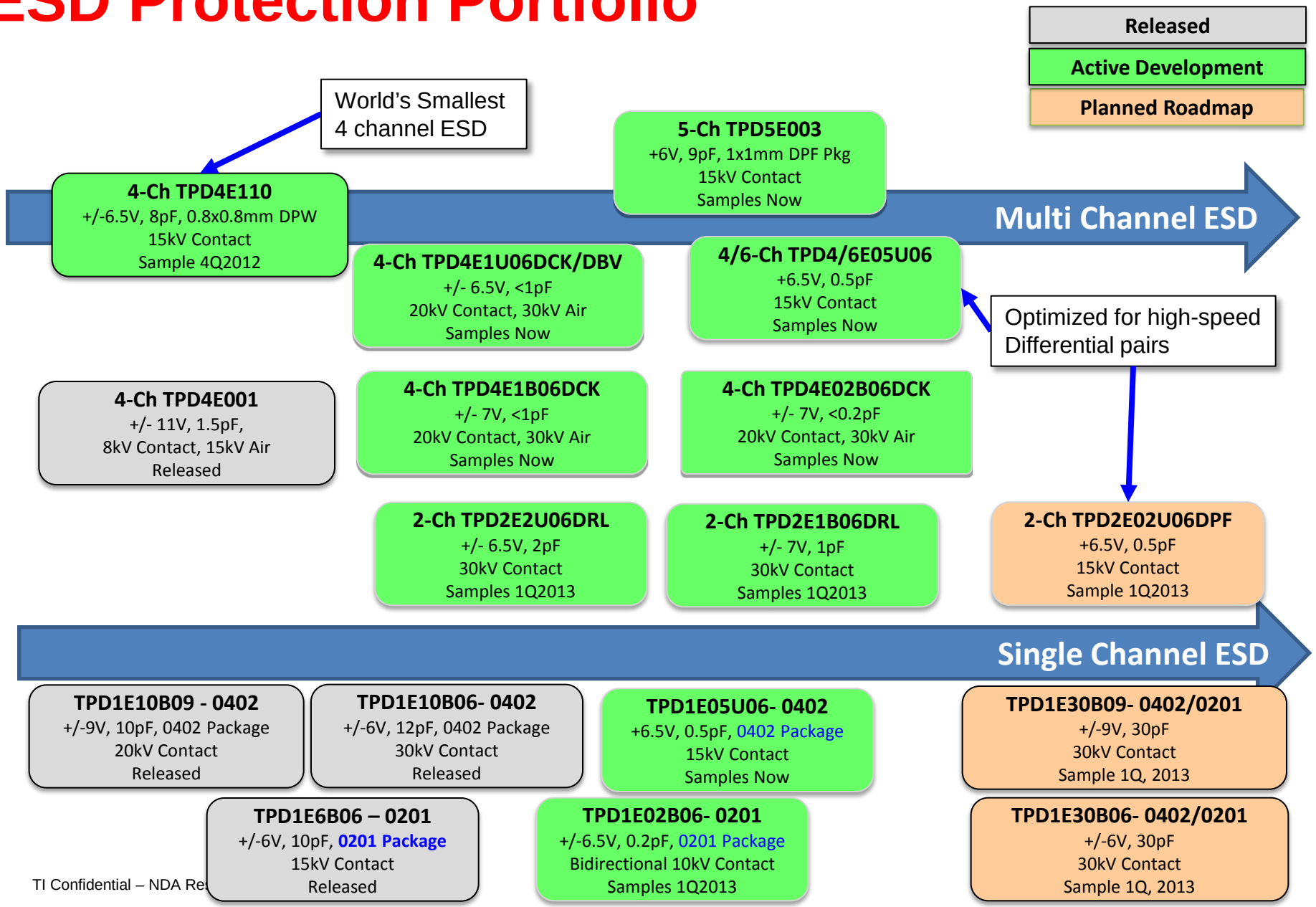
Supply Continuity

Industry's best lead times

Core, Safety, Surge

Broadest Portfolio

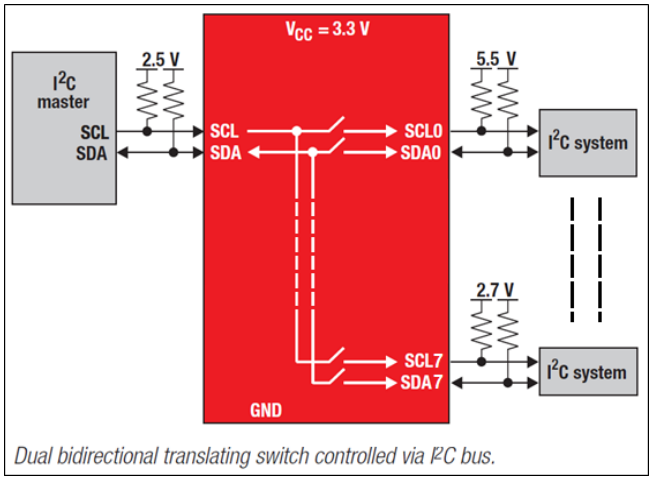
ESD Protection Portfolio



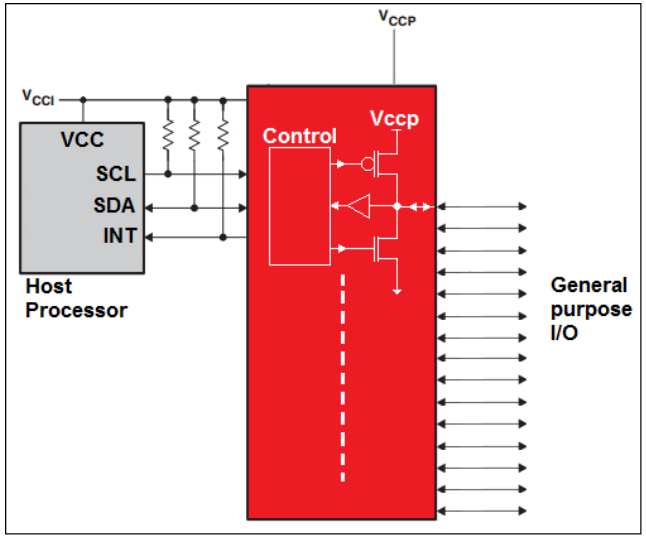
I²C Solutions

- TI I²C devices expand the capability of the most common subsystem communication bus
- Wider voltage range & lower power than competition
- I²C IO expanders provide more GPIO to increase flexibility
- I²C buffer/repeaters enable operation beyond maximum allowable bus capacitance
- I²C switches resolve address conflicts by switching in devices with the same address
- I²C translators support voltage level translation between buses in mixed voltage I²C systems

Device Categories	Features
I²C I/O Expanders	• Best solution for limited system I/Os • PCB complexity reduction
I²C Buffers and Repeaters	• Increases number of I²C devices on a single bus • Enables signals over longer traces and cables
I²C MUX/Switches	• Bus expansion/muxing • I²C bus isolation
I²C Specialty Functions	• Keypad controllers • LED Drivers



Dual bidirectional translating switch controlled via I²C bus.



IO Expander

Thank you!!!