TI_1_DVKIT

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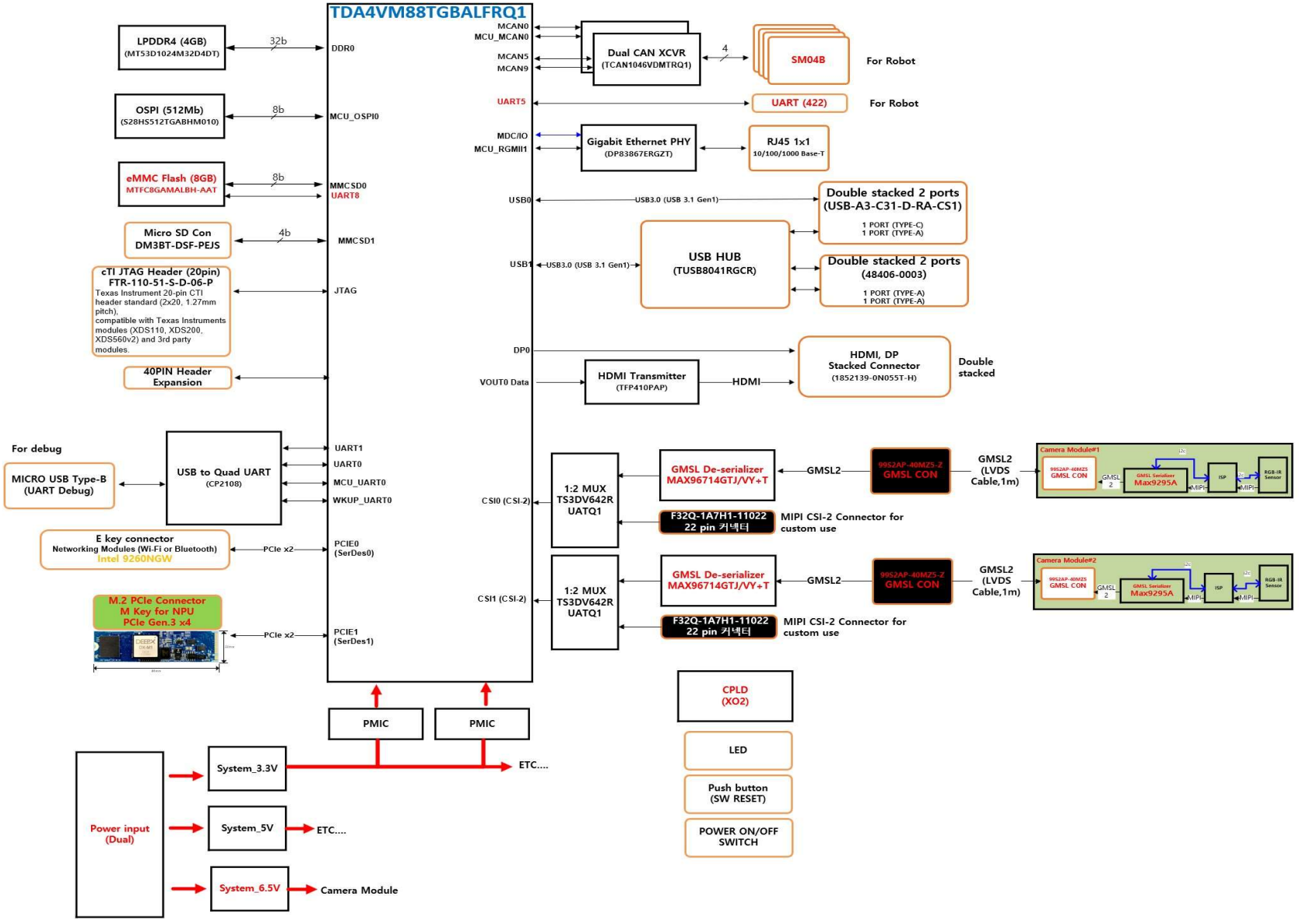
BLOCK DIAGRAM



DX SOLUTION

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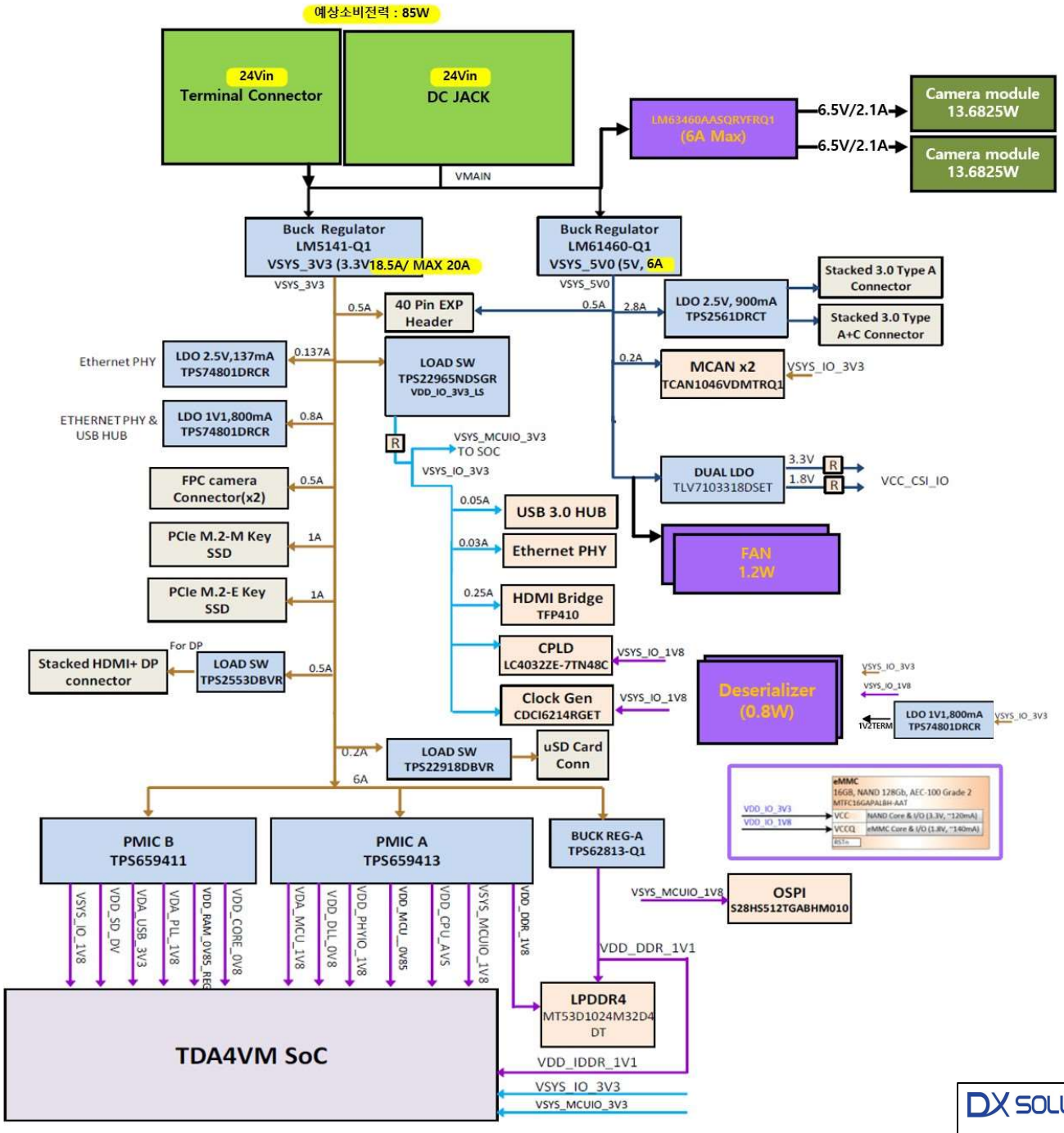
REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
	March 2024	1st release	Jaecheon Yoo	Taesan Lee	

FEATURE LIST

T1_1EVKIT	
항목	사양
CPU	ARM Cortex A72 Dual 64-bit (Up to 2.0GHz)
	ARM Cortex R5F Six (Up to1.0GHz)
RAM	32-Bit LPDDR4 4GB (2133MHz)
Memory	8GB eMMC, version 5.1 compliant for Boot
	4GByte LPDDR4 DRAM (2133 MHz)
	Secure Digital Card (Micro SD) Cage for general storage (up to 512GB)
	512 Mb Non-Volatile NOR OSPI Flash,
USB	USB3.1 (Gen1) Hub to 3x Type A (Host) USB3.1 (Gen1) 1x Type C (DFP and UFP modes)
Display	VESA Display Port (v1.4), supports 4K UHD with MST support
	DVI (v1.0) via HDMI Type A, supports 1080p
Camera Interfaces	GSML 2.0 two port or 2x MIPI CSI-2 FPC Connector (Selectable)
Ethernet Interface	Gigabit Ethernet (RJ45 Connector)
Can Interface	4x CAN-FD Headers (1x3) CONN HEADER SMD 4POS
Custom use interface	1x UART (422) 40-pin High Speed Connector (dual CSI-4L, I2C, GPIO, and so forth)
Debug	MICRO USB Type-B UART Interface
Ethernet Interface	Gigabit Ethernet (RJ45 Connector)
Expansion/Add-on	M.2 Key M Interface (PCIe/Gen3 x 2 Lane) for DeepX M1 NPU module
	M.2 Key E Interface (PCIe/Gen3 x 1 Lane, USB2.0, SDIO, I2S, UART, I2C) for custom use
Control/Indication	Push buttons (SW Reset, Power ON/OFF) LEDs (Power, User Defined, Ethernet Port Link/Act,FAN ERR LED)
Dimension	TBD
Operating Temperature	0C~+75C
Operating Humidity	+10 to +95 % (non condensing)
Power Input	Dual input Terminal Block Input (range : +19~+24V) DC Jack Input with AC Adaptor (range : TBD)

POWER FLOW DIAGRAM



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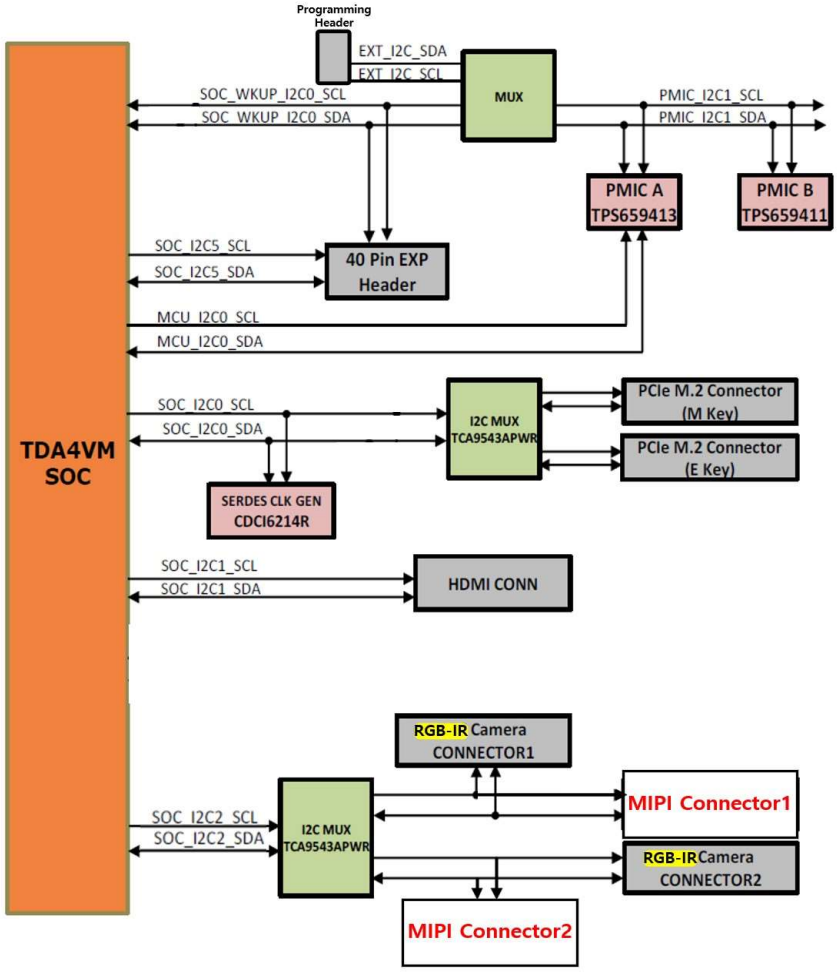
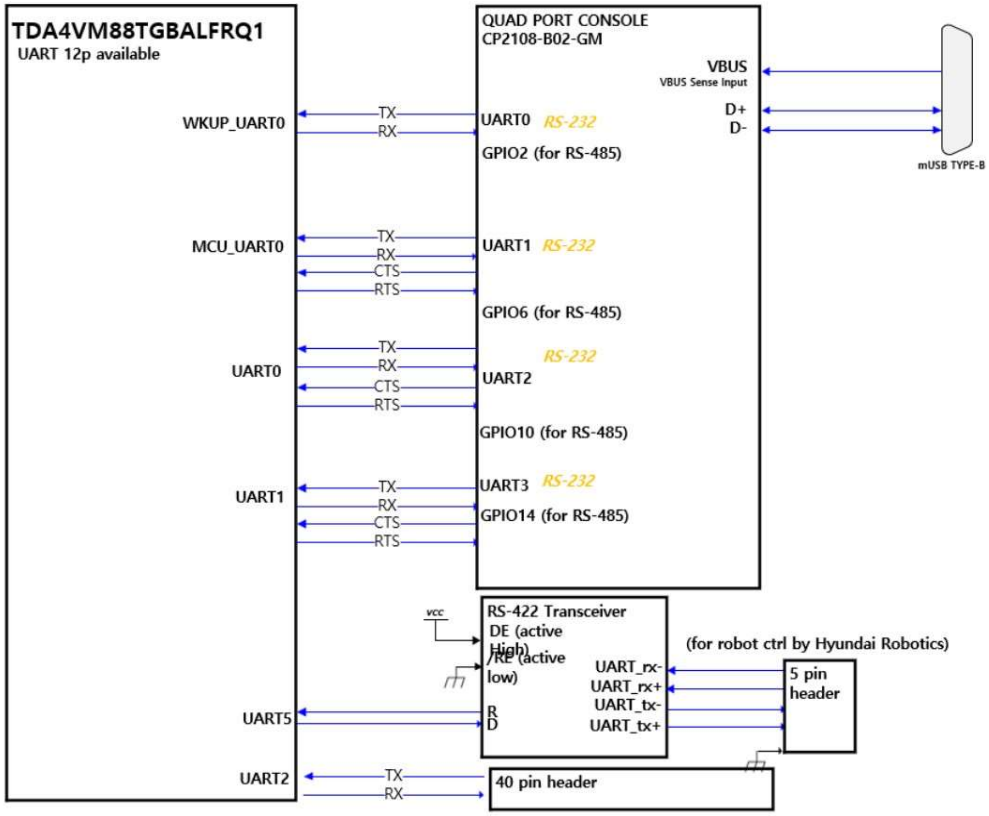
I2C TREE

I2C TREE



UART TREE



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3-Phase DUAL PMIC PDN Recommended for New Designs
(3-Phase Buck supplying VDD_CPU)

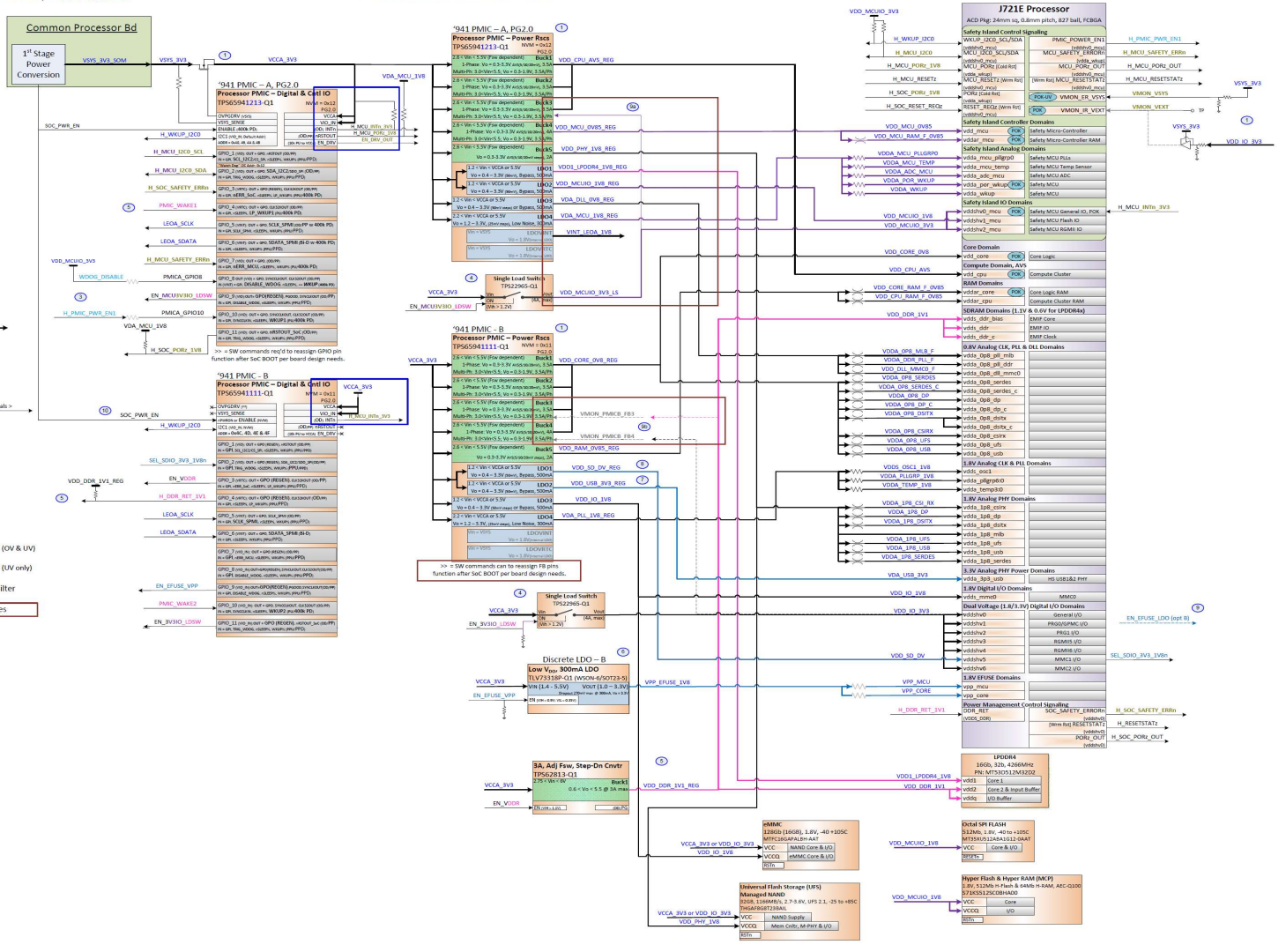
DRA829/TDA4VM 3-Phase Dual Leo2.0 PDN-0C
(Power Rail & GPIO Mapping Overview)

Leo PMIC-A, PN TPS6594**1213**RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = **13**, PG2.0)
Leo PMIC-B, PN TPS6594**1111**RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = **12**, PG2.0)

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable system with independent MCU & Main power for FFI
3. SDRAM: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash (SR1.1 only) & eMMC, UFS
5. Low power modes: MCU Only & DDR Retention
6. Signaling Levels: MCU & Main Dual VIO
7. End Product Options:
   a. Compliant high-speed SD Card
   b. Compliant USB 2.0 data eye
   c. HS SoC Efuse programming on-board

V0.14	1/27/2021	1. Added example of VDD_IO_3V3 OV/UV monitoring by SoC's VMON_IR_VEXT input connection option to voltage buffer & voltage R-div needed to interface with SoC's internal R-div network optimized for monitoring 1.8V power rails. 2. Added 2x ext voltage monitoring inputs options for OV/UV monitoring by Hera PMIC of any safety critical system power rails. Hera's quad buck config can reassign remote sense feedback inputs (FB3 & FB4) for power rail monitoring. 3. Updated notes 1 & 9 accordingly.
V0.15	2/13/2021	Following final PMIC NVM review for defining new common PN ("1213") for Leo PG2.0 used in PDN-0C & -1A: 1. Update notes 2. Changed PMIC-A FB3 VMON input to be connected to VCCA_3V3 since VDD_MCUIO_3V3 rail is not supported, see note 9a. 3. Added PMIC-B FB3 & FB4 assignment for VMON by SW after SoC boot for ext power rail monitoring options, see note 9b.
V0.16	3/2/2021	1. Removing discrete load switch from supplying PMIC's VIO_IN since PG2.0 PMICs validation testing confirms no excessive glitches on GPIO or reset signals during of NVM initialization. Related "Note #2" has been removed.



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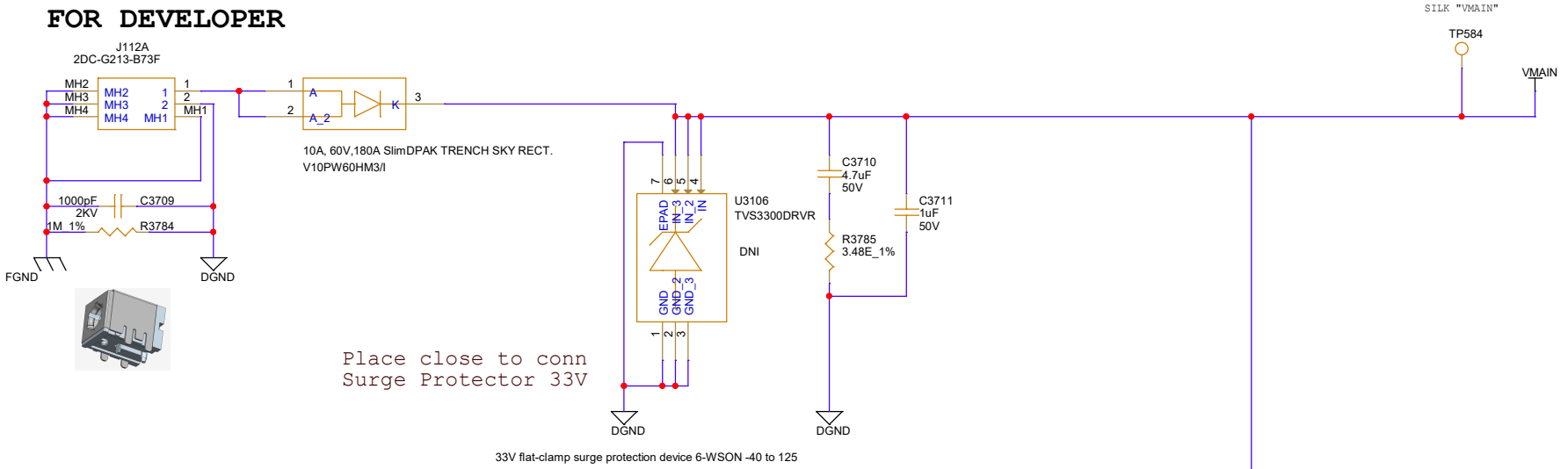
GPIO MAPPING TABLE

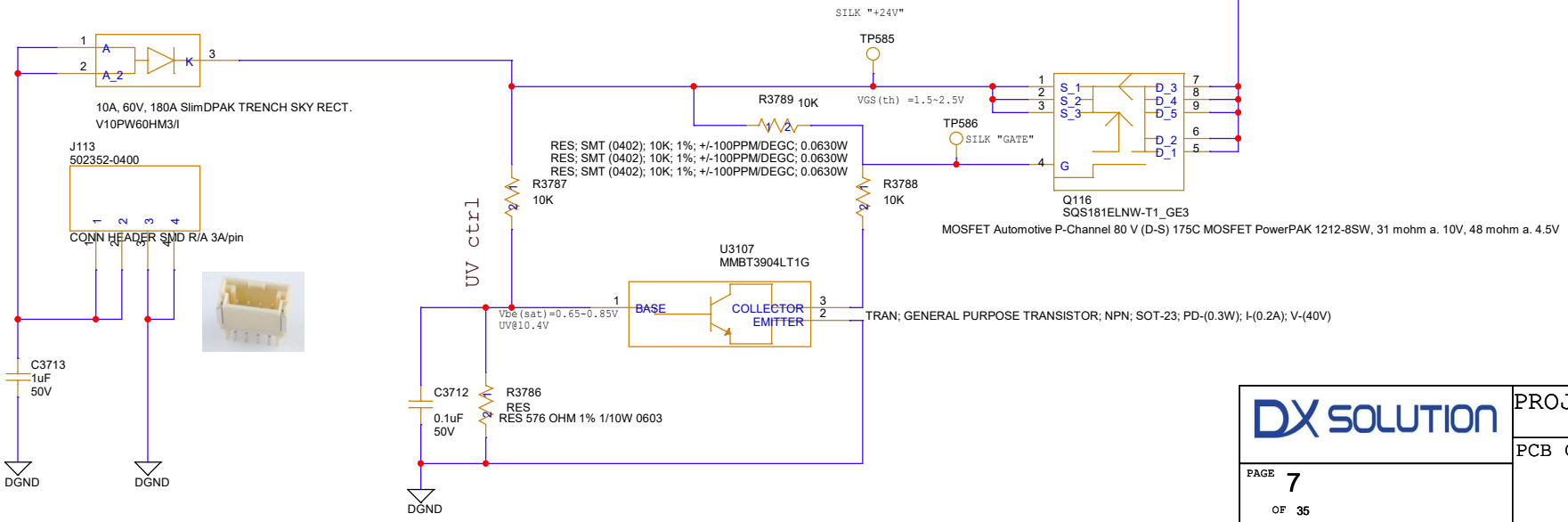
	Signal	GPIO	Net Name	Input/Output	IO LV	Default	State	Remarks
1	WKUP_GPIO0_3	WKUP_GPIO0_3	MCU_MCAN0_STB	Output	3.3V	NA	Active High	MCU CAN0 Standby
2	WKUP_GPIO0_4	WKUP_GPIO0_4	SOC_WAKE	Input	3.3V	PU	NA	SoC wake signal (Reset button)
3	WKUP_GPIO0_5	WKUP_GPIO0_5	BOARDID_EEPROM_WP	Output	3.3V	PD	Active High	Boot EEPROM Write protect
4	WKUP_GPIO0_6	WKUP_GPIO0_6	SOC_INTZz	Input	3.3V	PU	Active Low	Test Automation SOC Interrupt -> None
5	WKUP_GPIO0_7	WKUP_GPIO0_7	H_MCU_INT#	Input	3.3V	PU	NA	MCU domain Interrupt from PMIC A,B
6	WKUP_GPIO0_8	WKUP_GPIO0_8	GPIO_uSD_PWR_EN	Output	3.3V	PU	Active High	GPIO for micro SD card power load switch power enable
7	WKUP_GPIO0_9	WKUP_GPIO0_9	SEL_SDIO_3V3_1V8n	Output	3.3V	PU	Active Low	VDD_SD_DV 1.8V or 3.3V selection control
8	MCU_OSPI1_DQS	WKUP_GPIO0_31	MCU_OSPI0_INT#	Output	1.8V	PU	Active Low	OSPI Interrupt Pin
9	WKUP_GPIO0_10	WKUP_GPIO0_10	GPIO_RGMII3_RST#	Output	3.3V	NA	Active Low	Used as a reset signal for PRG0 Ethernet PHY Chip
10	WKUP_GPIO0_11	WKUP_GPIO0_11	SOC_PCIe1_M.2_RTSz	Output	3.3V	NA	NA	PCIe M.2 M key reset signal
11	MCU_OSPI1_D0	WKUP_GPIO0_32	CPLD_TCK	I/O	1.8V	PD	NA	JTAG Signals for CPLD
12	MCU_OSPI1_D1	WKUP_GPIO0_33	CPLD_TDI	I/O	1.8V	NA	NA	JTAG Signals for CPLD
13	MCU_OSPI1_D2	WKUP_GPIO0_34	CPLD_TDO	I/O	1.8V	NA	NA	JTAG Signals for CPLD
14	MCU_OSPI1_D3	WKUP_GPIO0_35	CPLD_TMS	I/O	1.8V	PU	NA	JTAG Signals for CPLD
15	MCU_OSPI1_CSN0	WKUP_GPIO0_36	M2_SDIO_RESET#	Output	1.8V	PU	Active Low	Reset to SDIO(WiFi) Interface for PCIe M.2 E key
16	MCU_OSPI1_CSN1	WKUP_GPIO0_37	M2_SDIO_WAKE#	Output	1.8V	PU	Active Low	Wake to SDIO(WiFi) Interface for PCIe M.2 E key
17	MCU_SPI0_CS0	WKUP_GPIO0_55	SYS_MCU_PWRDN	Output	3.3V	PD	Active High	System Power Down ('0' - normal operation, '1' - system power down)
18	PMIC_POWER_EN0	WKUP_GPIO0_66	RGMII_INT#	Input	3.3V	PU	NA	Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
19	PRG1_PRU0_GPO4	GPIO0_5	40 Pin EXP Hdr - GPIO1	I/O	3.3V	NA	NA	
20	PRG1_PRU0_GPO6	GPIO0_7	40 Pin EXP Hdr - GPIO2	I/O	3.3V	NA	NA	
21	PRG1_PRU0_GPO7	GPIO0_8	40 Pin EXP Hdr - GPIO3	I/O	3.3V	NA	NA	
22	PRG1_PRU0_GPO10	GPIO0_11	40 Pin EXP Hdr - GPIO4	I/O	3.3V	NA	NA	
23	PRG0_PRU1_GPO8	GPIO0_71	40 Pin EXP Hdr - GPIO5	I/O	3.3V	NA	NA	
24	PRG0_PRU1_GPO19	GPIO0_82	40 Pin EXP Hdr - GPIO6	I/O	3.3V	NA	NA	
25	RGMII6_TX_CTL	GPIO0_97	40 Pin EXP Hdr - GPIO7	I/O	3.3V	NA	NA	
26	SPI0_D1	GPIO0_115	40 Pin EXP Hdr - GPIO8	I/O	3.3V	NA	NA	
27	PRG0_PRU0_GPO18	GPIO0_61	M.2_W_DISABLE1#	Output	3.3V	PU	Active Low	WiFi disable1 signal for PCIe M.2 E key
28	PRG0_PRU0_GPO19	GPIO0_62	M.2_W_DISABLE2#	Output	3.3V	PU	Active Low	WiFi disable2 signal for PCIe M.2 E key
29	PRG0_PRU1_GPO1	GPIO0_64	USER_LED1	Output	3.3V	PU	Active Low	USER LED enable signal
30	PRG0_PRU1_GPO2	GPIO0_65	MCAN0_STB	Output	3.3V	NA	Active High	MCAN0 Standby
31	PRG0_PRU1_GPO3	GPIO0_66	MCAN5_STB	Output	3.3V	NA	Active High	MCAN5 Standby
32	PRG0_PRU1_GPO4	GPIO0_67	MCAN9_STB	Output	3.3V	NA	Active High	MCAN9 Standby
33	PRG0_PRU1_GPO9	GPIO0_72	UART8_RXD	Output	3.3V	NA	NA	PCIe M.2 E key reset signal -> UART8
34	PRG0_PRU1_GPO11	GPIO0_74	GPIO0_74->SOC_CAM0_GPIO1	I/O	3.3V	NA	NA	CSI2 Expansion Board Specific. ->FPC Camera0 GPIO LED indicator (Nvida)
35	PRG0_PRU1_GPO12	GPIO0_75	UART8_CTSn	Output	3.3V	NA	NA	CSI3 Expansion Board Specific. -> UART8
36	PRG0_PRU1_GPO13	GPIO0_76	UART8_RTSn	Output	3.3V	NA	NA	CSI4 Expansion Board Specific. -> UART8
37	PRG0_PRU1_GPO14	GPIO0_77	GPIO0_77->SOC_CAM0_GPIO2	I/O	3.3V	NA	NA	CSI5 Expansion Board Specific. -> FPC Camera0 GPIO Power Enable (Nvida)
38	PRG0_PRU1_GPO15	GPIO0_78	GPIO0_78->CSI_VIO_SEL	Output	3.3V	PU	NA	CSI6 Expansion Board Specific. ->CSI Dual IO selection 0 : 1.8V 1: 3.3V (Default)
39	PRG0_PRU1_GPO16	GPIO0_79	GPIO0_79->SOC_CAM1_GPIO1	I/O	3.3V	NA	NA	CSI7 Expansion Board Specific. -> FPC Camera1 GPIO LED indicator (Nvida)
40	SPI0_CS0	GPIO0_111	DP0_3V3_EN	Output	3.3V	PD	Active High	Display Port Load Switch enable
41	SPI1_CS0	GPIO0_116	SOC_CAM0_GPIO1 -> UART5_RXD	NA	NA	NA	NA	FPC Camera0 GPIO -> UART5_RXD
42	SPI1_CS1	GPIO0_117	SOC_CAM0_GPIO2 -> UART5_TXD	NA	NA	NA	NA	FPC Camera0 GPIO -> UART5_TXD
43	SPI1_CLK	GPIO0_118	CSI_VIO_SEL -> UART5_CTSn	NA	NA	NA	NA	CSI Dual IO selection 1.8V or 3.3V selection -> UART5_CTSn
44	SPI1_D0	GPIO0_119	SOC_CAM1_GPIO1 -> UART5_RTSn	NA	NA	NA	NA	FPC Camera1 GPIO -> UART5_RTSn
45	SPI1_D1	GPIO0_120	SOC_CAM1_GPIO2	I/O	3.3V	NA	NA	FPC Camera1 GPIO Power Enable (Nvida)
46	UART1_CTSN	GPIO0_127	HDMI_PDn	Output	3.3V	PD	Active Low	HDMI power down signal
47	UART1_RTSN	GPIO1_0	HDMI_HPD	Input	3.3V	NA	NA	HDMI hot plug detect
48	RGMII5_TD2	GPIO0_88	CSI_MUX_SEL_2	Output	3.3V	PD	NA	CSI I2C MUX select(default 1.8V)
49	RGMII5_TD3	GPIO0_87	HDMI_LS_OE	Output	3.3V	PU	Active Low	Enable signal for supply load switch for HDMI Connector
50	RGMII5_RD1	GPIO0_95	BT_UART_WAKE#	Output	3.3V	PU	Active Low	Wake signal for Bluetooth(PCIe M.2 E key)
51	MCAN1_RX	GPIO1_3	USBC_DIR	Input	3.3V	PU	NA	USB C direction indication(Low-Position 1,High-Position 2)
52	prg0_pru1_gpo6	GPIO0_69	SOC_PCIe0_M.2_RTSz	Output	3.3V	NA	NA	PCIe M.2 E key reset signal
53	prg0_pru0_gpo0	GPIO0_43	JAHWA_EN	Output	3.3V	NA	Active High	"0 : Camera Module POWER OFF/ 1 : POWER ON
54	prg0_pru1_gpo0	GPIO0_63	HW_RST	Output	3.3V	PD	Active High	To effectively disable the output, the EN/SYNC input must stay low for longer than 28 µs"
55	PRG0_PRU0_GPO1	GPIO0_44	FAN_ERR_LED	Output	3.3V	PU	Active Low	HW RESET 0 : normal state 1 : HW reset
56	PRG0_PRU0_GPO2	GPIO0_45	FAN_STT	Input	3.3V	PU		FAN ERR LED 0 : FAN ERR 1: FAN Normal operatioin
57	PRG0_PRU0_GPO3	GPIO0_46	FAN_ON	Output	3.3V	PU	Active High	1 : FAN RUN 0: FAN LOCK or OFF Status
58	prg0_pru0_gpo4	GPIO0_47	GMSL_ERR_1	Input	3.3V	PU		FAN ON/OFF ctrl 0: FAN OFF 1: FAN ON
59	rgmii6_rxc	GPIO0_104	GMSL_PWDNB_1	Output	3.3V	PU	Active Low	Deserializer#1 Function Pin : MFP8 ERRB: Open-Drain Error Indication Output with 40kΩ Pullup to VDDIO. ERRB low indicates an error has been detected
60	prg0_pru0_gpo6	GPIO0_49	LMN1_1	Input	3.3V	PU		Deserializer#1 PWDNB: Active-low, Input with a 1MΩ pulldown to ground. Set low to enter power-down mode.
61	rgmii5_tx_ctl	GPIO0_85	LMN1_2	Input	3.3V	PU		Deserializer#1 GPIO7: Configurable General-Purpose I/O.
62	rgmii6_rx_ctl	GPIO0_98	GMSL_PWDNB_2	Output	3.3V	PU	Active Low	Deserializer#2 GPIO7: Configurable General-Purpose I/O.
63	rgmii6_txc	GPIO0_103	GMSL_ERR_2	Input	3.3V	PU		Deserializer#2 PWDNB: Active-low, Input with a 1MΩ pulldown to ground. Set low to enter power-down mode.
64	prg0_pru0_gpo9	GPIO0_52	MFP0_1	Input	3.3V	PU		Deserializer#2 Function Pin : MFP8 ERRB: Open-Drain Error Indication Output with 40kΩ Pullup to VDDIO. ERRB low indicates an error has been detected
65	prg0_pru0_gpo10	GPIO0_53	MFP1_1	NA	3.3V			Deserializer#1 FSYNC_OUT or Configurable General-Purpose I/O.
66	prg0_pru0_gpo11	GPIO0_54	MFP2_1	Input	3.3V	PU		Deserializer#1 SDA1 or Configurable General-Purpose I/O.
67	prg0_pru0_gpo12	GPIO0_55	MFP5_1	Input	3.3V	PU		Deserializer#1 FSYNC_OUT or Configurable General-Purpose I/O.
68	prg0_pru0_gpo13	GPIO0_56	MFP0_2	Input	3.3V	PU		Deserializer#1 LOCK Configurable General-Purpose I/O.
69	prg0_pru0_gpo14	GPIO0_57	MFP1_2	NA	3.3V			Deserializer#2 FSYNC_OUT or Configurable General-Purpose I/O.
70	prg0_pru0_gpo15	GPIO0_58	MFP2_2	Input	3.3V	PU		Deserializer#2 SDA1 or Configurable General-Purpose I/O.
71	prg0_pru0_gpo16	GPIO0_59	MFP5_2	Input	3.3V	PU		Deserializer#2 FSYNC_OUT or Configurable General-Purpose I/O.
72	PRG0_PRU1_GPO14	GPIO0_77	CAM_EN_0	Output	3.3V	PU		Deserializer#2 LOCK Configurable General-Purpose I/O.
73	PRG0_PRU1_GPO16	GPIO0_79	CAM_LED_1	Output	3.3V	PU		CAM#1 Power Enable
74	PRG0_PRU1_GPO11	GPIO0_74	CAM_LED_0	Output	3.3V	PU		CAM#2 LED indicator
75	SPI1_D1	GPIO0_120	CAM_EN_1	Output	3.3V	PU		CAM#1 LED indicator
								CAM#2 Power Enable

Dual Power Input (12V AC Adaptor)

FOR DEVELOPER



Dual Power Input (19V-24V DC Terminal)



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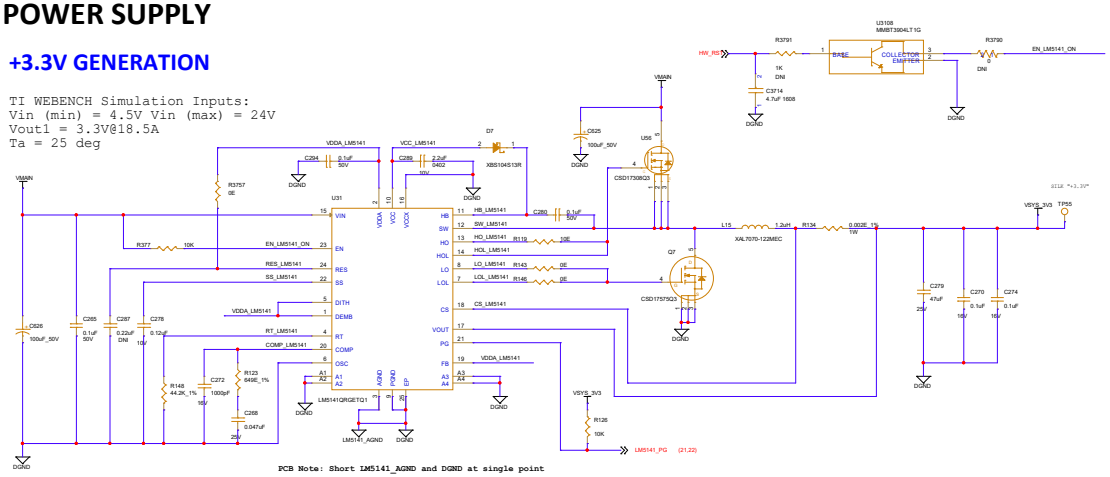
POWER SUPPLY

+3.3V GENERATION

TI WEBENCH Simulation Inputs:
Vin (min) = 4.5V Vin (max) = 24V
Vout1 = 3.3V@18.5A
Ta = 25 deg

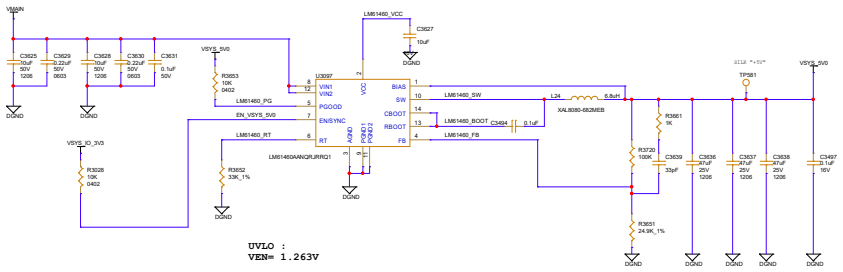


PCB Note: Short LM5141_AGND and DGND at single point

UVLO : 3.4V
VIL : 0.8V / VIH : 2.0V

+5.0V GENERATION

LM61460 5V BUCK REGULATOR
VinMin = 12V
VinMax = 36V
Vout = 5.0V
Iout = 6A

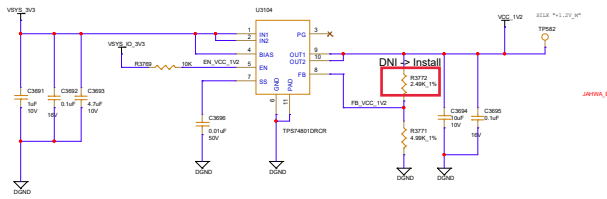


UVLO :
VEN= 1.263V

DESERIALIZER POWER

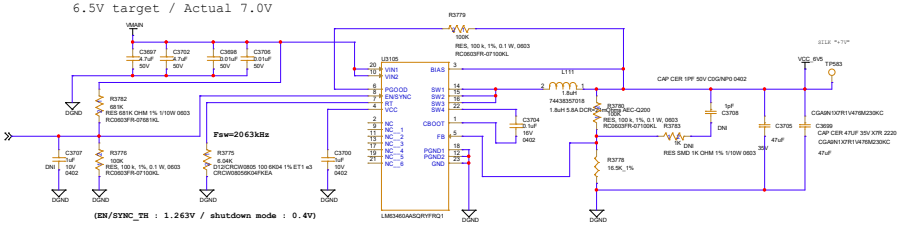
3.3V to 1.2V LDO

Iout=550mA



+7.0V Camera Module POWER

6.5V/4.2A
6.5V target / Actual 7.0V

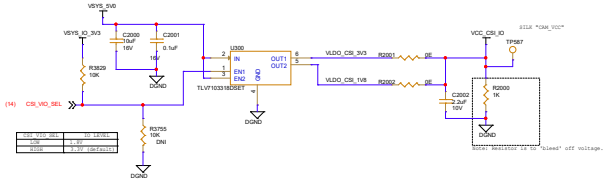


(EN/SYNC_TH : 1.263V / shutdown mode : 0.4V)

UVLO
turn on : 9.9V /turn off : 7.128V

EN/SYNC Level
VMAIN : 24V -> 3.072V / 12V -> 1.53V

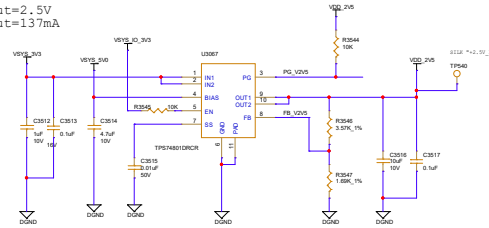
CAMERA IO SUPPLY SELECTION



ETHERNET POWER

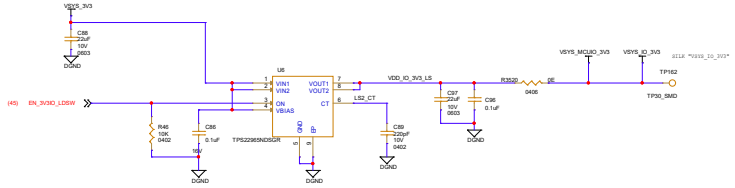
3.3V to 2.5V LDO

Vout=2.5V
Iout=137mA



+3.3V LOAD SWITCH

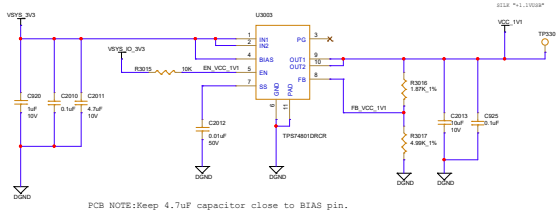
USB HUB / PHY / HDMI / CPLD / Clock Gen / TDA4VM



USB HUB & ETHERNET POWER

3.3V to 1.1V LDO

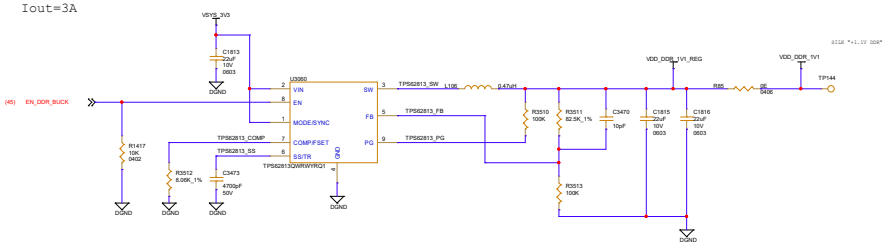
Vout=1.1V
Iout=888mA



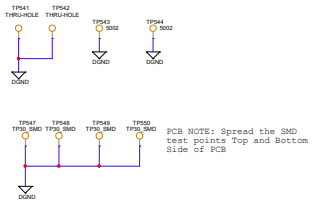
PCB NOTE:Keep 4.7uF capacitor close to BIAS pin.

+1.1V LPDDR4 & TDA4VM EMIF POWER

Vout=1.1V
Iout=3A



GROUND TEST POINTS



PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

DX SOLUTION	PROJECT	TI_1_DVKIT
	PCB CODE (REV)	DX-S2-001-A0(O)
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EVM's 3-Phase DUAL PMIC Power Distribution Network (PDN)

(3-Phase Buck supplying VDD_CPU)

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

PMIC- A

Route as Pseudo differential pair trace
(See "PCB Notes")

Programming Header

J15 — 62000311121 CON HDR 1X3 2.00MM PITCH ST TH

U60 — CCBTLV3257MPWREP

OEn	S	Bit State
0	0	A = B1
0	1	A = B2
1	X	Open

Install Shunt/Jumpers while programming PMIC on J21

U17 — PTPS65941213RWERQ1

U21 — SN74LVC1G07DRLRG4

PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

(EVM Bd Setting Default):

LEOA_WDOG_DISABLE	PD (Low)	Enable WDOG
	PU (High)	Disable WDOG

PROJECT	TI_1_DVKIT
PCB CODE (REV)	DX-S2-001-A0(O)
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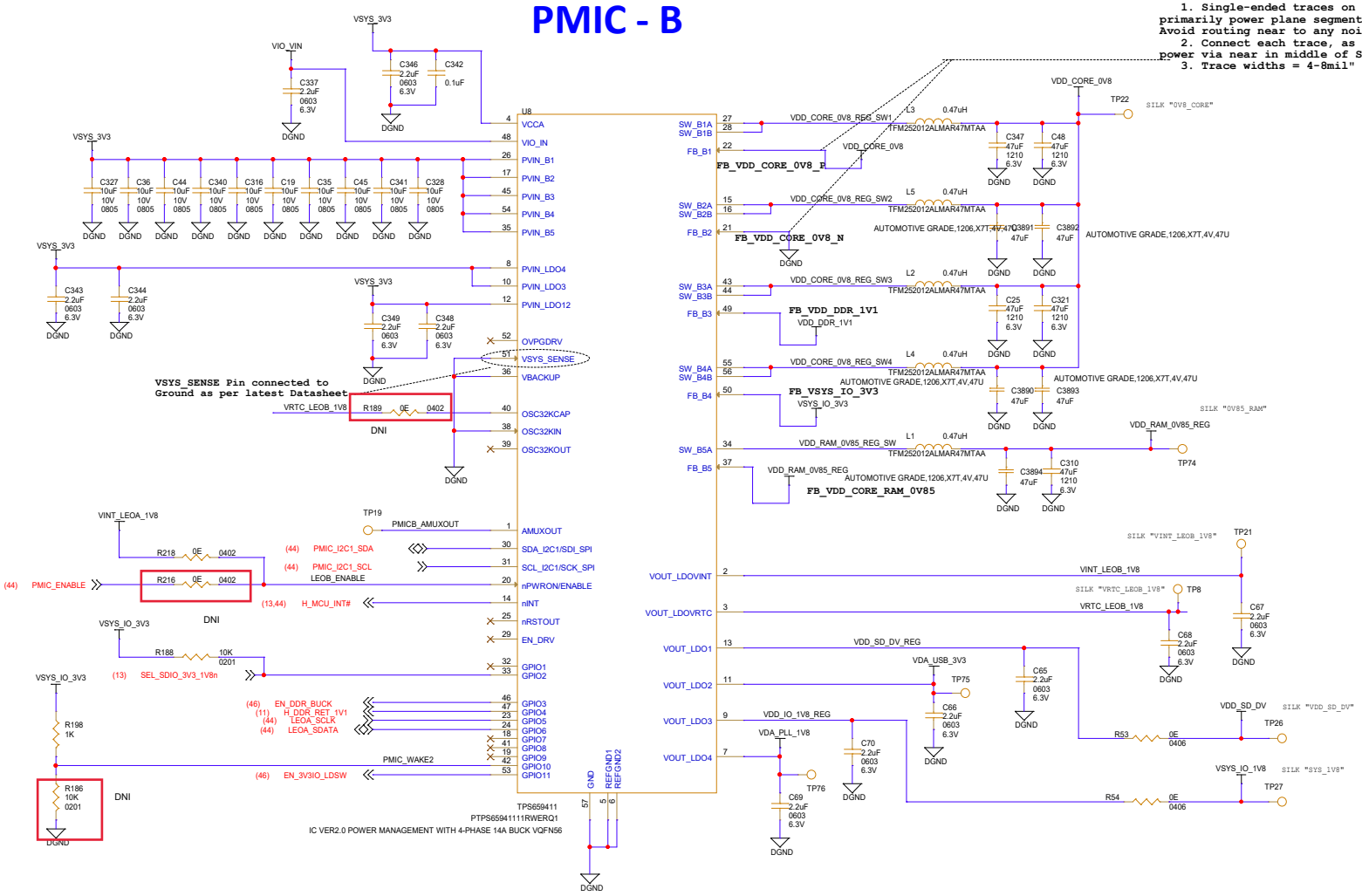
"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

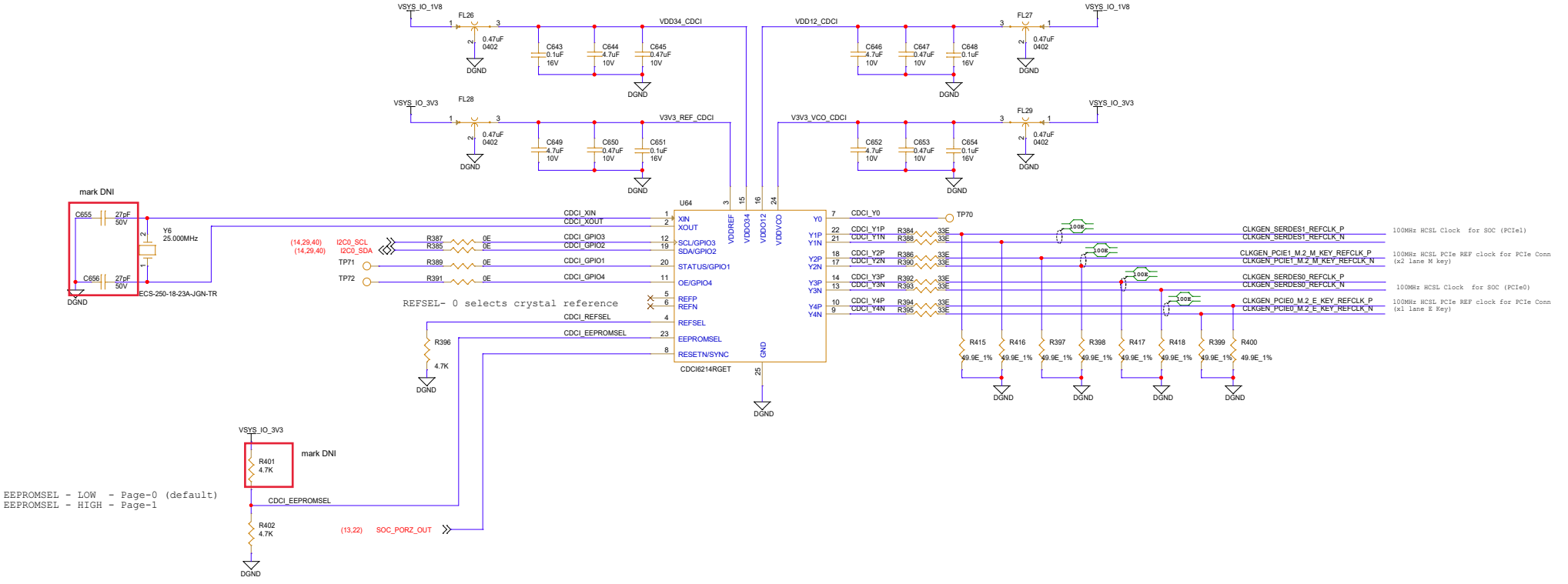
PMIC - B



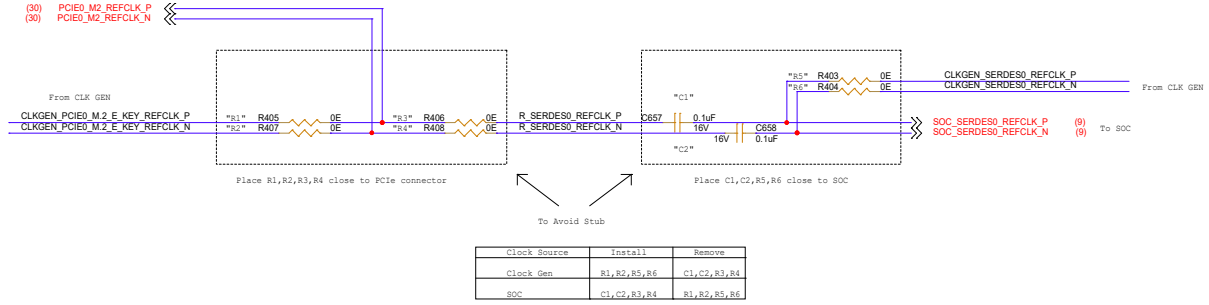
PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

DX SOLUTION	PROJECT TI_1_DVKIT
PAGE 10 OF 35	PCB CODE (REV) DX-S2-001-A0(O)

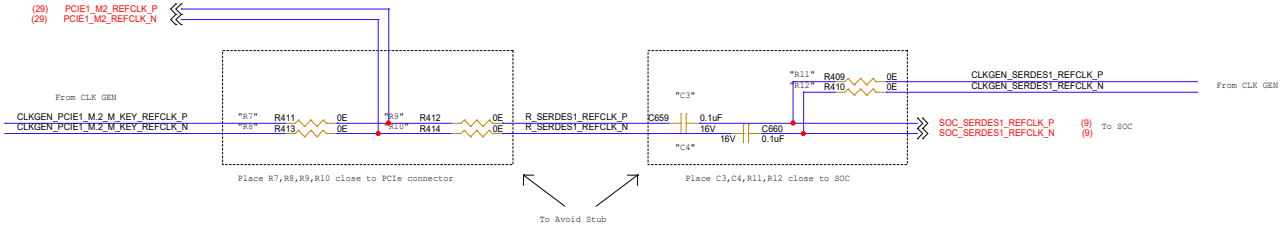
SERDES CLOCK GENERATOR



CLOCK ROOT SELECTION



Clock Source	Install	Remove
Clock Gen	R1,R2,R5,R6	C1,C2,R3,R4
SOC	C1,C2,R3,R4	R1,R2,R5,R6



Clock Source	Install	Remove
Clock Gen	R7,R8,R11,R12	C3,C4,R9,R10
SOC	C3,C4,R9,R10	R7,R8,R11,R12

DX SOLUTION

PROJECT TI_1_DVKIT

PCB CODE (REV)

DX-S2-001-A0(O)

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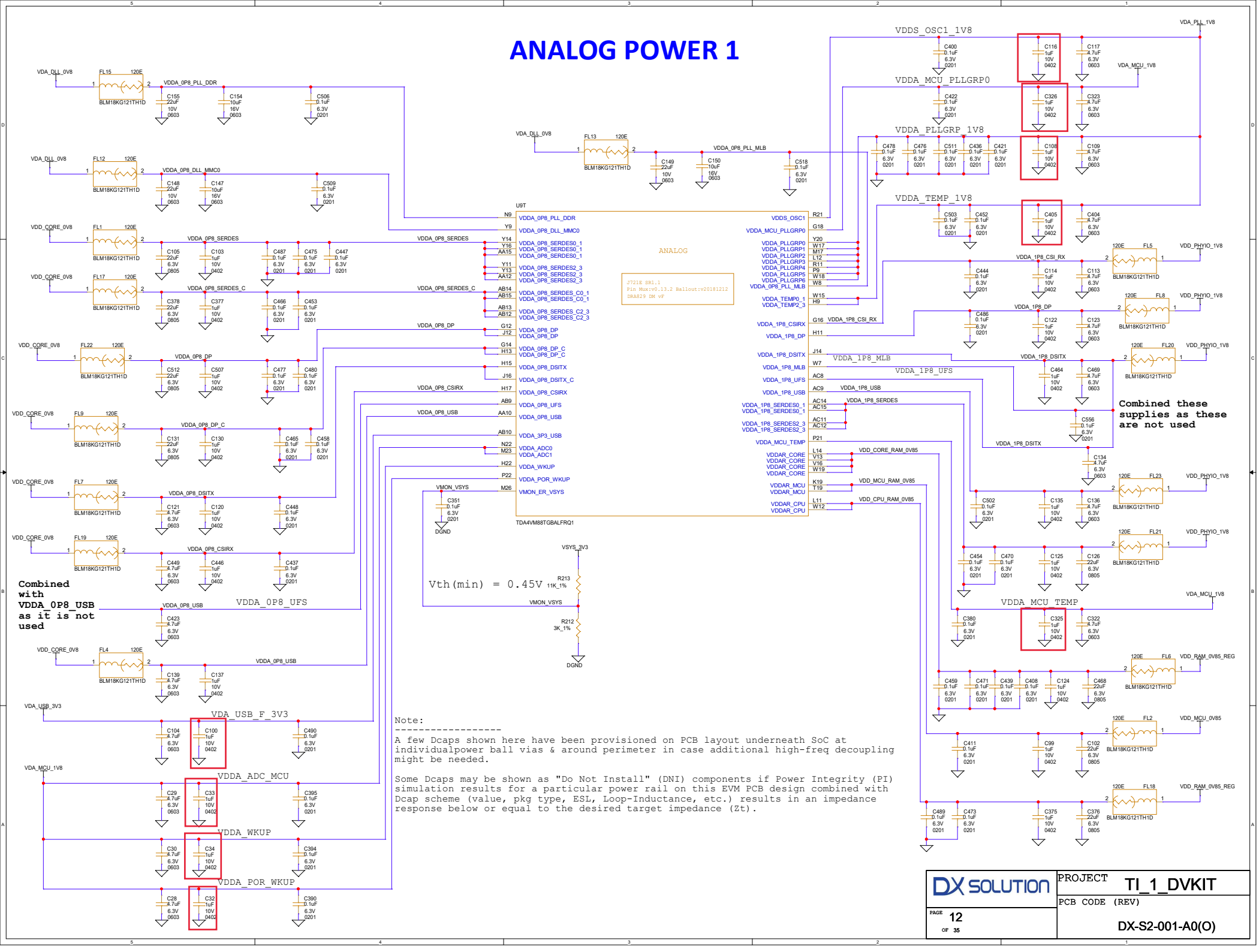
ANALOG POWER 1



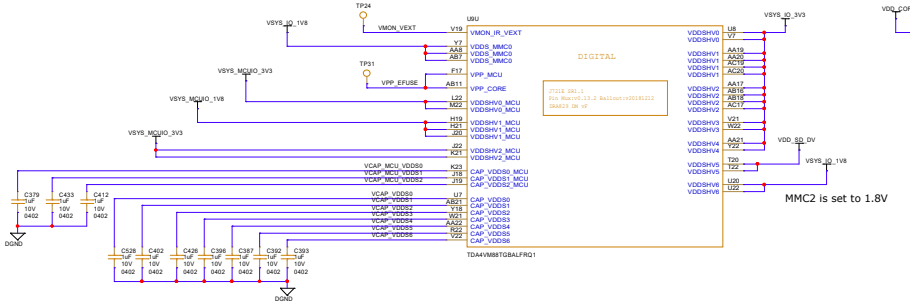
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

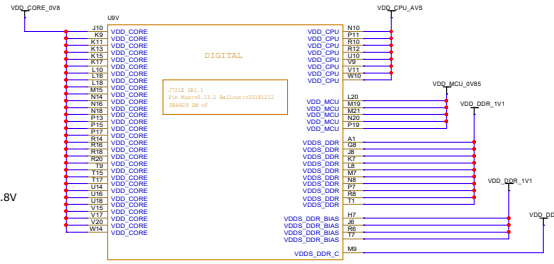
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

DX SOLUTION	PROJECT TI_1_DVKIT
PAGE 12 OF 35	PCB CODE (REV) DX-S2-001-A0(O)

DIGITAL POWER



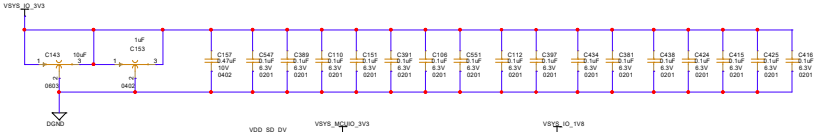
MMC2 is set to 1.8V

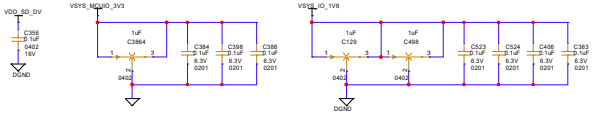


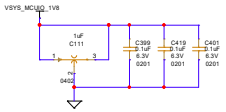
Note:

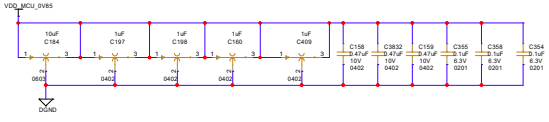
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

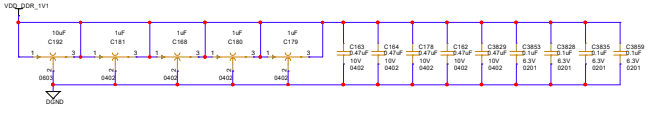
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

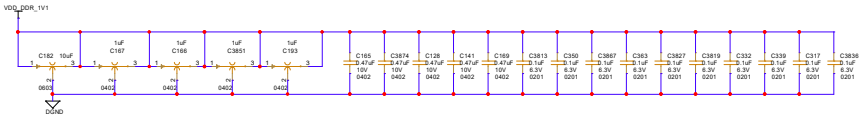


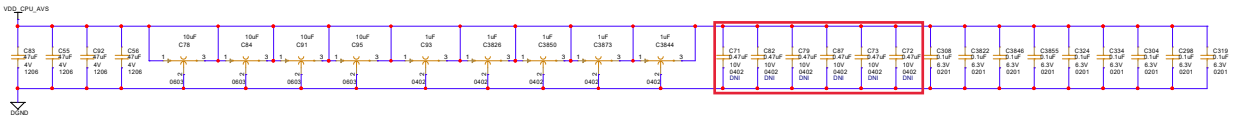


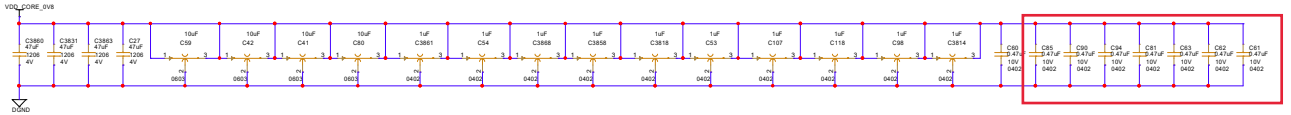


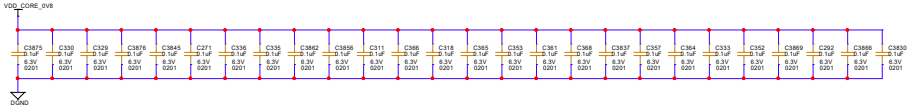








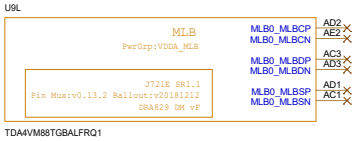




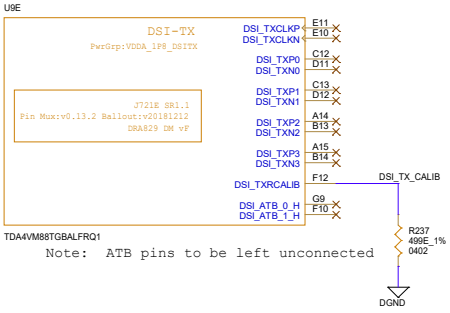
DX SOLUTION	PROJECT: TI_1_DVKIT
PAGE 13 OF 35	PCB CODE (REV): DX-S2-001-A0(O)

UNUSED BLOCK

MLB

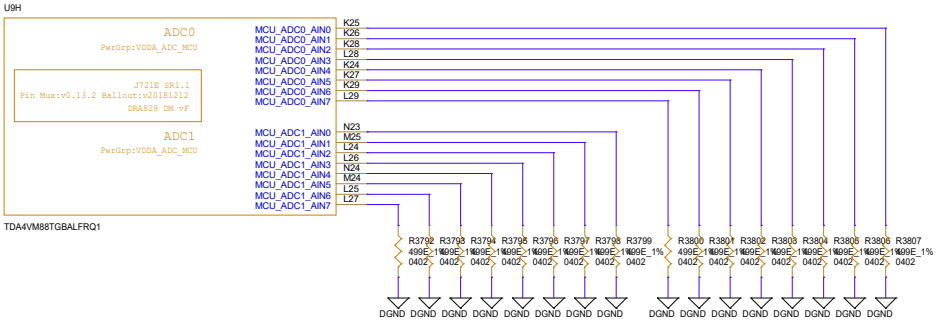


DSI

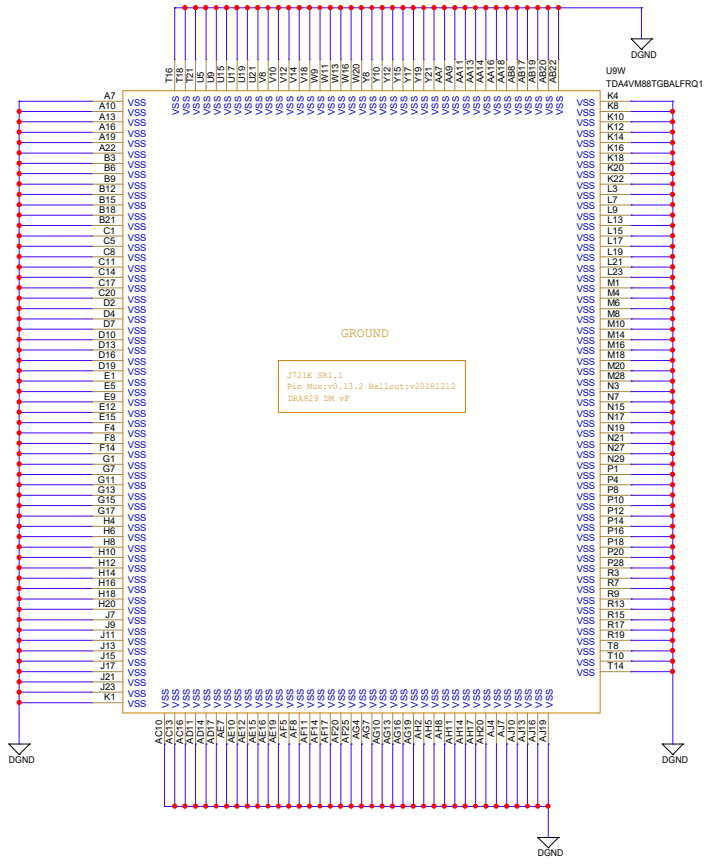


Note: ATB pins to be left unconnected

MCU ADCs

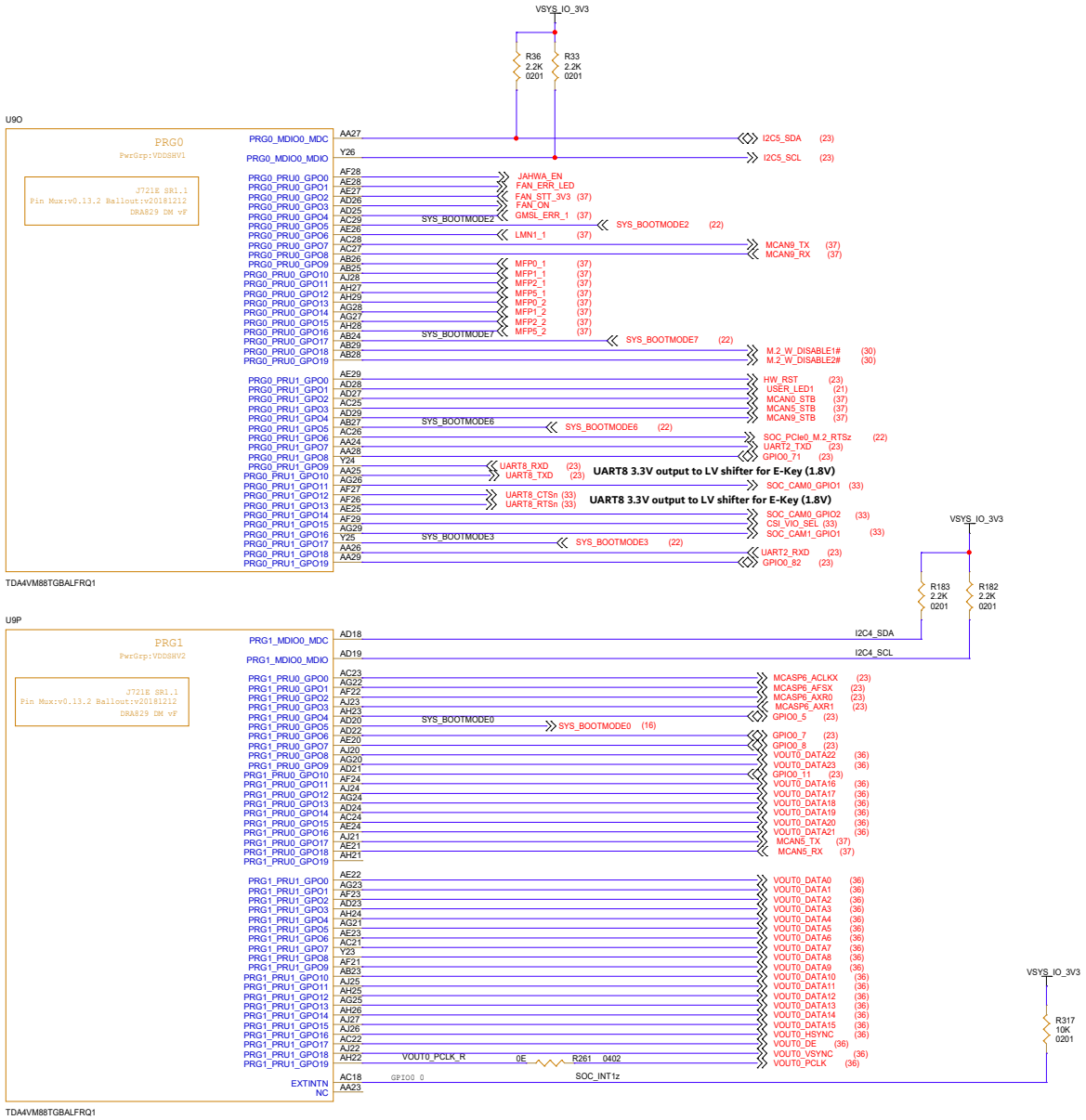


SOC GROUND



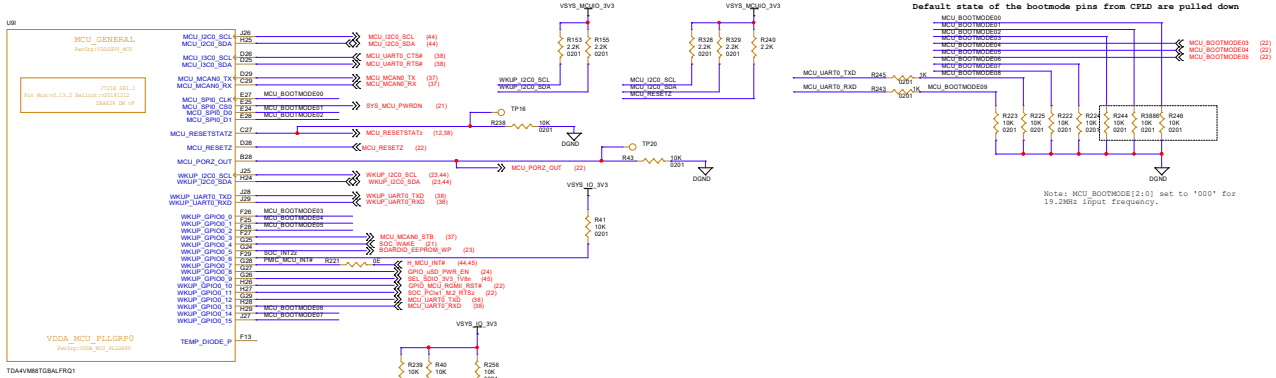
DX SOLUTION	PROJECT TI_1_DVKIT
PAGE 14 OF 35	PCB CODE (REV) DX-S2-001-A0(O)

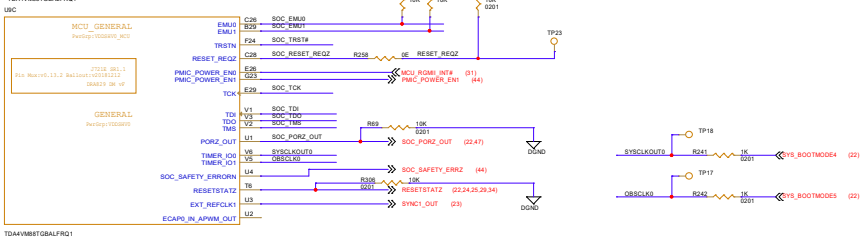
PRG0 & PRG1



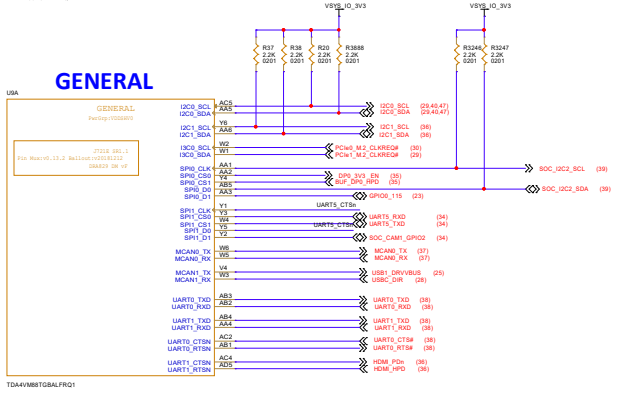
DX SOLUTION	PROJECT TI_1_DVKIT
PAGE 15 OF 35	PCB CODE (REV) DX-S2-001-A0(O)

MCU & MAIN GENERAL IO, OSC CLKS

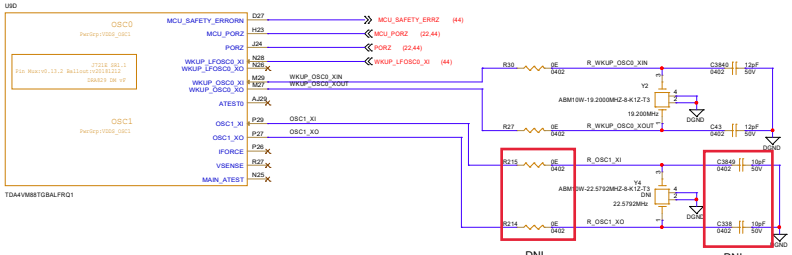




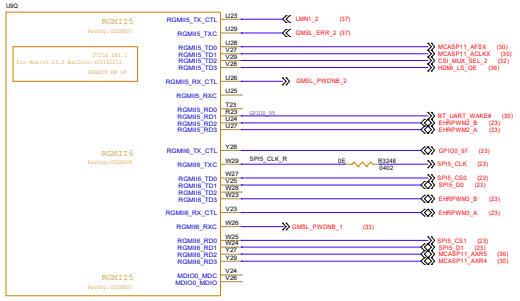
GENERAL



OSC

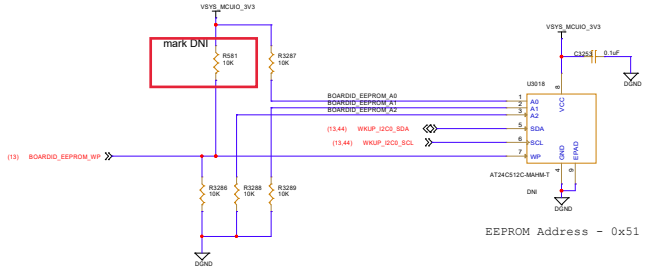


MAIN RGMII



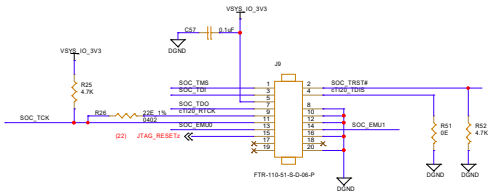
CLKS

BOARD ID EEPROM

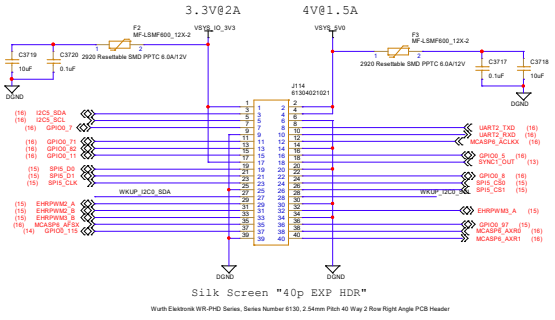


cTI 20PIN JTAG HEADER

Texas Instrument 20-pin CTI header standard (2x20, 1.27mm pitch), compatible with Texas Instruments modules (XDS110, XDS200, XDS560v2) and 3rd party modules.



40Pin Expansion Header (reserved)



Wurth Elektronik WR-PHD Series, Series Number 6130, 2.54mm Pitch 40 Way 2 Row Right Angle PCB Header

DX SOLUTION	PROJECT	TI_1_DVKIT
	PCB CODE (REV)	DX-S2-001-A0(O)
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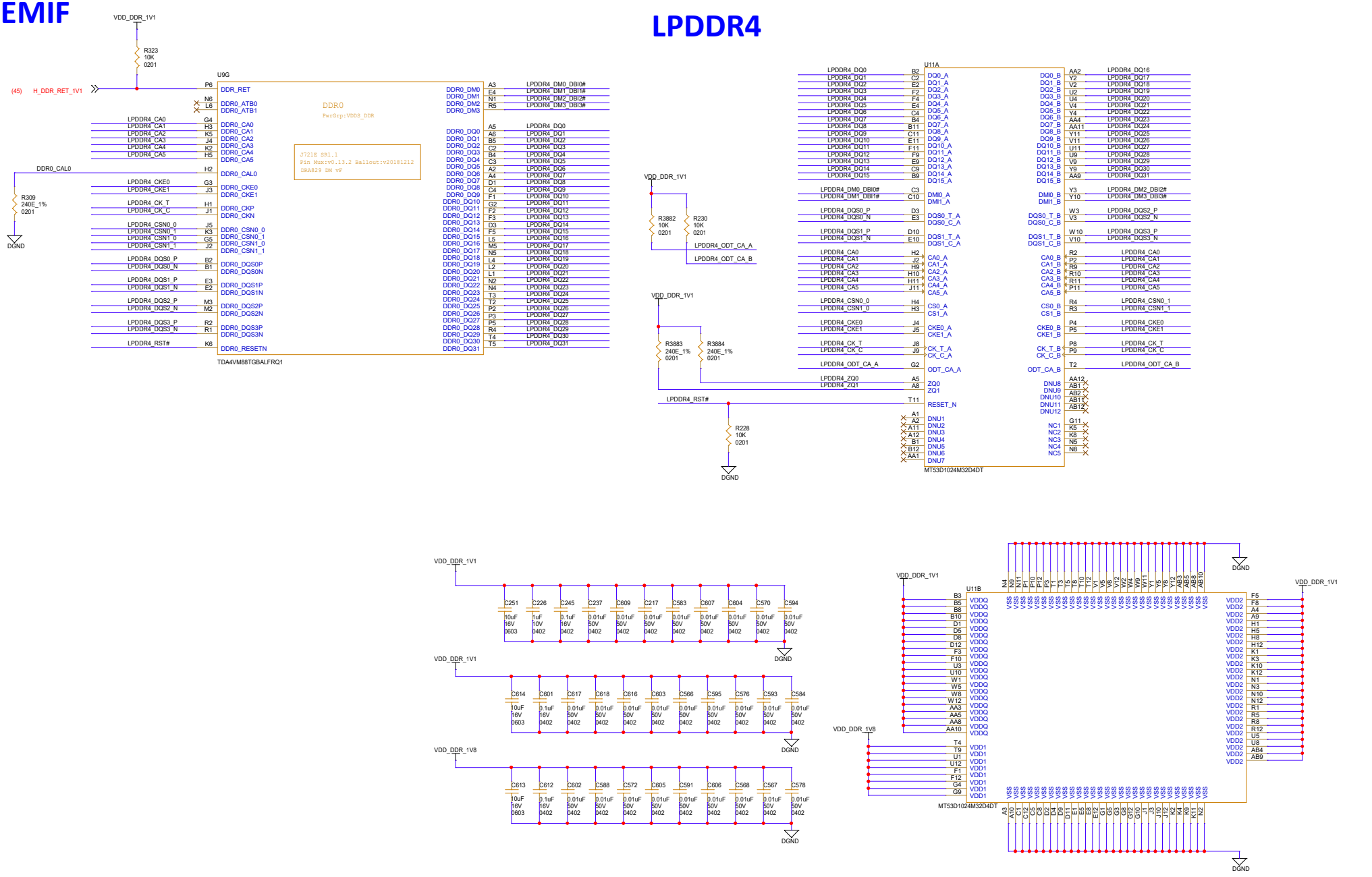
EMIF

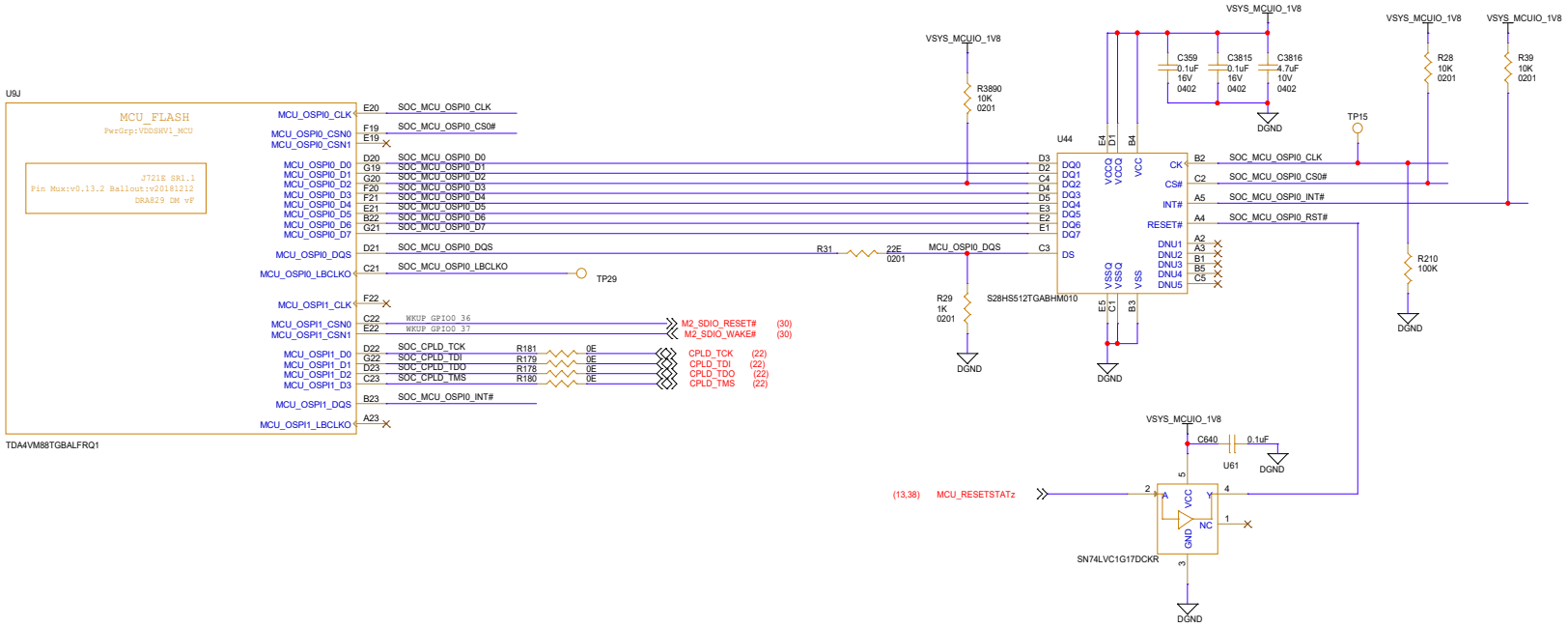
LPDDR4



DX SOLUTION	PROJECT TI_1_DVKIT
PAGE 17 OF 35	PCB CODE (REV) DX-S2-001-A0(O)

MCU FLASH

OSPI FLASH



DX SOLUTION	PROJECT TI_1_DVKIT
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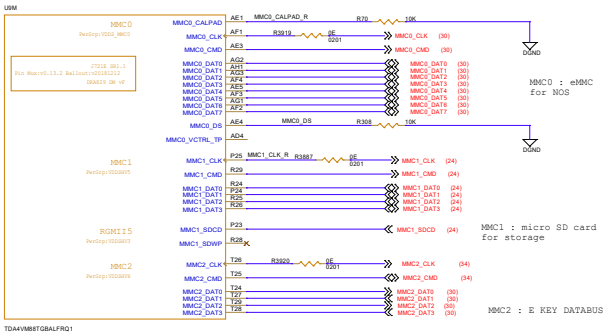
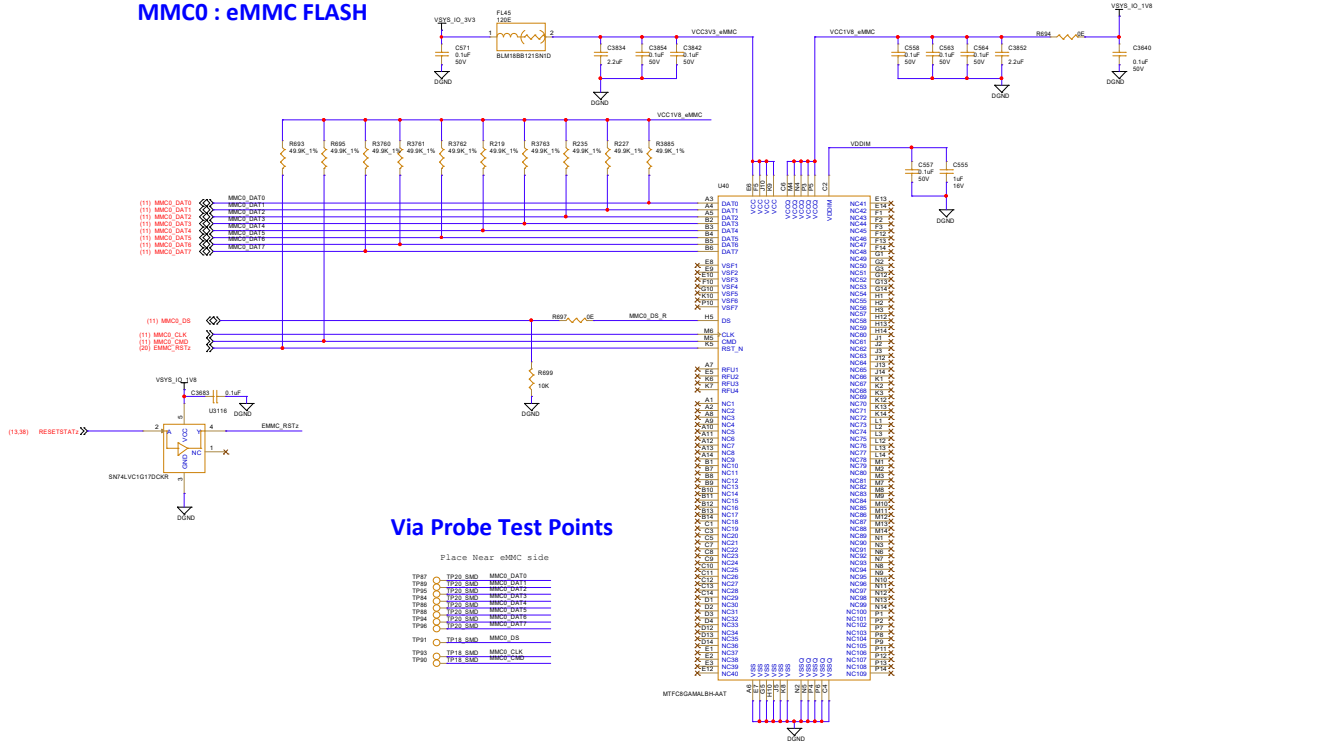
MMC Interface

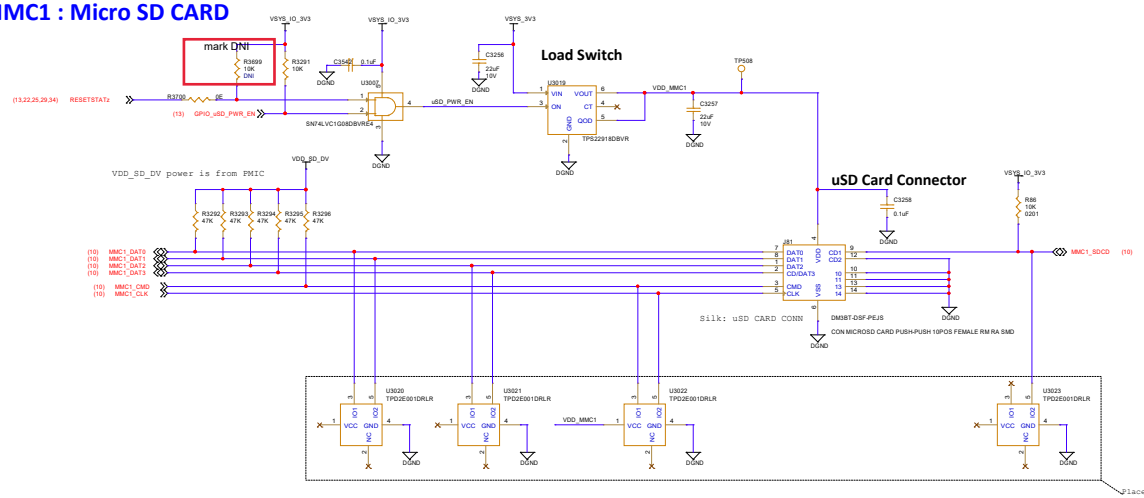


MMC0 : eMMC FLASH



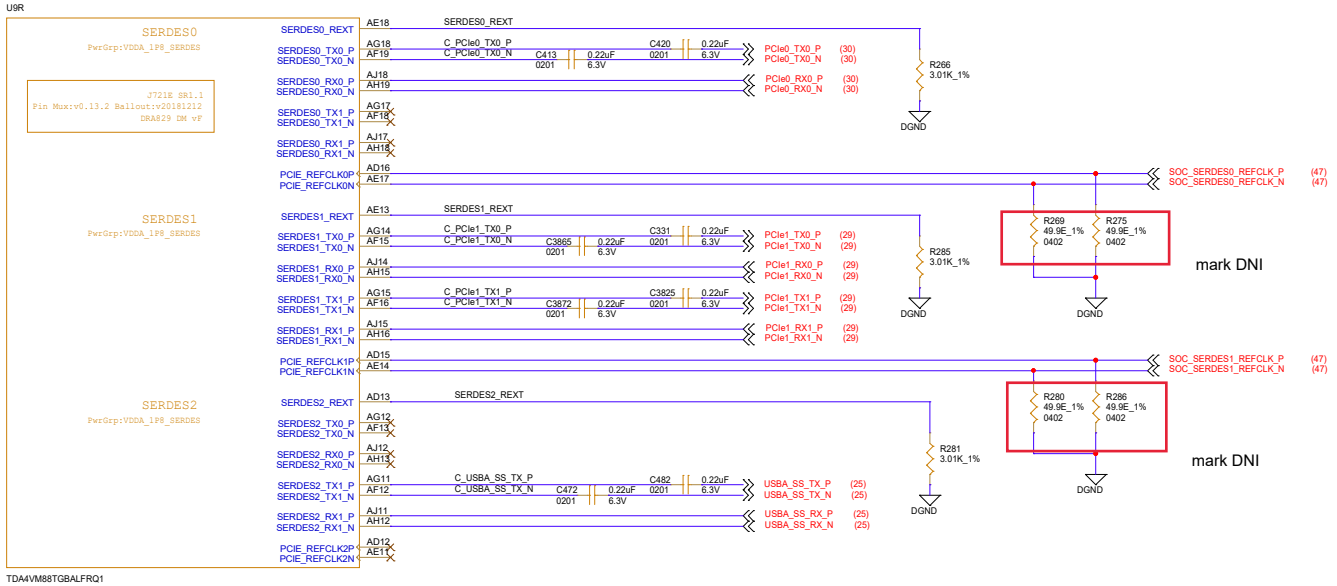
Via Probe Test Points

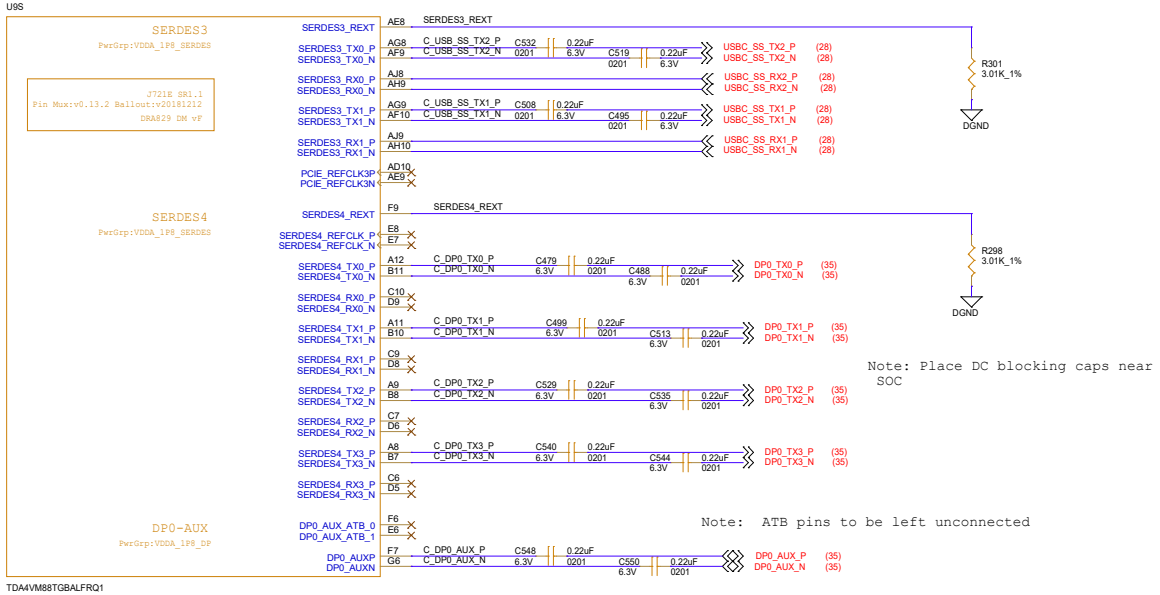
MMC1 : Micro SD CARD



DX SOLUTION	PROJECT TI_1_DVKIT
PAGE 19 OF 35	PCB CODE (REV) DX-S2-001-A0(O)

SERDES





DX SOLUTION	PROJECT TI_1_DVKIT
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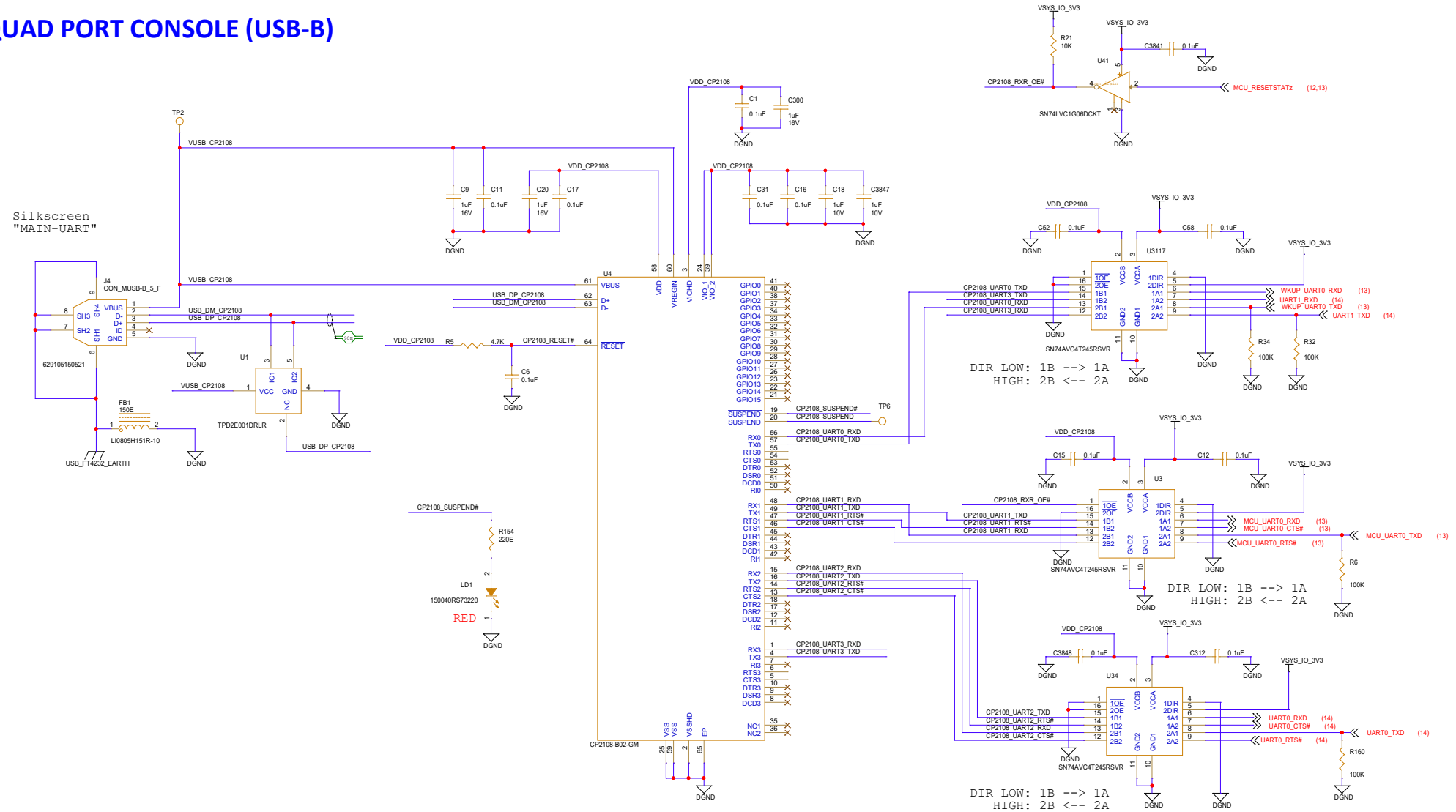
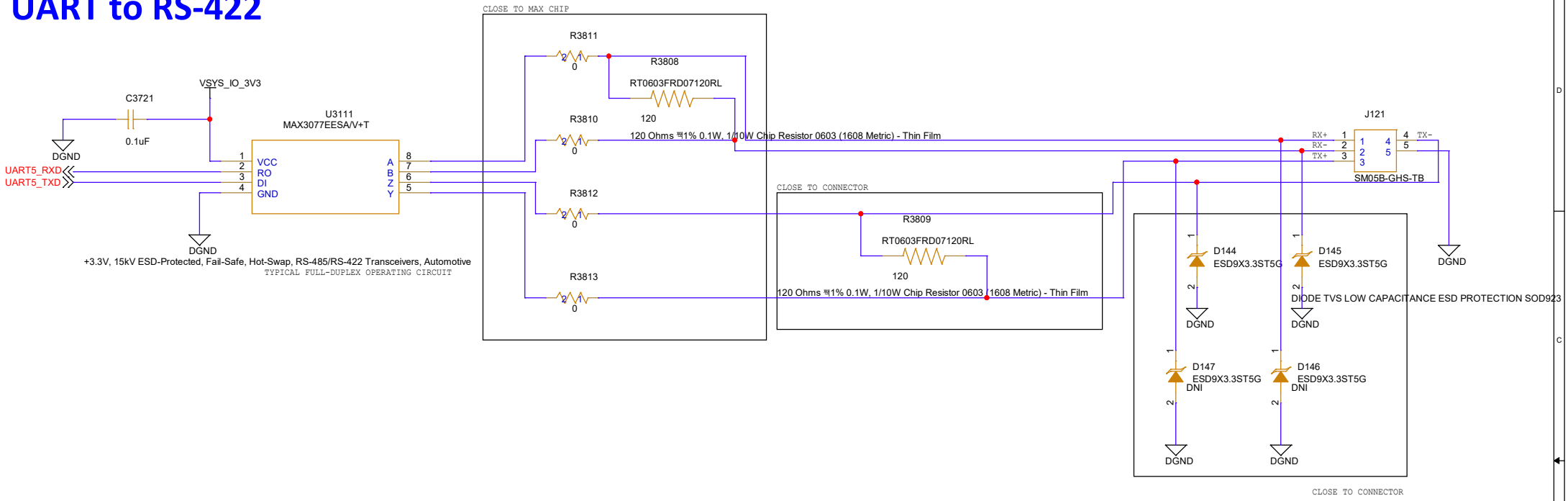
QUAD PORT CONSOLE (USB-B)



DX SOLUTION	PROJECT TI_1_DVKIT
PAGE 21 OF 35	PCB CODE (REV) DX-S2-001-A0(O)

UART to RS-422



DX SOLUTION	PROJECT TI_1_DVKIT
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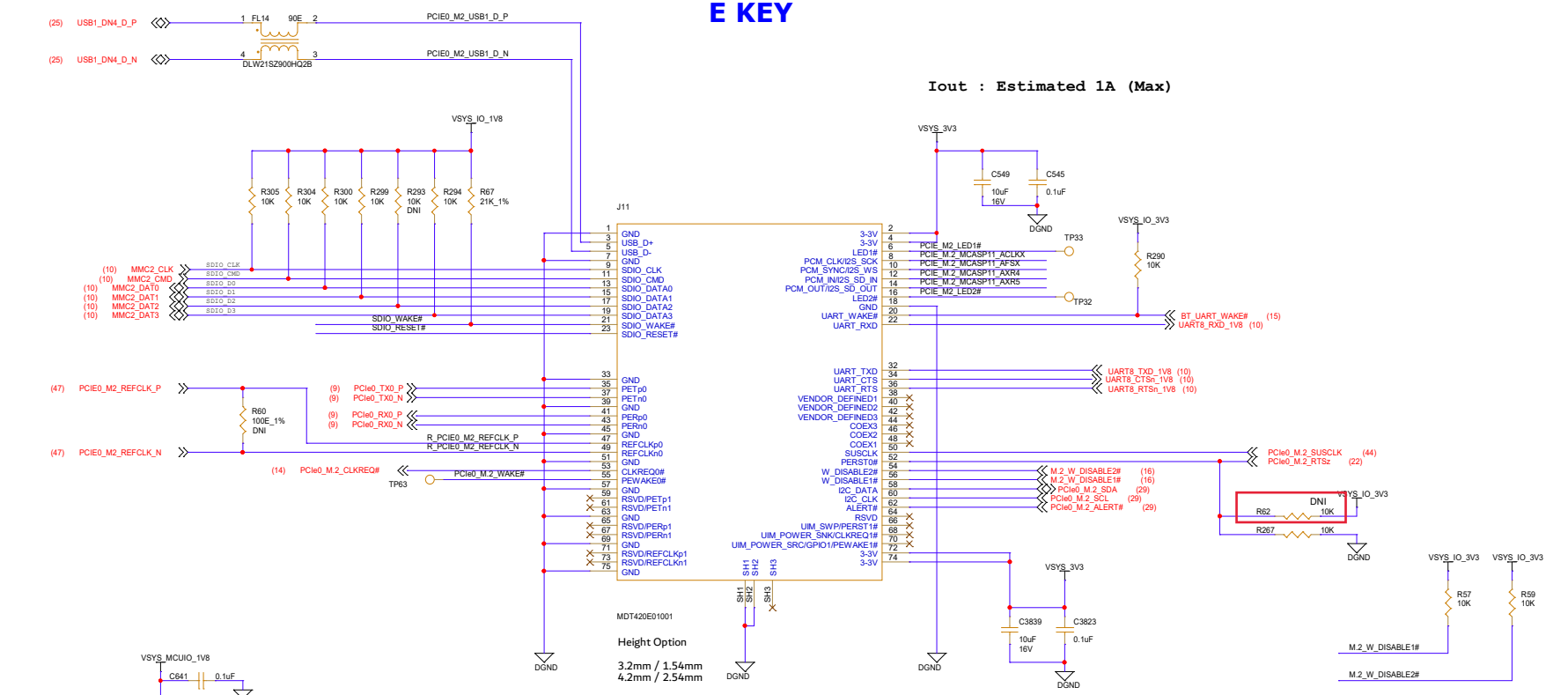
PCIe_M.2_INTERFACE - SDIO

E KEY



DX SOLUTION	PROJECT TI_1_DVKIT
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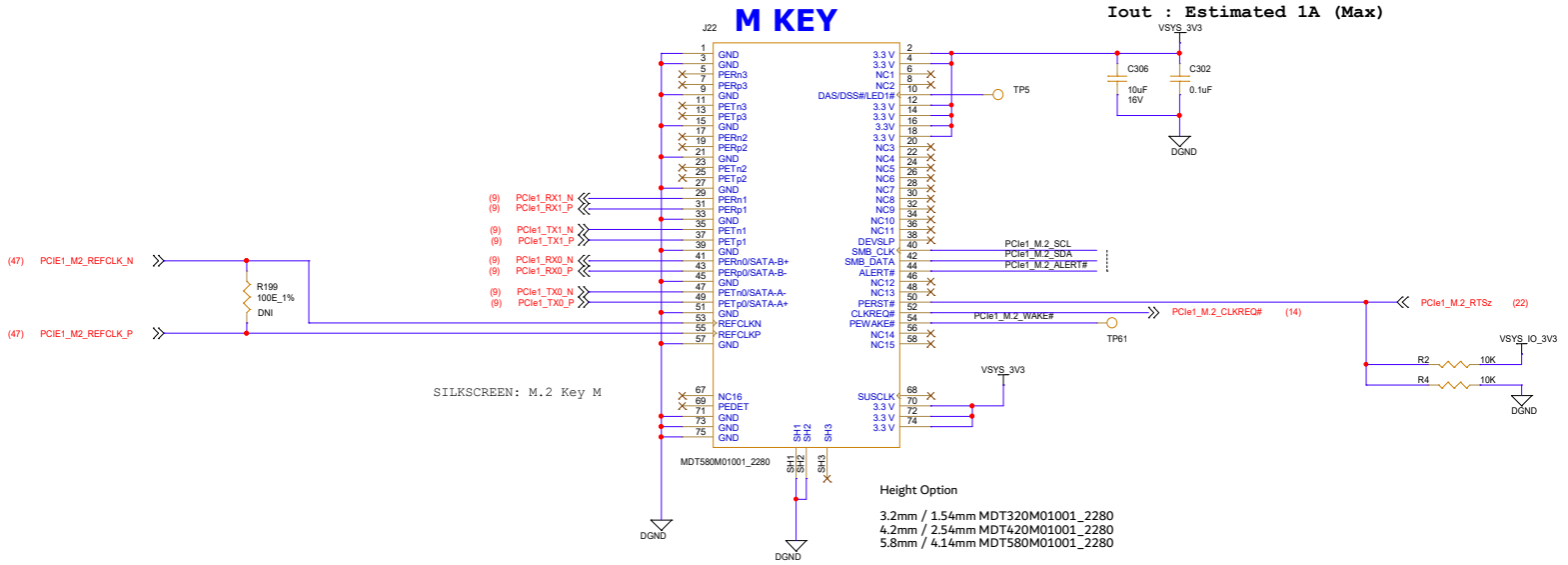
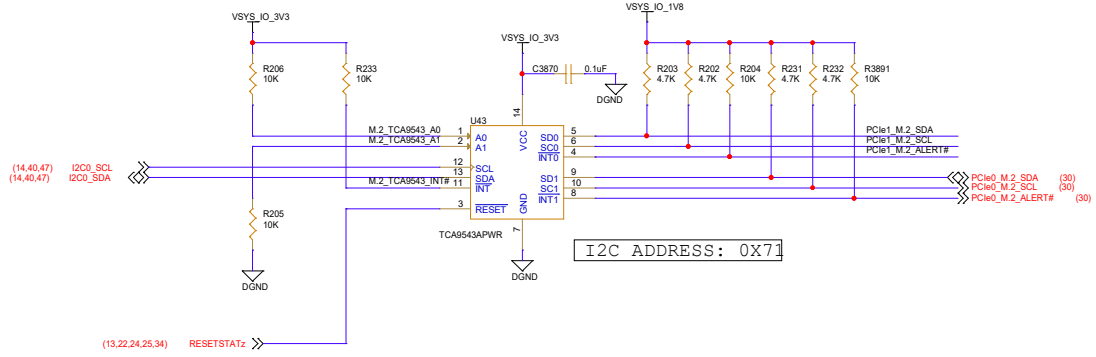
PCIe_M.2_INTERFACE SSD

M KEY



M.2 Stand Off 5.80H
MDT580STD001

3.3V To 1V8 Level translator



DX SOLUTION	PROJECT TI_1_DVKIT
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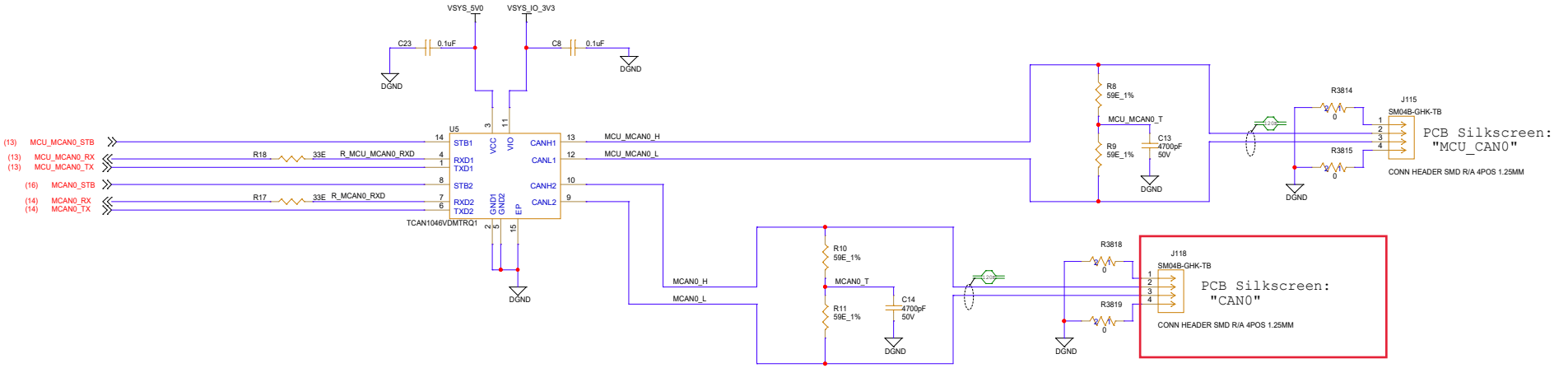
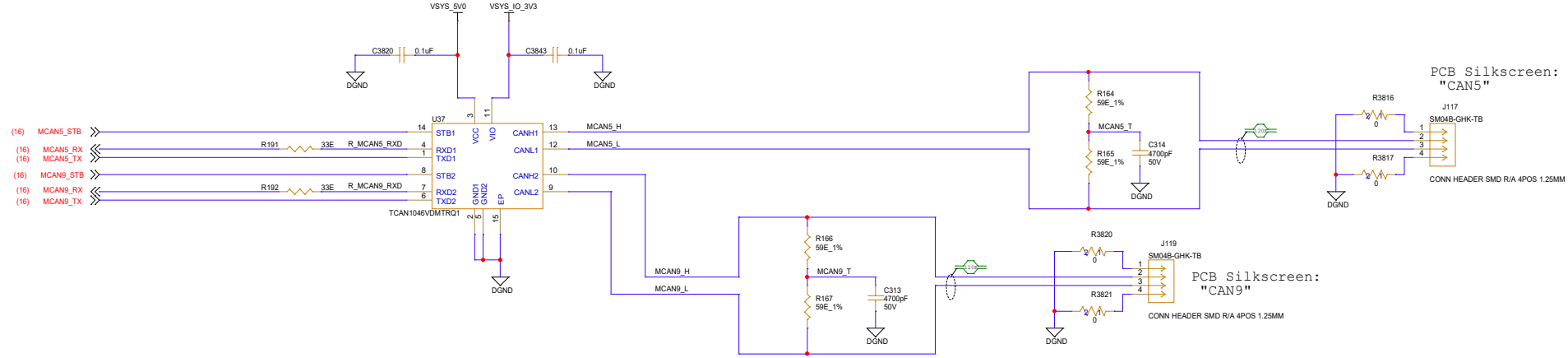
CAN TRANSCEIVERS #2-MAIN DOMAIN



무상샘플 지원. DV 수량은 구매 필요



DX SOLUTION	PROJECT TI_1_DVKIT
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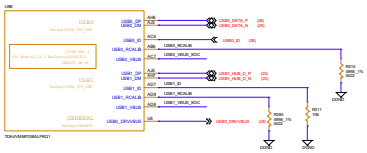
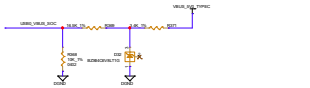
USB



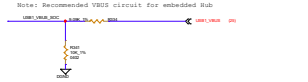
USB1_ID Pulled low. J7 SoC in Host Mode.

USB VBUS Resistor divider circuit

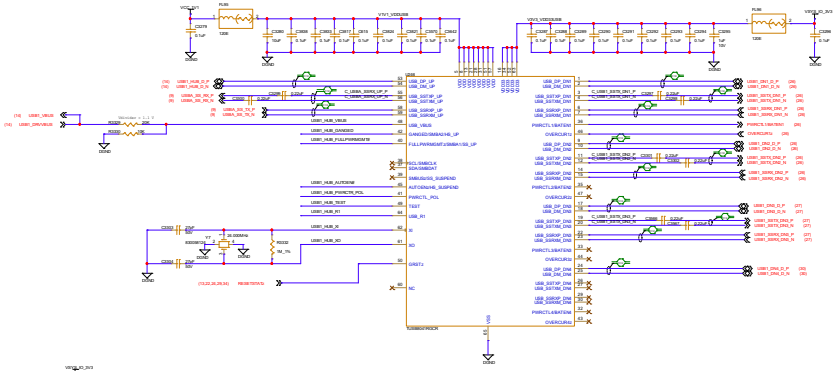
Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS

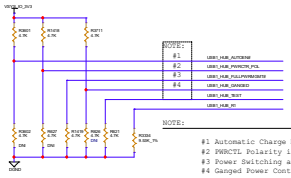


Note: Recommended VBUS circuit for embedded Hub



USB3.0 HUB

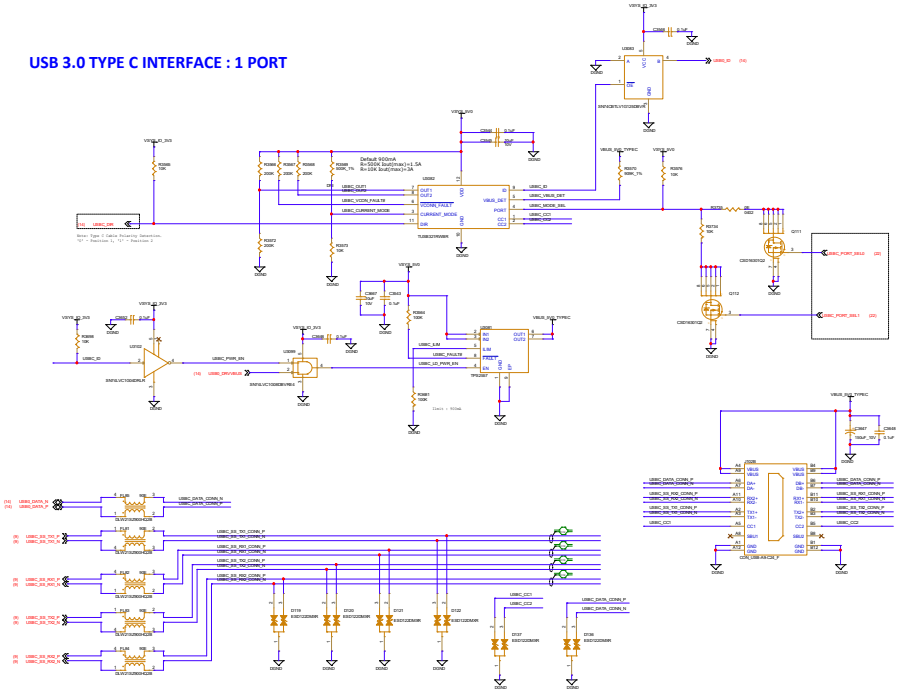




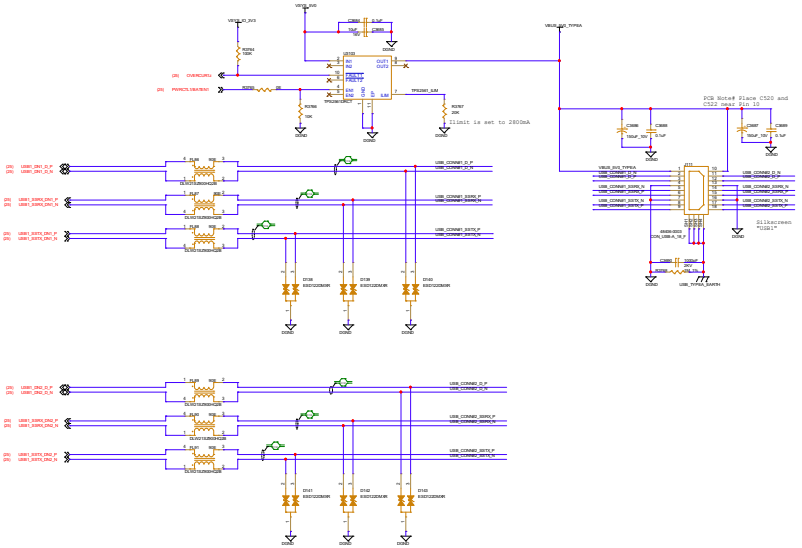
NOTE:

#1 Automatic Charge Mode Disabled
#2 PWRCTL Polarity is Active High
#3 Power Switching and Overcurrent Inputs Supported
#4 Ganged Power Control Enabled

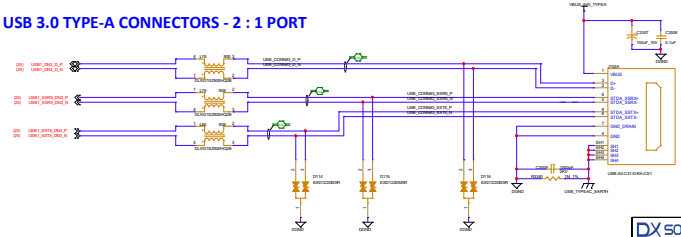
USB 3.0 TYPE C INTERFACE : 1 PORT



USB 3.0 TYPE-A CONNECTORS - 1 : 2 PORTS



USB 3.0 TYPE-A CONNECTORS - 2 : 1 PORT



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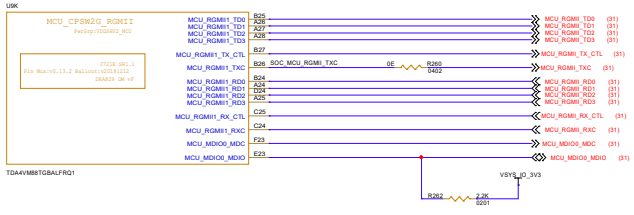
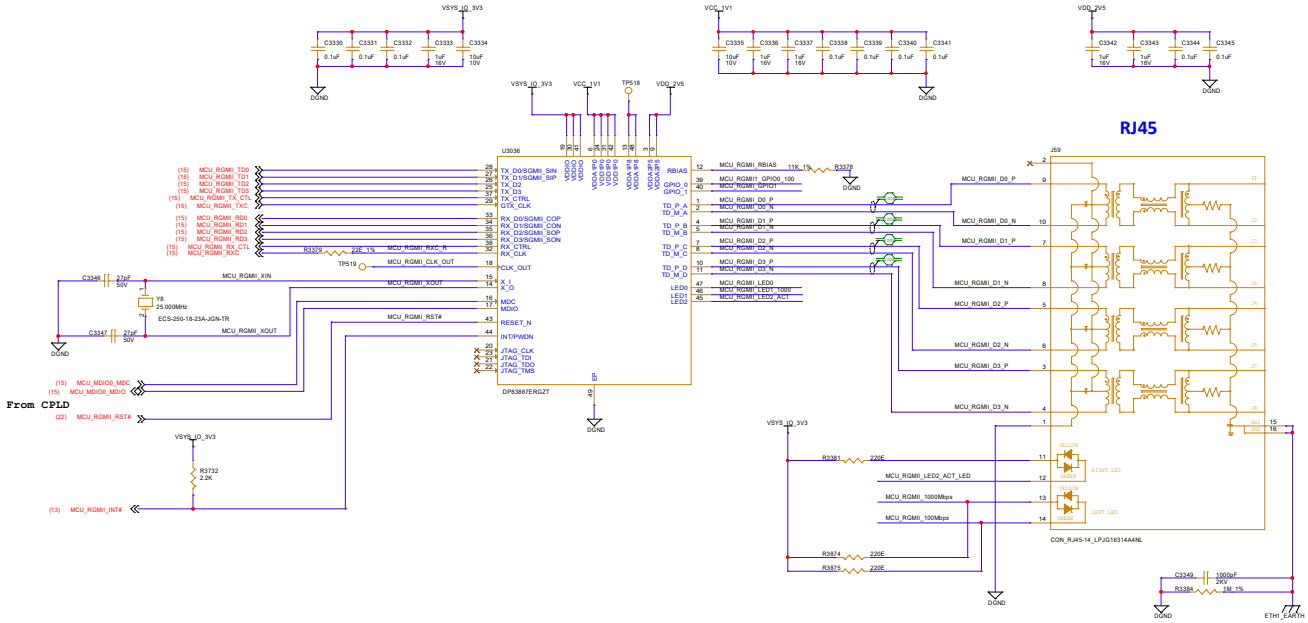
MCU_RGMII



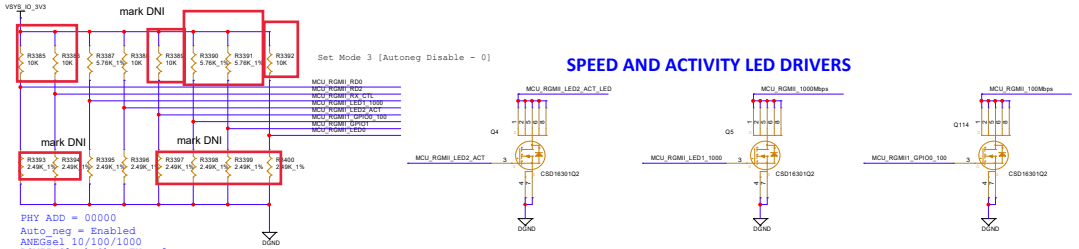
MCU GB ETHERNET



RJ45

RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

SPEED AND ACTIVITY LED DRIVERS



LED_2-MODE1 & LED_1-MODE2-TX SKEW=0nS
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2nS

DX SOLUTION	PROJECT TI_1_DVKIT
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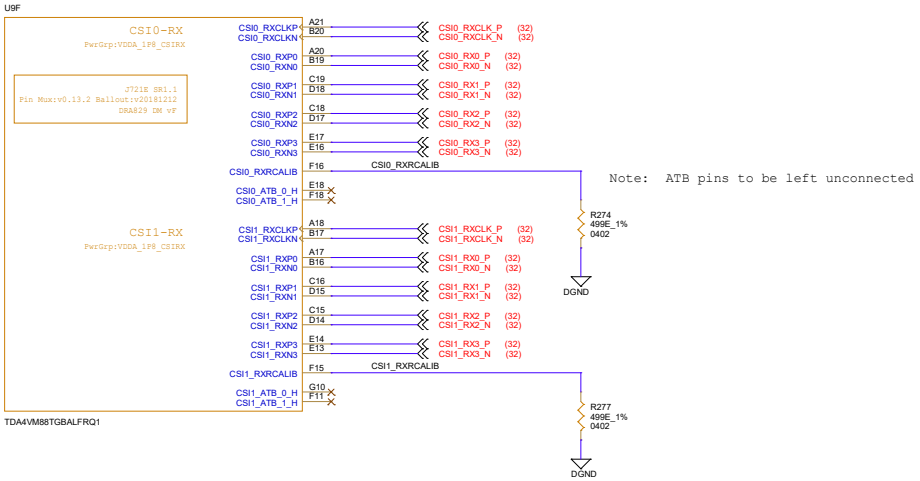
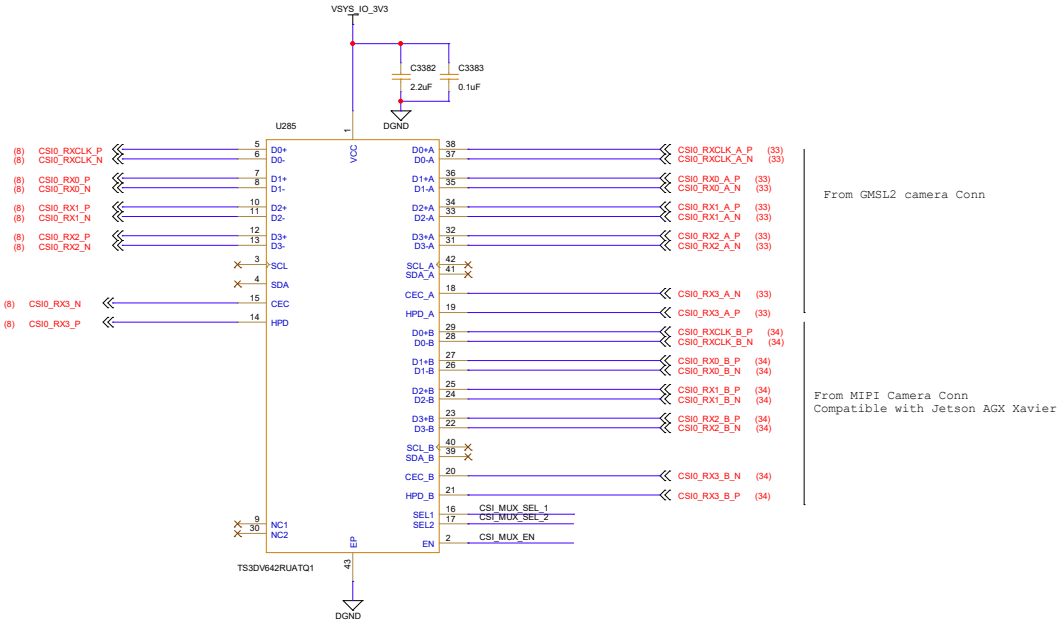
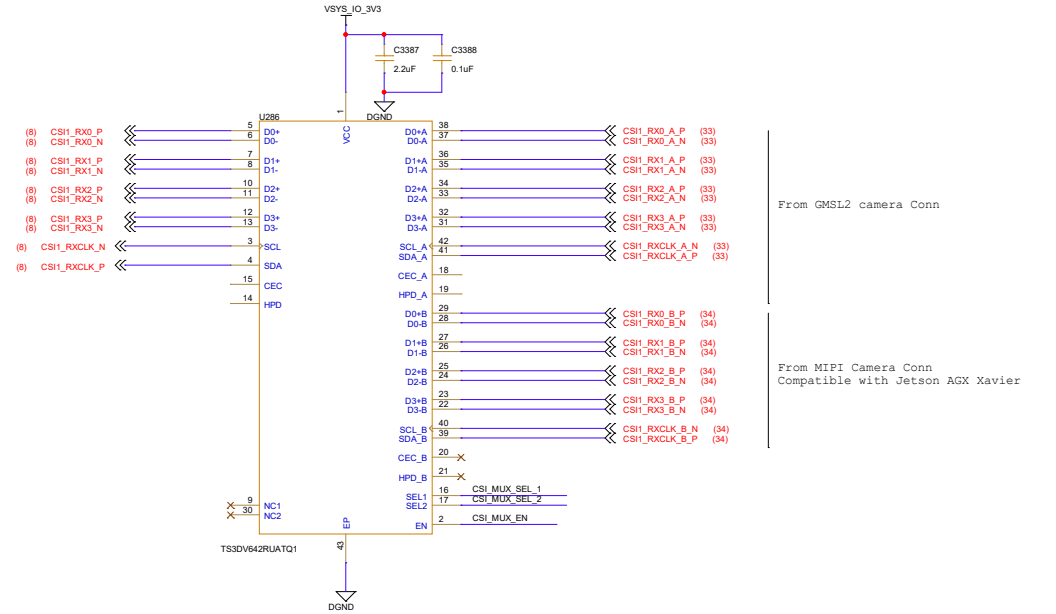
CSI Interface



Note: ATB pins to be left unconnected

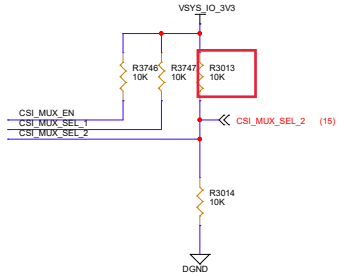
CSI MUX - DATA





CSI - 1:2 MUX : Truth Table

MUX_SEL_2	FUNCTION	
LOW	INPUT<--A port [GMSL2 Connector]	(default)
HIGH	INPUT<--B port [MIPI CSI-2 Camera Connector]	



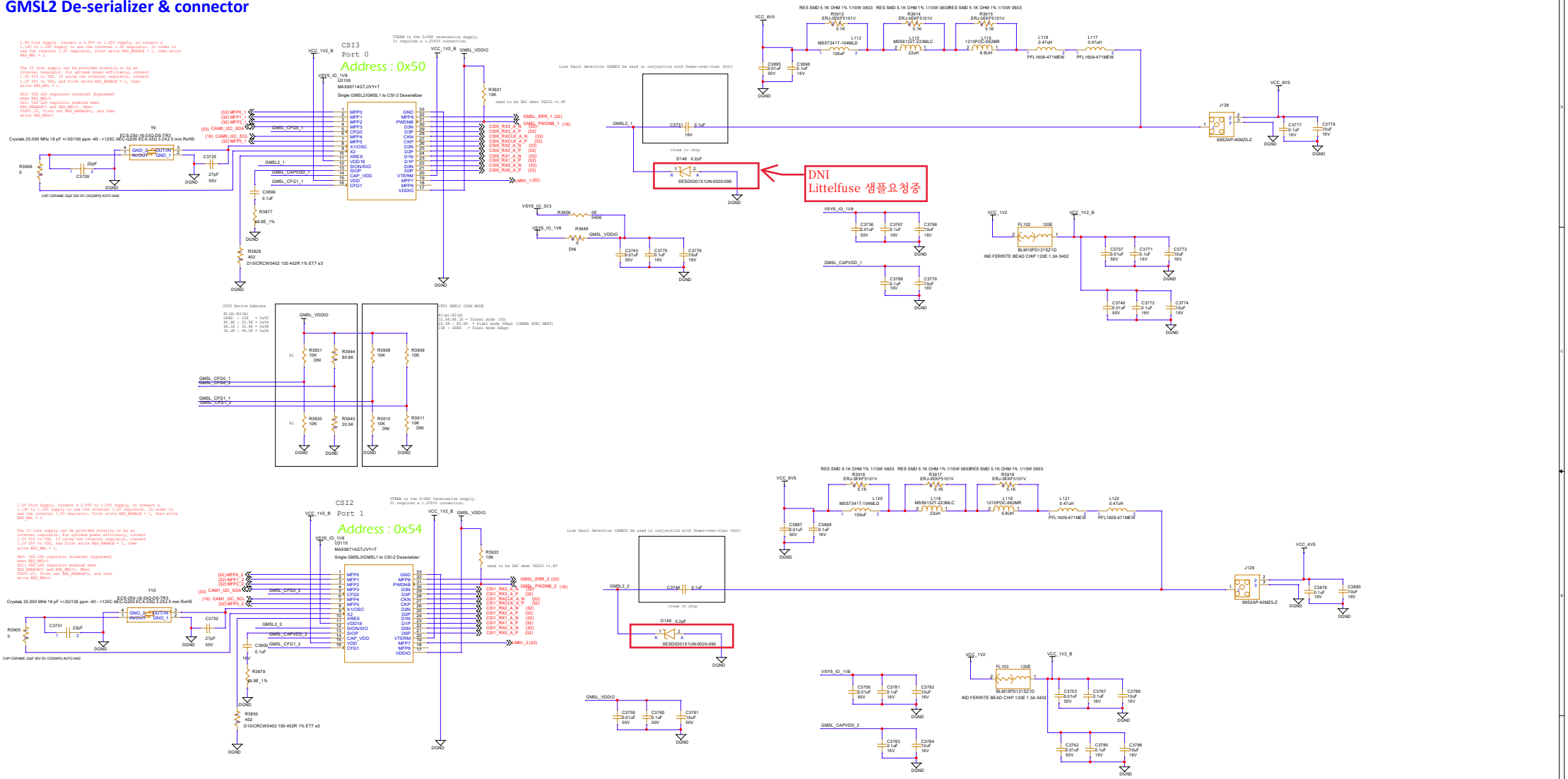
DX SOLUTION

PROJECT TI_1_DVKIT

PCB CODE (REV)

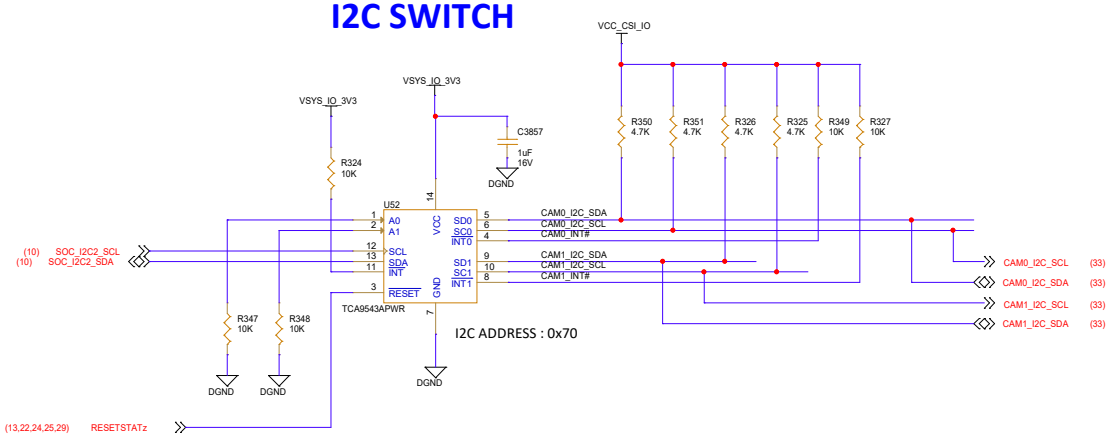
DX-S2-001-A0(O)

GMSL2 De-serializer & connector

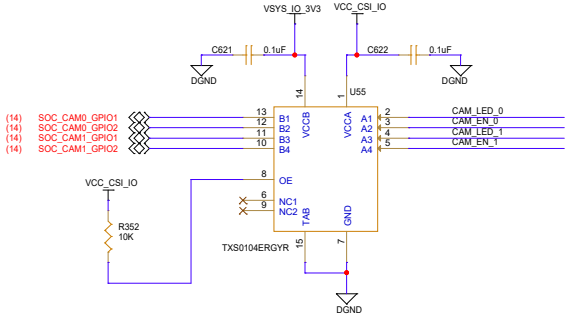


MIPI CSI-2 CONNECTORS

I2C SWITCH



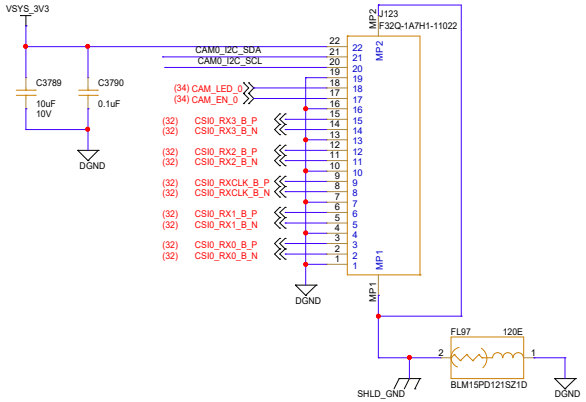
GPIO LEVEL TRANSLATOR



Silk Screen "CAM1"

FPC Camera Connector -1

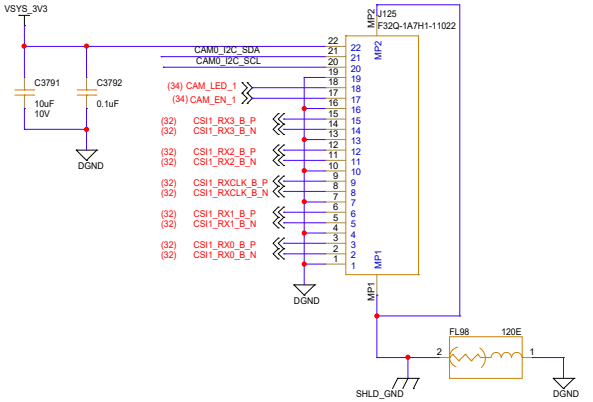
Flex Connector, 0.50mm Pitch, Height 2.00mm, Right angle, Slider type, ZIF, Upper contact, 22 position , Without MYLAR



Silk Screen "CAM2"

FPC Camera Connector -2

Flex Connector, 0.50mm Pitch, Height 2.00mm, Right angle, Slider type, ZIF, Upper contact, 22 position , Without MYLAR



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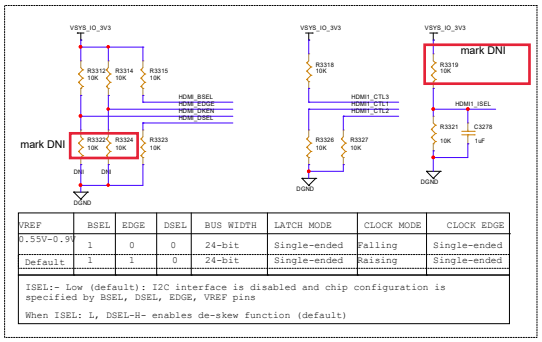
DVI/HDMI TRANSMITTER

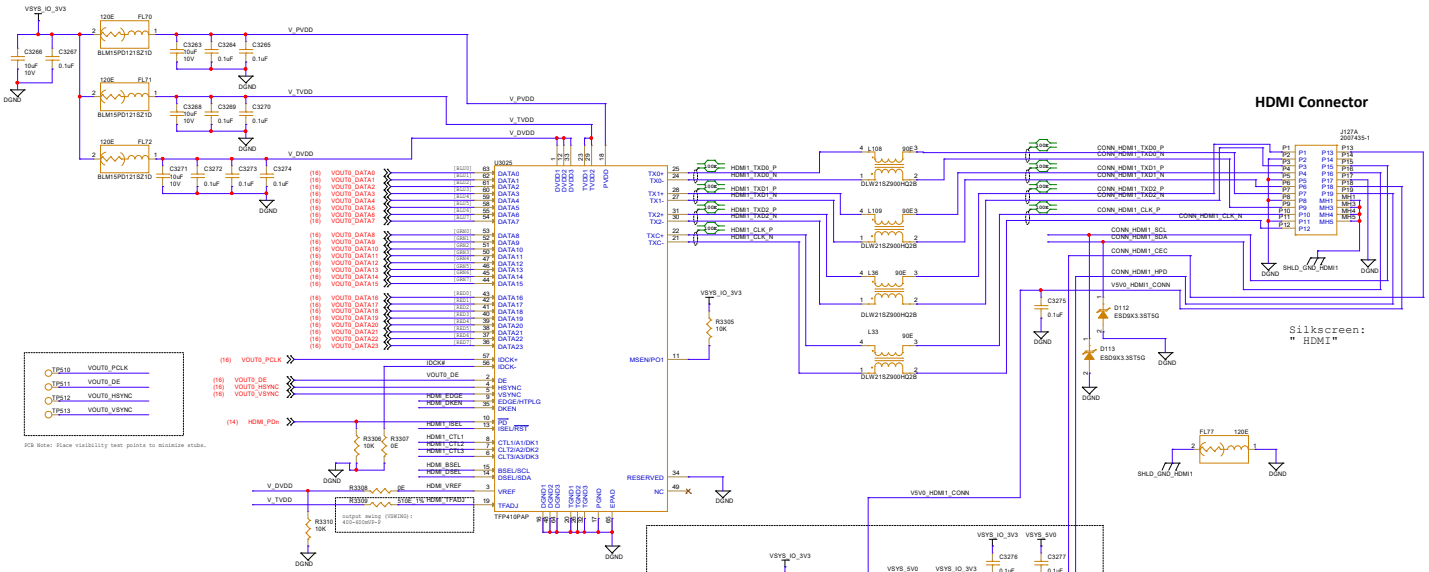
DVI Configuration Settings



VREF	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK MODE	CLOCK EDGE
0.55V~0.9V	1	0	0	24-bit	Single-ended	Falling	Single-ended
Default	1	1	0	24-bit	Single-ended	Raising	Single-ended

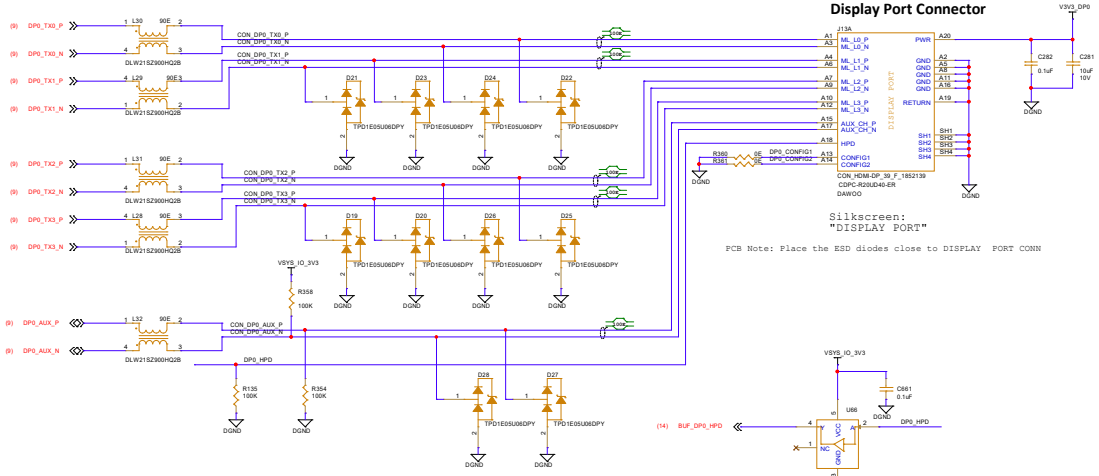
ISEL:- Low (default): I2C interface is disabled and chip configuration is specified by BSEL, DSEL, EDGE, VREF pins

When ISEL: L, DSEL-H- enables de-skew function (default)



HDMI Connector

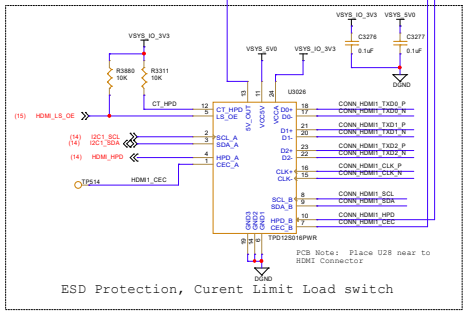
DISPLAY PORT INTERFACE



Display Port Connector

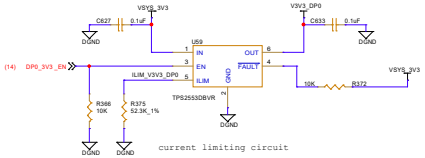
Silkscreen: "DISPLAY PORT"

PCB Note: Place the ESD diodes close to DISPLAY PORT CONN



ESD Protection, Curent Limit Load switch

Hot Plug Detect with Schmitt trigger



current limiting circuit

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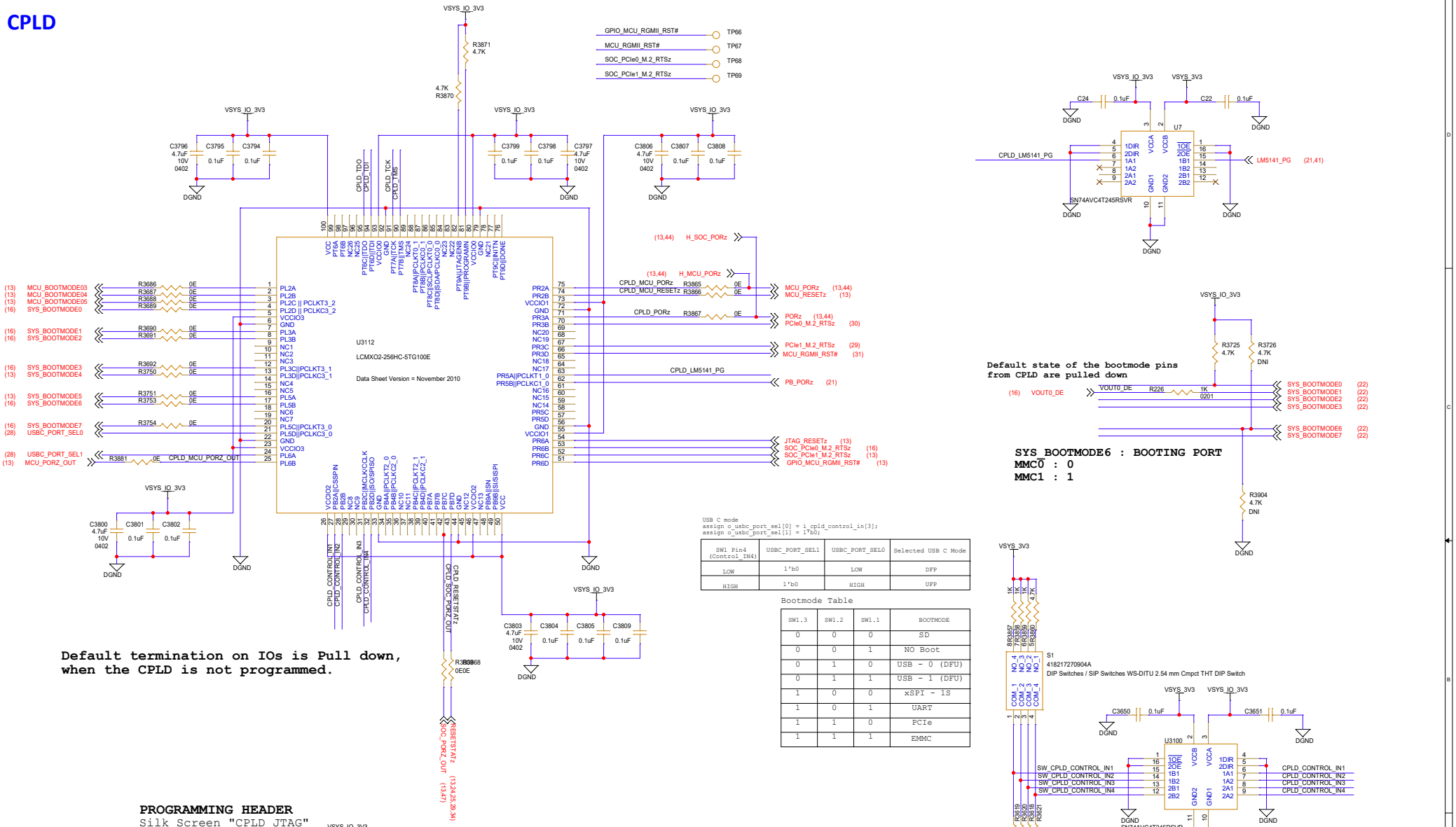
CPLD



Default termination on IOs is Pull down, when the CPLD is not programmed.

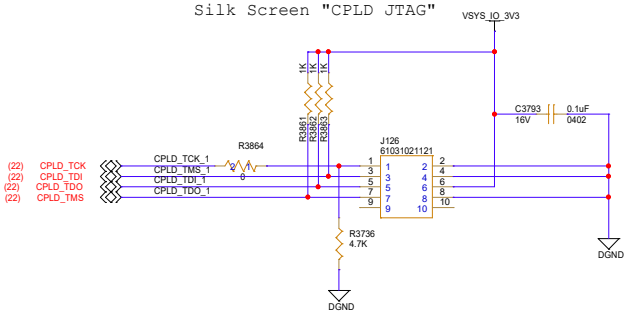
```
USB C mode
assign o_usbc_port_sel[0] = i_cpld_control_in[3];
assign o_usbc_port_sel[1] = 1'b0;
```

SW1 Pin4 (Control_IN4)	USBC_PORT_SEL1	USBC_PORT_SEL0	Selected USB C Mode
LOW	1'b0	LOW	DFP
HIGH	1'b0	HIGH	UFP

Bootmode Table

SW1.3	SW1.2	SW1.1	BOOTMODE
0	0	0	SD
0	0	1	NO Boot
0	1	0	USB - 0 (DFU)
0	1	1	USB - 1 (DFU)
1	0	0	xSPI - 1S
1	0	1	UART
1	1	0	PCIe
1	1	1	EMMC

PROGRAMMING HEADER
Silk Screen "CPLD JTAG"



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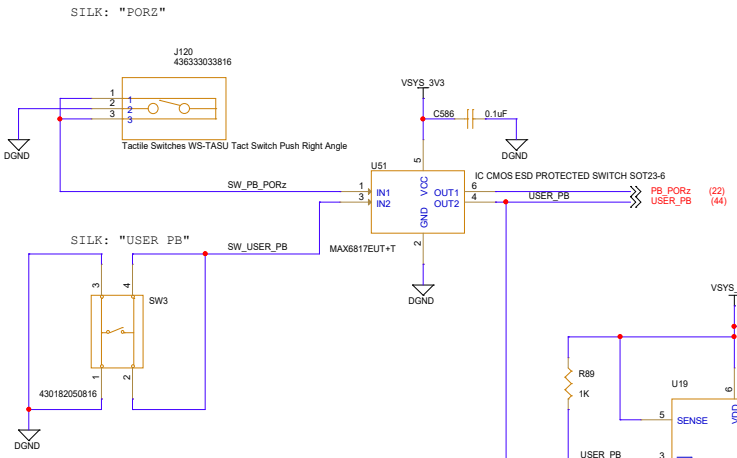
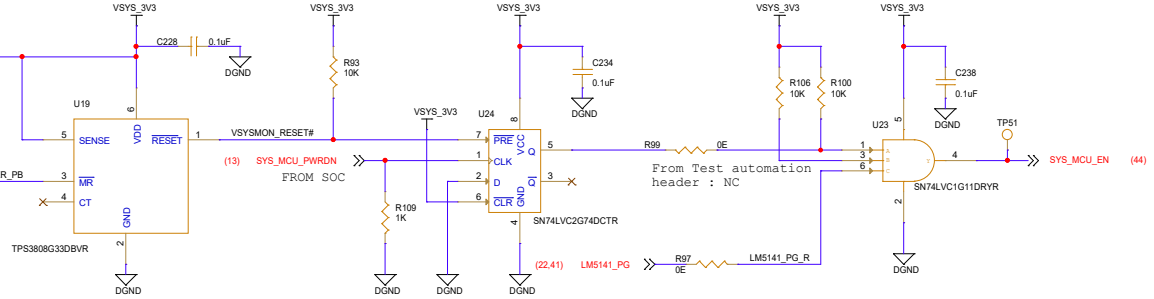
RESET BUTTONs

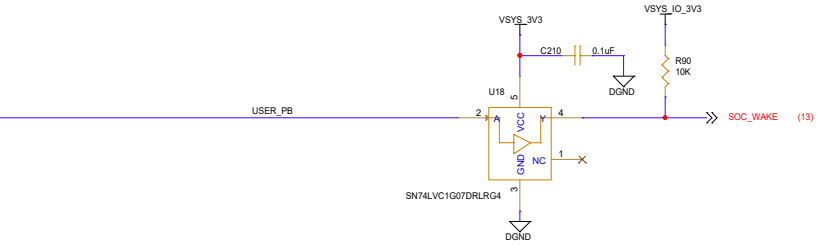
SW RESET PUSH BUTTON



USER Defined RESET BUTTON (On Board reserved)

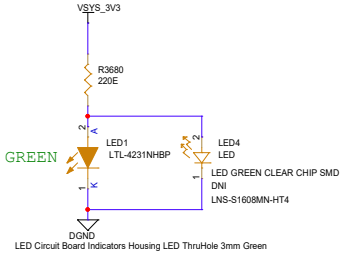


User Pushbutton [SW3] With User LED Indication [LD2]
The pushbutton [SW3] can be used for several different functions.
Function 1: System Wake from Shutdown. After software-initiated power down (using GPIO0_55), pressing pushbutton [SW3] will re-enable and boot the EVM.
Function 2: Power Management Input/Interrupt. The pushbutton [SW3] is connected with Power Management IC (IO4), and can be programmed for different power related functions (ex. Wake from Sleep).
Function 3: User Defined Input/Interrupt. The pushbutton [SW3] is connected with the TDA4VM processor (GPIO0_4), and can be programmed for variety of user input/interrupt needs.
A red LED [LD2] is available as user indicator, and is controlled via the TDA4VM processor (GPIO0_64)

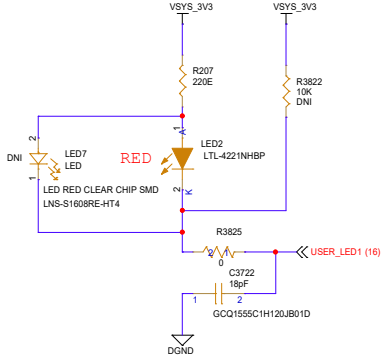


LEDs

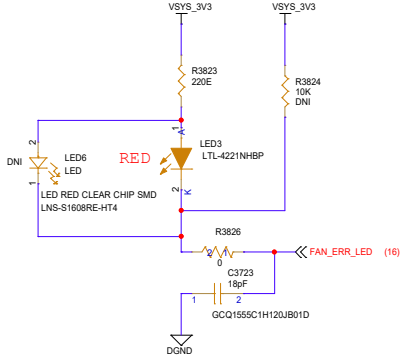
POWER LED



USER DEFINED LED



FAN ERR LED



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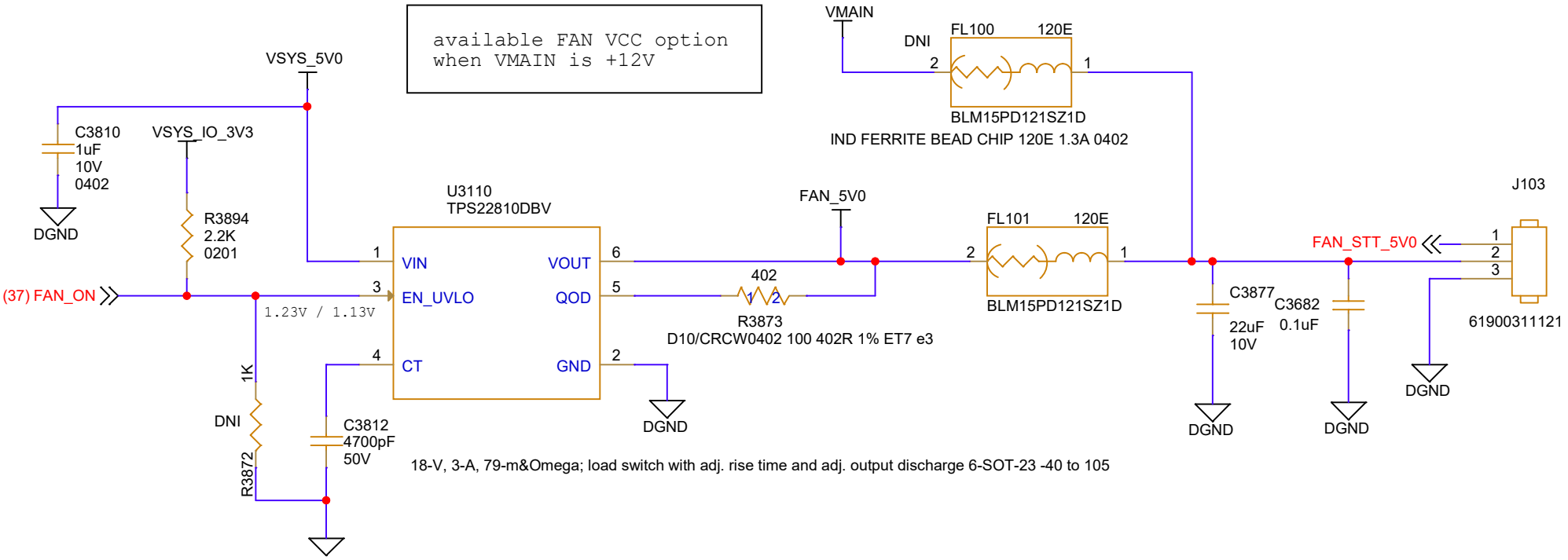
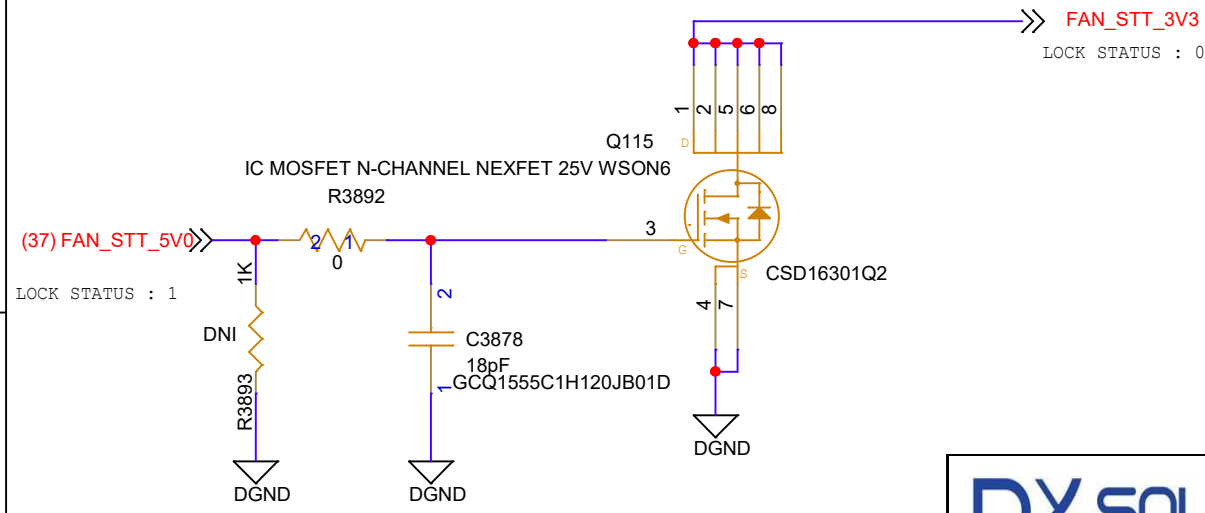
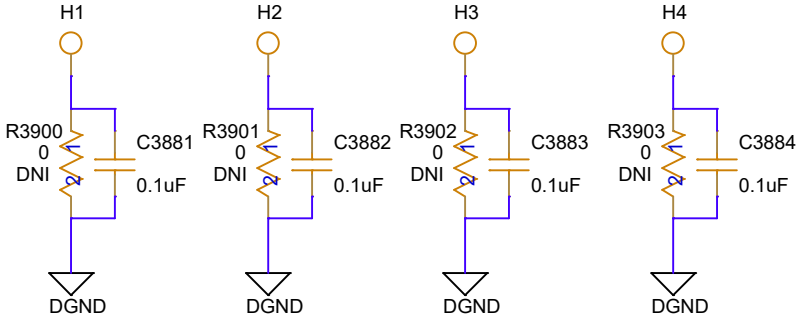
FAN

FAN HEADER





MT HOLE



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