TMS320C6670 EVM Board for TI

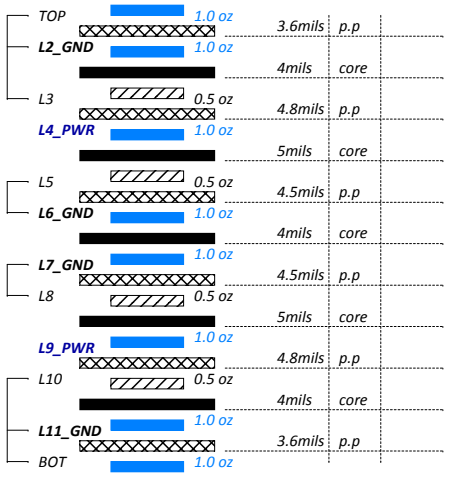
Product name : DSPM-8302E

Rev. A103-1

PCB PN : 19C2830202

Project Code :

PCB Thickness : 62 mils(1.6mm)
12 Layers



Texas Instruments
20450 Century Blvd
Germantown, MD 20874
USA

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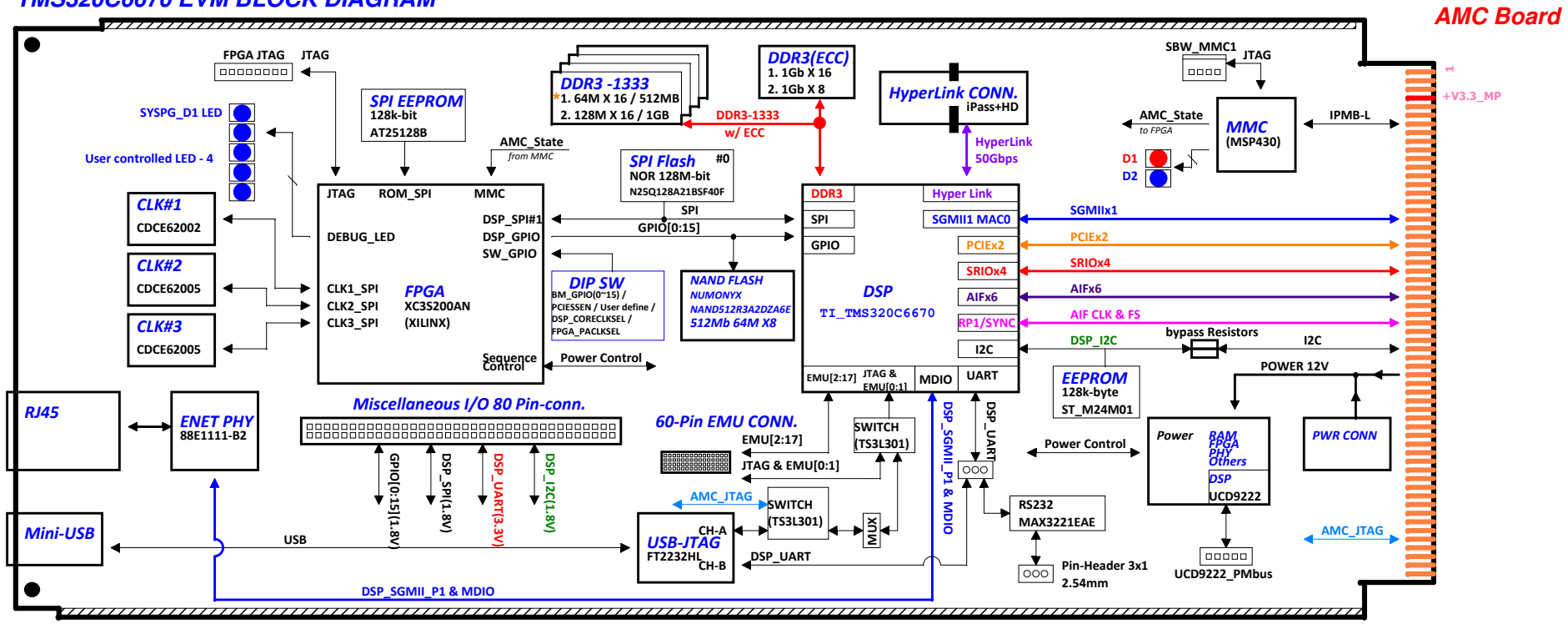
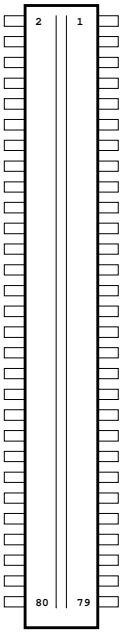
TMS320C6670 EVM BLOCK DIAGRAM



Miscellaneous I/O 80 Pin conn. Signal

PIN	Port mapping
02	VCC5
04	VCC5
06	GND
08	GND
10	
12	VCC3V3_AUX
14	VCC3V3_AUX
16	GND
18	GND
20	
22	VCC1V8_AUX
24	VCC1V8_AUX
26	GND
28	GND
30	
32	
34	
36	
38	
40	

PIN	Port mapping
42	
44	
46	
48	
50	GPIO00
52	GPIO01
54	GPIO02
56	GPIO03
58	GPIO04
60	GPIO05
62	GPIO06
64	GPIO07
66	GPIO08
68	GPIO09
70	GPIO10
72	GPIO11
74	GPIO12
76	GPIO13
78	GPIO14
80	GPIO15



PIN	Port mapping
01	Gnd
03	SDA
05	SCL
07	
09	
11	
13	
15	
17	
19	
21	
23	
25	
27	
29	
31	
33	
35	
37	
39	

PIN	Port mapping
41	
43	
45	
47	CLK2_SYNC
49	CLK3_SYNC
51	PHYSYNC_R
53	RADSYNC_R
55	TIMI0
57	TIMO0
59	TIMI1
61	TIMO1
63	SSPMISO
65	SSPMOSI
67	SSPCS1
69	SSPCK
71	UARTTXD
73	UARTRXD
75	UARTRTS
77	UARTCTS
79	Gnd

AMC Port mapping

PIN	Port mapping
TCLKA	TCLKA
TCLKB	TCLKB
FCLKA	100MHz
00	SGMII
01	
02	
03	
04	PCI-E_1
05	PCI-E_2
06	
07	
08	SRIO_1
09	SRIO_2
10	SRIO_3

PIN	Port mapping
11	SRIO_4
12	AIF_0
13	AIF_1
14	AIF_2
15	AIF_3
16	TCLKC TCLKD
17	AIF_4
18	AIF_5
19	RP1FB & F/R(SYNC)
20	Expansion I2C & external RP1CLK
JTAG	AMC_JTAG

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Title: BLOCK DIAGRAM_AMC

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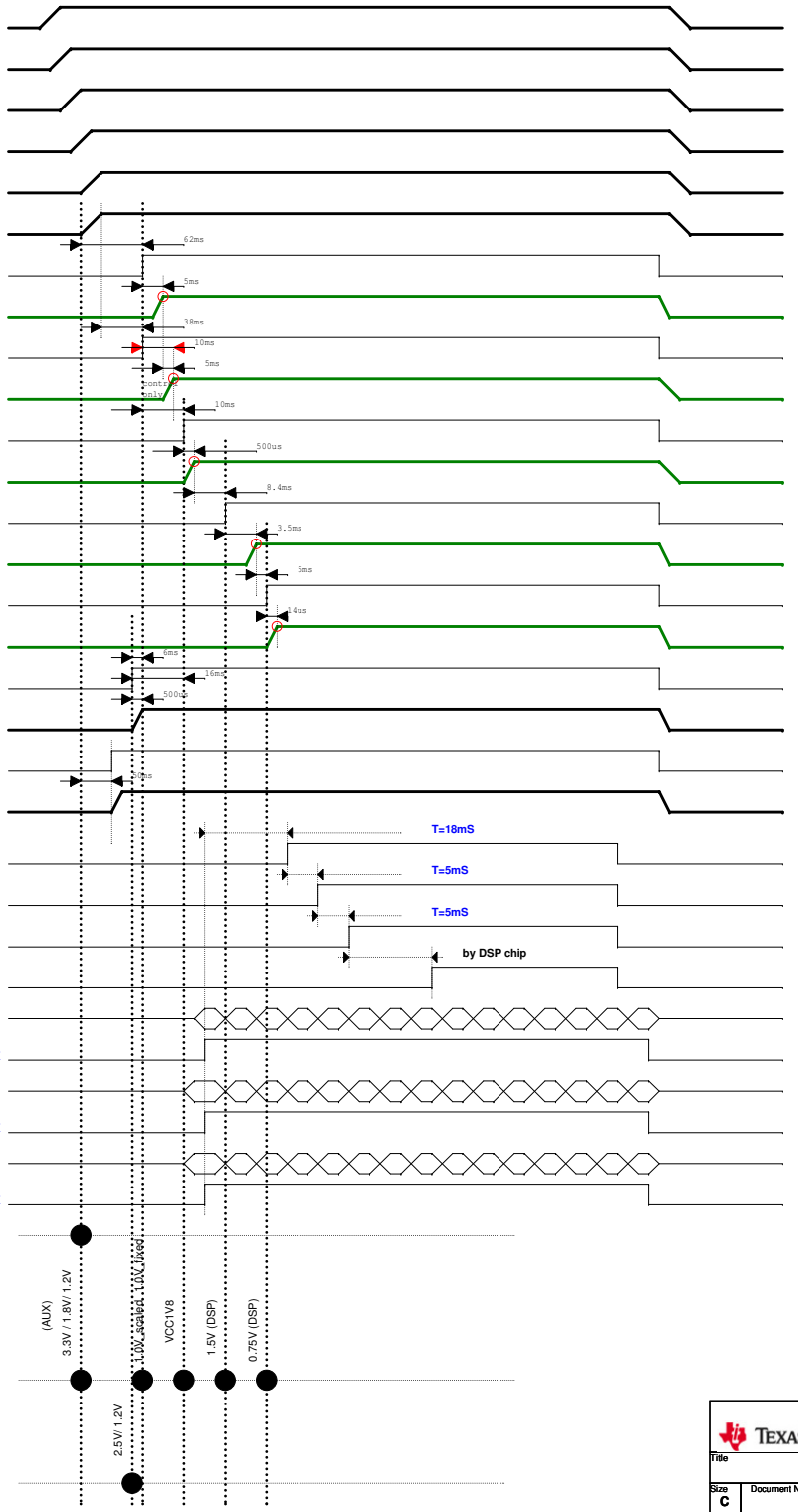
Power Sequence

				VCC3V3_MP_AMC
S0		MMC		VCC3V3_MP
S1				VCC12
S2	Other	FT2232H	XC3S200AN	VCC3V3_AUX
S3			XC3S200AN	VCC1V8_AUX
S4		88E1111	XC3S200AN	VCC1V2
S5				PMBUS & UCD9222_ENA1
S6		DSP TMS320C6670		CVDD
S7				PMBUS & UCD9222_ENA2
S8		DSP TMS320C6670		VCC1V0
S9				VCC1V8_EN
S10		DSP TMS320C6670		VCC1V8
S11				VCC1V5_EN
S12	DDR3	DSP TMS320C6670		DDR3 SDRAM VCC1V5
S13				VCC0V75_EN
S14	DDR3	DSP TMS320C6670		DDR3 Vref VCC0V75
S15				VCC2V5_EN
S16		88E1111		VCC2V5
S17				VCC5_EN
S18		XDS560V2 Mazzenine Board		VCC5



Ther is no specific power-up nor power-down sequence.

When power on: VDD → VCC_1V0 scaled → VCC_1V0 Fixed
→ VCC1V8 → 1.5V/(DDR3_IO) 0.75V/(DDR3_Vref)

When power down: 1.5V/(DDR3_IO) 0.75V/(DDR3_Vref) → VCC1V8 → VCC_1V0 Fixed
→ VCC_1V0 scaled → VDD

Ther is no specific power-up nor power-down sequence.

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POWER CONSUMPTION

	V	I	Qty	Isub.	Efficiency	Max. Power Design Pd (W)	Max. Power Design I12V	Max. Power Design I3vsb	Operating (for Thermal) Utilization	Operating (for Thermal) Pd (W)	Note
1.0V Adjustable core (12V-->1.0V)				**9.750**			**0.914**				UCD9222 +UCD74110
TMS320C6670	0.90	9.750	1	9.750	80%	10.969	0.914	x	70%	7.678	
1.0V Fixed core (12V-->1.0V)				**4.520**			**0.419**				UCD9222 +UCD74106
TMS320C6670	1.00	4.520	1	4.520	90%	5.022	0.419	x	70%	3.516	
1.5V (12V-->1.5V)				**2.266**			**0.315**				TPS54620
TMS320C6670	1.50	0.266	1	0.266	90%	0.443	0.037	x	70%	0.310	
DDR3	1.50	0.300	5	1.500	90%	2.500	0.208	x	100%	2.500	
0.75V(VTT for DDR3) 1.5V-->0.75V							x				TPS51200
DDR3	0.75	0.100	5	0.500	45%	0.833	0.069	x	70%	0.583	
3.3V_AUX (12V-->3.3V_AUX)				**1.000**			**0.679**				TPS54620
FPGA	3.30	0.024	1	0.024	85%	0.093	0.008	x	70%	0.065	
XDS560V2 Mazzenine Board	3.30	0.300	1	0.300	85%	1.165	0.097	x	70%	0.815	
FT2232H	3.30	0.210	1	0.210	85%	0.815	0.068	x	70%	0.571	
Others	3.30	0.660	1	0.660	85%	2.562	0.214	x	70%	1.794	
1.2V_AUX (3.3V_AUX-->1.2V_AUX)							x				TPS73701DCQ
FPGA	1.20	0.125	1	0.125	30%	0.500	0.042	x	70%	0.350	
88E1111	1.00	0.250	1	0.250	90%	0.278	0.023	x	70%	0.194	
1.8V (3.3V_AUX-->1.8V_AUX)							x				TPS73701DCQ
FPGA	1.80	0.200	1	0.200	46%	0.783	0.065	x	70%	0.548	
Others	1.80	0.100	1	0.100	46%	0.391	0.033	x	70%	0.274	
1.8V (1.8V_AUX-->1.8V)							x				TPS73701DCQ
TMS320C6670	1.80	0.116	1	0.116	46%	0.454	0.038	x	70%	0.318	
FT2232H	1.80	0.075	1	0.075	46%	0.293	0.024	x	70%	0.205	
2.5V (3.3V-->2.5V)							x				TPS73701DCQ
88E1111	2.50	0.210	1	0.210	65%	0.808	0.067	x	70%	0.565	
5V (12V-->5V)				**1.000**			**0.490**				TPS54231
XDS560V2 Mazzenine Board	5.00	1.000	1	1.000	85%	5.882	0.490	x	70%	4.118	
3.3V_MP (150mA)				**0.048**			x	**0.048**			
MMC_MSP430	3.30	0.048	1	0.048	100%	0.158	x	0.048	70%	0.111	
Total power consumption						**Pmax.**	**I12V**	**I3VSB**		**Pop.**	
						33.951	**2.816**	**0.096**		**24.515**	

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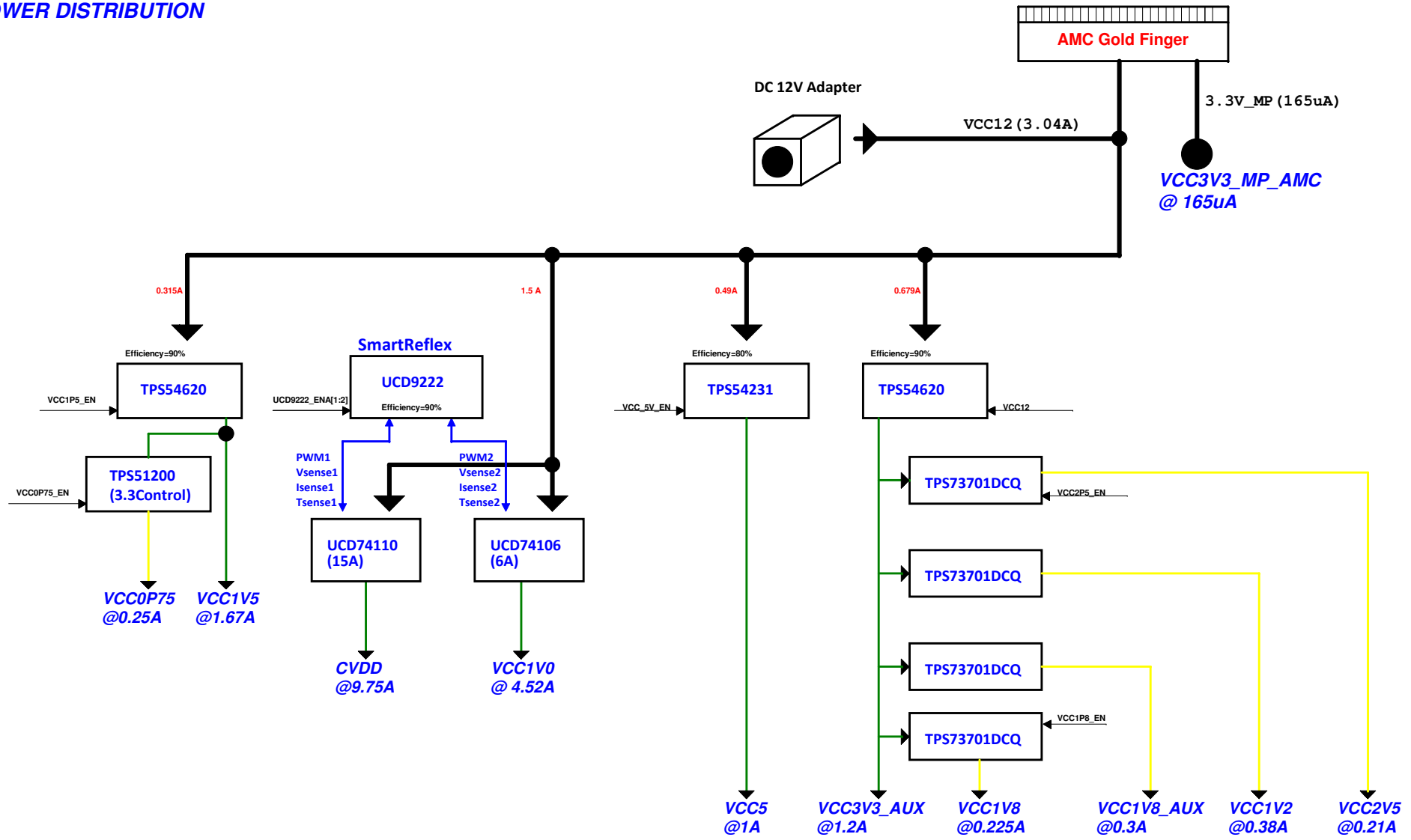
POWER DISTRIBUTION



* DDR3
1.5V / 0.24A (VDD)*5 Total:1.2A
0.75V / 0.25A (Vref)

Quad Core DSP
TI_TMS320C6670
VCC1V0 / 9.75A Scaled/(CVDD)
VCC1V0 / 4.52A Fixed/(CVDD1)
VCC1V8 / 0.15A (DVDD18)
1.5V / 0.47A (DDR3_IO)
0.75V/(DDR3_Vref)

RS232
3.3V

XDS560V2 Mazzenine Board
5.0V / 1A
3.3V / 0.3A

EEPROM
3.3V

FT2232H(USB-JTAG)
3.3V / 0.21A
1.8V / 0.075A

MicronNAND FLASH
1.8V / 0.02A

NOR FLASH
Standyby mode 1.8V/80uA

XILINX_XC3S200AN
1.2V_AUX/ 0.125A (VCCINT)
3.3V_AUX/ 0.024A (VCCAUX)

88E1111 (PHY)
2.5V / 0.21A
1.2V / 0.25A

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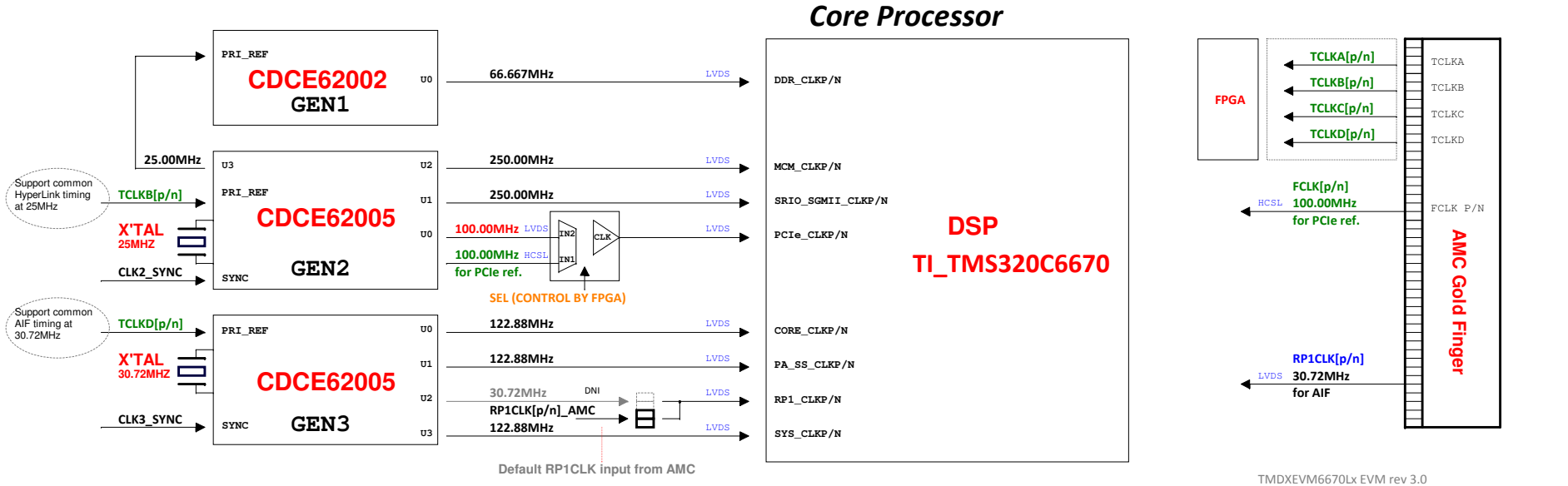
CLOCK DIAGRAM



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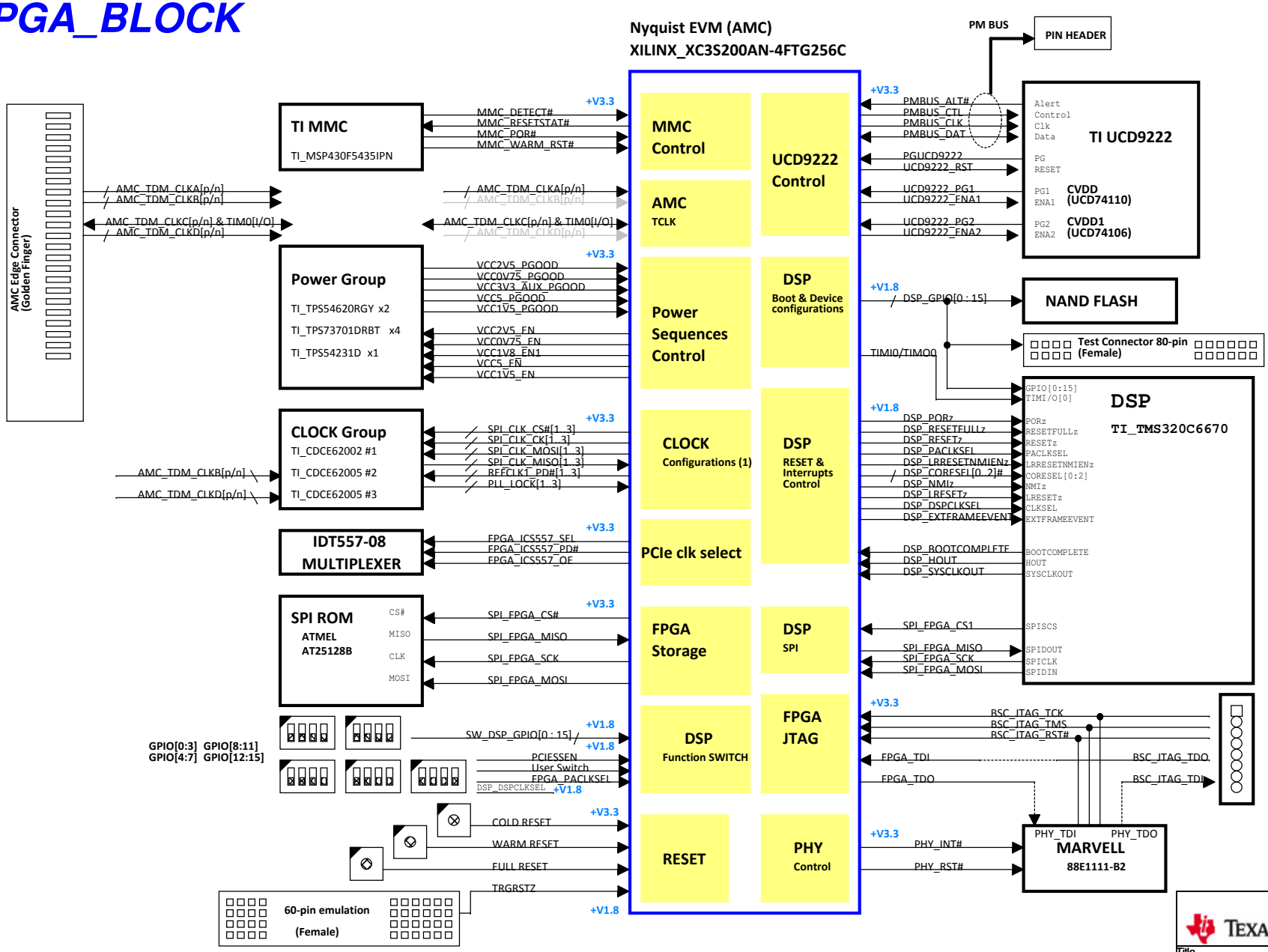
FPGA_BLOCK



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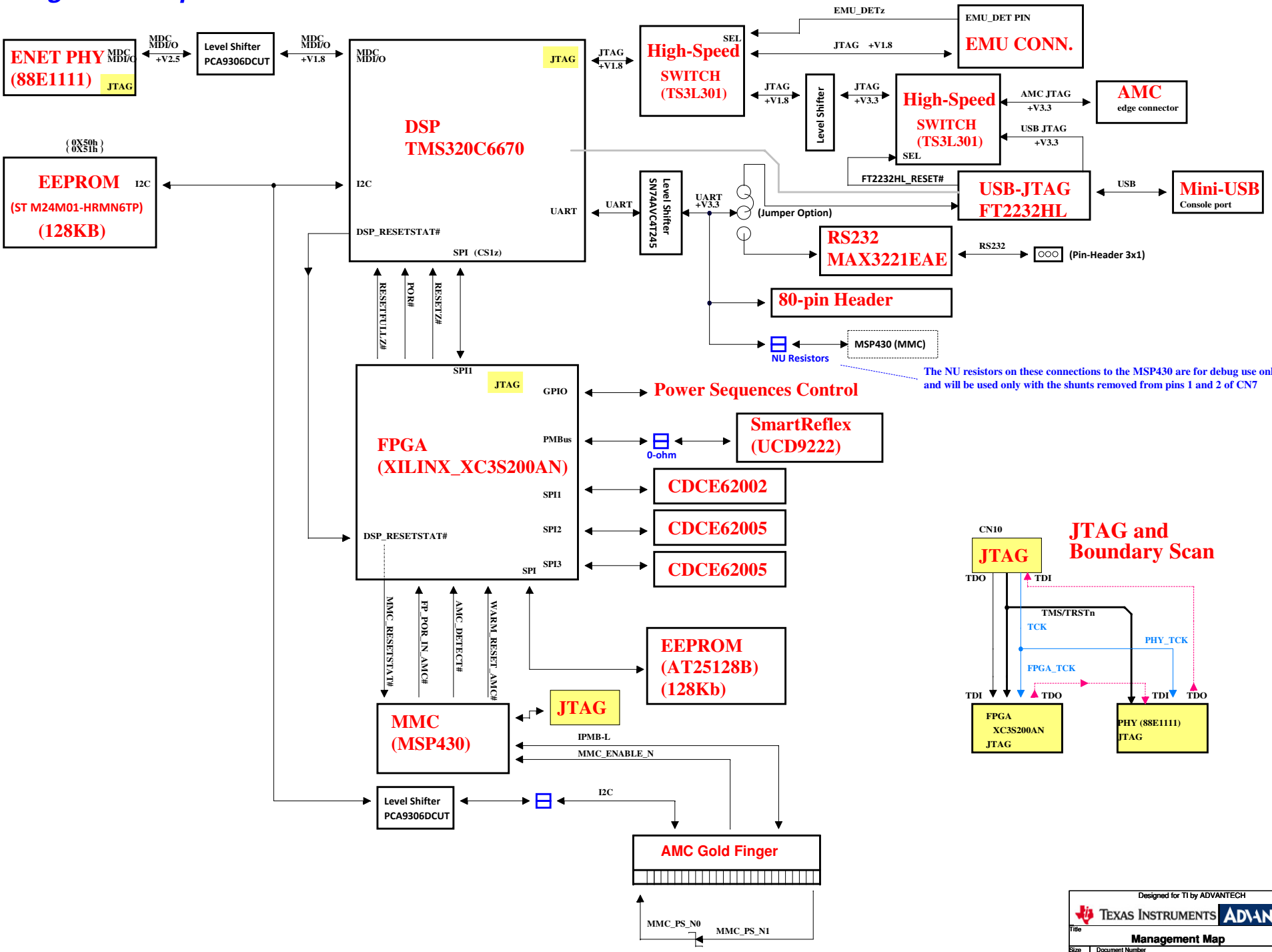
Management Map



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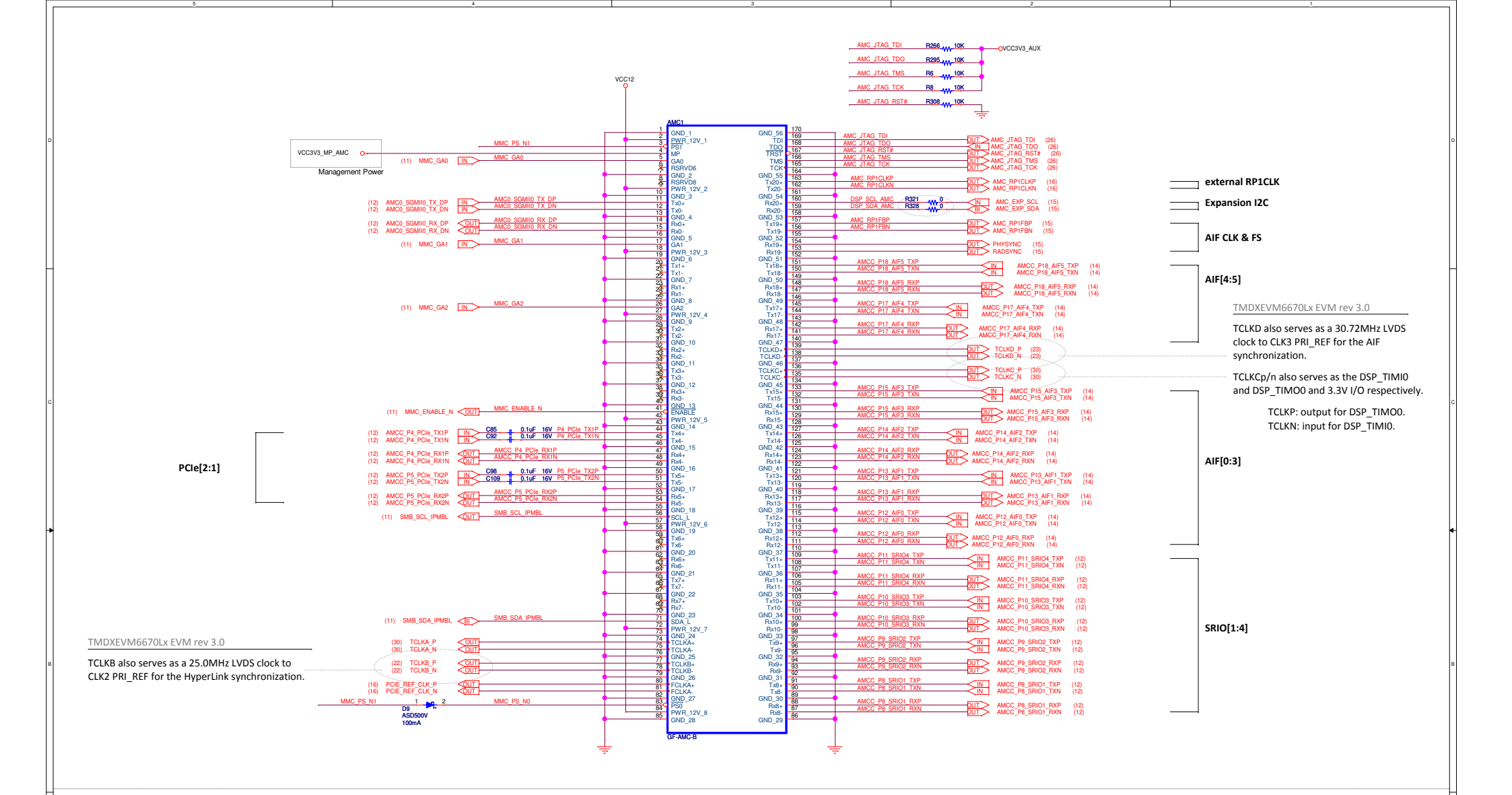
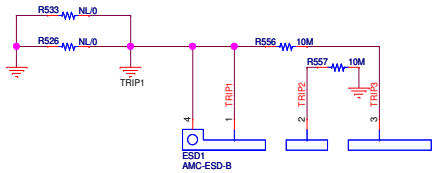
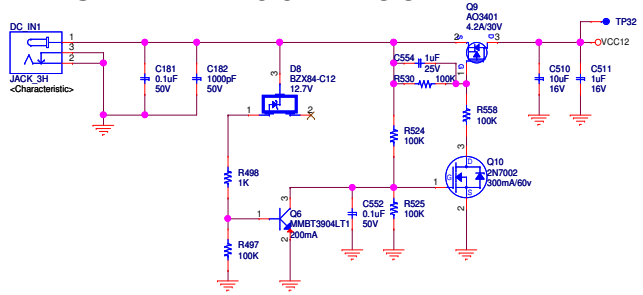


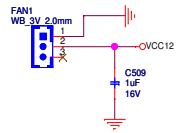
Front panel and ESD Strip



OVP: ~12.7V+0.6V = ~13.3V



DC FAN Connet for DSP



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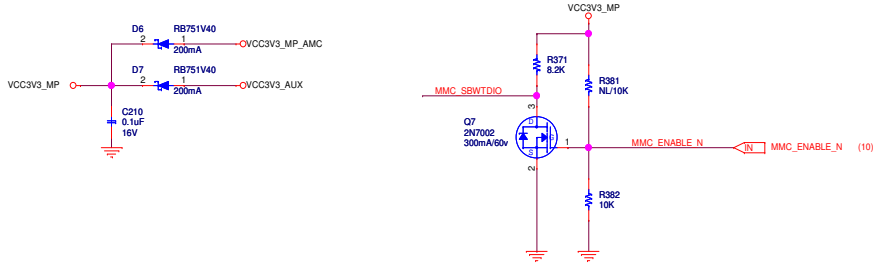
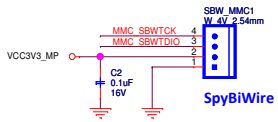
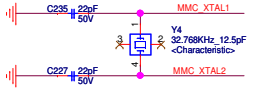
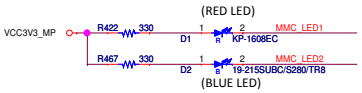
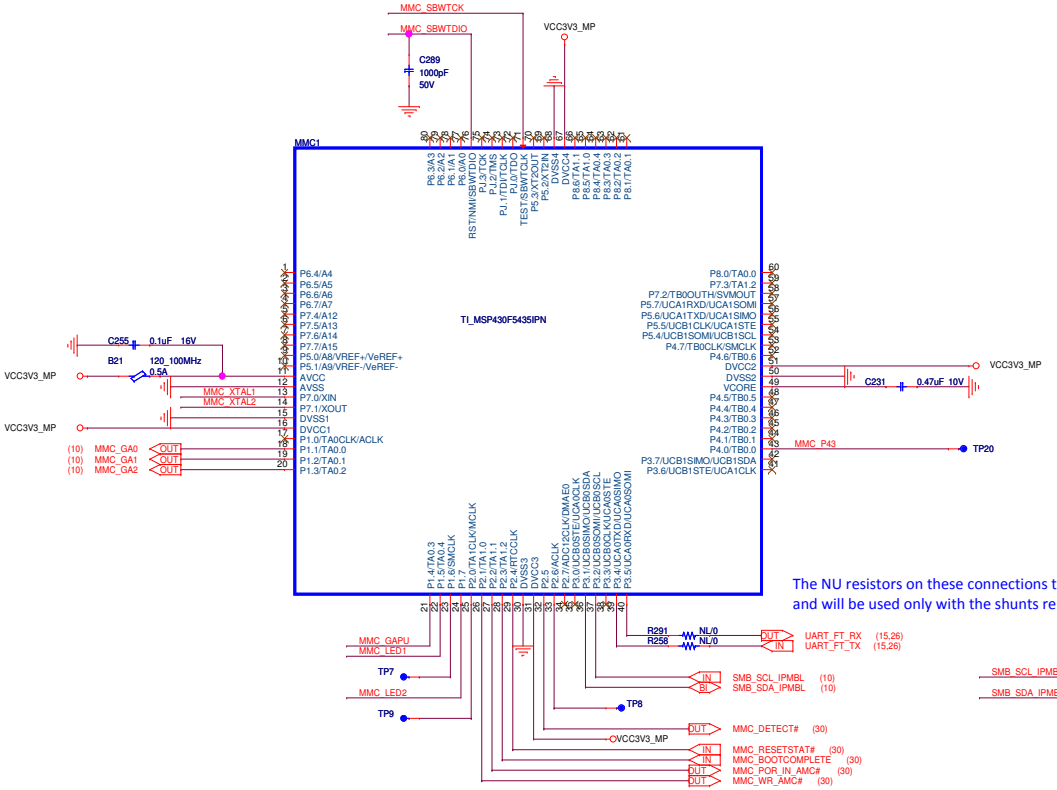
Power for MSP430



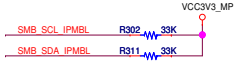


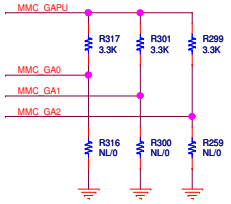


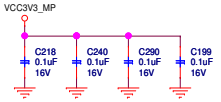




The NU resistors on these connections to the MSP430 are for debug use only and will be used only with the shunts removed from pins 1 and 2 of COM_SEL1







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MMC		
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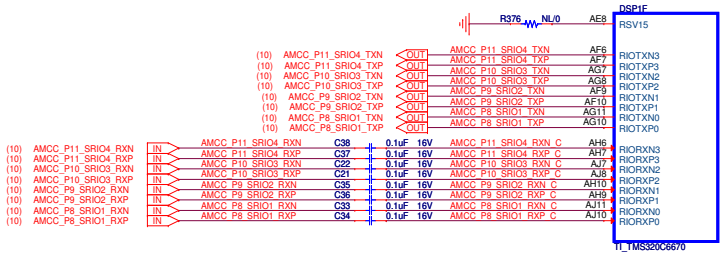
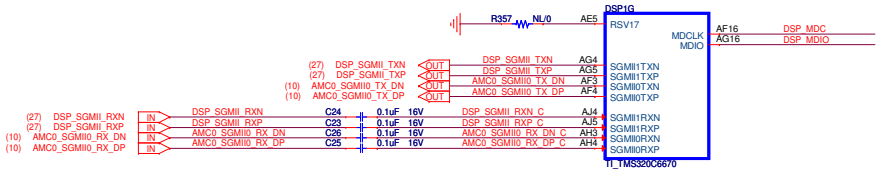
SRIO

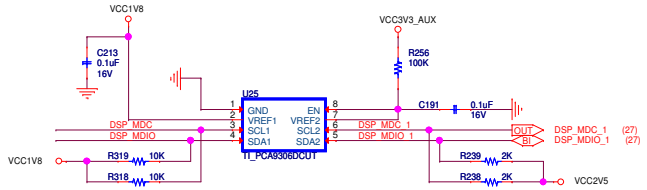


Caution!

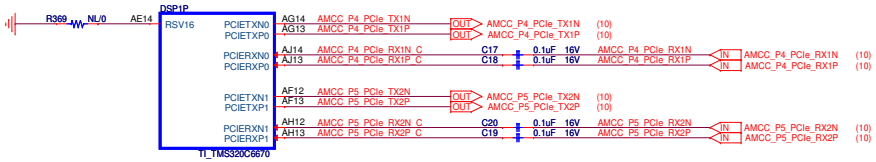
"Place ALL SERDES DC-blocking caps on top layer adjacent to the DSP's RX pins so that there are no additional vias"

SGMII



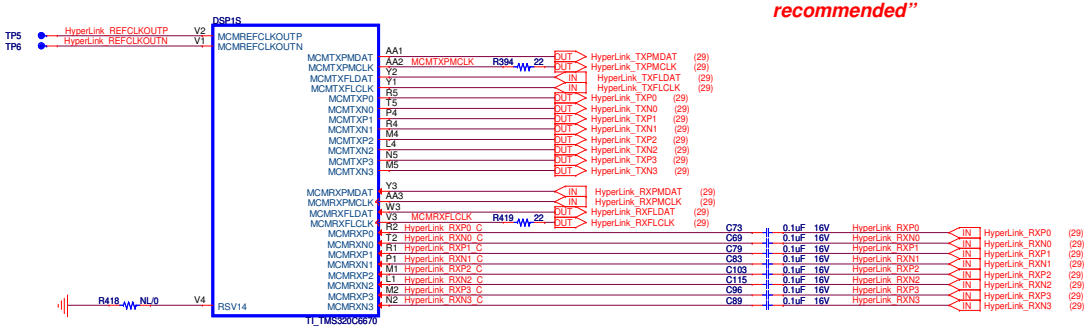


PCIE



HyperLink

"The HyperLink routes must have a maximum of 2 vias and no via stubs – top layer routing recommended"



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Title: DSP_SERDES_PORTS

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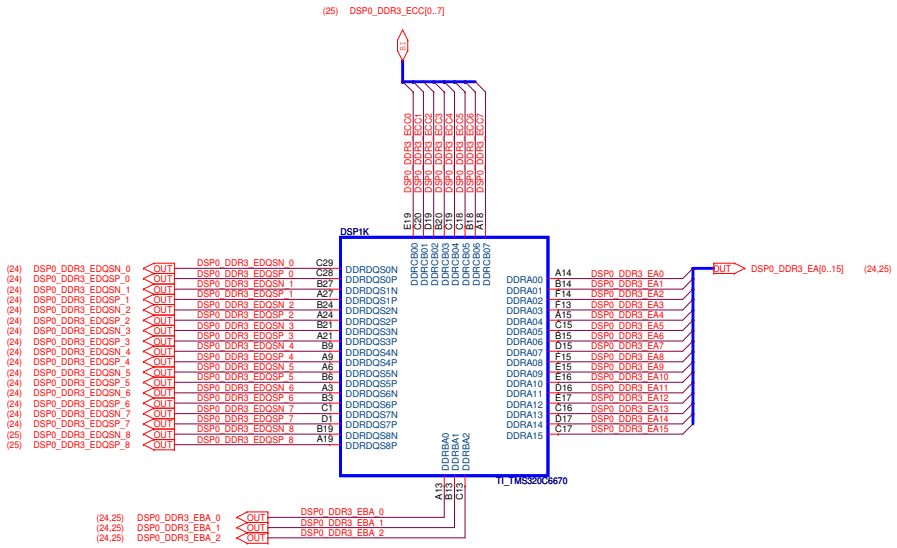
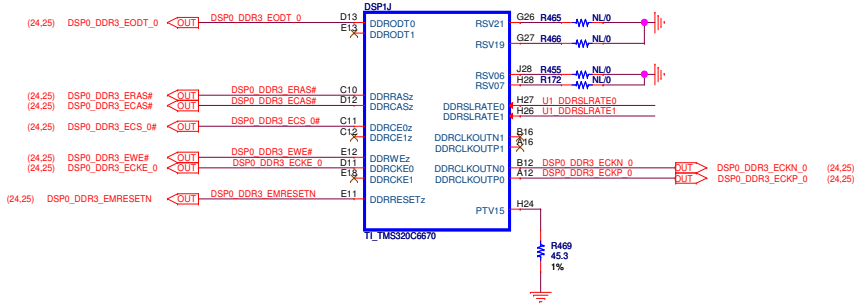
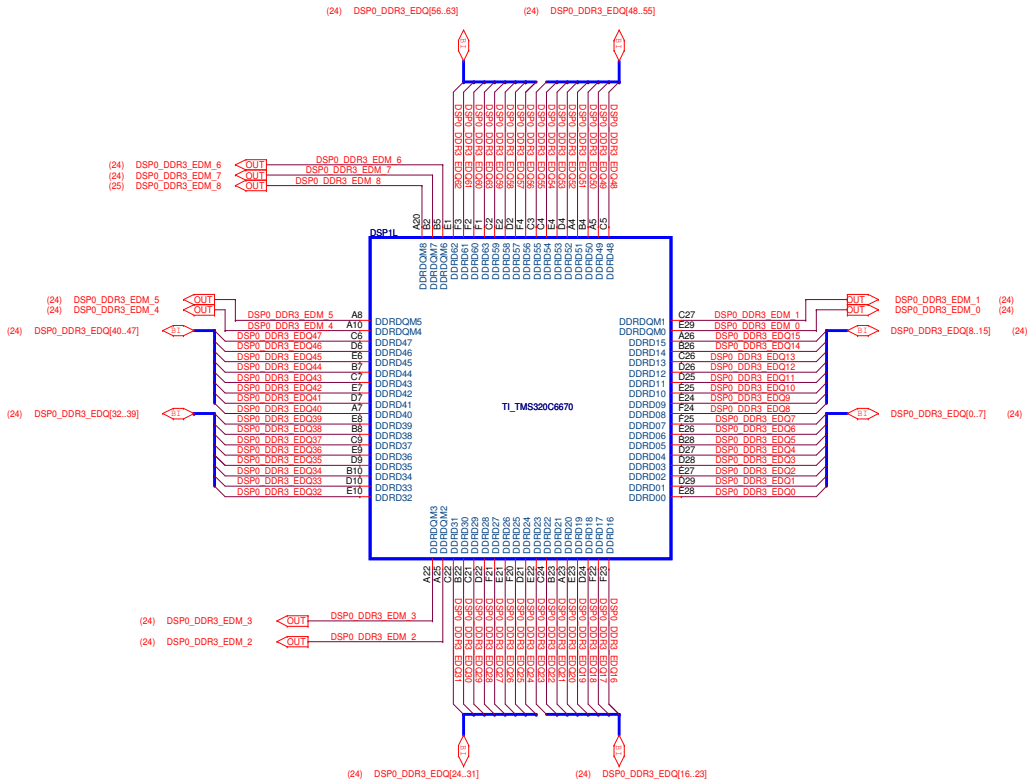
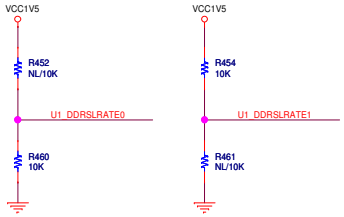


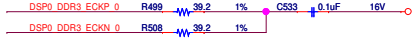




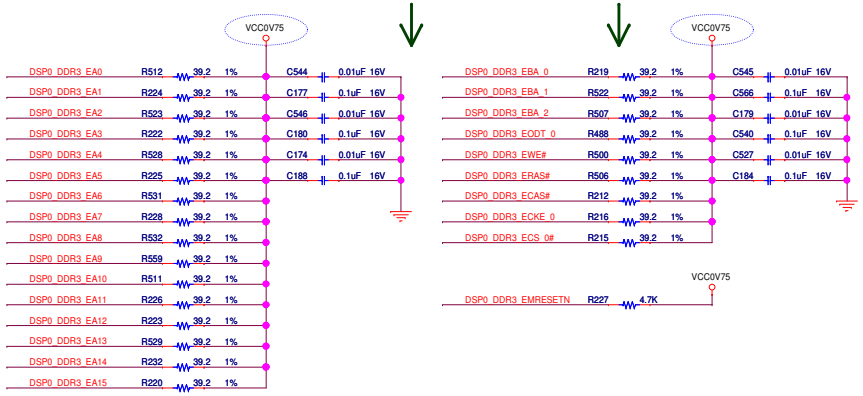


DDR3 Slew-Rate Setting (DDRSLRATE[1:0]):

0 0 Fastest
1 0 Fast
0 1 Slow
1 1 Slowest



Place these resistors at the end of the trace.



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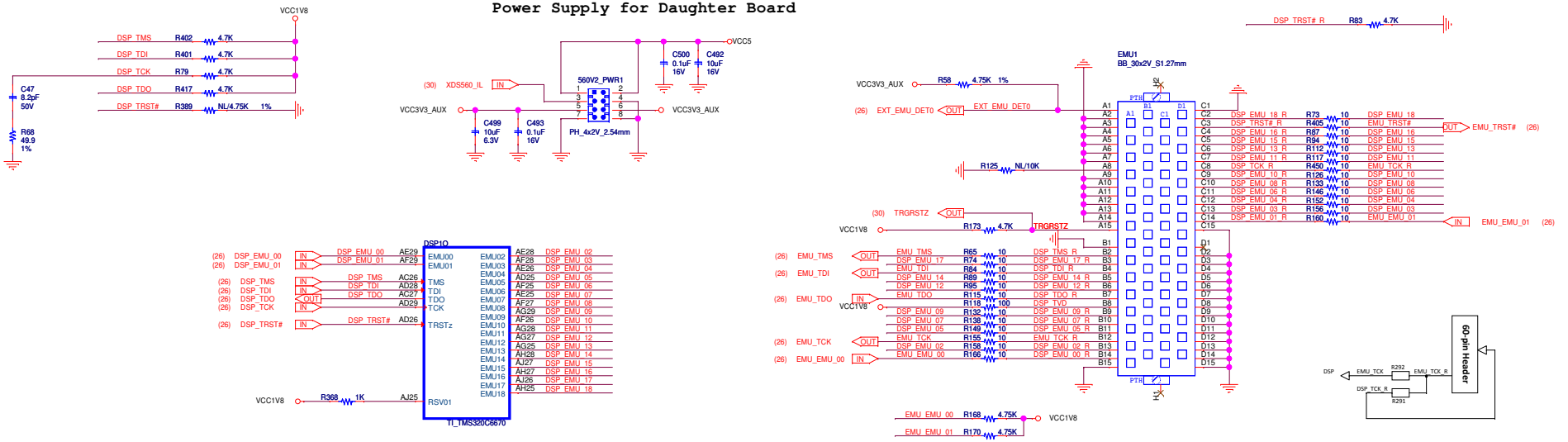
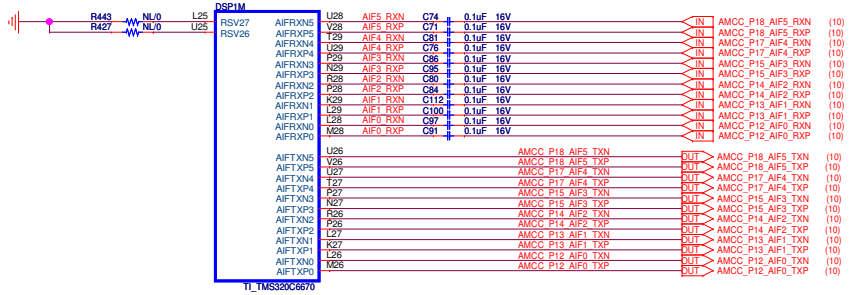
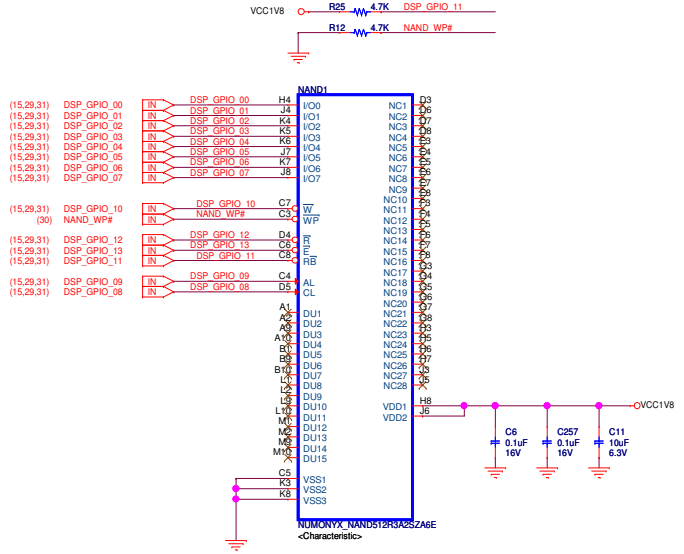
JTAG & EMU



DSP AIF



NAND FLASH



(NUMONYX_NAND512R3A2SZA6E, 1410021742)

[TI] Verify this connection matches the C6474L FLASH pin matching shown in the following table:

GP[7:0]	This 8-bit data bus is mapped to the 8-bit data bus of NAND Flash Memory.
GP[8]	This pin is mapped to the Command Latch Enable (CLE) pin of NAND Flash Memory.
GP[9]	This pin is mapped to the Address Latch Enable (ALE) pin of NAND Flash Memory.
GP10	This pin is mapped to the Write Enable (nWE) pin of the NAND Flash Memory.
GP11	This pin is mapped to the Ready/Busy (RB) pin of the NAND Flash Memory.
GP12	This pin is mapped to the Read Enable (nRE) pin of the NAND Flash Memory.
GP13	This pin is mapped to the Chip Enable (nCE) pin of the NAND Flash Memory.

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Title	DSP_JTAG_EMU_AIF	
Size: C	Document Number: DSPM-8302E	Rev: A103-1
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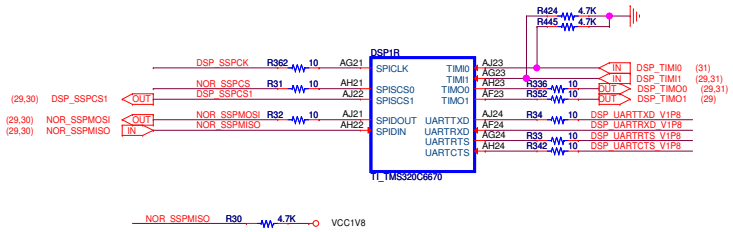
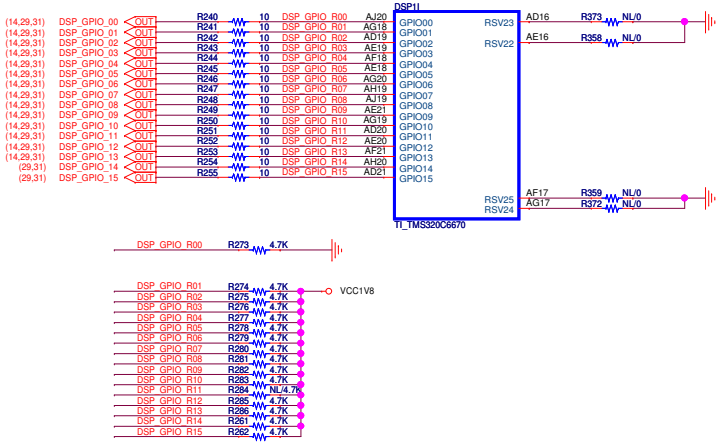
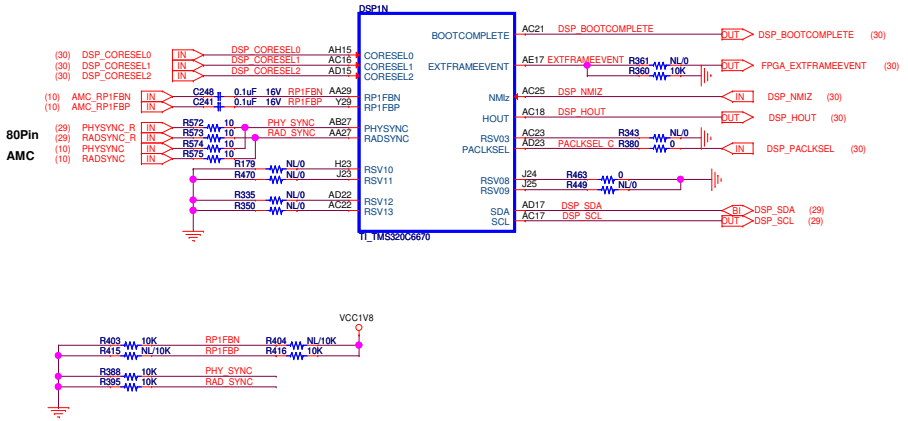
I2C, TIMER0,1, SPI, UART



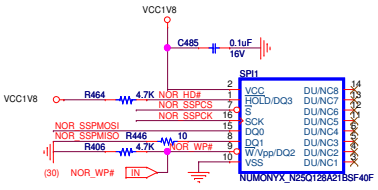
GPIO



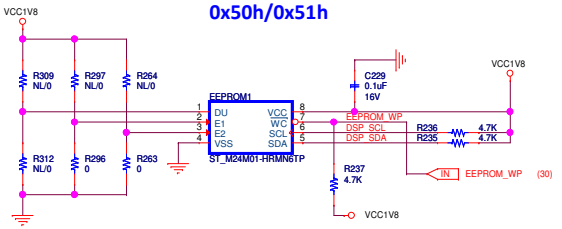
Core Control

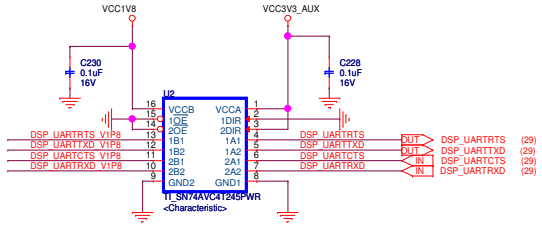


16M SPI NOR Flash

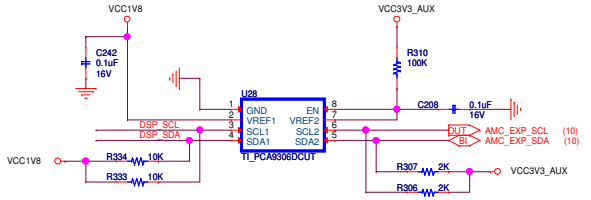


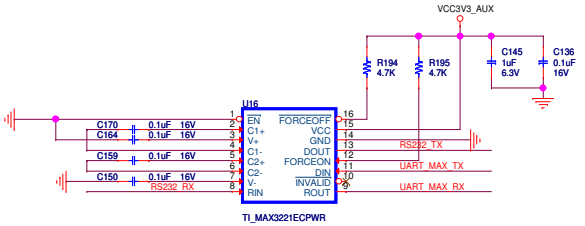
1M-bit I2C EEPROM 0x50h/0x51h

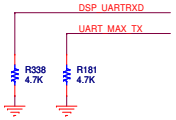


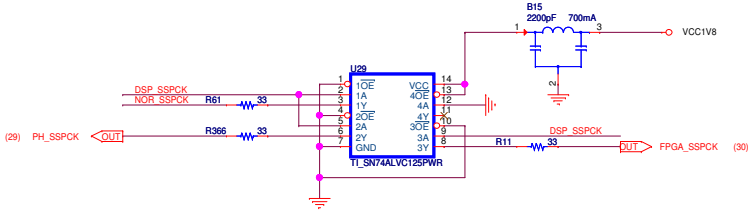


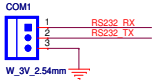
SCL/SDA



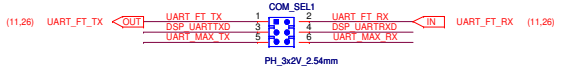








JP-UART(1-3) & (2-4) : UART over USB Connector (Default)
JP-UART(3-5) & (4-6) : UART over 3-Pin Header J5



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TEXAS INSTRUMENTS ADVANTECH

Title		
DSP_MISC		
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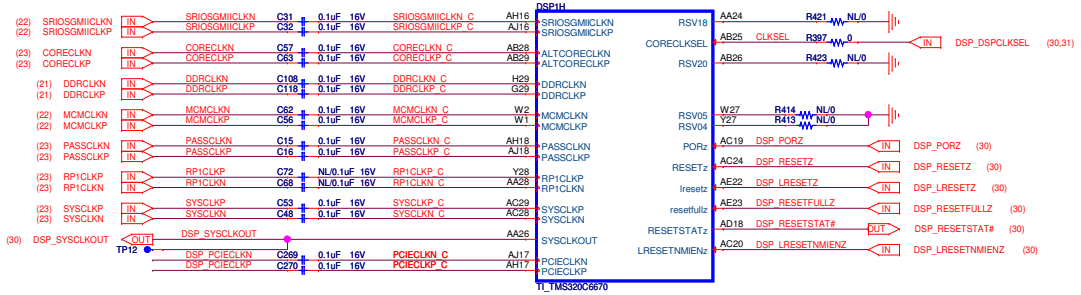
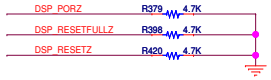
DSP CLOCK / RESET

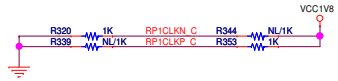
All blocking capacitors should be placed near DSP to keep connecting routes short and minimize vias

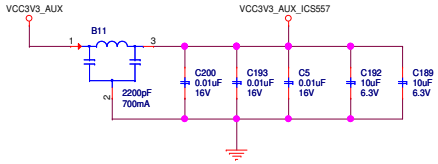
250.00MHz Input
122.88MHz Input
66.67MHz Input
250.00MHz Input
122.88MHz Input
30.72MHz Input
122.88MHz Input
100.00MHz Input

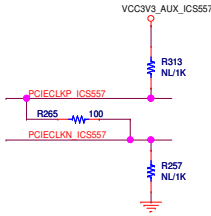


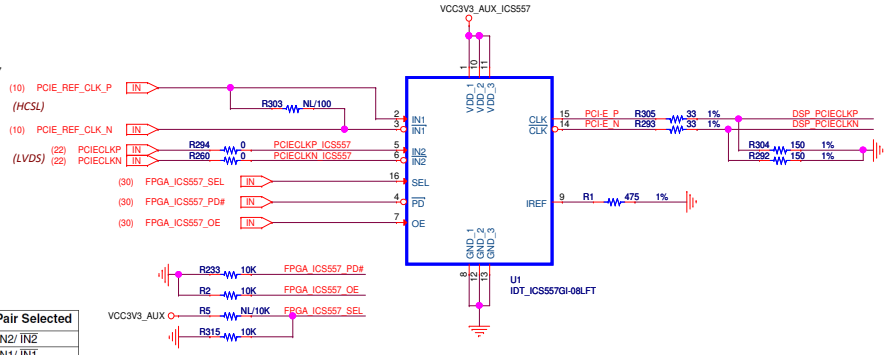


Default setting install C379,C366 caps from AMC , remove C72,C68 caps from clk3 source
Not used external connection RP1CLKP/N need pull-up and pull-down resistors









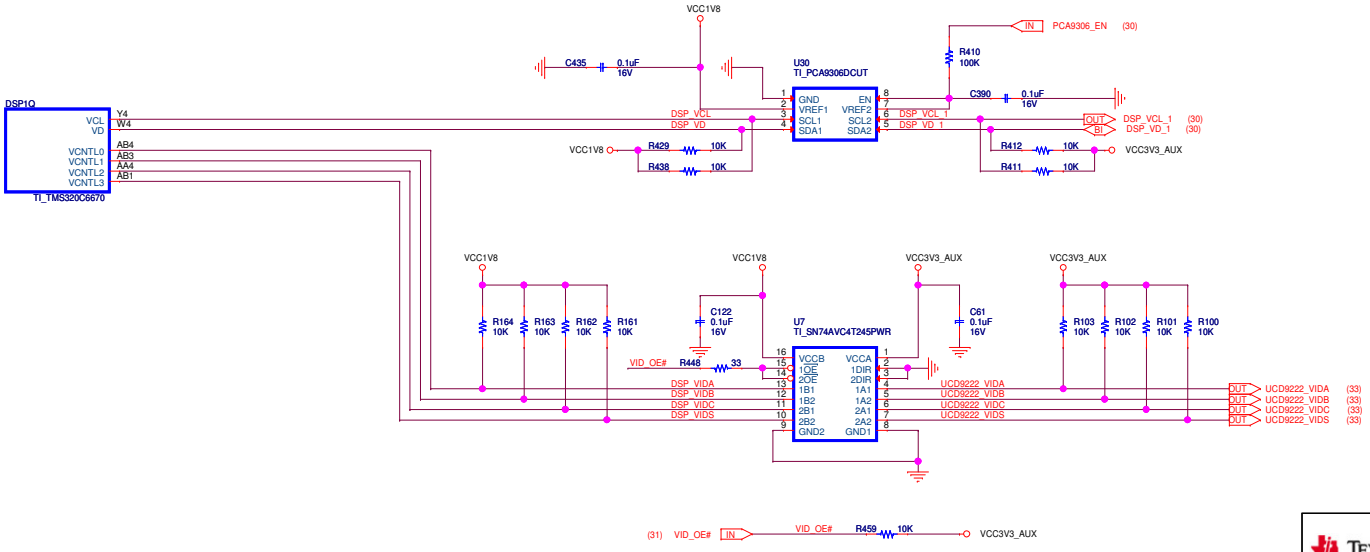
Layout From Clock Device
REF_CLK output

Select Table

SEL	Input Pair Selected
0	IN2/ $\overline{IN2}$
1	IN1/ $\overline{IN1}$

Default: IN2/CDCE62005

Smart Reflex



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Title	DSP_CLOCK_Smart Reflex	
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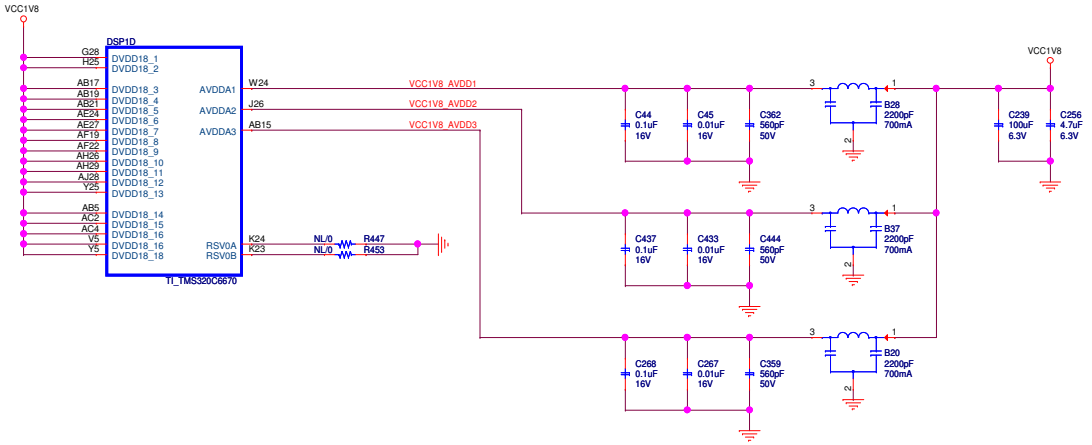
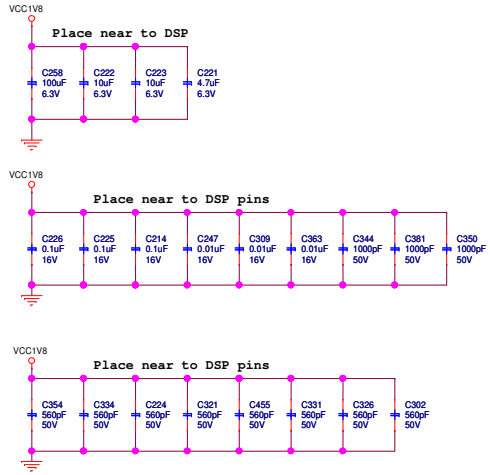
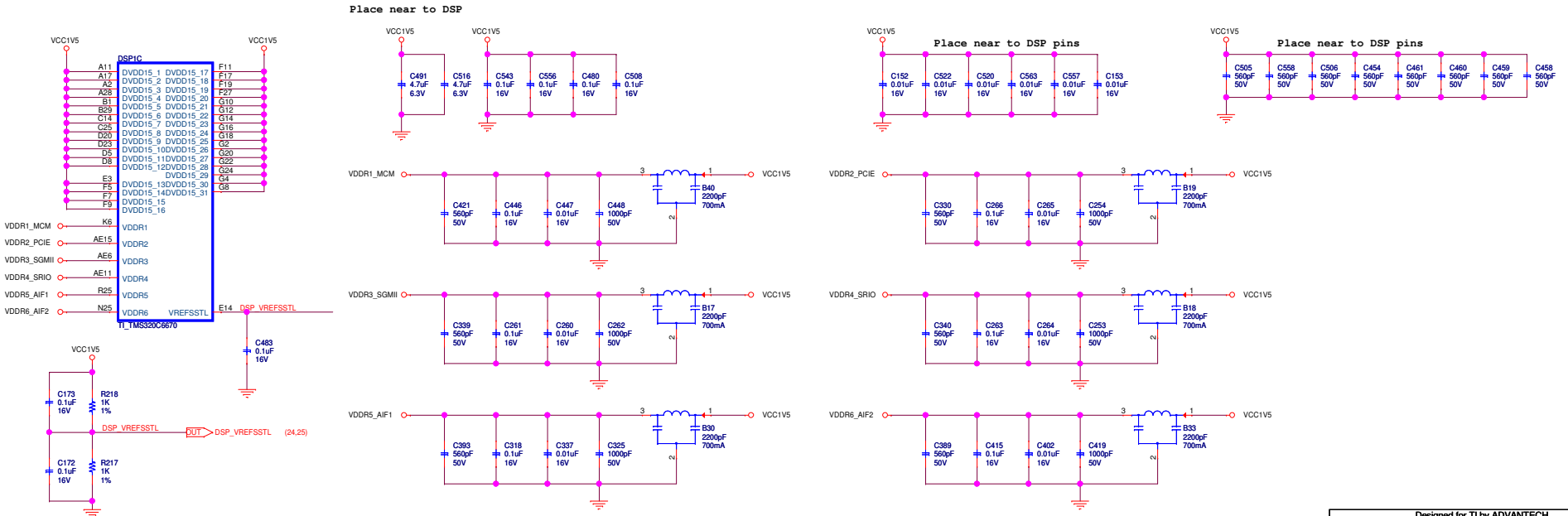
1.8V





1.5V



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Title		
DSP_POWERA		
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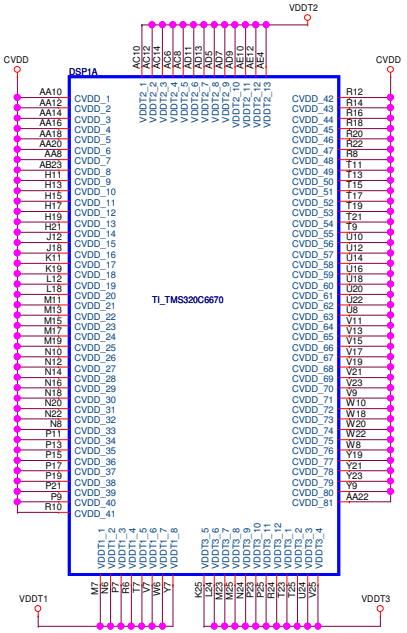
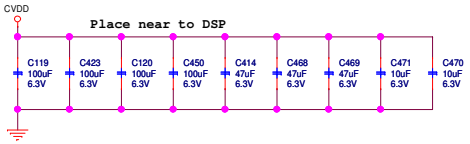
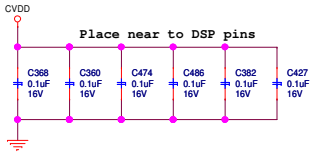
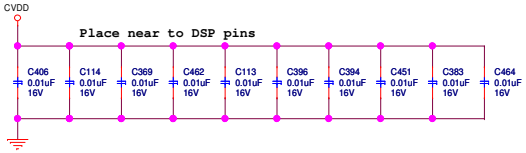
0.6V - 1.1V (CVDD) (Smart Reflex)

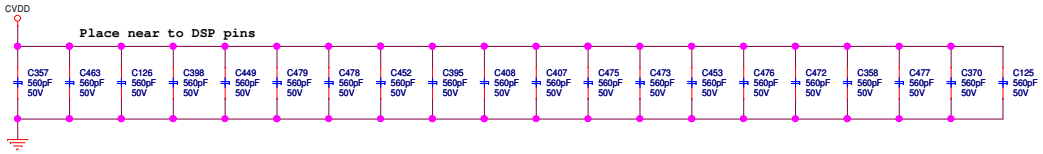
Fix_1.0V(VCC1P0)

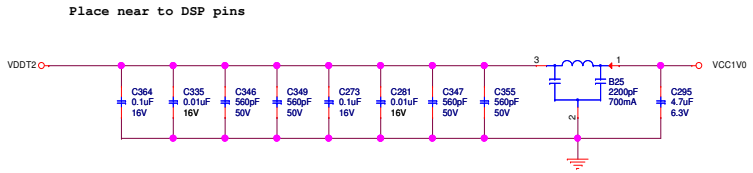


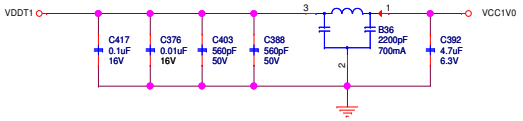


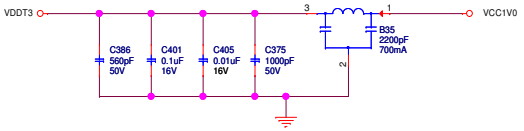












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TEXAS INSTRUMENTS ADVANTECH

Title	DSP_POWERB	
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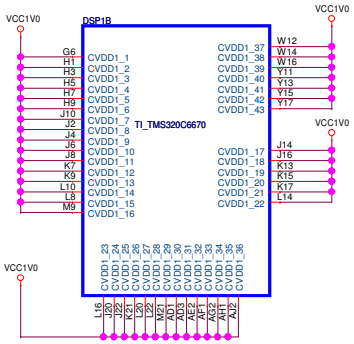
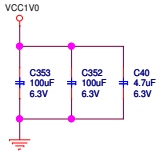
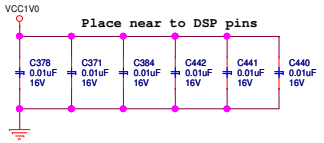
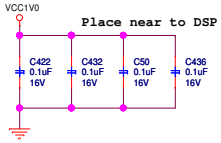
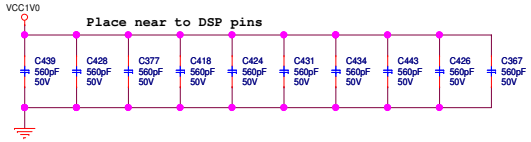
1.0V Serdes











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TEXAS INSTRUMENTS ADVANTECH

Title	DSP_POWERC	
Size: C	Document Number: DSPM-8302E	Rev: A103-1
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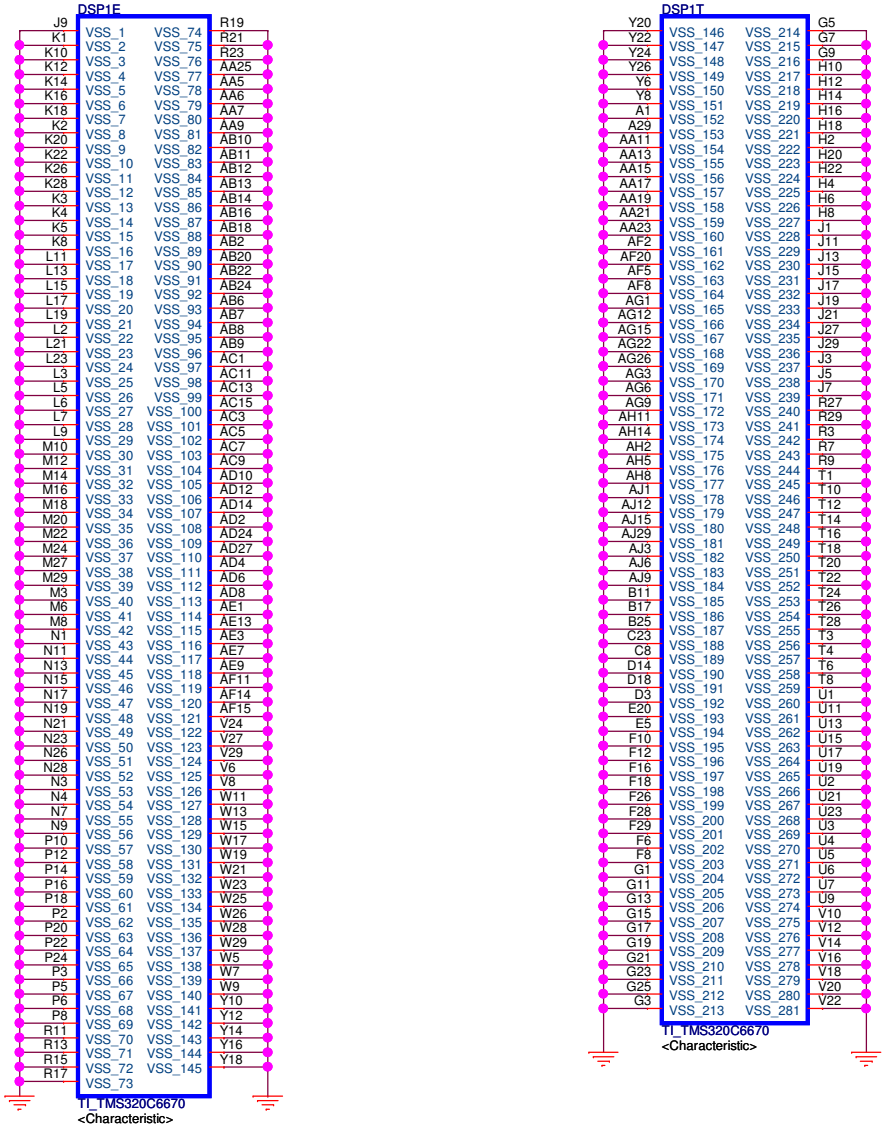

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TEXAS INSTRUMENTS ADVANTECH

Title	DSP_GND	
Size: B	Document Number: DSPM-8302E	Rev: A103-1
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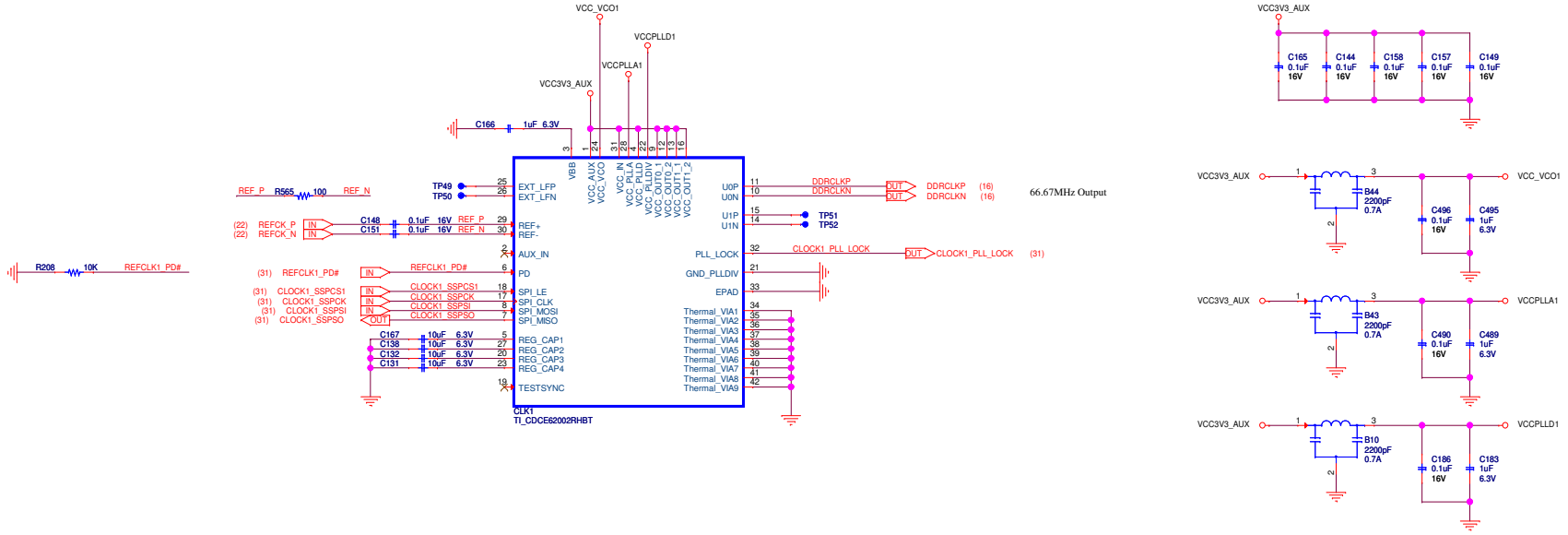
CLOCK GEN1 (DDR3)



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Title		
CLOCK GEN1		
Size: C	Document Number: DSPM-8302E	Rev: A103-1
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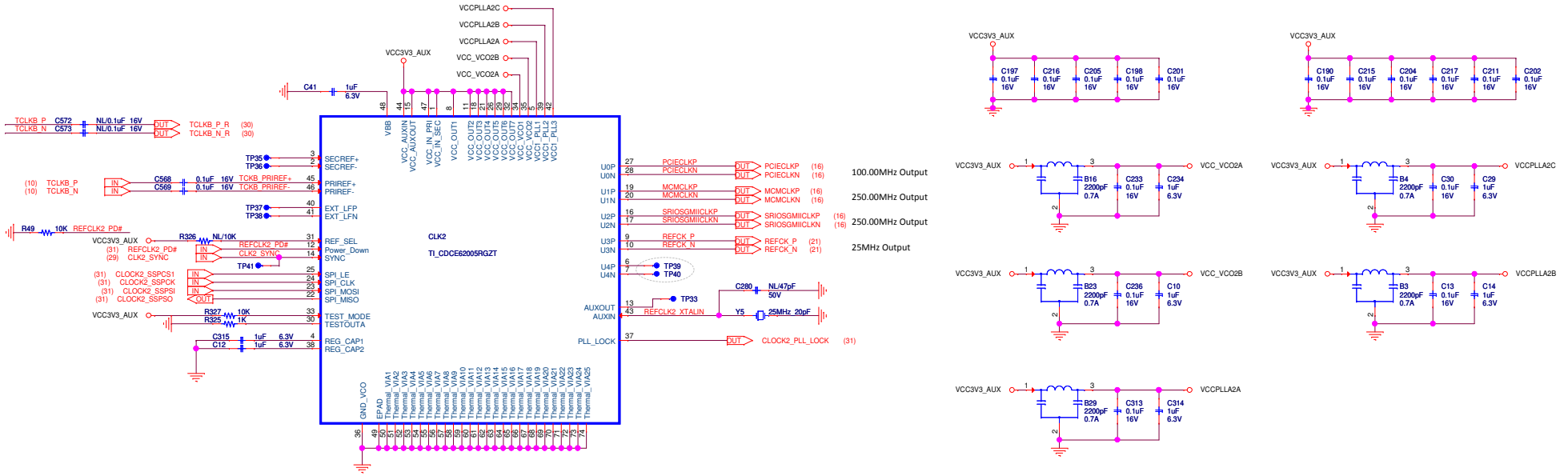
CLOCK GEN2



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TEXAS INSTRUMENTS ADVANTECH

Title	CLOCK GEN2	
Size: C	Document Number: DSPM-8302E	Rev: A103-1
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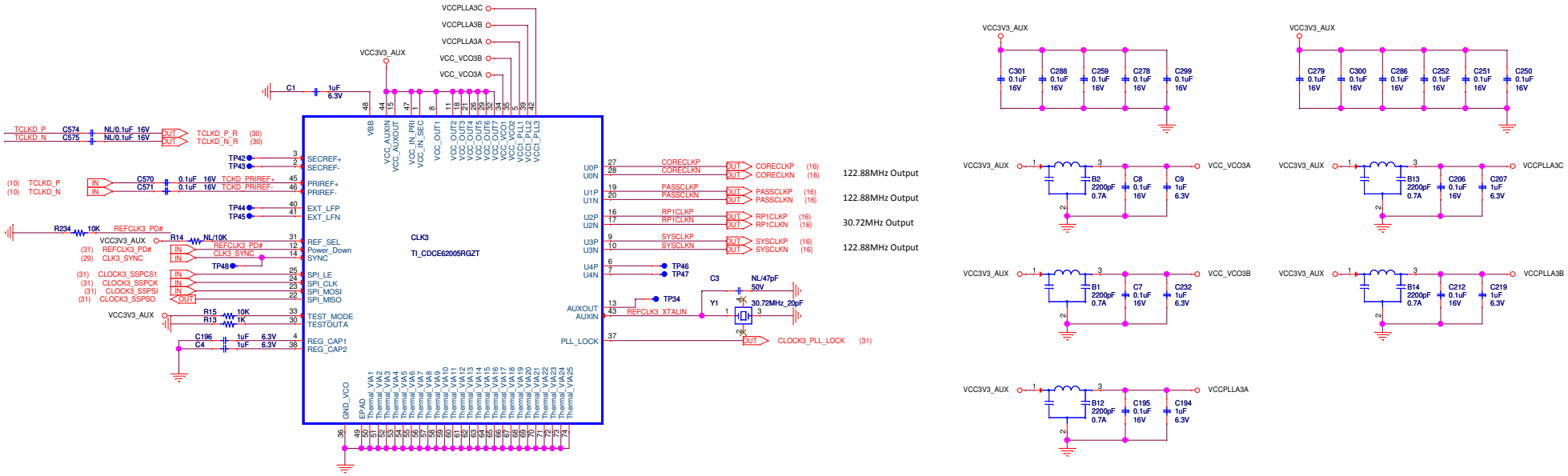
CLOCK GEN3



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TEXAS INSTRUMENTS ADVANTECH

Title		
CLOCK GEN3		
Size: C	Document Number: DSPM-8302E	Rev: A103-1
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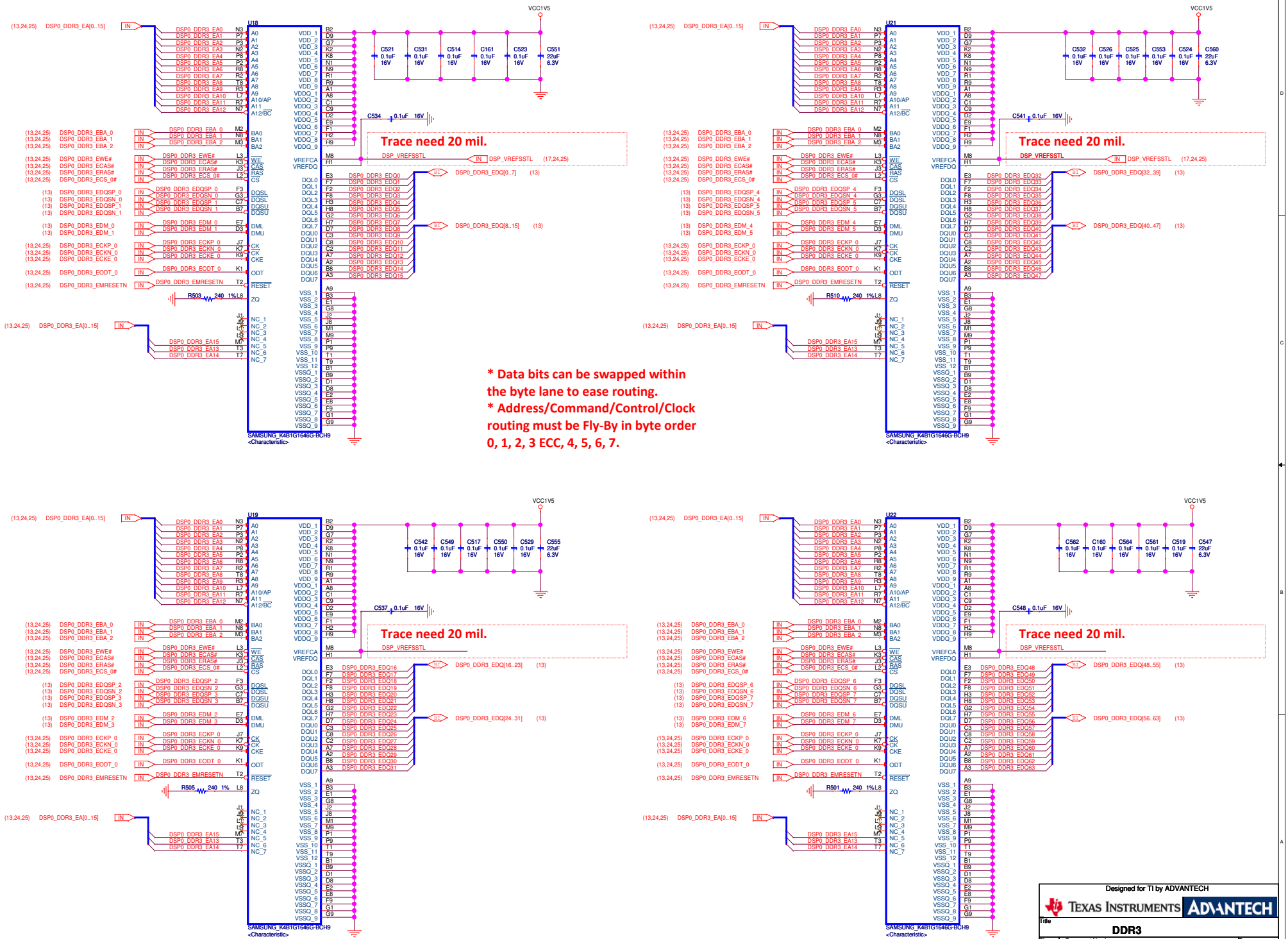
VCC1V5
U18
U21
U19
U22
Trace need 20 mil.
DSP_VREFSSTL
* Data bits can be swapped within the byte lane to ease routing.
* Address/Command/Control/Clock routing must be Fly-By in byte order 0, 1, 2, 3 ECC, 4, 5, 6, 7.
SAMSUNG_K4B1G1646G-BCH9
<Characteristic>
Designed for TI by ADVANTECH
TEXAS INSTRUMENTS
ADVANTECH
Title
DDR3
Size C
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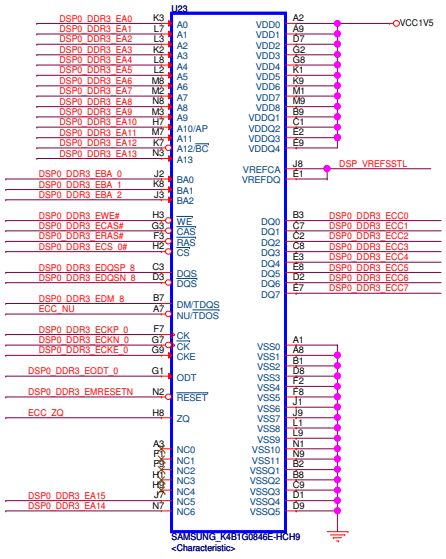
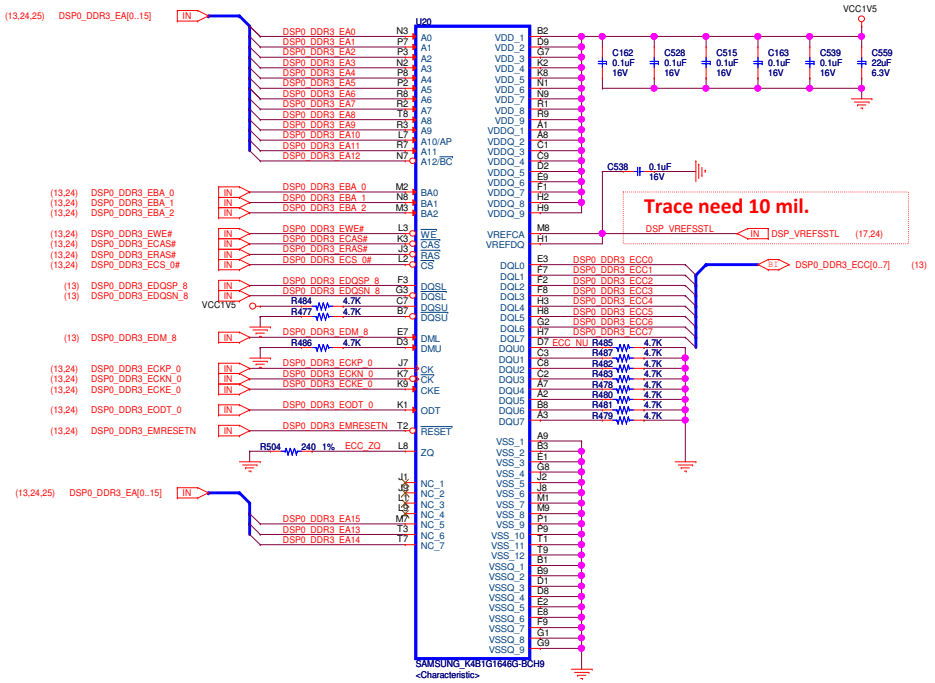
CO-LAYOUT





There are two combinations of DDR3
3.a. 512MB: 1410021410 (1Gb, X16)_DDR3-1333

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TEXAS INSTRUMENTS ADVANTECH

Title	DDR3_ECC	
Size: C	Document Number: DSPM-8302E	Rev: A103-1
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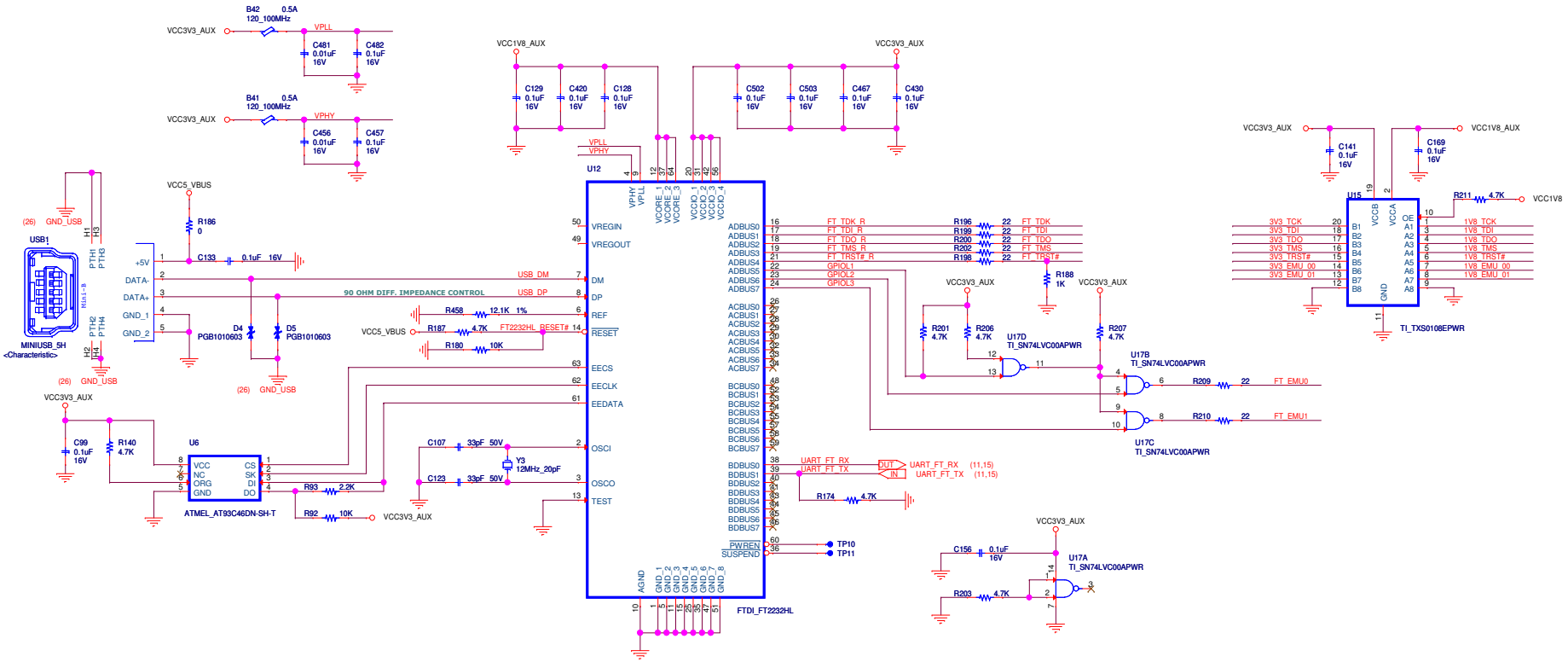
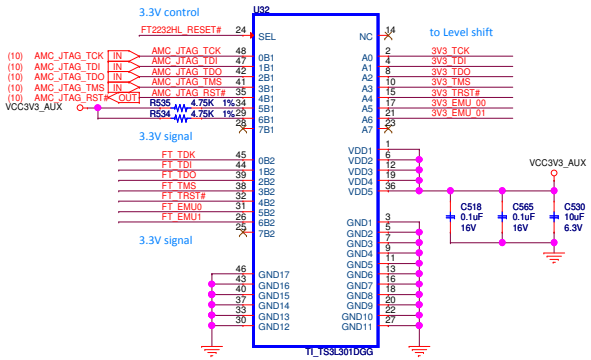
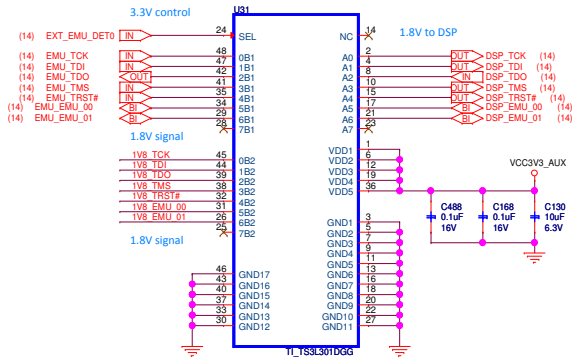


FOR EMI

B9 0.5A 120_100MHz





FUNCTION TABLE

INPUT SEL	INPUT/OUTPUT An	FUNCTION
L	nB_1	$A_n = nB_1$
H	nB_2	$A_n = nB_2$

Switch for JTAG emulation
FT2232HL_RESET# = 0 --> AMC
FT2232HL_RESET# = 1 --> Mini USB

Switch for JTAG emulation
EXT_EMU_DET = 0 --> External / Mezzanine Emulator
EXT_EMU_DET = 1 --> On board emulation

Designed for TI by ADVANTECH

Title: USB-JTAG

Size	Document Number	Rev
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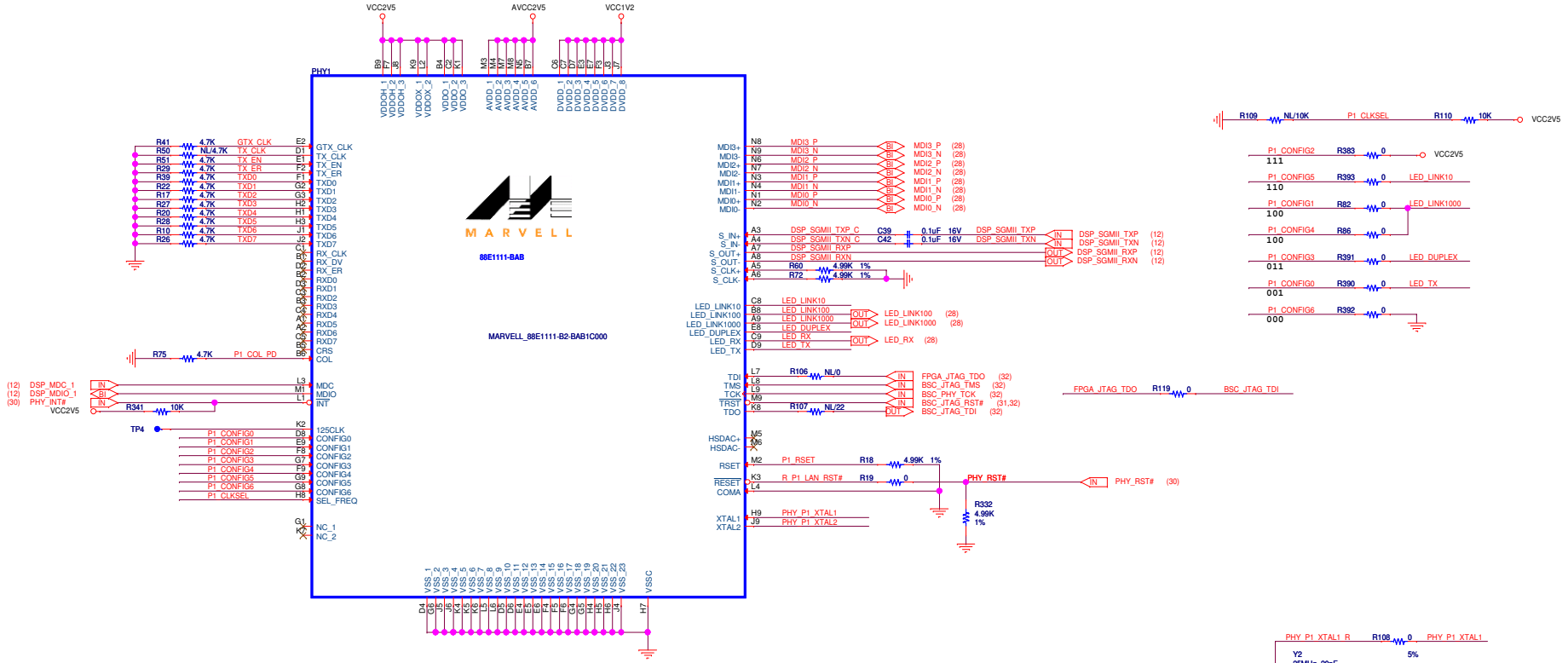

88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

PHY Address = 0x01

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	001	LED_TX	PHY Address bit[2:0] 001
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
CONFIG6	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

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Title: Gigabit Ethernet PHY

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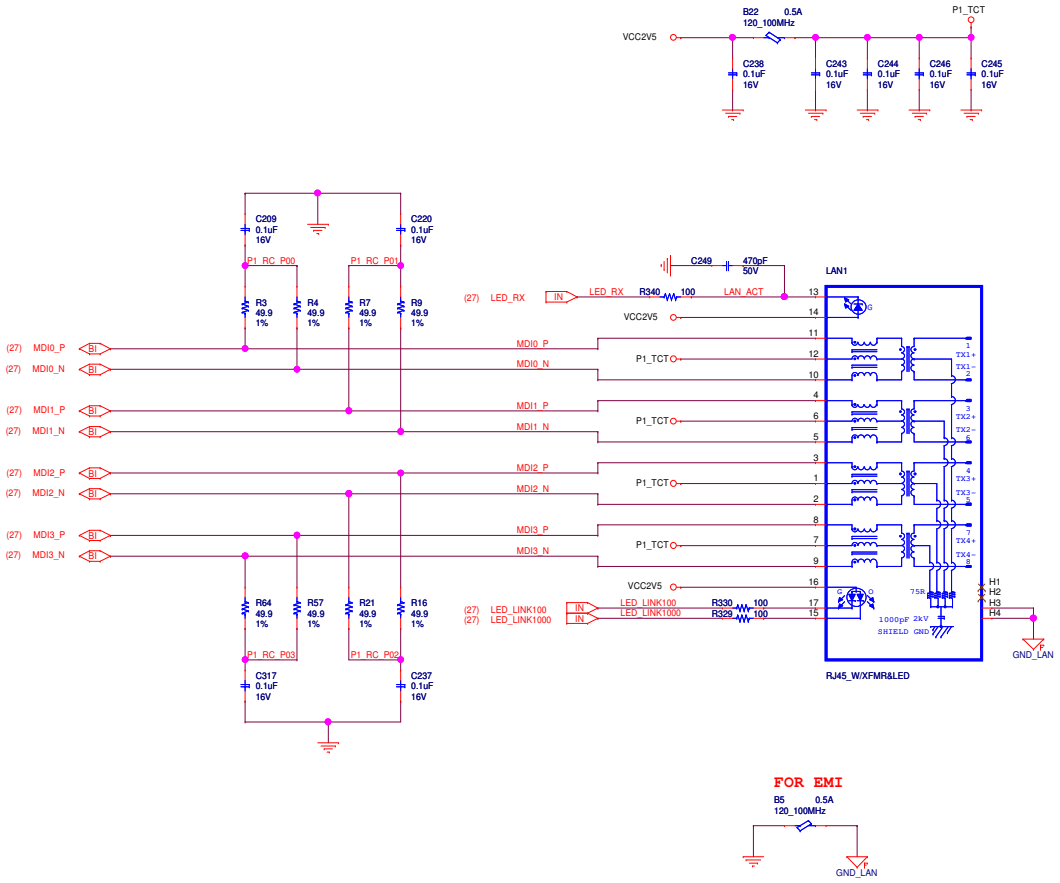
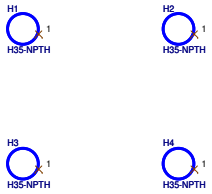
RJ-45

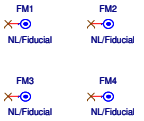


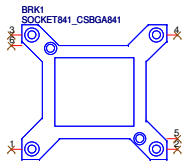
Heatsink Holes



AMC Hole

On board





(Bottom Side 3mm) Placed Capacitors

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Title		
RJ45		
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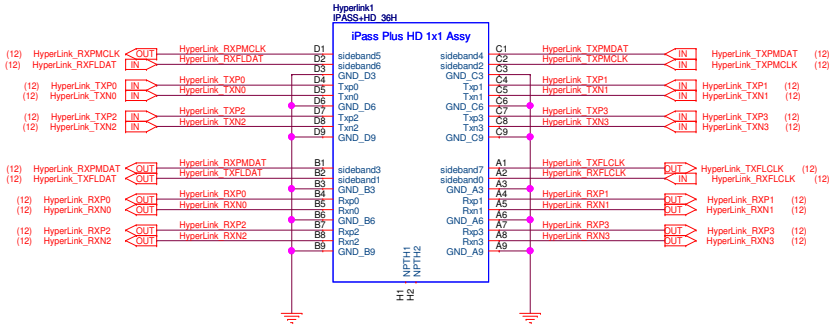
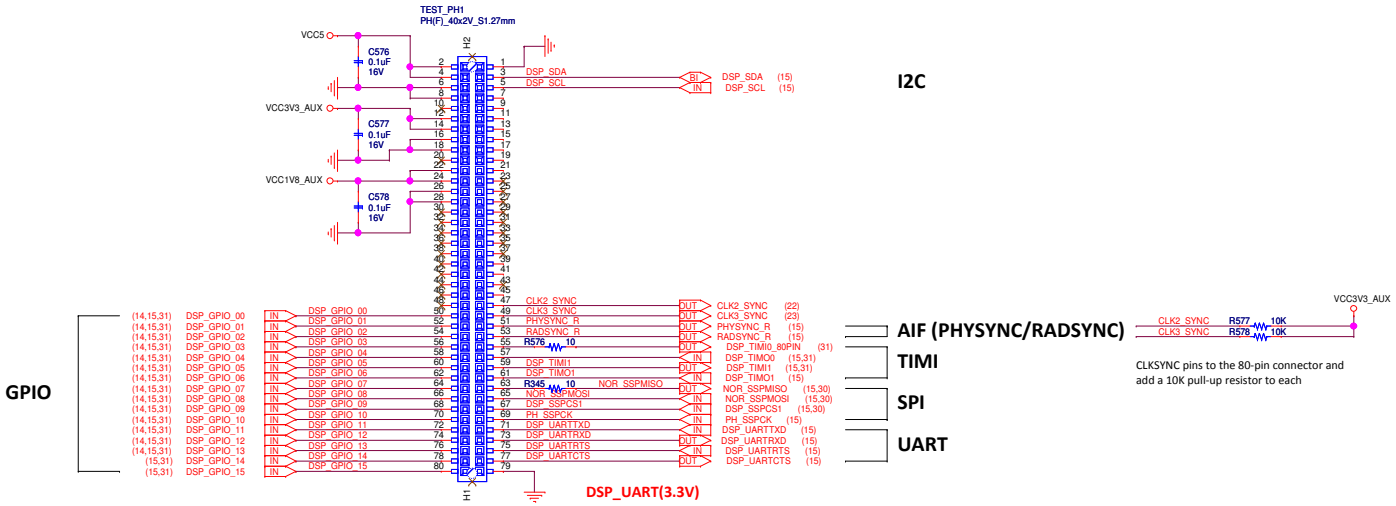
IPASS+HD for HyperLink Bus connection



80-pin Expansion Header

the interfaces on the 80-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS



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Title	Connectors for HyperLink & Debug	
Size: C	Document Number: DSPM-8302E	Rev: A103-1
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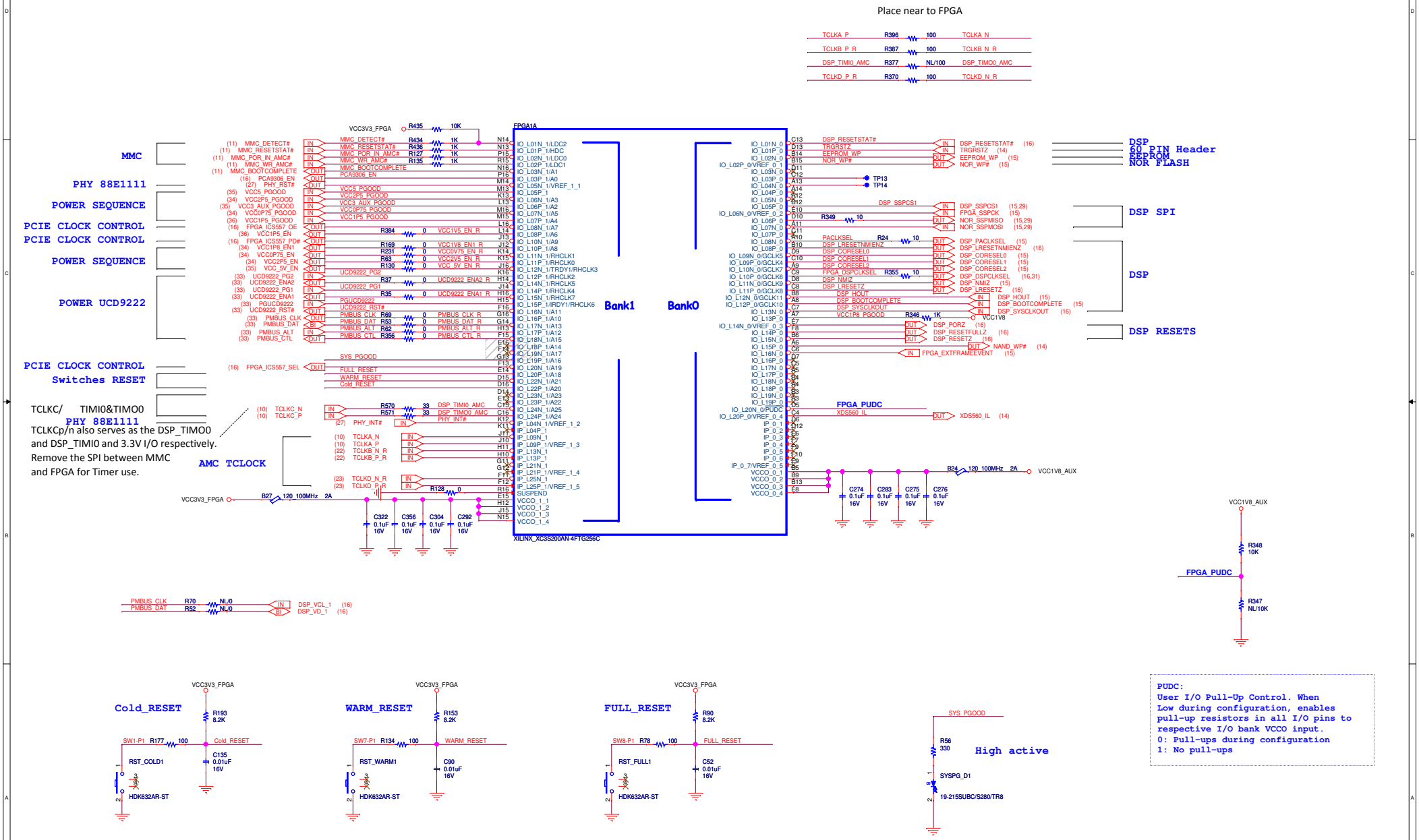
Place near to FPGA
TCLKA_P R396 100 TCLKA_N
TCLKB_P_R R387 100 TCLKB_N_R
DSP_TIMI0_AMC R377 NL/100 DSP_TIMO0_AMC
TCLKD_P_R R370 100 TCLKD_N_R
MMC
PHY 88E1111
POWER SEQUENCE
PCIE CLOCK CONTROL
PCIE CLOCK CONTROL
POWER SEQUENCE
POWER UCD9222
PCIE CLOCK CONTROL
Switches RESET
PHY 88E1111
TCLKC/ TIMI0&TIMO0
TCLKCp/n also serves as the DSP_TIMO0 and DSP_TIMI0 and 3.3V I/O respectively. Remove the SPI between MMC and FPGA for Timer use.
AMC TCLOCK
VCC3V3_FPGA
FPGA1A
Bank1
Bank0
XILINX_XC3S200AN-4FTG256C
DSP
60 PIN Header
EEPROM
NOR FLASH
DSP SPI
DSP
DSP RESETS
FPGA_PUDC
VCC1V8_AUX
PUDC:
User I/O Pull-Up Control. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank VCCO input.
0: Pull-ups during configuration
1: No pull-ups
Cold_RESET
WARM_RESET
FULL_RESET
SYS_PGOOD
High active
Designed for TI by ADVANTECH
Title
FPGA_XC3S200AN_A
Size C
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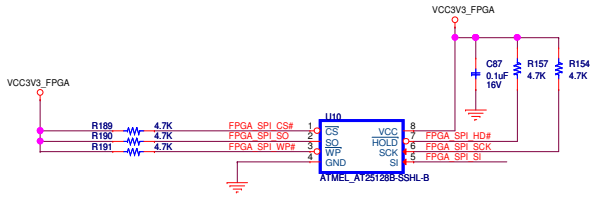
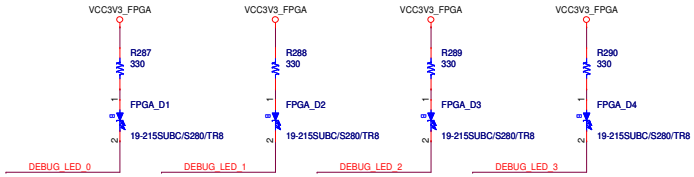
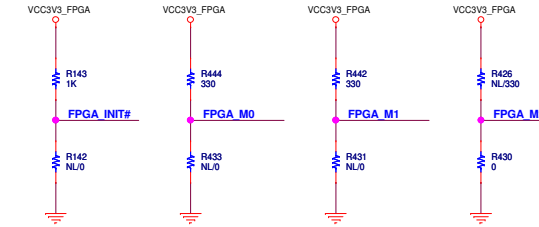
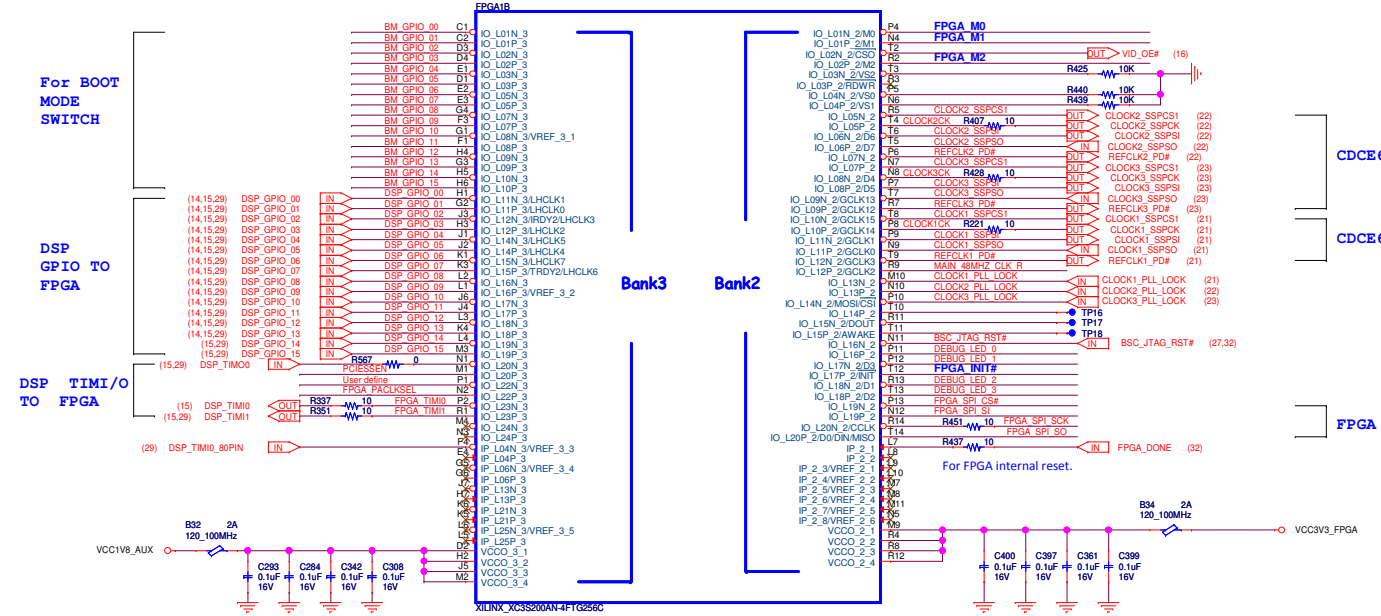


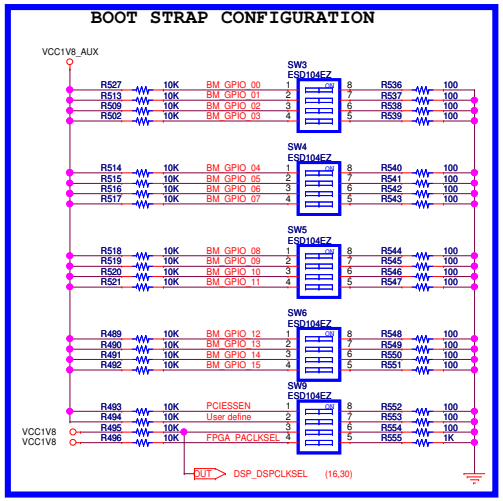
SPI_EEPROM

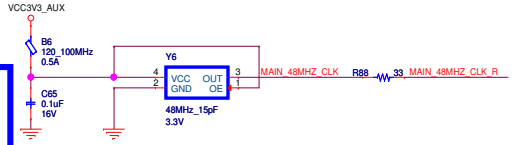


DEBUG_LED









Boot Device

BM_GPIO 3 2 1	BOOT Device	NOTE
0 0 0	EMIF16	
0 0 1	sRIO	
0 1 0	SMGII	PA driven from core clk
0 1 1	SGMII	PA driver from PA clk
1 0 0	PCIe	
1 0 1	I2C	
1 1 0	SPI	
1 1 1	HyperLink	

Device Configuration

BM_GPIO [10:4]	Device Configuration Field	The device configuration fields GPIO[10:4] are used to configure the boot peripheral and, therefore, the bit definitions depend on the boot mode.

PLL Settings

BM_GPIO 13 12 11	INPUT CLK (MHz)	CorePac System PLL Configuration
0 0 0	50.00	
0 0 1	66.67	
0 1 0	80.00	PA driven from core clk
0 1 1	100.00	PA driver from PA clk
1 0 0	156.25	
1 0 1	250.00	
1 1 0	312.50	
1 1 1	122.88	

PCIESSEN

Input	Description
0	Initial state of the power domain and the clock domain for PCIE subsystem is disabled
1	Initial state of the power domain and the clock domain for PCIE subsystem is enabled

PCIe Mode selection(PCIESSMODE[1:0])

BM_GPIO[15:14] INPUT	Description
00b	PCIe in End-point mode
01b	PCIe in Legacy End-point mode(no support for MSI)
10b	PCIe in Legacy Root complex mode

CLK Mode

Clock	Input	Description
SYSCLK / ALTCORECLK	DSP_DSPCLKSELL = 0	SYSCLK used to clock the core PLL.
	DSP_DSPCLKSEL = 1	ALTCORECLK is used to clock the core PLL
PASSCLK	FPGA_PACLKSEL = 0	PASSCLK is not used and should be tied to a static state.
	FPGA_PACLKSEL = 1	PASSCLK is used as a source for the PA_SS PLL. It must be present before the PA_SS PLL is removed from reset and programmed

Boot Configuration

DIP Switch	DSP	Boot Mode	Primary Function	
			Pull Up	Pull Down
BM_GPIO0	GPIO0	LENDIAN	Little Endian	Big Endian
BM_GPIO1	GPIO1	BOOTMODE00	Boot Device	
BM_GPIO2	GPIO2	BOOTMODE01	Boot Device	
BM_GPIO3	GPIO3	BOOTMODE02	Boot Device	
BM_GPIO4	GPIO4	BOOTMODE03	Device Cfg	
BM_GPIO5	GPIO5	BOOTMODE04	Device Cfg	
BM_GPIO6	GPIO6	BOOTMODE05	Device Cfg	
BM_GPIO7	GPIO7	BOOTMODE06	Device Cfg	
BM_GPIO8	GPIO8	BOOTMODE07	Device Cfg	
BM_GPIO9	GPIO9	BOOTMODE08	Device Cfg	
BM_GPIO10	GPIO10	BOOTMODE09	Device Cfg	
BM_GPIO11	GPIO11	BOOTMODE10	PLL Multiplier/I2C	
BM_GPIO12	GPIO12	BOOTMODE11	PLL Multiplier/I2C	
BM_GPIO13	GPIO13	BOOTMODE12	PLL Multiplier/I2C	
BM_GPIO14	GPIO14	PCIESSMODE0	Endpt/RootComplex	
BM_GPIO15	GPIO15	PCIESSMODE1	Endpt/RootComplex	

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TEXAS INSTRUMENTS ADVANTECH

Title	FPGA_XC3S200AN_B	
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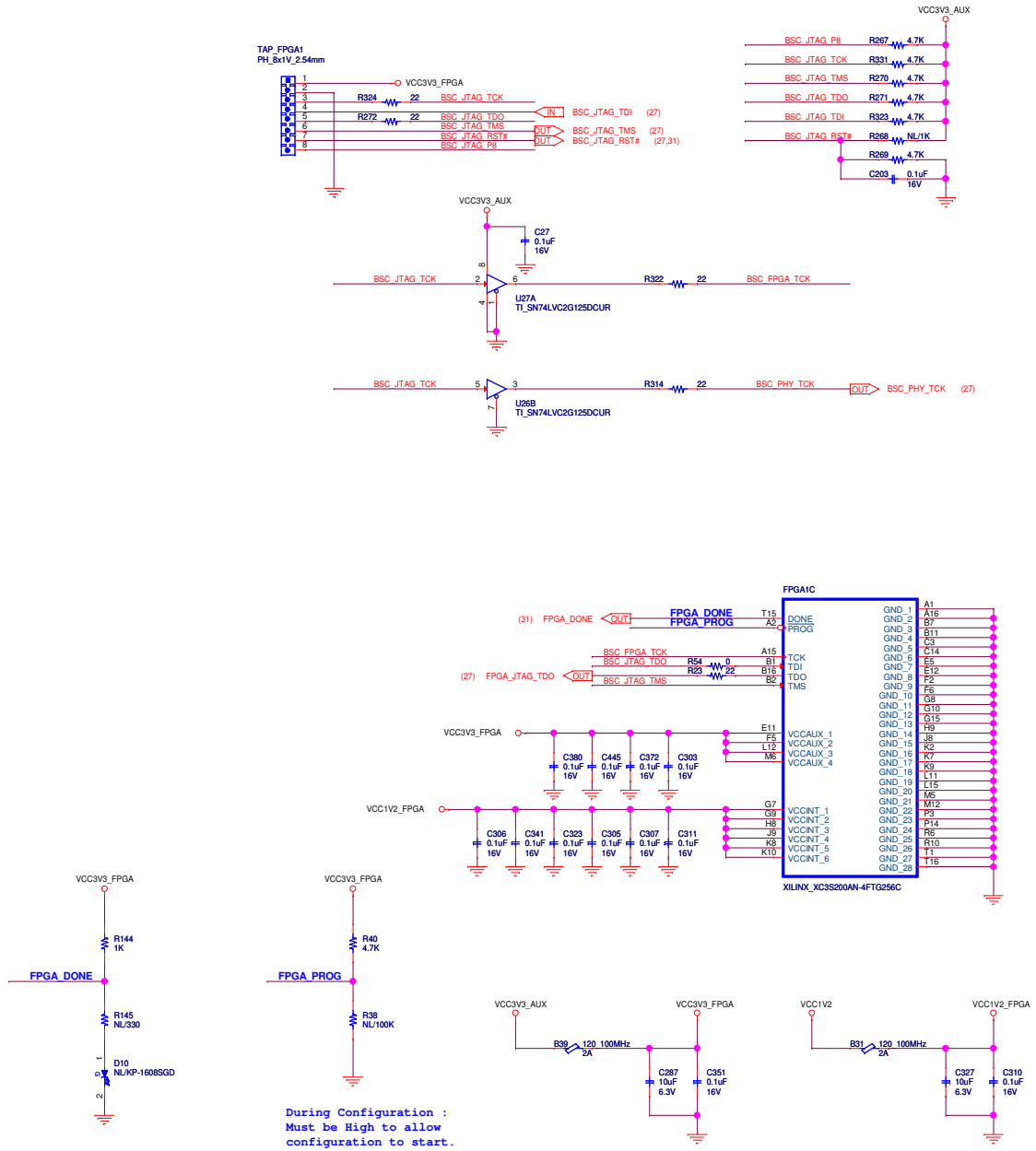

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TEXAS INSTRUMENTS ADVANTECH

Title	FPGA_XC3S200AN_C	
Size: C	Document Number: DSPM-8302E	Rev: A103-1
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CVDD

Place the caps close UCD9222 on the top side.

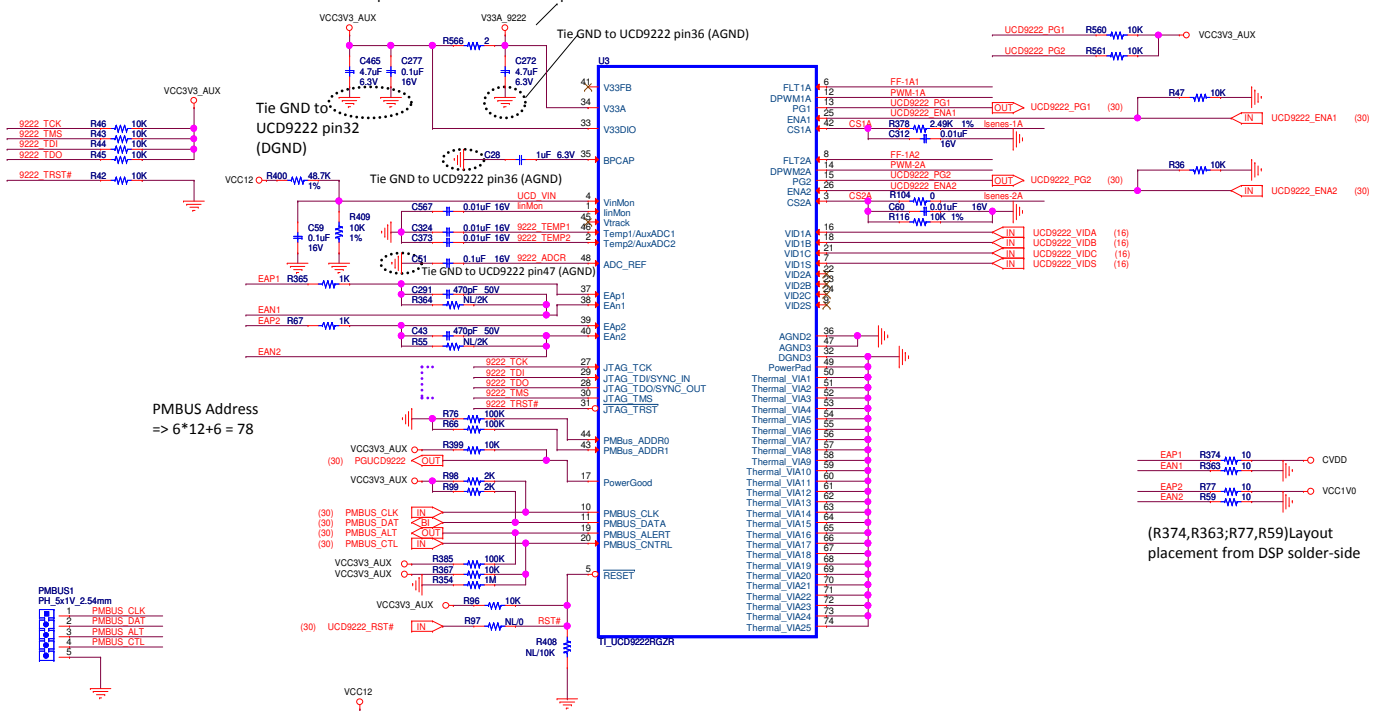
Tie GND to UCD9222 pin36 (AGND)

Tie GND to UCD9222 pin32 (DGND)

Tie GND to UCD9222 pin36 (AGND)

Tie GND to UCD9222 pin47 (AGND)

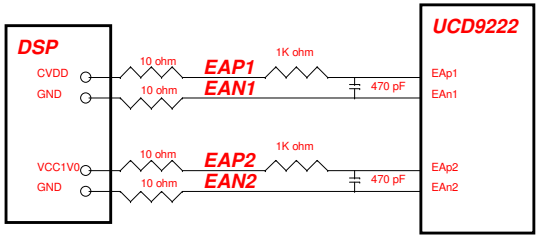
PMBUS Address
=> 6*12+6 = 78



(R374,R363;R77,R59)Layout placement from DSP solder-side

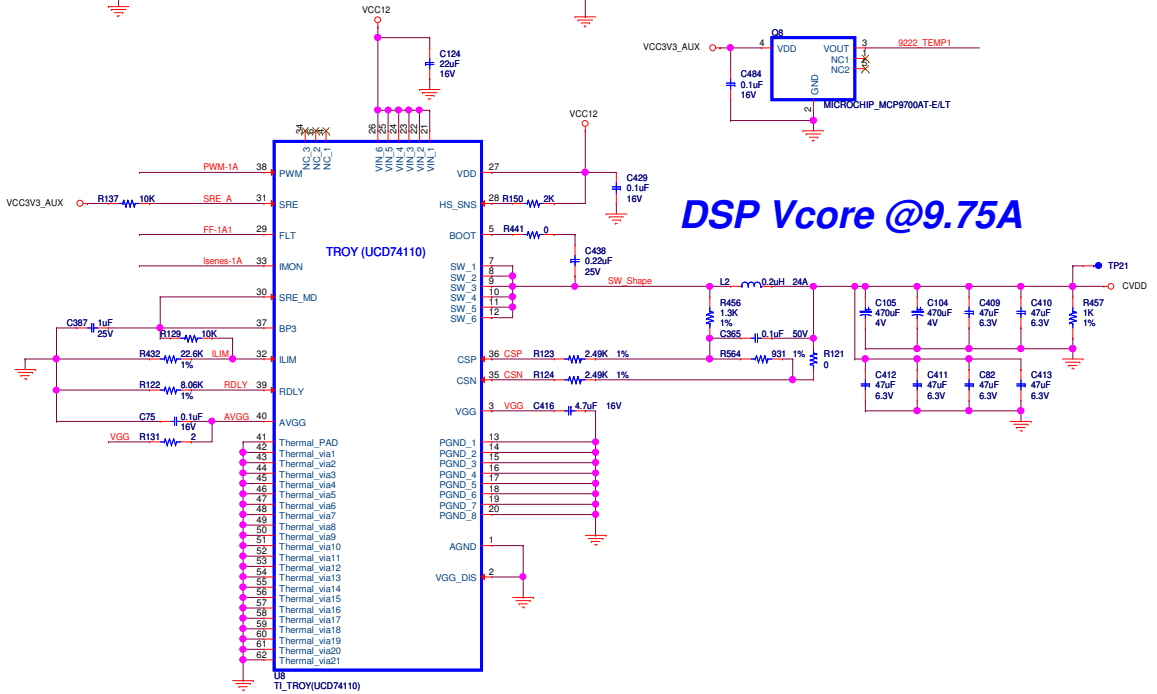
PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--

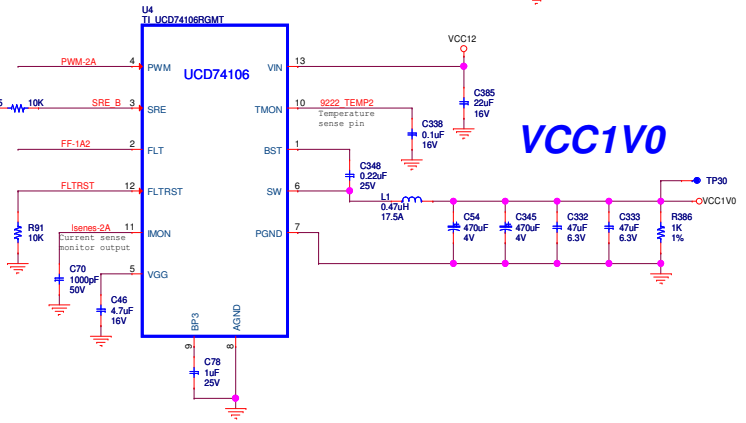


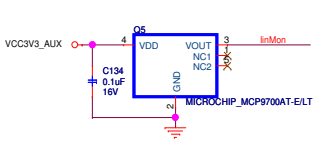
Series resistors on EA nets to be placed at the load for proper voltage feedback.

DSP Vcore @9.75A



VCC1V0





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Title: Power UCD9222

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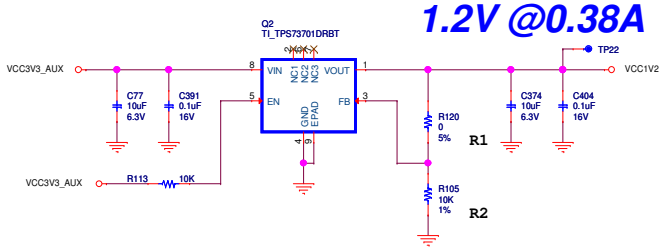
VCC1V2

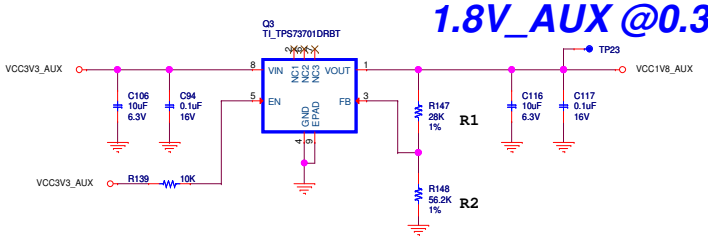
1.2V @0.38A



Vout=(R1+R2)/R2 x 1.204
1.204V = (0+10k)/10k x 1.204

VCC1V8_AUX

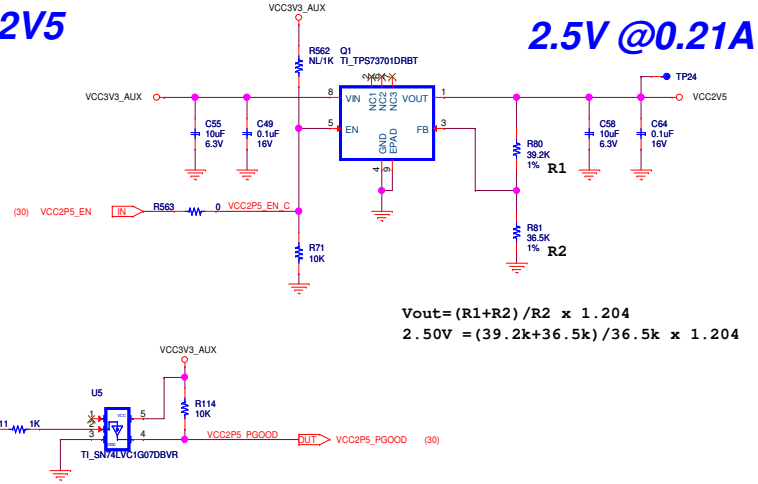
1.8V_AUX @0.3A



Vout=(R1+R2)/R2 x 1.204
1.805V =(28k+56.2k)/56.2k x 1.205

VCC2V5

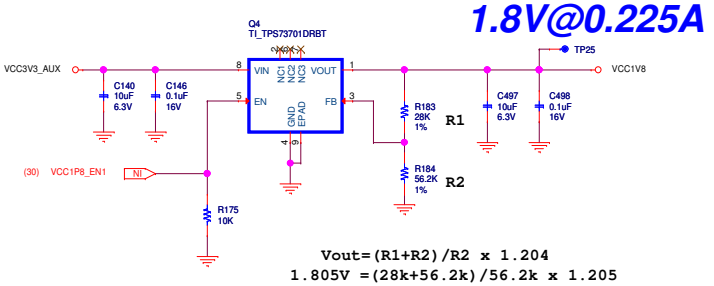
2.5V @0.21A



Vout=(R1+R2)/R2 x 1.204
2.50V =(39.2k+36.5k)/36.5k x 1.204

VCC1V8

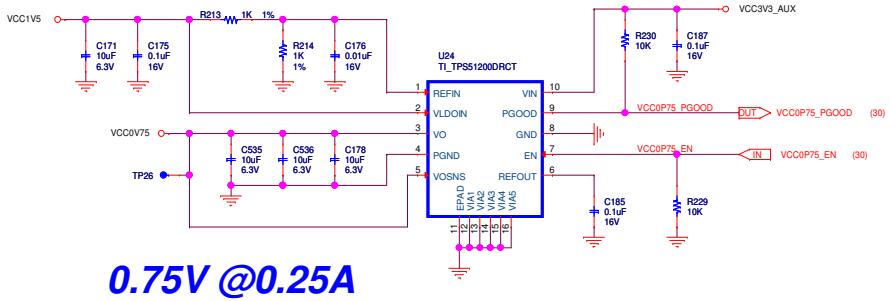
1.8V@0.225A



Vout=(R1+R2)/R2 x 1.204
1.805V =(28k+56.2k)/56.2k x 1.205

VCC0V75

0.75V @0.25A



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Title		
Power_1.2V/1.8V/2.5V/0.75V		
Size: C	Document Number: DSPM-8302E	Rev: A103-1
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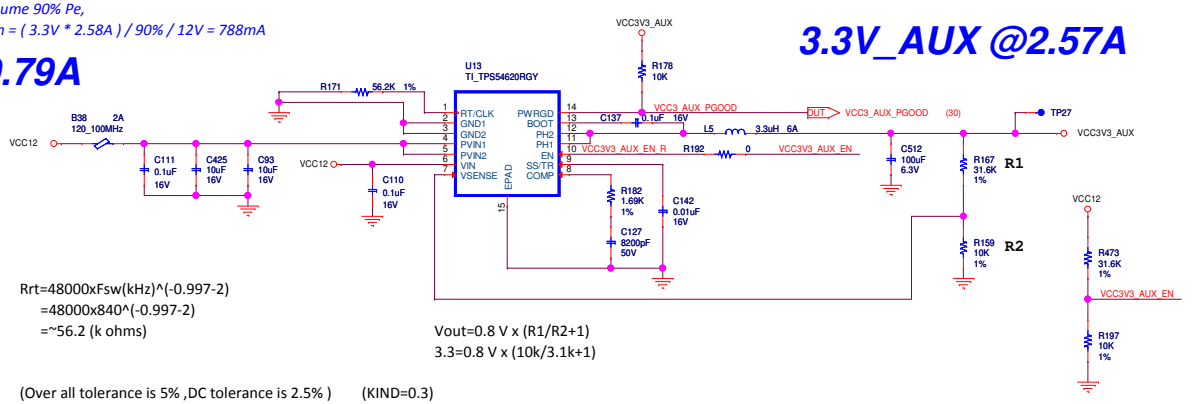
VCC3V3_AUX

Assume 90% Pe,
*Iin = (3.3V * 2.58A) / 90% / 12V = 788mA*

12V@0.79A

3.3V_AUX @2.57A



Rrt=48000xFsw(kHz)^(-0.997-2)
=48000x840^(-0.997-2)
=~56.2 (k ohms)

Vout=0.8 V x (R1/R2+1)
3.3=0.8 V x (10k/3.1k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%)
+++output capacitor Calculation+++
Cout:(2 x delta(Iout))/(Fsw x delta(Vout))
Cout:(2 x 3/(840kHz x 0.0825)
Cout:~87uF

Reference Capacitor:100uF

(KIND=0.3)
+++Inductor Calculation+++
L : (Vin - Vout)/(Iout x Kind) x (Vout/(Vin x Fsw)
L : ((12 - 3.3)/(3A x 0.3) x (3.3 / (12 x 840kHz))
L : 9.67 x 0.33u
L : ~3.2 uH

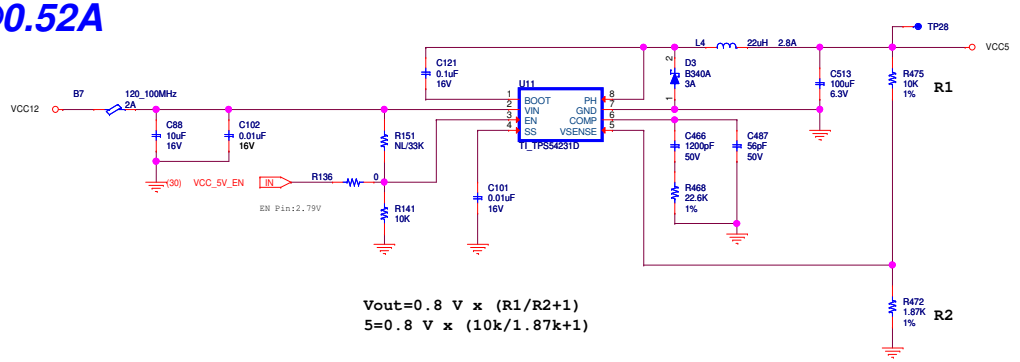
Reference Inductor: 3.3uH

VCC5

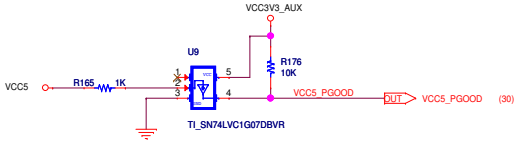
Assume 80% Pe,
*Iin = (5V * 1A) / 80% / 12V = 520mA*

12V@0.52A

5V @1A



Vout=0.8 V x (R1/R2+1)
5=0.8 V x (10k/1.87k+1)



+++output capacitor Calculation+++

$$C_{O\_min} = 1/(2 \times \pi \times R_O \times F_{CO\_max})$$

Cout:1/(2 x 3.14 x 5 x 25K)
Cout:1.3 uf

Reference Capacitor:100uF

+++Inductor Calculation+++ (KIND=0.3)
L : ((Vin(max) - Vout)/Iout x Kind)) x (Vout/(Vin(max) x Fsw))
L : ((12.6 - 5)/1 x Kind) x (5 / (12.7 x 570K))
L : ((7.6/ 0.3) x (5 / (7239K))
L : (25.3) x (0.69M)
L : 17.5uH

Reference Inductor 22uH

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Title		
Power_VCC5 / VCC3V3_AUX		
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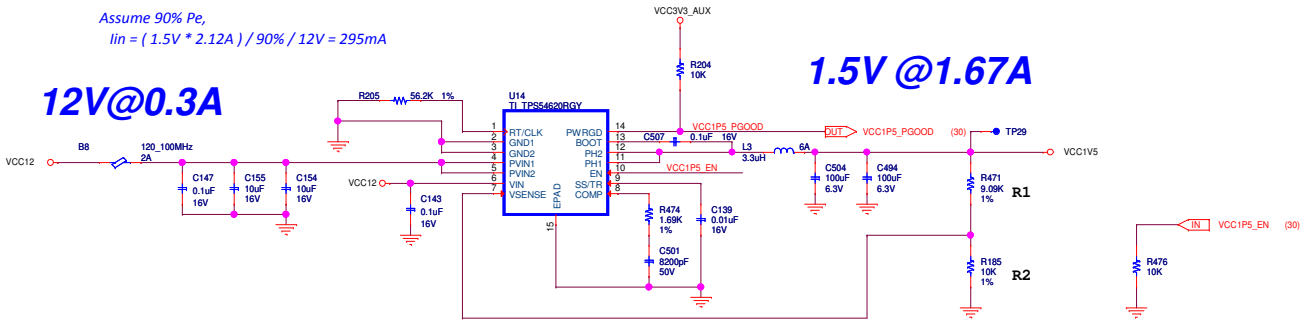
VCC1V5



Vout=0.8 V x (R1/R2+1)

1.52=0.8 V x (9.09k/10k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%) (KIND=0.3)

+++output capacitor Calculation+++
Cout:(2 x delta(Iout))/(Fsw x delta(Vout))
Cout:(2 x 2A)/(840kHz x 0.0375)
Cout: 4/31.5k
Cout:~127uF
Reference Capacitor:200uF

+++Inductor Calculation+++
L : (Vin - Vout)/(Iout x Kind) x Vout/(Vin x Fsw)
L : (12 - 1.5)/(2A x 0.3) x 1.5 / (12 x 840kHz)
L : (17.5) x (0.15u)
L : ~2.63uH
Reference Inductor:3.3uH

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Title: Power VCC1V5		
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