TMS320C6713 to TMS320C6748 Migration Guide

Contents

Introduction

This document provides a summary of the significant differences in the C6713 and C6748 devices, and may be used as a help for planning a migration to the C6748 device.

An engineer who is familiar with C6713 device design and development might face a new challenging task to migrate towards C6748 device. This document will help the users to easily handle those challenges by providing enough guidelines and significant differences.

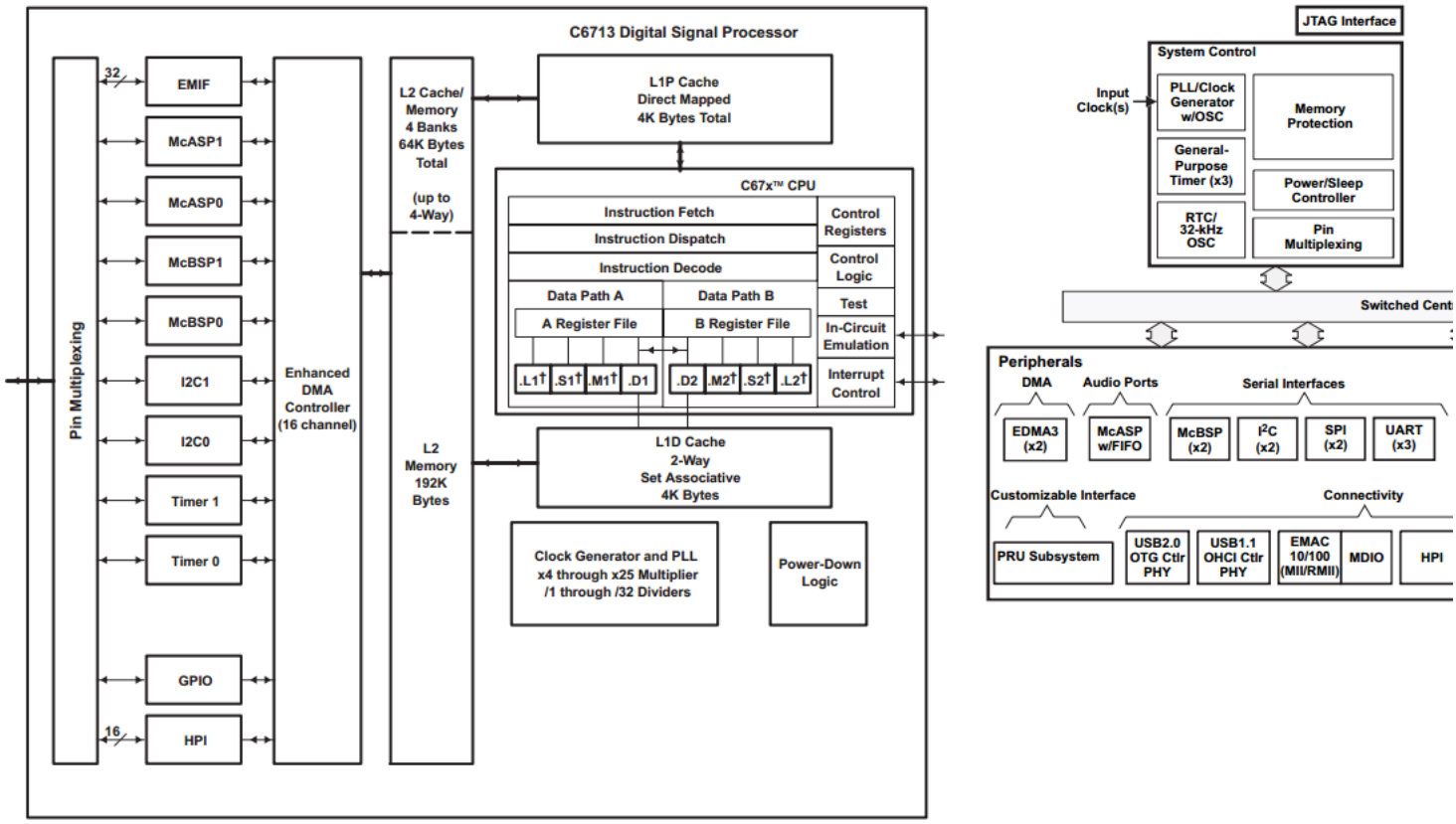
This document also covers key differences between C6713 and C6748 devices, which include the boot modes, power modes, clocking, voltage rails and so on

All of the documentation referenced in this migration guide can also be found on the TI website located in the respective product folders. The device folders are found at the following web pages.

- C6713 (http://focus.ti.com/docs/prod/folders/print/tms320c6713.html)
- C6748 (http://focus.ti.com/docs/prod/folders/print/tms320c6748.html)

Basic Feature comparison

The figures and table below show a comparison of the basic features of the C6713 and C6748 devices. The remaining sections in this document further explains the peripheral feature set, power and clocking comparison of both devices in detail, and also provides references to the appropriate documentation for further information..



C6713 and C6748 Block Diagram

Device Family	C6713	C6748
Device Family	C6713 Fixed/Floating-Point DSP	C6748 Fixed/Floating-Point DSP
Package Options		
Packages	208-Pin PowerPAD™ Plastic (Low-Profile) Quad Flatpack (PYP) 272-Pin BGA Packages (GDP and ZDP)	361-Ball Pb-Free Plastic Ball Grid Array (PBGA) [ZCE Suffix], 0.65-mm Ball Pitch 361-Ball Pb-Free PBGA [ZWT Suffix], 0.80-mm Ball Pitch
Co-processors and Subsystems		
DSP Processor	Fixed/Floating-Point VLIW Processor up to 225 MHz; 4KB Instruction and Data Caches	Fixed/Floating-Point VLIW Processor up to 456 MHz; 32KB Instruction and Data Caches
EDMA	16 Channel (V2.0)	Two 32 Channel (V3.0)
PRUSS	No	Two 150 MHz PRU Cores
Memory Interfaces:		
Memory Subsystem	32/16 Bit EMIF (100 MHz) supports SRAM, EPROM, Flash, SBSRAM, and SDRAM	16 Bit DDR2/mDDR Controller; 16 Bit EMIFA (Async Mode - 148MHz, SDRAM Mode - 100MHz)
Security		
Secure Boot	No	Yes
Memory Protection	No	Yes
Video Interfaces		
LCD Controller	No	Yes
VPIF	No	Yes
Peripherals		
USB	No	USB 2.0 OTG, USB 1.1
eMAC	No	10/100 Mbps
McASP	2	1
McBSP	2	2
UART	No	3
SPI	No	2

I2C	2	2
GPIO	1 Bank	9 Banks
eCAP	No	3
eHRPWM	No	2
HPI	16 Bit	16 Bit
uPP	No	1
SATA Controller	No	1
Removable Media		
MMC/SD/SDIO	No	2
Power, Reset, and Clock Management		
RTC	No	Yes
Test Interfaces		
JTAG	Yes	Yes
Misc		
GP Timer	2 32 Bit	4 64 Bit
Watchdog Timer	No	1 64 Bit

Hardware Migration

CPU and Memory

DSP Processor

C6713 is based on fixed/floating-point VLIW DSP processor, while C6748 is based on fixed/floating-point VLIW DSP processor. The table below shows a comparison between these two devices.

C6713 and C6748 DSP Processor Comparison

DSP Processor	C6713	C6748
DSP Processor	C67x/C62x core Fixed/Floating-Point VLIW	C674x (aka C67x+/C64x+) core Fixed/Floating-Point VLIW
CVdd Supported	1.2 V	1.0/1.1/1.2/1.3 V
Operating Frequencies	225/200/167 MHz (@1.2 V)	456/375/200/100 MHz (@1.3/1.2/1.1/1.0 V)
L1 Instruction Cache	4 Kbytes	32 Kbytes
L1 Data Cache	4 Kbytes	32 Kbytes
L2 Cache	256 Kbytes	256 Kbytes
RAM Size	N/A	128 Kbytes

Power and Sleep Controller

C6713 does not contain a dedicated power and sleep controller.

C6748 integrates power and sleep controller that manages transitions of system power on/off, clock on/off, resets (device level and module level).

EDMA Controller

C6713 EDMA supports up to 16 EDMA channels. Four of the sixteen channels (channels 8–11) are reserved for EDMA chaining, leaving 12 EDMA channels available to service peripheral devices.

C6748 contains two EDMA3 controllers with 32 independent channels per controller. It also supports 16 Quick DMA channels.

Programmable Real-Time Unit SubSystem (PRUSS)

C6713 does not have programmable real-time unit subsystem.

The PRUSS supported on C6748 run at 150MHz and has the following features.

- Two Independent Programmable Real-Time Unit (PRU) Cores
- 32-Bit load-store RISC architecture
- 4KB of instruction RAM per core
- 512 Bytes of data RAM per core
- PRUSS can be disabled via software to save power
- Register 30 of each PRU is exported from the subsystem in addition to the normal R31 output of the PRU cores

- A Switched Central Resource (SCR) for connecting the various internal and external masters to the resources inside the PRUSS

Additional On-Chip Memory

C6713 does not have on-chip memory.

C6748 has 128KB RAM additional on-chip memory.

External Memory Interfaces

C6713 supports 32-bit EMIF for interfacing with external memories.

The EMIF is used to interface with asynchronous and SDRAM external memories. Up to 4 CS signals are supported. The controller supports the following devices:

- SRAM
- EPROM
- Flash
- SBSRAM
- SDRAM

C6748 supports a memory subsystem that includes the DDR2/mDDR controller and EMIFA for interfacing with external memories.

The DDR2/mDDR controller provides interface for:

- 16-Bit DDR2 SDRAM with 256-MB address space
- 16-Bit mDDR SDRAM with 256-MB address space

CAS latencies:

- DDR2 => 2, 3, 4 and 5
- mDDR => 2 and 3

Internal banks:

- DDR2 => 1, 2, 4, and 8
- mDDR => 1, 2, and 4

The EMIFA provides a 16-bit asynchronous interface to NAND, NOR and SRAM memories. The controller supports up to four asynchronous CS signals. The device supports 16-bit SDRAM in addition to the asynchronous memories. The following CAS latencies and internal banks are supported:

CAS latencies:

- SDRAM => 2 and 3

Internal banks:

- SDRAM => 1, 2 and 4

Power, Reset, and Clock Management

Voltage Rails

The following table compares the power supplies for C6713 and C6748:

C6713 Voltage Rails

Signal	Description	Value
CVDD	Core Supply Voltage	1.2V
DVDD	I/O Supply Voltage	3.3V

C6748 Voltage Rails

SIGNAL	DESCRIPTION	VALUE
CVDD	Core Supply Voltage	1.3V to 1.0V (Variable)
RVDD	Internal RAM Supply	1.2V or 1.3V
RTC_CVDD	RTC Core Logic Supply	1.2V
PLL0_VDDA	PLL0 Supply Voltage	1.2V
PLL1_VDDA	PLL1 Supply Voltage	1.2V
DVDD18	I/O Supply	1.8V
DVDD3318_A	I/O Supply Group A (1.8V Operation)	1.8V
DVDD3318_B	I/O Supply Group B (1.8V Operation)	1.8V
DVDD3318_C	I/O Supply Group C (1.8V Operation)	1.8V

DVDD3318_A	I/O Supply Group A (3.3V Operation)	3.3V
DVDD3318_B	I/O Supply Group B (3.3V Operation)	3.3V
DVDD3318_C	I/O Supply Group C (3.3V Operation)	3.3V
USB0_VDDA33	USB0 PHY Supply	3.3V
USB0_VDDA18	USB0 PHY Supply	1.8V
USB0_VDDA12	USB0 PHY LDO Output	1.2V
USB_CVDD	USB0 Core Logic Supply	1.2V
USB1_VDDA33	USB1 PHY Supply	3.3V
USB1_VDDA18	USB1 PHY Supply	1.8V
SATA_VDD	SATA PHY Logic Supply	1.2V
DDR_DVDD18	DDR2 PHY Supply	1.8V
DDR_VREF	DDR2/mDDR reference voltage	0.5* DDR_DVDD18

Power Modes

The following table compares the power modes for C6713 and C6748:

C6713 Power Modes

Power Mode	Device Power Excluding IO (mW)	Description
PD1	476	CPU halted
PD2	52	Output clock from PLL is halted
PD3	50	Input clock to the PLL stops generating clocks
Typical/Active*	671 - 1.2V/200MHz 809 - 1.26V/225MHz	The device power values for typical/active mode assume the DSP is running at typical activity and EMIF, EDMA, McBSP0, McBSP1 are enabled and all other modules are not used.

C6748 Power Modes

Power Mode	Total Device Power (mW)	Description
RTC-Only	0.02	Only RTC voltage domain is alive.
Static/DeepSleep	10.93	CPU halted. RTC and baseline power consumption only.
Standby	36.25	PLL0 is powered down/disabled and the system is operating in bypass mode with the 24MHz CLKIN as the system clock. The DSP is in the wait for interrupt sleep mode and all peripherals are disabled.
Typical/Active	660.46 - 1.3V/456MHz 426.93 - 1.2V/300MHz	All Features.

** Note, the Power and Sleep Controller (PSC) is used to enable and disable any peripheral. This prevents consumption of any unnecessary power.*

Internal Clocks

The following table compares the clock inputs for C6713 and C6748:

C6713 Clock Inputs

CLOCK NAME	SOURCE	VALUE
Ref CLK for PLL	External oscillator	12 to 100 MHz

C6748 Clock Inputs

CLOCK NAME	SOURCE	VALUE
Ref CLK for PLL	External crystal External oscillator	12 to 30 MHz 12 to 50 MHz
Ref CLK for RTC	External 32.768-kHz crystal or external clock source of the same frequency	32768 Hz Precise

PLLs

C6713 has a phase-locked loop controller (PLLC), driven by the reference clock for PLL:

- PLL - for DSP Core, EMIF, EDMA, McASP0, McASP1, McBSP0, McBSP1, I2C0, I2C1, Timer0, Timer1, GPIO, HPI, Observation clock.

C6748 has the following phase-locked loop controllers (PLLCs), driven by the reference clock for PLLs:

- PLL0 - DSP Core, Shared RAM, UART0, EDMA, SPI0, MMC/SD0/1, VPIF, LCDC, SATA, uPP, DDR2/mDDR (Bus Ports), USB2.0, HPI, PRU, EMIFA, GPIO, PLLC, PSC, I2C0/1, EMAC/MDIO, USB1.1, Timer64P0/P1, RTC, McASP0 Serial Clock, Observation Clock.
- PLL1 - DDR/mDDR PHY, ECAPs, UART1/2, Timer64P2,P3, eHRPWMs, McBSPs, McASP0, SPI1, PLL0 Input Reference Clock.

Power Management Feature Comparison

HW Provisions for Power Optimization/ Control	C6713	C6748
Individually Switchable Power Domains	Not supported	Individual Power Domain ON/OFF for the following: Controls the sleep state for DSP L1 and L2 Memories and 128K on-chip RAM.
Dynamically gating OFF of Clocks to one/more of groups of modules (clock domains) when inactive to conserve power	Not Supported	Supported
Operating Voltage-Frequencies	1.26/1.2V 225/200/167 MHz	1.0/1.1/1.2/1.3V 456/375/200/100 MHz
Memory Retention	Not supported	Supported
Dynamic Voltage and Frequency Scaling	Not supported	Supported
Low Power Deep-Sleep State w/ Auto Wakeup	Not Supported	Supported*
RTC Only Cold State	Not Supported	Supported
Splitting of Primary Voltage Supply Rails	CVDD, DVDD	CVDD, RVDD, DVDD, RTC_CVDD

* Refer C6748 Power Module (http://processors.wiki.ti.com/index.php/Power_Module_for_C6748_and_OMAP-L138#Sleep_Modes)

Boot Modes

The available boot modes for C6713 and C6748 are shown in the table below.

Available Boot modes on C6713 and C6748

C6713	C6748	Boot Type	Description
N	Y	NOR	This mode allows booting over the asynchronous interface. DSP pulls data from a memory device such as a NOR flash. For C6748, NOR Flash should be connected to the EMIFA peripheral on EMA_CS[2].
N	Y	NAND	This mode starts downloading code from an NAND memory. For C6748, NAND flash should be connected to the EMIFA peripheral on EMA_CS[3]. The ALE and CLE pins of the NAND device should be connected to the EMA_A[1] and EMA_A[2] pins of the EMIFA peripheral, respectively.
N	Y	SPI	This mode starts downloading code from an SPI EEPROM or SPI Flash or External Host (Slave mode). For C6748, the external SPI device should be connected to the SPI chip select 0 signal (SPI0_SCS[0] or SPI1_SCS[0]).
N	Y	UART	In this mode, the UART sends a BOOTME request to the UART peripheral and waits for a response along with code from a host processor. C6748 must be booted using a baud rate of 115200. C6748 can boot from UART0-2.
N	Y	MMCSD	This mode starts booting code from an MMC/SD Controller. For C6748, the MMC/SD cards should be connected to MMC/SD0.
Y	Y	HPI	This mode allows for booting code through the HPI port.
N	Y	I2C	This mode starts downloading code from an I2C. For C6748, either I2C0 or I2C1 can be used.

Y	N	External ROM	This mode starts downloading code from an external 8, 16, 32-bit ROM memory. For C6713, ROM memory should be connected to the EMIF peripheral on CE[1].

Multimedia Hardware Components

LCD

The C6748 LCD controller consists of two independent controllers, the Raster Controller and the LCD Interface Display Driver (LIDD) controller. The maximum resolution for the LCD controller is 1024 x 1024 pixels. The maximum frame rate is determined by the image size in combination with the pixel clock rate.

The LCD controller does not exist on C6713.

VPIF

The C6748 Video Port Interface (VPIF) allows the capture and display of digital video streams. Features include:

- Up to 2 Video Capture Channels
- Two 8-bit Standard-Definition (SD) Video
- Single 16-bit High-Definition (HD) Video
- Single Raw Video (8-/10-/12-bit)
- Up to 2 Video Display Channels

The VPIF module does not exist on C6713.

Communication Interfaces

MMC/SD

The C6748 device support different versions of industry standards (shown below). It supports FIFO size of 512-bit.

Feature Comparison

Feature	C6748
Spec Compliance	MMC v4.0 SD Physical Layer v1.1 SDIO v2.0
Data Width *	8-bit (MMCSD0/1)
Max Clock Rate	52MHz

The MMCSD controller does not exist on C6713.

** Note the supported data width is subject to pinmux constraints.*

USB

The C6748 supports one USB 1.1 OHCI (Host) With Integrated PHY (USB1) and one USB 2.0 OTG Port With Integrated PHY (USB0). The USB 2.0 OTG peripheral supports 4KB endpoint FIFO RAM.

The C6713 does not have any of the USB controllers.

I2C

Both C6748 and C6713 support two I2C ports.

Both the devices are compatible with I2C specification revision 2.1, supports fast mode up to 400kbps, master and slave functionality.

UART

C6748 has 3 UART ports, all supporting modem control signals. None of the UART ports support IrDA. C6748 UARTs support 16-byte storage space for both the transmitter and receiver FIFOs.

The UART module does not exist in C6713.

McBSP/McASP

C6748 has 2 McBSP ports and 1 McASP ports. McASP0 supports up to 16 McASP serializers.
C6713 has 2 McBSP ports and 2 McASP ports. McASP0/1 supports up to 8 McASP serializers.

SPI

The C6748 support two (2) SPI ports. It supports 1 CS on each port and 2-16 bit word length. The C6713 supports SPI interface with the use of McBSP module.

Ethernet

C6748 supports one Ethernet MAC with a maximum data rate of 100 Mbps. The C6748 MAC interfaces include MII/RMII and MDIO.

The Ethernet controller does not exist in C6713.

eCAP/ eHRPWM

The C6748 supports both eCAP and eHRPWM peripherals as separate modules. The eCAP module has 4 event time-stamp registers and captures single shot or continuous mode. The eHRPWM has dedicated 16-Bit time-base counter with period and frequency control.

C6713 does not support either eCAP or eHRPWM.

HPI

Both C6748 and C6713 devices has HPI module with 16-bit interface.

uPP

The C6748 supports uPP interface with programmable data width per channel (from 8 to 16 bits inclusive). The uPP module does not exist on C6713.

SATA controller

The C6748 supports Serial ATA 1.5 Gbps (Gen 1i) and 3 Gbps (Gen 2i) line speeds. The SATA controller does not exist on C6713.

Timers

GP Timer

C6748 supports four (4) 64-bit GP timers. Each can be configured as two (2) 32-Bit timers.

C6713 supports two (2) 32-bit GP timers

WD Timer

C6748 supports 1 WD timer that can be configured as one 64-bit or two 32-bit WD timers.

C6713 does not provide WD timer.

RTC

C6748 support 1 RTC with 32 KHz oscillator and separate power rail. It provides Binary-Coded-Decimal (BCD) representation of time, calendar and alarm.

RTC does not exist on C6713.

Misc

GPIOs

C6748 supports 9 banks of GPIO signals. Each bank supports 16 GPIOs. Every GPIO pin may be configured to generate an interrupt request on detection of rising and/or falling edges on the pin.

C6713 supports 1 bank of GPIO signals. The GPIO bank supports 16 GPIOs.

Additional Interfaces in C6748

The following are additional interfaces in the C6748 device that do not exist in C6713. Any details about these interfaces can be found in the Technical Reference Manual for C6748.

- LCD Controller
- VPIF
- USB
- eMAC
- UART
- eCAP/eHRPWM
- uPP
- SATA
- MMC/SD/SDIO

The C6713 has older version (V2.0) of EDMA whereas C6748 has newer version (V3.0).

* Refer EDMA V2.0 to EDMA V3.0 Migration (http://www.ti.com/lit/an/spraap4a/spraap4a.pdf)

Pin and package

The C6713 and the C6748 devices are offered in two different package types. The physical dimensions and pin out of the packages are also different. The table below lists the difference between the C6713 and the C6748 devices.Please refer the individual device datasheet for detailed pin outs, terminal functions and BGA ball map for the package type mentioned below.

Pin and Package Comparison

Device	Size (mm)	Pitch (mm)	No. of Pins	Package Designator
C6713	30.00 x 30.00 mm	0.5 mm	208	PYP
	27.00 x 27.00 mm	1.27 mm	272	GDP
C6748	13.00 x 13.00 mm	0.65 mm	361	ZCE
	16.00 x 16.00 mm	0.80 mm	361	ZWT

{{

1. switchcategory:MultiCore=
   - For technical support on MultiCore devices, please post your questions in the C6000 MultiCore Forum
   - For questions related to the BIOS MultiCore SDK (MCSDK), please use the BIOS Forum

   Please post only comments related to the article **TMS320C6713 to TMS320C6748 Migration Guide** here.

Keystone=
- For technical support on MultiCore devices, please post your questions in the C6000 MultiCore Forum
- For questions related to the BIOS MultiCore SDK (MCSDK), please use the BIOS Forum

Please post only comments related to the article **TMS320C6713 to TMS320C6748 Migration Guide** here.

C2000=*For technical support on the C2000 please post your questions on The C2000 Forum. Please post only comments about the article* ***TMS320C6713 to TMS320C6748 Migration Guide*** *here.*

DaVinci=*For technical support on DaVincoplease post your questions on The DaVinci Forum. Please post only comments about the article* ***TMS320C6713 to TMS320C6748 Migration Guide*** *here.*

MSP430=*For technical support on MSP430 please post your questions on The MSP430 Forum. Please post only comments about the article* ***TMS320C6713 to TMS320C6748 Migration Guide*** *here.*

OMAP35x=*For technical support on OMAP please post your questions on The OMAP Forum. Please post only comments about the article* ***TMS320C6713 to TMS320C6748 Migration Guide*** *here.*

OMAPL1=*For technical support on OMAP please post your questions on The OMAP Forum. Please post only comments about the article* ***TMS320C6713 to TMS320C6748 Migration Guide*** *here.*

MAVRK=*For technical support on MAVRK please post your questions on The MAVRK Toolbox Forum. Please post only comments about the article* ***TMS320C6713 to TMS320C6748 Migration Guide*** *here.*

For te pleas quest http:// Pleas comn article ***to TM Migra*** *here.*

}}

Links

Amplifiers & Linear
Audio
Broadband RF/IF & Digital Radio
Clocks & Timers
Data Converters
DLP & MEMS
High-Reliability
Interface
Logic
Power Management
Processors
- ARM Processors
- Digital Signal Processors (DSP)
- Microcontrollers (MCU)
- OMAP Applications Processors

Switches & Multiplexers
Temperature Sensors & Control ICs
Wireless Connectivity