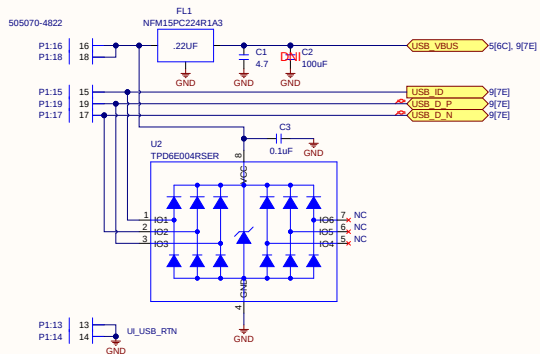
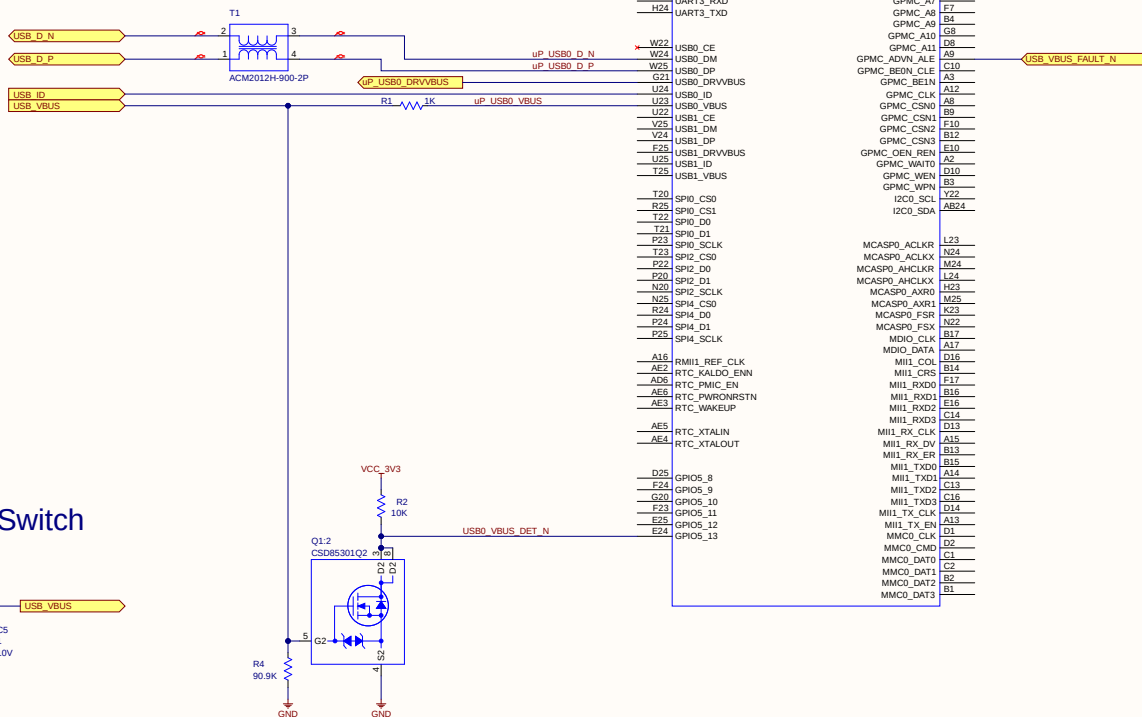
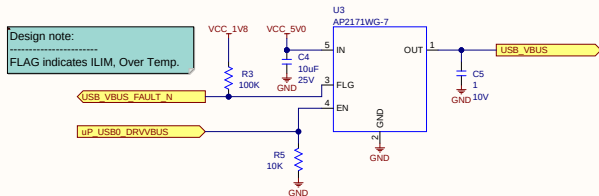


CONNECTOR INTERFACING WITH USB

USB



5V USB VBUS Load Switch



U1-2		PROCESSOR	
AM34739B2DNA100			
G24	ECAP0_IN_PWM0_OUT	GPMC_A00	B5
N23	EMUI0	GPMC_A01	B6
T24	EMUI1	GPMC_A02	B7
G25	EXTINTN	GPMC_A03	A6
		GPMC_A04	A7
Y23	PWNRSTN	GPMC_A05	C8
N25	TRSTRT	GPMC_A06	B8
A25	UART0_RX	GPMC_A07	B10
T25	TDI	GPMC_A08	A9
A24	TDO	GPMC_A09	F11
Y24	TMS	GPMC_A10	D11
		GPMC_A11	E11
		GPMC_A12	C11
		GPMC_A13	C11
		GPMC_A14	A11
		GPMC_A15	A11
L25	UART0_CTSN	GPMC_A0	C3
J25	UART0_RFSN	GPMC_A1	A3
K25	UART0_RXD	GPMC_A2	C5
J24	UART0_TXD	GPMC_A3	A4
K24	UART1_CTSN	GPMC_A4	F7
L27	UART1_RFSN	GPMC_A5	E7
K21	UART1_RXD	GPMC_A6	D7
L21	UART1_TXD	GPMC_A7	F6
K21	UART1_CTSN	GPMC_A8	E7
K24	UART1_RFSN	GPMC_A9	B4
H25	UART3_RXD	GPMC_A7	F6
H24	UART3_TXD	GPMC_A8	E7
		GPMC_A9	B4
		GPMC_A10	G8
		GPMC_A11	A3
		GPMC_ADV0_ALE	C10
		GPMC_BE0N_CLE	A9
		GPMC_BE1N_A3	A12
		GPMC_CLE	A8
		GPMC_CS0N	F10
		GPMC_CS1N	B12
		GPMC_CS2N	E10
		GPMC_CS3N	F10
		GPMC_DEN_REN	A2
		GPMC_WAIT0	D10
		GPMC_WEN	B3
		GPMC_WPEN	Y22
		IC20_SCL	ZB24
		IC20_SDA	AB24
T20	SP0_C0		
R25	SP0_CS1		
T22	SP0_D0		
T21	SP0_SC1K		
T23	SP0_C0	MCASP0_ACLKR	L23
T20	SP0_D0	MCASP0_ACLKX	N24
T21	SP0_SC1K	MCASP0_AHCLKR	M24
N20	SP0_C0	MCASP0_AHCLKX	L24
N20	SP0_SC1K	MCASP0_AXR0	H23
T24	SP0_D0	MCASP0_AXR1	M23
T24	SP0_D0	MCASP0_FSR	K21
T24	SP0_SC1K	MCASP0_F0X	N12
P25	SP0_C0	MDIO_CLK	B87
		MDIO_DATA	D16
A6	RMI0_REF_CLK	MI01_COL	B14
A6	RTC_KALDO_ENN	MI01_CRS	A17
A6	RTC_PMC_EN	MI01_RXD0	F17
A6	RTC_PWNRSTN	MI01_RXD1	B15
A6	RTC_WAKEUP	MI01_RXD2	E16
		MI01_RXD3	D13
A6	RTC_XTALIN	MI01_RX_CLK	C14
A6	RTC_XTALOUT	MI01_RX_DK	A15
		MI01_TXD0	B15
		MI01_TXD1	C14
		MI01_TXD2	A16
		MI01_TXD3	C14
		MI01_TX_CLK	D14
		MI01_TX_EN	A13
		MMIO_CLK	C1
		MMIO_CMD	D2
		MMIO_DAT0	C2
		MMIO_DAT1	B2
		MMIO_DAT2	B2
		MMIO_DAT3	B1

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY.

#NAME?