Snip of Note 1 below:

Table 7-18. VOUT3 IOSETs (continued)

SIGNALS	IOSET1		IOSET2 (1)		IOSET3 (1)	
	BALL	MUX	BALL	MUX	BALL	MUX
vout3_d1	M2	3	AD2	4	AG6	3
vout3_d0	M6	3	AD3	4	AH4	3
vout3_de	N9	3	AD9	4		
vout3_vsync	R4	3	AF8	4	AF8	4
vout3_clk	P1	3	AF9	4	AF9	4
vout3_hsync	N7	3	AE9	4	AE9	4
vout3_fld	P9	3	AG8	4		

(1) The VOUT3 interface when multiplexed onto balls mapped to the VDDSHV6 supply rail is restricted to operating in 1.8V mode only (i.e., VDDSHV6 must be supplied with 1.8V). 3.3V mode is not supported. This must be considered in the pin mux programming and VDDSHVx supply connections.

Currently our VOUT3 pinmux is ball-mapped as shown below (or next page). Notice that all balls are set to IOSET1. Can TI confirm whether or not our VOUT3 setup is capable of operating in 3.3V mode. We believe we are ok, but would like for TI to confirm.

MyVOUT2

Name:	MyVOUT1
Use Case:	All pins of peripheral
Use Peripheral:	VOUT3
Preferred Voltage:	3.3
IO Set:	VOUT3_IOSet_1 View IO Sets
Mode:	Rising-edge Clock Reference

VOUT Signals	VOUT Pins
clk(vout3_clk)	Any(P1)
d0(vout3_d0)	Any(M6)
d1(vout3_d1)	Any(M2)
d2(vout3_d2)	Any(L5)
d3(vout3_d3)	Any(M1)
d4(vout3_d4)	Any(L6)
d5(vout3_d5)	Any(L4)
d6(vout3_d6)	Any(L3)
d7(vout3_d7)	Any(L2)
d8(vout3_d8)	Any(L1)
d9(vout3_d9)	Any(K2)
d10(vout3_d10)	Any(J1)
d11(vout3_d11)	Any(J2)
d12(vout3_d12)	Any(H1)
d13(vout3_d13)	Any(J3)
d14(vout3_d14)	Any(H2)
d15(vout3_d15)	Any(H3)
d16(vout3_d16)	Any(R6)
d17(vout3_d17)	Any(T9)
d18(vout3_d18)	Any(T6)
d19(vout3_d19)	Any(T7)
d20(vout3_d20)	Any(P6)
d21(vout3_d21)	Any(R9)
d22(vout3_d22)	Any(R5)
d23(vout3_d23)	Any(P5)
de(vout3_de)	Any(N9)
fld(vout3_fld)	Any(P9)
hsync(vout3_hsync)	Any(N7)
vsync(vout3_vsync)	Any(R4)