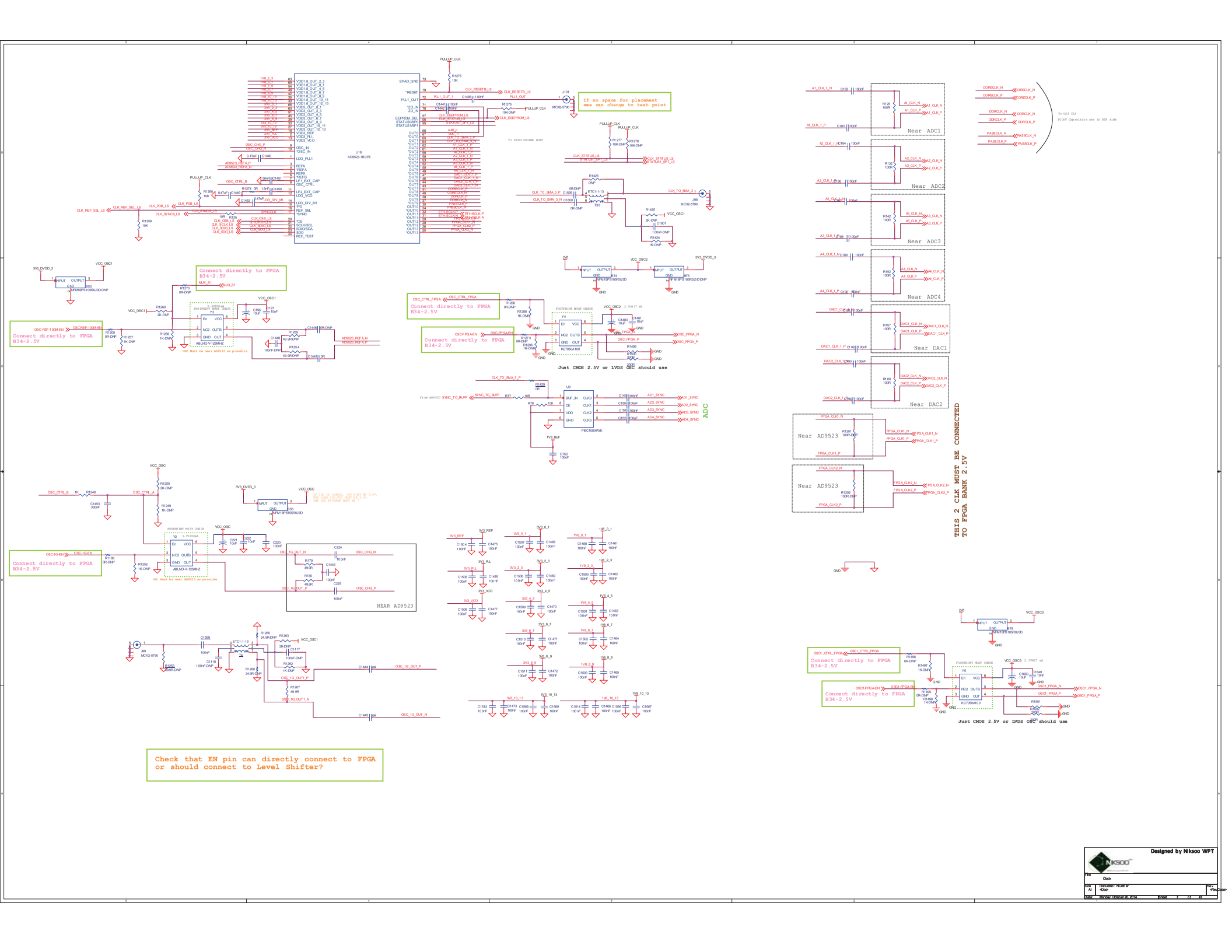
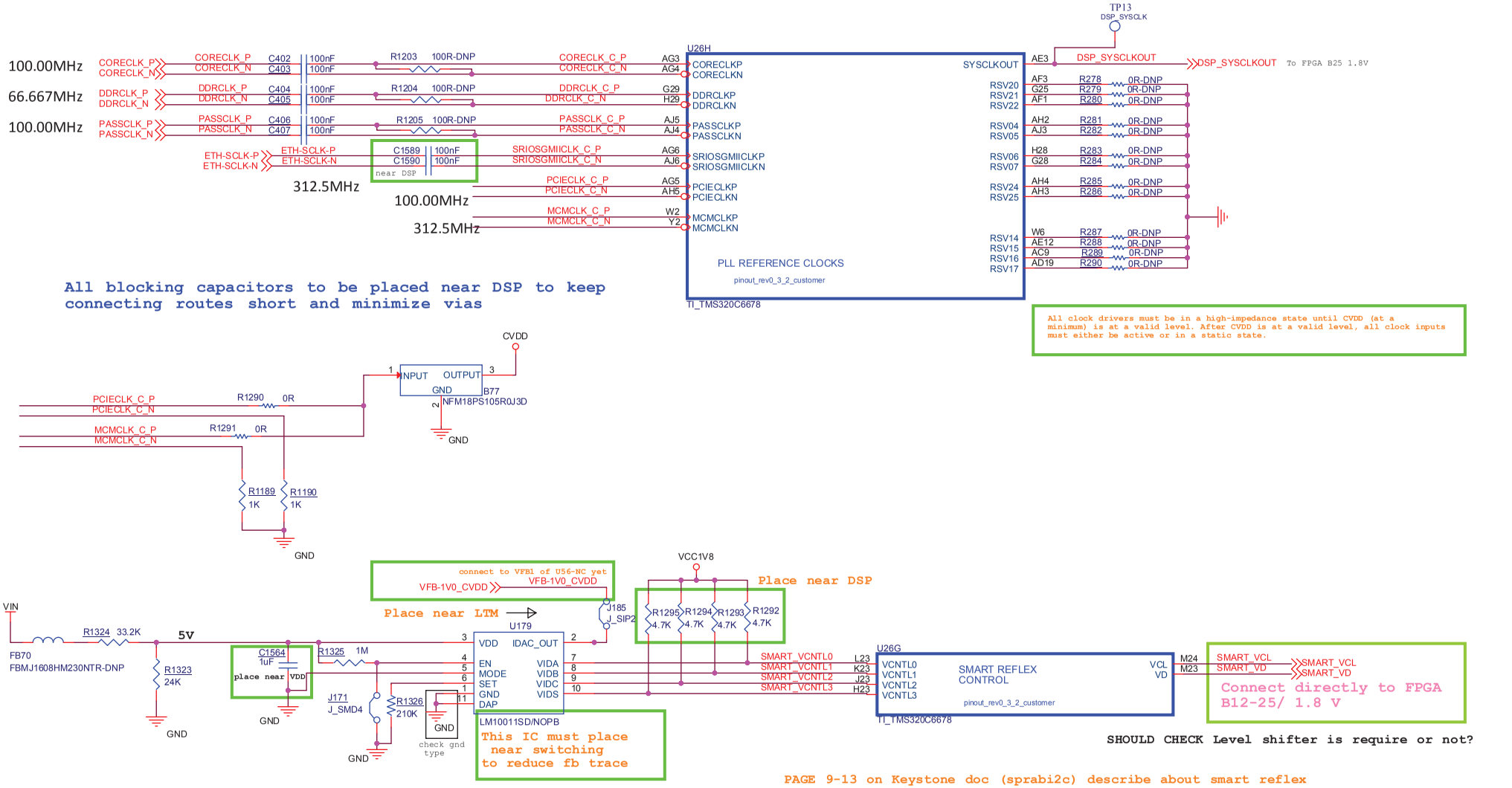
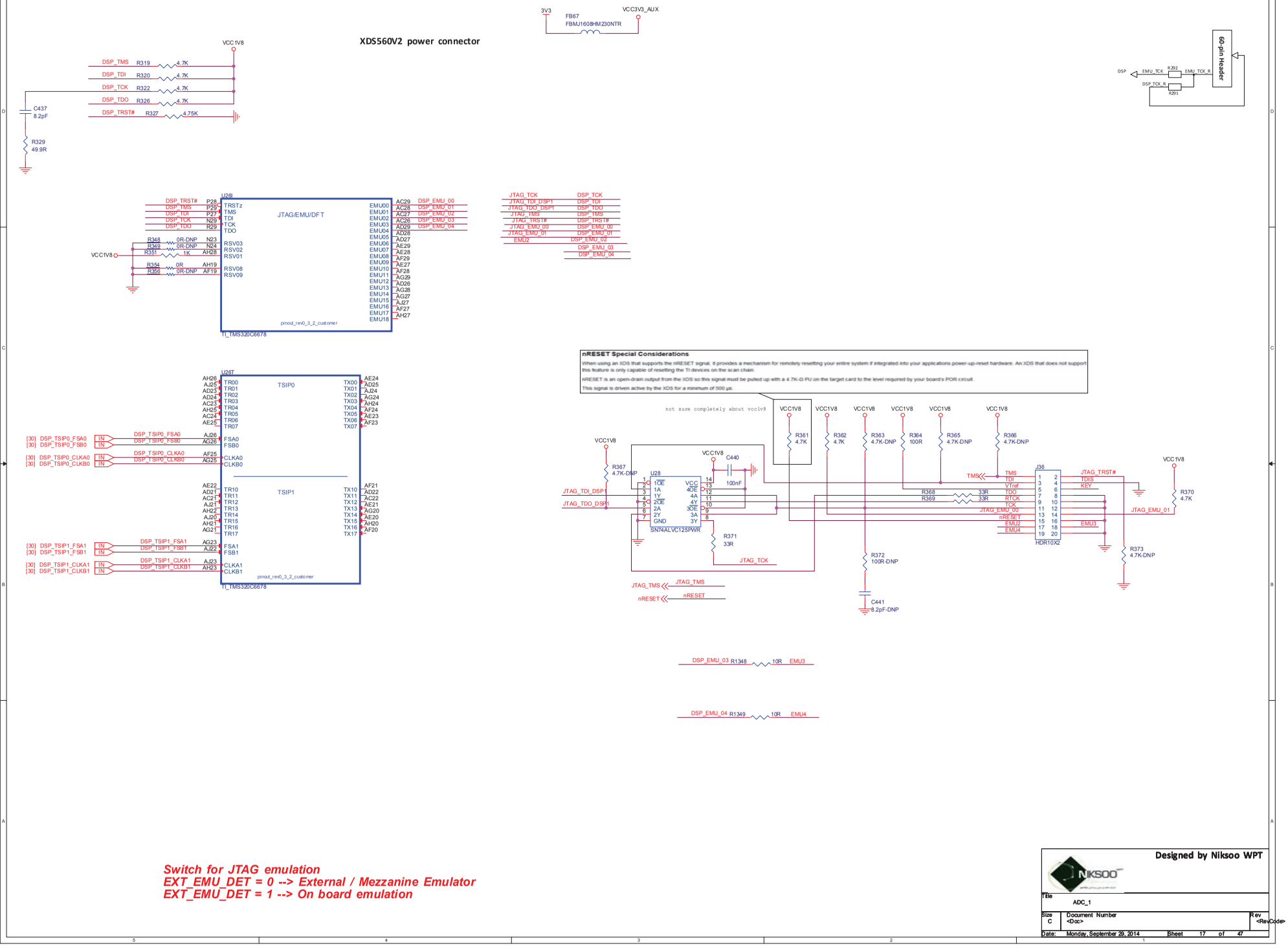

U18
AD9523-1BCPZ
Connect directly to FPGA B34-2.5V
Connect directly to FPGA B34-2.5V
Connect directly to FPGA B34-2.5V
Connect directly to FPGA B34-2.5V
Connect directly to FPGA B34-2.5V
Connect directly to FPGA B34-2.5V
If no space for placement sma can change to test point
Just CMOS 2.5V or LVDS OSC should use
Just CMOS 2.5V or LVDS OSC should use
Near AD9523
Near AD9523
Near ADC1
Near ADC2
Near ADC3
Near ADC4
Near DAC1
Near DAC2
ADC
THIS 2 CLK MUST BE CONNECTED TO FPGA BANK 2.5V
Check that EN pin can directly connect to FPGA or should connect to Level Shifter?
Designed by Niksoo WPT
Clock


100.00MHz
66.667MHz
100.00MHz
312.5MHz
100.00MHz
312.5MHz
CORECLK_P
CORECLK_N
DDRCLK_P
DDRCLK_N
PASSCLK_P
PASSCLK_N
ETH-SCLK-P
ETH-SCLK-N
C402
C403
C404
C405
C406
C407
C1589
C1590
100nF
R1203
R1204
R1205
100R-DNP
near DSP
U26H
CORECLKP
CORECLKN
DDRCLKP
DDRCLKN
PASSCLKP
PASSCLKN
SRIOSGMIICLKP
SRIOSGMIICLKN
PCIECLKP
PCIECLKN
MCMCLKP
MCMCLKN
PLL REFERENCE CLOCKS
pinout_rev0_3_2_customer
TI_TMS320C6678
SYSCLKOUT
TP13
DSP_SYSCLK
DSP_SYSCLKOUT
To FPGA B25 1.8V
RSV20
RSV21
RSV22
RSV04
RSV05
RSV06
RSV07
RSV24
RSV25
RSV14
RSV15
RSV16
RSV17
0R-DNP
All clock drivers must be in a high-impedance state until CVDD (at a minimum) is at a valid level. After CVDD is at a valid level, all clock inputs must either be active or in a static state.
All blocking capacitors to be placed near DSP to keep connecting routes short and minimize vias
CVDD
INPUT
OUTPUT
GND
B77
NFM18PS105R0J3D
PCIECLK_C_P
PCIECLK_C_N
MCMCLK_C_P
MCMCLK_C_N
R1290
R1291
0R
R1189
R1190
1K
VIN
FB70
FBMJ1608HM230NTR-DNP
R1324 33.2K
5V
R1323
24K
C1564
1uF
place near
R1325 1M
J171
J_SMD4
R1326
210K
check gnd type
connect to VFB1 of U56-NC yet
VFB-1V0_CVDD
Place near LTM
U179
VDD
EN
MODE
SET
GND
DAP
IDAC_OUT
VIDA
VIDB
VIDC
VIDS
LM10011SD/NOPB
This IC must place near switching to reduce fb trace
J185
J_SIP2
VCC1V8
Place near DSP
R1295
R1294
R1293
R1292
4.7K
SMART_VCNTL0
SMART_VCNTL1
SMART_VCNTL2
SMART_VCNTL3
L23
K23
J23
H23
U26G
VCNTL0
VCNTL1
VCNTL2
VCNTL3
SMART REFLEX CONTROL
pinout_rev0_3_2_customer
TI_TMS320C6678
VCL
VD
M24
M23
SMART_VCL
SMART_VD
Connect directly to FPGA B12-25/ 1.8 V
SHOULD CHECK Level shifter is require or not?
PAGE 9-13 on Keystone doc (sprabi2c) describe about smart reflex
Designed by Niksoo WPT
Title
Clock
Size
B
Document Number
<Doc>
<RevCode>
Rev
Date:
Wednesday, May 21, 2014
Sheet
13
of
47

Designed by Niksoo WPT

Title	ADC_1	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, May 21, 2014	Sheet 16 of 47	


XDS560V2 power connector
3V3
FB67
FBMJ1608HM230NTR
VCC3V3_AUX
60-pin Header
DSP
EMU_TCK
EMU_TCK_R
DSP_TCK_R
R292
R291
VCC1V8
DSP_TMS R319 4.7K
DSP_TDI R320 4.7K
DSP_TCK R322 4.7K
DSP_TDO R326 4.7K
DSP_TRST# R327 4.75K
C437 8.2pF
R329 49.9R
U26I
JTAG/EMU/DFT
TRSTz
TMS
TDI
TCK
TDO
RSV03
RSV02
RSV01
RSV08
RSV09
EMU00
EMU01
EMU02
EMU03
EMU04
EMU05
EMU06
EMU07
EMU08
EMU09
EMU10
EMU11
EMU12
EMU13
EMU14
EMU15
EMU16
EMU17
EMU18
DSP_EMU_00
DSP_EMU_01
DSP_EMU_02
DSP_EMU_03
DSP_EMU_04
R348 0R-DNP
R349 0R-DNP
R351 1K
R354 0R
R356 0R-DNP
pinout_rev0_3_2_customer
TI_TMS320C6678
JTAG_TCK
JTAG_TDI_DSP1
JTAG_TDO_DSP1
JTAG_TMS
JTAG_TRST1#
JTAG_EMU_00
JTAG_EMU_01
EMU2
DSP_TCK
DSP_TDI
DSP_TDO
DSP_TMS
DSP_TRST#
DSP_EMU_00
DSP_EMU_01
DSP_EMU_02
DSP_EMU_03
DSP_EMU_04
U26T
TSIP0
TSIP1
TR00
TR01
TR02
TR03
TR04
TR05
TR06
TR07
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TX00
TX01
TX02
TX03
TX04
TX05
TX06
TX07
TX10
TX11
TX12
TX13
TX14
TX15
TX16
TX17
FSA0
FSB0
CLKA0
CLKB0
FSA1
FSB1
CLKA1
CLKB1
[30] DSP_TSIP0_FSA0
[30] DSP_TSIP0_FSB0
[30] DSP_TSIP0_CLKA0
[30] DSP_TSIP0_CLKB0
[30] DSP_TSIP1_FSA1
[30] DSP_TSIP1_FSB1
[30] DSP_TSIP1_CLKA1
[30] DSP_TSIP1_CLKB1
nRESET Special Considerations
When using an XDS that supports the nRESET signal, it provides a mechanism for remotely resetting your entire system if integrated into your applications power-up-reset hardware. An XDS that does not support this feature is only capable of resetting the TI devices on the scan chain.
nRESET is an open-drain output from the XDS so this signal must be pulled up with a 4.7K-Ω PU on the target card to the level required by your board's POR circuit.
This signal is driven active by the XDS for a minimum of 500 µs.
not sure completely about vcc1v8
R361 4.7K
R362 4.7K
R363 4.7K-DNP
R364 100R
R365 4.7K-DNP
R366 4.7K-DNP
R367 4.7K-DNP
C440 100nF
U28
SN74ALVC125PWR
R368 33R
R369 33R
R371 33R
R372 100R-DNP
C441 8.2pF-DNP
R370 4.7K
R373 4.7K-DNP
J36
HDR10X2
TMS
TDI
VTref
TDO
RTCK
TCK
nRESET
EMU2
EMU4
TDIS
KEY
JTAG_TRST#
JTAG_EMU_01
EMU3
JTAG_TDI_DSP1
JTAG_TDO_DSP1
JTAG_TMS
nRESET
JTAG_TCK
DSP_EMU_03 R1348 10R EMU3
DSP_EMU_04 R1349 10R EMU4
Switch for JTAG emulation
EXT_EMU_DET = 0 --> External / Mezzanine Emulator
EXT_EMU_DET = 1 --> On board emulation
Designed by Niksoo WPT
NIKSOO
Title
ADC_1
Size C
Document Number <Doc>
Rev <RevCode>
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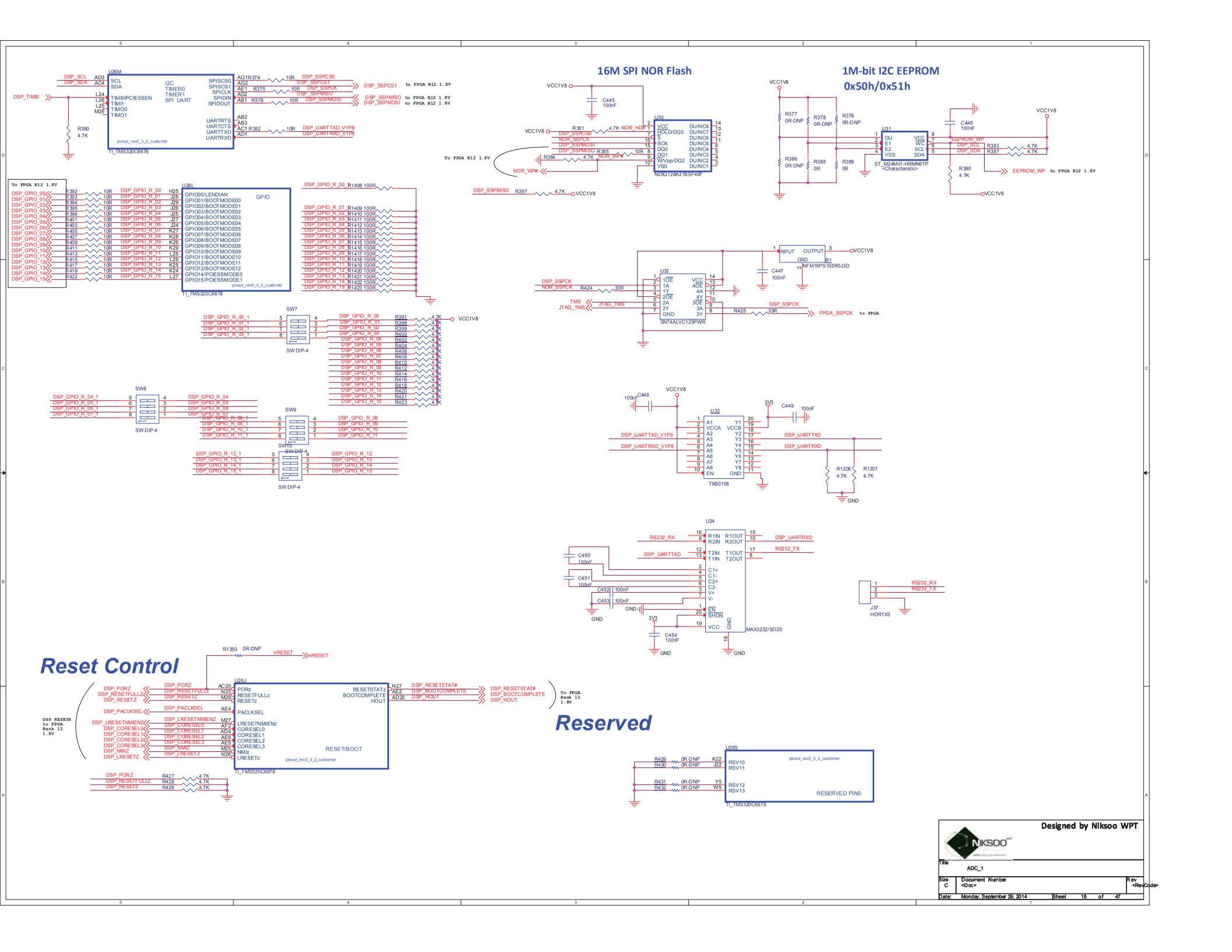
16M SPI NOR Flash
1M-bit I2C EEPROM
0x50h/0x51h
Reset Control
Reserved
U26M
TI_TMS320C6678
U26L
GPIO
U30
N25Q128A21BSF40F
U31
ST_M24M01-HRMN6TP
U32
5N74ALVC125PWR
U33
TXB0108
U34
MAX3222/SO20
U26J
RESET/BOOT
U26S
RESERVED PINS
SW DIP-4
NFM18PS105R0J3D
HDR1X3
Designed by Niksoo WPT
Title
ADC_1
Size C
Document Number
Rev
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0.9V - 1.1V (Smart Reflex)

U26A — 0.9V - 1.1V SMARTREFLEX CORE SUPPLY — TI_TMS320C6678

H7	CVDD_1	CVDD_42	R18
H9	CVDD_2	CVDD_43	R20
H11	CVDD_3	CVDD_44	R22
H13	CVDD_4	CVDD_45	T9
H15	CVDD_5	CVDD_46	T11
H17	CVDD_6	CVDD_47	T13
H19	CVDD_7	CVDD_48	T15
H21	CVDD_8	CVDD_49	T17
J10	CVDD_9	CVDD_50	T19
J12	CVDD_10	CVDD_51	T21
J16	CVDD_11	CVDD_52	U8
J18	CVDD_12	CVDD_53	U10
J20	CVDD_13	CVDD_54	U18
K11	CVDD_14	CVDD_55	U20
K17	CVDD_15	CVDD_56	U22
K21	CVDD_16	CVDD_57	V9
L10	CVDD_17	CVDD_58	V11
L12	CVDD_18	CVDD_59	V17
L16	CVDD_19	CVDD_60	V19
L18	CVDD_20	CVDD_61	V21
M11	CVDD_21	CVDD_62	W8
M13	CVDD_22	CVDD_63	W10
M15	CVDD_23	CVDD_64	W18
M17	CVDD_24	CVDD_65	W20
M19	CVDD_25	CVDD_66	W22
N8	CVDD_26	CVDD_67	Y9
N10	CVDD_27	CVDD_68	Y11
N12	CVDD_28	CVDD_69	Y13
N14	CVDD_29	CVDD_70	Y15
N16	CVDD_30	CVDD_71	Y17
N18	CVDD_31	CVDD_72	Y19
P9	CVDD_32	CVDD_73	Y21
P11	CVDD_33	CVDD_74	AA8
P13	CVDD_34	CVDD_75	AA10
P15	CVDD_35	CVDD_76	AA12
P17	CVDD_36	CVDD_77	AA14
P19	CVDD_37	CVDD_78	AA16
P21	CVDD_38	CVDD_79	AA18
R8	CVDD_39	CVDD_80	AA22
R10	CVDD_40		
	CVDD_41		

pinout_rev0_3_2_customer

Place near to DSP

C455 470uF, C456 470uF, C457 100uF, C458 100uF, C459 220uF, C460 220uF, C461 47uF, C465 47uF, C466 47uF, C467 47uF, C468 47uF, C469 47uF, C470 47uF, C463 10uF, C462 10uF, C464 100nF, C471 100nF, C473 100nF, C474 100nF, C475 100nF, C476 100nF, C477 100nF, C478 100nF, C479 100nF, C480 100nF, C481 100nF, C482 100nF, C483 100nF

Place near to DSP pins

C486 10nF, C487 10nF, C488 10nF, C489 10nF, C490 10nF, C491 10nF, C492 10nF, C493 10nF, C494 10nF, C495 10nF, C502 10nF, C503 10nF, C484 10nF, C485 10nF

C504 560pF, C505 560pF, C506 560pF, C507 560pF, C508 560pF, C509 560pF, C510 560pF, C511 560pF, C512 560pF, C513 560pF, C514 560pF, C515 560pF, C516 560pF, C517 560pF, C518 560pF, C519 560pF, C520 560pF, C521 560pF, C522 560pF, C523 560pF

U26E — pinout_rev0_3_2_customer — TI_TMS320C6678

M7	VDDT1_1	VDDT2_1	AB9
N6	VDDT1_2	VDDT2_2	AB11
P7	VDDT1_3	VDDT2_3	AB13
R6	VDDT1_4	VDDT2_4	AB15
T7	VDDT1_5	VDDT2_5	AC8
U6	VDDT1_6	VDDT2_6	AC10
V7	VDDT1_7	VDDT2_7	AC12
		VDDT2_8	AC14
V5	VDDR1	VDDT2_9	AC16
		VDDT2_10	AC18
		VDDT2_11	AD7
		VDDT2_12	AD9
		VDDT2_13	AD11
		VDDT2_14	AD13
		VDDT2_15	AD15
		VDDT2_16	AD17
		VDDT2_17	AE18
		VDDT2_18	AB17
	1.0V SERDES TERMINATION SUPPLY	AE10	VDDR2
	1.5V SERDES REGULATOR SUPPLY	AE16	VDDR3
		AE14	VDDR4

VCC1V0

U26B — 1.0V CORE MEMORY SUPPLY — TI_TMS320C6678

J8	CVDD1_1	CVDD1_14	N22
J14	CVDD1_2	CVDD1_15	R12
K7	CVDD1_3	CVDD1_16	R14
K9	CVDD1_4	CVDD1_17	R16
K13	CVDD1_5	CVDD1_18	U12
K15	CVDD1_6	CVDD1_19	U14
L8	CVDD1_7	CVDD1_20	U16
L14	CVDD1_8	CVDD1_21	V13
L20	CVDD1_9	CVDD1_22	V15
L22	CVDD1_10	CVDD1_23	W12
M9	CVDD1_11	CVDD1_24	W14
M21	CVDD1_12	CVDD1_25	W16
N20	CVDD1_13		

pinout_rev0_3_2_customer

Place near to DSP

C529 100uF, C530 100uF, C531 47uF, C532 100nF, C533 100nF, C534 100nF, C535 100nF, C536 100nF, C537 100nF, C538 10nF, C539 10nF, C540 10nF, C541 10nF, C542 10nF, C543 10nF

Place near to DSP pins

C552 560pF, C553 560pF, C554 560pF, C555 560pF, C556 560pF, C557 560pF, C558 560pF, C559 560pF, C560 560pF, C561 560pF, C605 10uF, C606 10uF, C614 10uF, C615 10uF

VDDT1 → INPUT OUTPUT → VCC1V0: C524 100nF, C525 10nF, C526 560pF, C527 560pF, NFM18PS105R0J3D B2, C528 10uF

VDDR2 → INPUT OUTPUT → VCC1V5: C544 560pF, C545 100nF, C546 10nF, C547 1000pF, NFM18PS105R0J3D B3

VDDR4 → INPUT OUTPUT → VCC1V5: C548 560pF, C549 100nF, C550 10nF, C551 1000pF, NFM18PS105R0J3D B4

VDDT2 → INPUT OUTPUT → VCC1V0: C562 100nF, C563 10nF, C564 560pF, C565 560pF, C566 100nF, C567 10nF, C568 560pF, C569 560pF, NFM18PS105R0J3D B5, C570 10uF

VDDR1 → INPUT OUTPUT → VCC1V5: C584 560pF, C585 100nF, C586 10nF, C587 1000pF, NFM18PS105R0J3D B6

VDDR3 → INPUT OUTPUT → VCC1V5: C596 560pF, C597 100nF, C598 10nF, C599 1000pF, NFM18PS105R0J3D B7

1.8V

U26D — 1.8V I/O SUPPLY — TI_TMS320C6678

AB7	DVDD18_1	DVDD18_12	AB21
N26	DVDD18_2	DVDD18_13	AB28
P23	DVDD18_3	DVDD18_14	AC3
T23	DVDD18_4	DVDD18_15	AF26
U26	DVDD18_5	DVDD18_16	AG22
V23	DVDD18_6	DVDD18_17	AH1
Y7	DVDD18_7	DVDD18_18	AH29
Y23	DVDD18_8	DVDD18_19	AJ2
AB5	DVDD18_9	DVDD18_20	AJ28
H24	DVDD18_10	DVDD18_21	AA6
AB19	DVDD18_11	DVDD18_22	AF5

R433 0R-DNP AA21, R434 0R-DNP AA20 — RESERVED PINS: RSV0A, RSV0B

1.8V PLL SUPPLY: H22 AVDDA1, AC6 AVDDA2, AD5 AVDDA3

Place near to DSP

C571 100uF, C572 10uF, C573 10uF, C574 10uF

Place near to DSP pins

C575 100nF, C576 100nF, C577 100nF, C578 10nF, C579 10nF, C580 10nF, C581 1000pF, C582 1000pF, C583 1000pF

1000pF 0402

Place near to DSP pins

C588 560pF, C589 560pF, C590 560pF, C591 560pF, C592 560pF, C593 560pF, C594 560pF, C595 560pF

1.5V

U26C — 1.5V DDR3 I/O SUPPLY — TI_TMS320C6678

A2	DVDD15_1	DVDD15_18	F17
A11	DVDD15_2	DVDD15_19	F19
A17	DVDD15_3	DVDD15_20	F26
A28	DVDD15_4	DVDD15_21	F28
B1	DVDD15_5	DVDD15_22	G2
B29	DVDD15_6	DVDD15_23	G4
C14	DVDD15_7	DVDD15_24	G8
C25	DVDD15_8	DVDD15_25	G10
D5	DVDD15_9	DVDD15_26	G12
D8	DVDD15_10	DVDD15_27	G14
D20	DVDD15_11	DVDD15_28	G16
D23	DVDD15_12	DVDD15_29	G18
E3	DVDD15_13	DVDD15_30	G20
F5	DVDD15_14	DVDD15_31	G23
F7	DVDD15_15		
F9	DVDD15_16		
F11	DVDD15_17		

pinout_rev0_3_2_customer

VCC1V8_AVDD3 → INPUT OUTPUT → VCC1V8: C600 100nF, C601 10nF, C602 560pF, NFM18PS105R0J3D B8, C603 100uF, C604 10uF

VCC1V8_AVDD2 → INPUT OUTPUT → VCC1V8: C619 100nF, C620 10nF, C621 560pF, NFM18PS105R0J3D B9

VCC1V8_AVDD1 → INPUT OUTPUT → VCC1V8: C630 100nF, C631 10nF, C632 560pF, NFM18PS105R0J3D B10

Place near to DSP

C607 10uF, C608 10uF, C609 10uF, C610 10uF

Place near to DSP pins

C622 10nF, C623 10nF, C624 10nF, C625 10nF, C626 10nF, C627 10nF, C628 10nF, C629 10nF

Place near to DSP pins

C633 560pF, C634 560pF, C635 560pF, C636 560pF, C637 560pF, C638 560pF, C639 560pF, C640 560pF

C611 100nF, C612 100nF, C613 100nF, C616 100nF, C617 100nF, C618 100nF

Designed by Niksoo WPT

Title	ADC_1	
Size C	Document Number <Doc>	Rev <RevCode>
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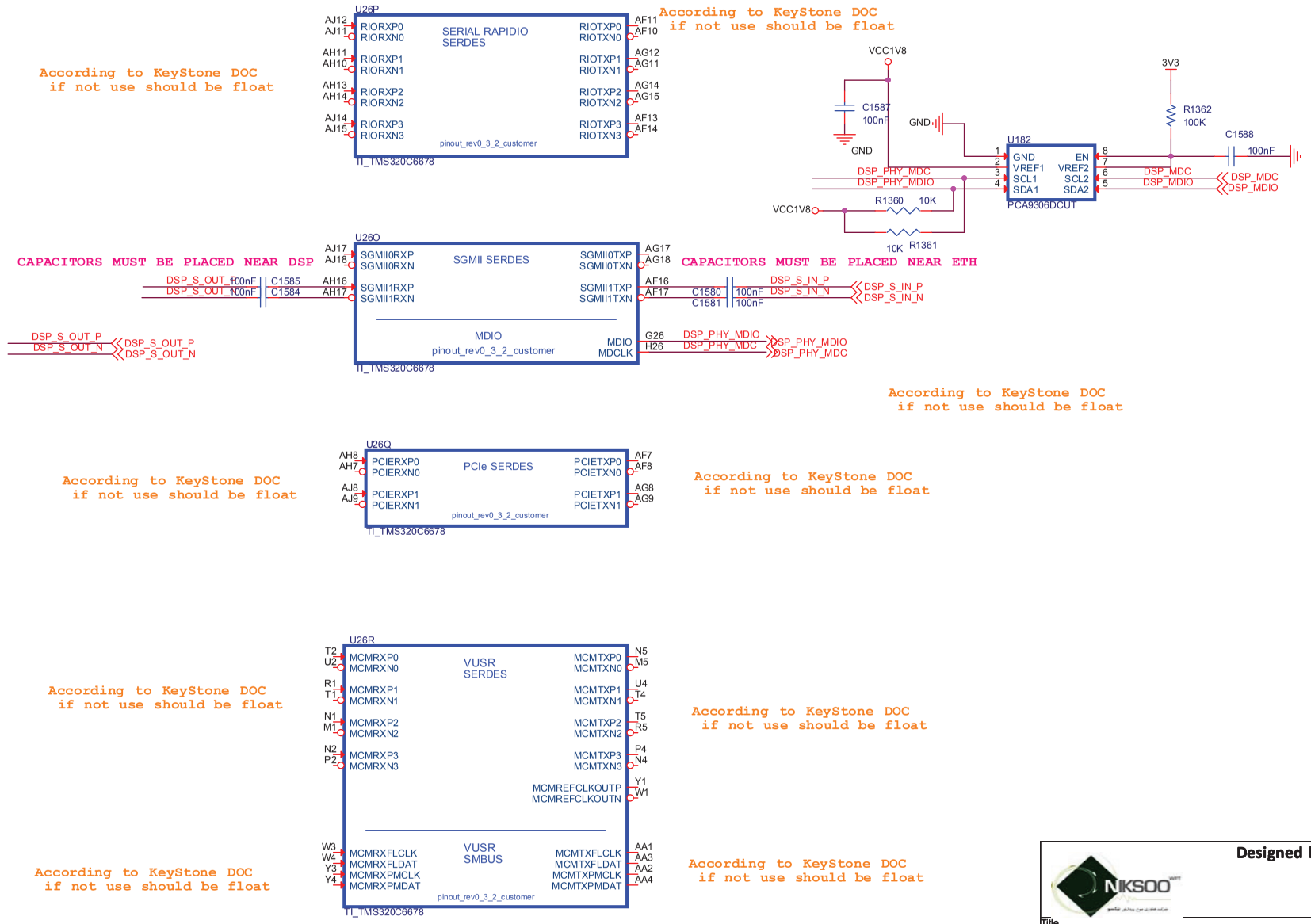
According to KeyStone DOC
if not use should be float
U26P
SERIAL RAPIDIO
SERDES
pinout_rev0_3_2_customer
TI_TMS320C6678
According to KeyStone DOC
if not use should be float
VCC1V8
3V3
C1587
100nF
GND
R1362
100K
C1588
100nF
U182
PCA9306DCUT
DSP_PHY_MDC
DSP_PHY_MDIO
DSP_MDC
DSP_MDIO
R1360
10K
R1361
10K
CAPACITORS MUST BE PLACED NEAR DSP
U26O
SGMII SERDES
MDIO
pinout_rev0_3_2_customer
TI_TMS320C6678
CAPACITORS MUST BE PLACED NEAR ETH
DSP_S_OUT_P
DSP_S_OUT_N
DSP_S_IN_P
DSP_S_IN_N
C1585
C1584
C1580
C1581
100nF
According to KeyStone DOC
if not use should be float
U26Q
PCIe SERDES
pinout_rev0_3_2_customer
TI_TMS320C6678
According to KeyStone DOC
if not use should be float
According to KeyStone DOC
if not use should be float
U26R
VUSR
SERDES
VUSR
SMBUS
pinout_rev0_3_2_customer
TI_TMS320C6678
According to KeyStone DOC
if not use should be float
According to KeyStone DOC
if not use should be float
According to KeyStone DOC
if not use should be float
Designed by Niksoo WPT
NIKSOO
Title
ADC_1
Size
B
Document Number
<Doc>
Rev
<RevCode>
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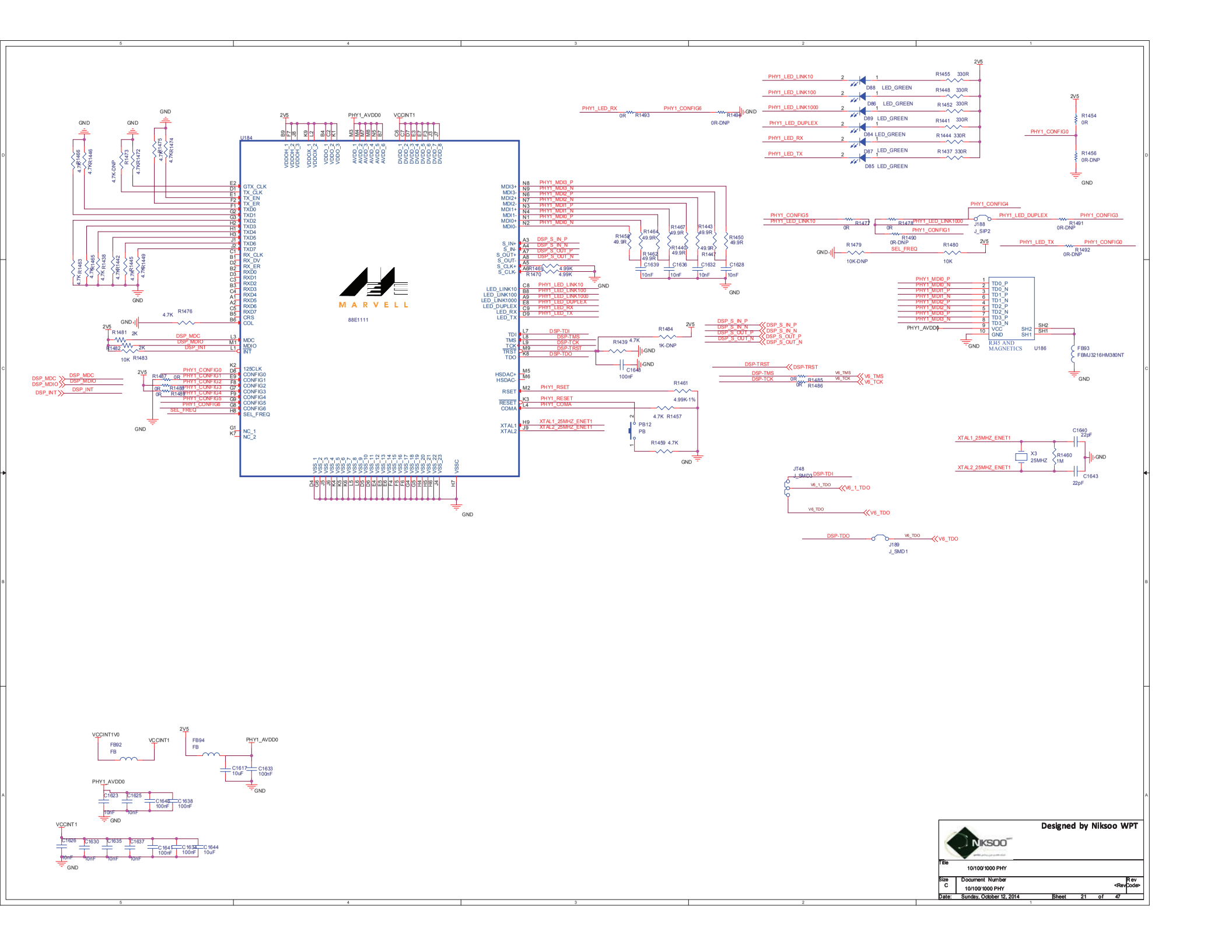
U184
88E1111
MARVELL
GTX_CLK
TX_CLK
TX_EN
TX_ER
TXD0
TXD1
TXD2
TXD3
TXD4
TXD5
TXD6
TXD7
RX_CLK
RX_DV
RX_ER
RXD0
RXD1
RXD2
RXD3
RXD4
RXD5
RXD6
RXD7
CRS
COL
MDC
MDIO
INT
125CLK
CONFIG0
CONFIG1
CONFIG2
CONFIG3
CONFIG4
CONFIG5
CONFIG6
SEL_FREQ
NC_1
NC_2
MDI3+
MDI3-
MDI2+
MDI2-
MDI1+
MDI1-
MDI0+
MDI0-
S_IN+
S_IN-
S_OUT+
S_OUT-
S_CLK+
S_CLK-
LED_LINK10
LED_LINK100
LED_LINK1000
LED_DUPLEX
LED_RX
LED_TX
TDI
TMS
TCK
TRST
TDO
HSDAC+
HSDAC-
RSET
RESET
COMA
XTAL1
XTAL2
PHY1_MDI3_P
PHY1_MDI3_N
PHY1_MDI2_P
PHY1_MDI2_N
PHY1_MDI1_P
PHY1_MDI1_N
PHY1_MDI0_P
PHY1_MDI0_N
DSP_S_IN_P
DSP_S_IN_N
DSP_S_OUT_P
DSP_S_OUT_N
PHY1_LED_LINK10
PHY1_LED_LINK100
PHY1_LED_LINK1000
PHY1_LED_DUPLEX
PHY1_LED_RX
PHY1_LED_TX
DSP-TDI
DSP-TMS
DSP-TCK
DSP-TRST
DSP-TDO
PHY1_RSET
PHY1_COMA
XTAL1_25MHZ_ENET1
XTAL2_25MHZ_ENET1
PHY1_CONFIG0
PHY1_CONFIG1
PHY1_CONFIG2
PHY1_CONFIG3
PHY1_CONFIG4
PHY1_CONFIG5
PHY1_CONFIG6
SEL_FREQ
DSP_MDC
DSP_MDIO
DSP_INT
V6_TMS
V6_TCK
V6_TDI
V6_TDO
V6_1_TDO
PHY1_AVDD0
VCCINT1
VCCINT1V0
2V5
GND
RJ45 AND MAGNETICS
U186
J188
J_SIP2
J189
J_SMD1
JT48
J_SMD3
X3
25MHZ
PB12
PB
D88 LED_GREEN
D86 LED_GREEN
D89 LED_GREEN
D84 LED_GREEN
D87 LED_GREEN
D85 LED_GREEN
FB93
FBMJ3216HM380NT
FB92
FB94
FB
Designed by Niksoo WPT
NIKSOO
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10/100/1000 PHY
Size
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Rev
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Sunday, October 12, 2014
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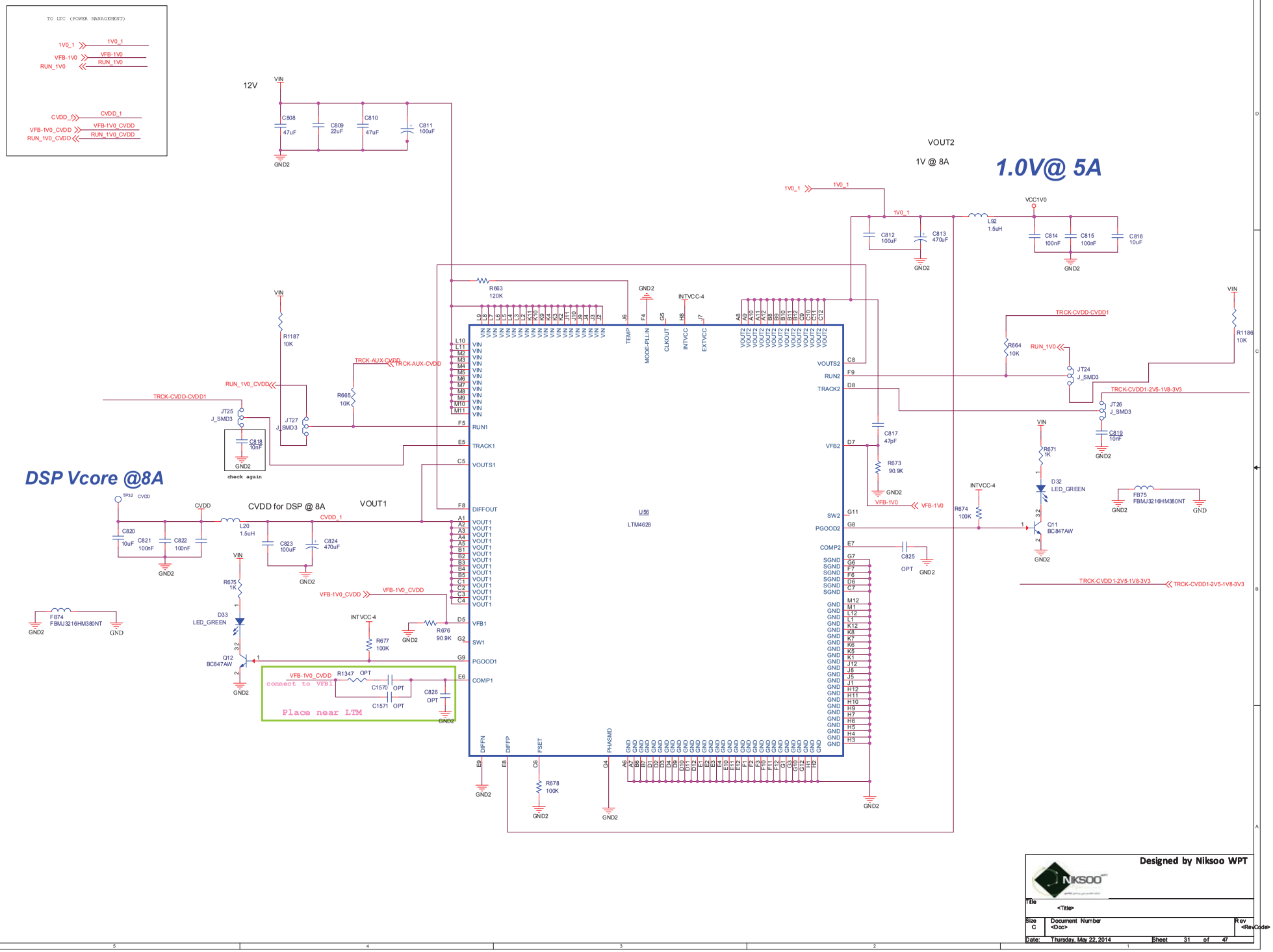
TO LIC (POWER MANAGEMENT)
1V0_1
VFB-1V0
RUN_1V0
CVDD_1
VFB-1V0_CVDD
RUN_1V0_CVDD
12V
VIN
C808 47uF
C809 22uF
C810 47uF
C811 100uF
GND2
VOUT2
1V @ 8A
1.0V@ 5A
C812 100uF
C813 470uF
L92 1.5uH
VCC1V0
C814 100nF
C815 100nF
C816 10uF
R663 120K
GND2
INTVCC-4
R1187 10K
TRCK-AUX-CVDD
RUN_1V0_CVDD
TRCK-CVDD-CVDD1
R665 10K
JT25 J_SMD3
JT27 J_SMD3
C818 10nF
check again
R664 10K
RUN_1V0
JT24 J_SMD3
R1186 10K
TRCK-CVDD1-2V5-1V8-3V3
JT26 J_SMD3
C819 10nF
DSP Vcore @8A
CVDD for DSP @ 8A
VOUT1
TP52 CVDD
C820 10uF
C821 100nF
C822 100nF
L20 1.5uH
C823 100uF
C824 470uF
C817 47pF
R673 90.9K
VFB-1V0
R671 1K
D32 LED_GREEN
FB75 FBMJ3216HM380NT
R674 100K
Q11 BC847AW
C825 OPT
U56
LTM4628
R675 1K
D33 LED_GREEN
FB74 FBMJ3216HM380NT
GND
VFB-1V0_CVDD
INTVCC-4
R677 100K
R676 90.9K
Q12 BC847AW
R1347 OPT
C1570 OPT
C1571 OPT
C826 OPT
connect to VFB1
Place near LTM
R678 100K
TEMP
MODE-PLLIN
CLKOUT
INTVCC
EXTVCC
VOUTS2
RUN2
TRACK2
VFB2
SW2
PGOOD2
COMP2
RUN1
TRACK1
VOUTS1
DIFFOUT
VFB1
SW1
PGOOD1
COMP1
DIFFN
DIFFP
FSET
PHASMD
Designed by Niksoo WPT
NIKSOO
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<Title>
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Rev <RevCode>
Date: Thursday, May 22, 2014
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