CIF (352x288) C

General Description

a high performance CMOS device for digital still image and video/still camera products.

A incorporates a 352 x 288 (CIF) image array and an on-chip 10-bit A/D converter capable of operating at up to 30 frames per second (fps) at full resolution and 60 fps at QCIF (176 x 144) resolution. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), and provides superior black level calibration for optimal color performance. The control registers allow for flexible control of timing, polarity, and CAMERACHIP sensor operation, which in turn allows the engineer a great deal of freedom in product design.

Features

- Optical black level calibration
- Video or snapshot operations
- Programmable exposure and gain control
- Horizontal and vertical sub-sampling (2:1 and 2:1, respectively)
- Programmable image windowing
- Variable frame rate control
- On-chip R/G/B Channel and Luminance Average Counter
- Internal/External frame synchronization
- SCCB slave interface
- Power on reset and power down mode

Ordering Information

Product	Package
	PLCC

Note: The A is available in a lead-free package.

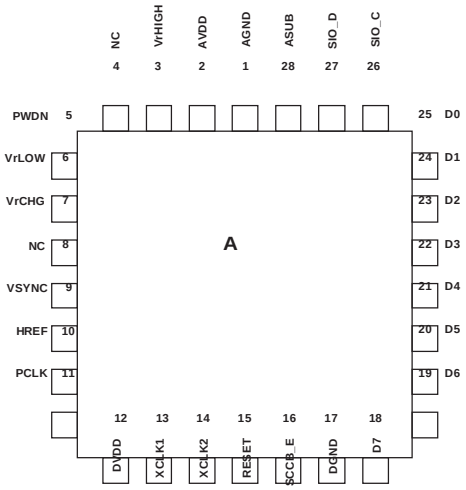
Applications

- Digital still cameras
- Video/Still camcorders

Key Specifications

Array Size	CIF	352 x 288
	QCIF	176 x 144
Power Supply	Core	3.3 VDC ± 10%
	Analog	3.3 VDC ± 10%
	I/O	3.3 VDC ± 10%
Power Requirements	Active	30 mA
	Standby	< 10 µA
Electronics Exposure	CIF	Up to 334:1
	QCIF	Up to 166:1
Output Format		8-bit digital raw RGB data
Lens Size		1/9.4"
Maximum Image Transfer Rate	CIF	30 fps
	QCIF	60 fps
Sensitivity		1.0 V/Lux-sec
S/N Ratio		54 dB
Dynamic Range		60 dB (due to ADC limitations)
Scan Mode		Progressive
Maximum Exposure Interval		334 x t_{ROW}
Pixel Size		4.2 µm x 4.2 µm
Dark Current		28 mV/s
Fixed Pattern Noise		< 0.03% of $V_{PEAK-TO-PEAK}$
Image Area		1.48 mm x 1.21 mm
Package Dimensions		9mm x 9 mm

Figure 1 A Pin Diagram (Top View)



Functional Description

Figure 2 shows the functional block diagram of t includes: A

- Image Sensor Array (360 x 306 resolution)
- Analog Amplifier
  - Gain Control
- Black Level Compensation
- Timing Generator and Control Logic
  - Frame Rate Timing
  - Frame Rate Adjust
- SCCB Interface
- Channel Average Calculator

Figure 2 Functional Block Diagram

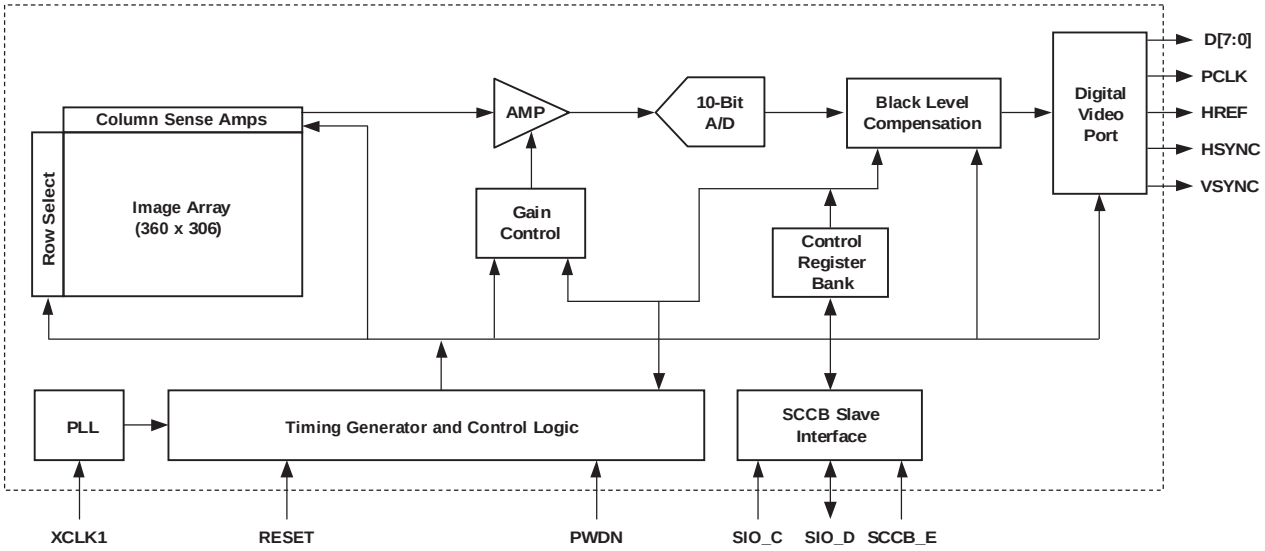
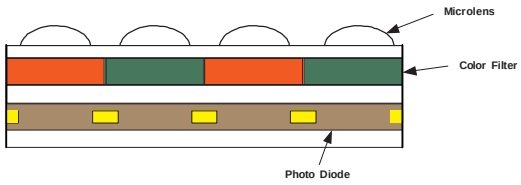


Image Sensor Array

Th A sensor is a 1/9.4-inch CMOS imaging device. The sensor contains 110,160 pixels. However, the maximum output window size is 352 columns by 288 rows.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme. Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Analog Amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

Gain Control

The amplifier gain can only be programmed by the user.

Black Level Compensation

After the pixel data has been digitized, black level calibration can be applied before the data is output. The black level calibration block subtracts the average signal level of optical black pixels to compensate for the temperature and exposure time generated dark current in the pixel output. The user can disable black level calibration.

Timing Generator and Control Logic

In general, the timing generator controls the following:

- Frame Rate Timing
- Frame Rate Adjust

Frame Rate Timing

Default frame timing is illustrated in Figure 9. Refer to Table 1 for the actual pixel rate at different frame rates at full resolution.

Table 1 Frame and Pixel Rates

Frame Rate (fps)	30	15	7.5
PCLK (MHz)	6	3	1.5
NOTE: Based on 24 MHz external clock and internal PLL on, frame rate is adjusted by the main clock divide method.			

Frame Rate Adjust

A offers three methods for frame rate adjustment:

- Clock prescaler:
  By changing the system clock divide ratio, the frame rate and pixel rate will change together.
- Line adjustment:
  By adding a dummy pixel timing in each line, the frame rate can be changed while leaving the pixel rate as is.
- Vertical sync adjustment:
  By adding dummy line periods to the vertical sync period, the frame rate can be altered while the pixel rate remains the same.

After changing registers COML (0x2A) and FRARL (0x2B) to adjust the dummy pixels, it is necessary to write to register COMH (0x12) or CLKRC (0x11) to reset the counter. Generally, OmniVision suggests users write to register COMH (0x12) (to change the sensor mode) as the last one. However, if you want to adjust the cropping window, it is necessary to write to those registers after changing register COMH (0x12). To use COMH to reset the counter, it is necessary to generate a pulse on resolution control register bit COMH[6] or COMH[5].

SCCB Interface

A provides an on-chip SCCB serial control port that allows access to all internal registers, for complete control and monitoring of A operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

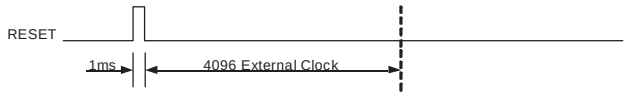
Channel Average Calculator

A provides average output level data for the R/G/B channels along with frame-averaged luminance level. Access to the data is provided via the serial control port.

Reset

The RESET pin (pin 15) is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the RESET pin is low.

Figure 4 RESET Timing Diagram



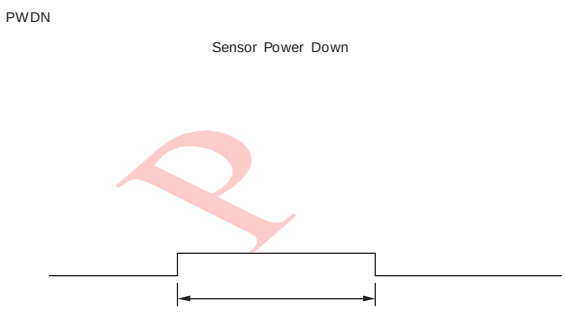
There are two ways for a sensor reset:

1. Hardware reset - Pulling the RESET pin high and keeping it high for at least 1 ms. As shown in Figure 4, after a reset has been initiated, the sensor will be most stable after the period shown as 4096 External Clock.
2. Software reset - Writing 0x80 to register 0x12 (see "COMH" on page 13) for a software reset. If a software reset is used, a reset operation done twice is recommended to make sure the sensor is stable and ready to access registers. When performing a software reset twice, the second reset should be initiated after the 4096 External Clock period as shown in Figure 4.

Power Down Mode

The PWDN pin (pin 5) is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the PWDN pin is low.

Figure 5 PWDN Timing Diagram



Two methods of power-down or standby operation are available with the A .

- Hardware power-down may be selected by pulling the PWDN pin high (+3.3VDC). When this occurs, A internal device clock is halted and all internal counters are reset. The current draw is less than 10 µA in this standby mode.
- Software power-down can be effected by setting the COMC[4] register bit high (see "COMC" on page 12). Standby current will be less then 2 mA when in software power-down.

Video Output

RGB Raw Data Output

A sensor offers 8-bit RGB raw data output.

Line/Pixel Timing

A digital video port can be programmed to work in either master or slave mode.

Pixel Output Pattern

Table 2 shows the output data order from the A . The data output sequence following the first HREF and after VSYNC is: $B_{0,0}$ $G_{0,1}$ $B_{0,2}$ $G_{0,3}$… $B_{0,350}$ $G_{0,351}$. After the second HREF, the output is $G_{1,0}$ $R_{1,1}$ $G_{1,2}$ $R_{1,3}$… $G_{1,350}$ $R_{1,351}$…, etc. If the sensor is programmed to output QCIF resolution data, horizontal and vertical sub-sampling will occur. The default output sequence for the first line of output will be: $B_{0,0}$ $G_{0,1}$ $B_{0,4}$ $G_{0,5}$… $B_{0,286}$ $G_{0,287}$. The second line of output will be: $G_{1,0}$ $R_{1,1}$ $G_{1,4}$ $R_{1,5}$… $G_{1,286}$ $R_{1,287}$.

Table 2 Data Pattern

R/C	0	1	2	3	. . .	350	351
0	$B_{0,0}$	$G_{0,1}$	$B_{0,2}$	$G_{0,3}$	. . .	$B_{0,350}$	$G_{0,351}$
1	$G_{1,0}$	$R_{1,1}$	$G_{1,2}$	$R_{1,3}$	. . .	$G_{1,350}$	$R_{1,351}$
2	$B_{2,0}$	$G_{2,1}$	$B_{2,2}$	$G_{2,3}$	. . .	$B_{2,350}$	$G_{2,351}$
3	$G_{3,0}$	$R_{3,1}$	$G_{3,2}$	$R_{3,3}$	. . .	$G_{3,350}$	$R_{3,351}$
. .					. .		
286	$B_{286,0}$	$G_{286,1}$	$B_{286,2}$	$G_{286,3}$		$B_{286,350}$	$G_{286,351}$
287	$G_{287,0}$	$R_{287,1}$	$G_{287,2}$	$R_{287,3}$		$G_{287,350}$	$R_{287,351}$

Note that after writing to register COMH (0x12) to change the sensor mode, registers related to the sensor's cropping window will be reset back to its default value.

Pin Description

Table 3 Pin Description

Pin Number	Name	Pin Type	Function/Description
01	AGND	Power	Analog ground
02	AVDD	Power	3.3 V supply for analog circuits
03	VrHIGH	Analog	Sensor reference 1 - connect to ground using a 0.1 µF capacitor
04	NC	–	No connection
05	PWDN	Input (0)[a]	Power down mode enable, active high
06	VrLOW	Analog	Sensor reference 3 - connect to ground using a 0.1 µF capacitor
07	VcCHG	Analog	Sensor reference 4 - bypass to ground using a 1 µF capacitor
08	NC	–	No connection
09	VSYNC	Output	Vertical synchronization output when chip is in master mode.
10	HREF	Output	Horizontal reference output
11	PCLK	Output	Pixel clock output
12	DVDD	Power	3.3 V supply for digital circuits
13	XCLK1	Input	Crystal clock input
14	XCLK2	Output	Crystal clock output
15	RESET	Input (0)	Chip reset, active high
16	SCCB_E	Input (0)	SCCB interface enable signal, active low
17	DGND	Power	Digital ground
18	D7	Output	Video port output bit[7]
19	D6	Output	Video port output bit[6]
20	D5	Output	Video port output bit[5]
21	D4	Output	Video port output bit[4]
22	D3	Output	Video port output bit[3]
23	D2	Output	Video port output bit[2]
24	D1	Output	Video port output bit[1]
25	D0	Output	Video port output bit[0]
26	SIO_C	Input	SCCB serial interface clock input
27	SIO_D	I/O	SCCB serial interface data I/O
28	ASUB	Power	Analog ground (substrate)

a. Input (0) represents an internal pull-down low resistor.

Electrical Characteristics

Table 4 Operating Conditions

Parameter	Min	Max	Unit
Operating temperature[a]	0	40	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

a. Exceeding the stresses listed may permanently damage the device. This is a stress rating only and functional operation of the sensor at these and any other condition above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for any extended period may affect reliability.

Table 5 DC Characteristics (0°C < T_A < 85°C, Voltages referenced to GND)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD-A}	Supply voltage (AVDD)	3.0	3.3	3.6	V
V_{DD-D}	Supply voltage (DVDD)	3.0	3.3	3.6	V
I_{DD}	Operating current (V_{DD-A}, V_{DD-D} = 3.3V at 30fps, CIF)		25	30	mA
Digital Inputs					
V_{IL}	Input voltage LOW			0.8	V
V_{IH}	Input voltage HIGH	2			V
C_{IN}	Input capacitor			10	pF
Digital Outputs (standard loading 25 pF, 1.2 KΩ to 3 V)					
V_{OH}	Output voltage HIGH	2.4			V
V_{OL}	Output voltage LOW			0.6	V
SCCB Inputs					
V_{IL}	SIO_C and SIO_D	-0.5	0	1	V
V_{IH}	SIO_C and SIO_D	2.5	3.3	V_{DD} + 0.5	V

Table 6 AC Characteristics (0°C < T_A < 85°C, V_{DD} = 3.3V)

Symbol	Parameter	Min	Typ	Max	Unit
ADC Parameters					
B	Analog bandwidth		12		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	Settling time for hardware reset			<1	ms
	Settling time for software reset			<1	ms
	Settling time for QCIF/CIF mode change			<1	ms
	Settling time for register setting			<300	ms

Table 7 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Oscillator and Clock Input					
f_{OSC}	Frequency (XCLK1, XCLK2)	8	24	48	MHz
t_r, t_f	Clock input rise/fall time			2	ns
	Clock input duty cycle	45	50	55	%

Timing Specifications

Figure 6 SCCB Timing Diagram

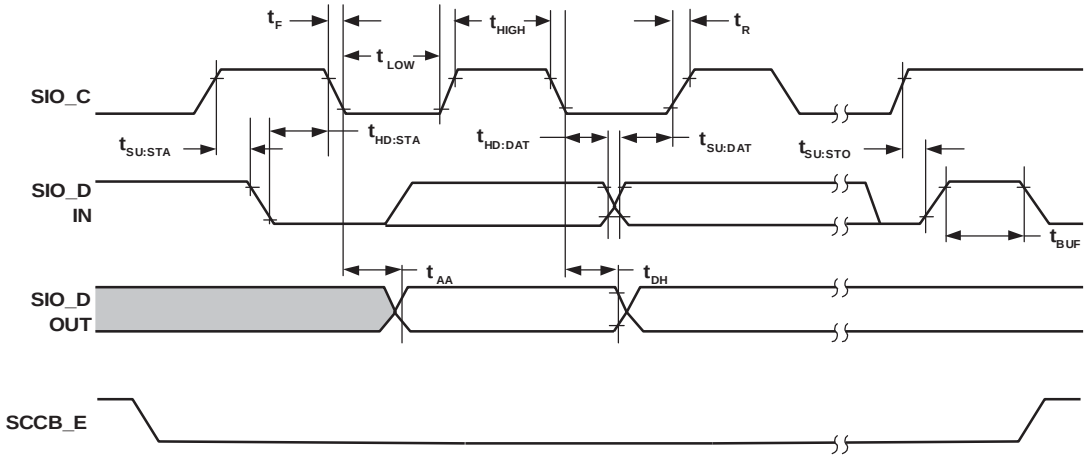


Table 8 SCCB Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock frequency			400	KHz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_{AA}	SIO_C low to data out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition hold time	600			ns
$t_{SU:STA}$	START condition setup time	600			ns
$t_{HD:DAT}$	Data in hold time	0			µs
$t_{SU:DAT}$	Data in setup time	100			ns
$t_{SU:STO}$	STOP condition setup time	600			ns
t_R, t_F	SCCB rise/fall times			300	ns
t_{DH}	Data out hold time	50			ns

Figure 7 CIF Line/Pixel Output Timing

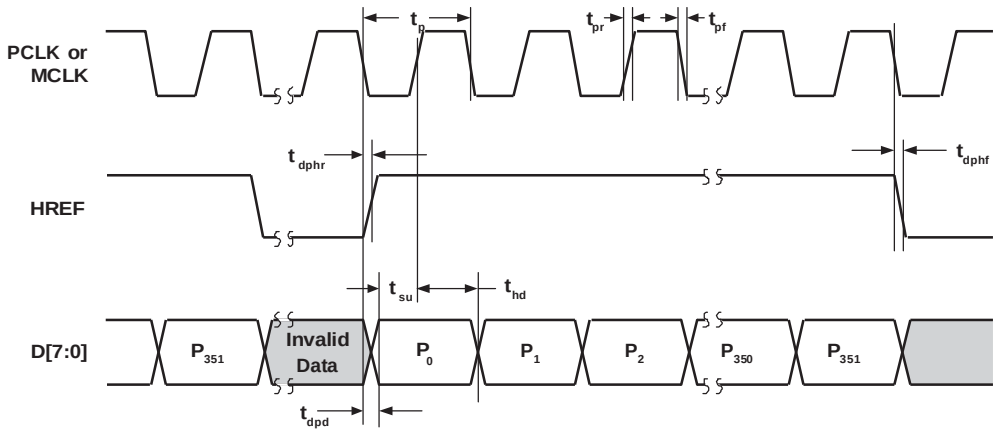


Figure 8 QCIF Line/Pixel Output Timing

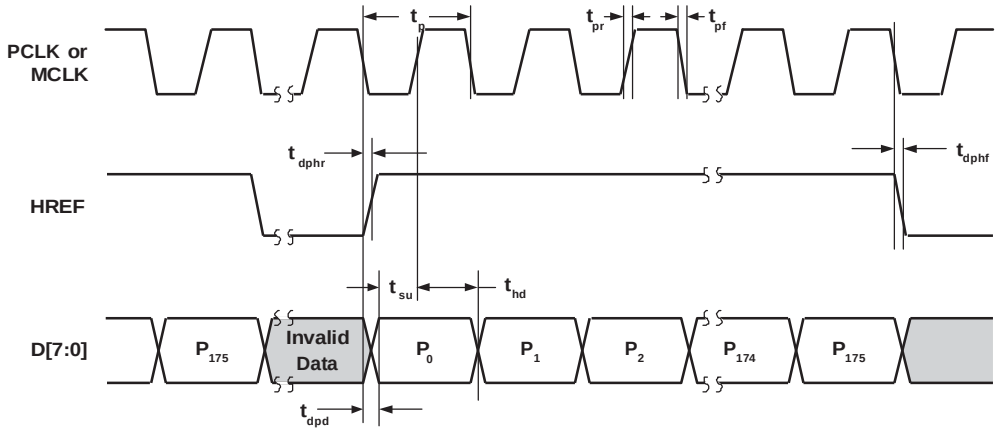


Figure 9 CIF Frame Timing

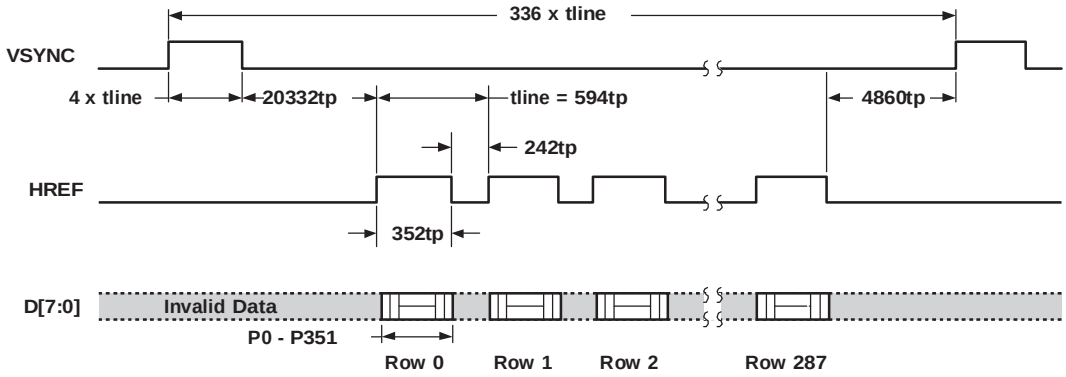


Figure 10 QCIF Frame Timing

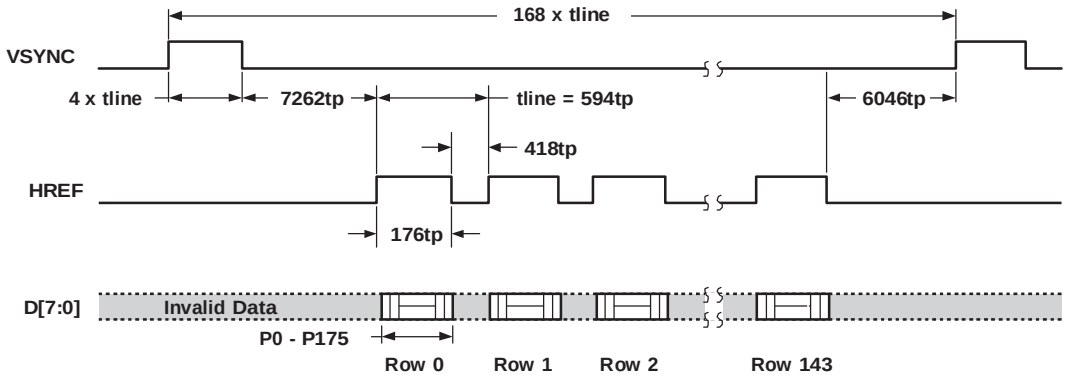
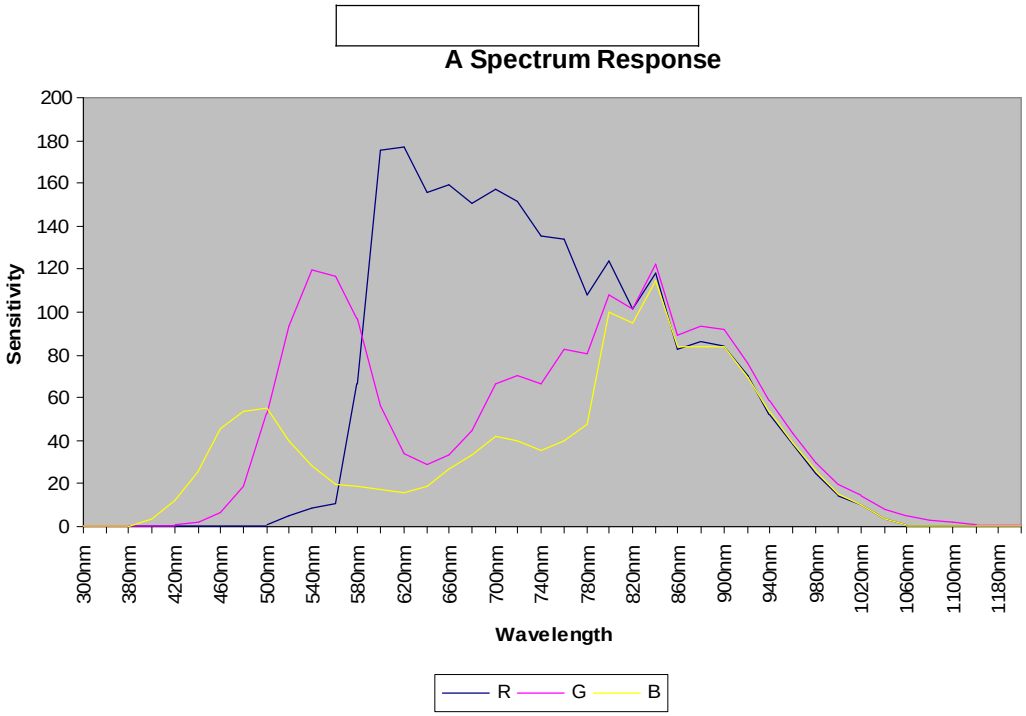


Table 9 Pixel Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit
t_p	PCLK period		166.67		ns
t_{pr}	PCLK rising time		40		ns
t_{pf}	PCLK falling time		20		ns
t_{dphr}	PCLK negative edge to HREF rising edge	0		20	ns
t_{dphf}	PCLK negative edge to HREF negative edge	0		20	ns
t_{dpd}	PCLK negative edge to data output delay	0		20	ns
t_{su}	Data bus setup time	15			ns
t_{hd}	Data bus hold time	8			ns

Light Response

Figure 11 A Light Response



Register Set

Table 10 provides a list and description of the Device Control registers contained in A A. The device slave addresses A are 42 for write and 43 for read.

Table 10 Device Control Register List (Sheet 1 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	Gain Control (GC) Gain Setting Bit[7:0]: Gain control gain setting • Range: 1x to 8x Gain = (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16)
01-02	RSVD	XX	–	Reserved
03	COMA	4F	RW	Common Control A Bit[7:4]: Reserved Bit[3:2]: Vertical window end position 2 LSB Bit[1:0]: Vertical window start position 2 LSB
04	COMB	02	RW	Common Control B Bit[7:3]: Reserved Bit[2:0]: Exposure Control (EC) lower 3 bits – EC[2:0]
05	BAVG	00	RW	B Channel Average
06	GbAVG	00	RW	G Channel Average - Picked G pixels in the same line with B pixels.
07	GrAVG	00	RW	G Channel Average - Picked G pixels in the same line with R pixels.
08	RAVG	00	RW	R Channel Average
09	COMC	01	RW	Common Control C Bit[7:5]: Reserved Bit[4]: Sleep mode enable 0: Normal mode 1: Sleep mode Bit[3:2]: Reserved Bit[1:0]: Output Drive Select 00: Weakest 01: Double capability 10: Double capability 11: Triple drive current
0A	PIDH	66	R	Product ID Number MSB (Read only)
0B	PIDL	28	R	Product ID Number LSB (Read only)
0C	COMD	28	RW	Common Control D Bit[7:2]: Reserved Bit[1]: Sensor precharge voltage selection 0: Selects internal reference as precharge voltage 1: Selects SVDD as precharge voltage Bit[0]: Snapshot option 0: Enable live video output after snapshot sequence 1: Output single frame only

Table 10 Device Control Register List (Sheet 2 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0D-0F	RSVD	XX	–	Reserved
10	EC	26	RW	Exposure Control (EC) Most Significant 8 bits for EC[10:3] (least significant 3 bits in register COMB[2:0] - see "COMB" on page 12). Bit[10:0]: Exposure time $T_{EX} = t_{LINE}$ x EC[10:0]
11	CLKRC	00	RW	Clock Rate Control Bit[7]: Internal PLL ON/OFF selection 0: PLL disabled 1: PLL enabled Bit[6]: Reserved Bit[5:0]: Clock divider CLK = XCLK1/(decimal value of CLKRC[5:0] + 1)
12	COMH	00	RW	Common Control H Bit[7]: SRST 1: Initiates soft reset. All register are set to factory default values after which the chip resumes normal operation Bit[6]: Reserved Bit[5]: Resolution selection 0: CIF 1: QCIF Bit[4:2]: Reserved Bit[1]: Color bar test pattern 0: OFF 1: ON Bit[0]: Reserved
13	RSVD	XX	–	Reserved
14	COMJ	76	RW	Common Control J Bit[7:3]: Reserved Bit[2]: VSYNC drop option 0: Disabled 1: Enabled Bit[1]: Frame data drop option 0: Disable data drop 1: Drop data frame if exposure is not within tolerance. In EC mode, data is normally dropped when data is out of range. Bit[0]: Freeze current Exposure and Gain values 0: Normal 1: Freeze

Table 10 Device Control Register List (Sheet 3 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
15	COMK	00	RW	Common Control K Bit[7]: CHSYNC pin output swap 0: CHSYNC 1: HREF Bit[6]: HREF pin output swap 0: HREF 1: CHSYNC Bit[5]: PCLK output selection 0: PCLK always output 1: PCLK output qualified by HREF Bit[4]: PCLK edge selection 0: Data valid on PCLK falling edge 1: Data valid on PCLK rising edge Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for data valid Bit[2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: HSYNC polarity 0: Positive 1: Negative
16	RSVD	XX	–	Reserved
17	HSTRT	11	RW	Horizontal Window line start most significant 8 bits, 3 LSB in COMM register (see "COMM" on page 15). Bit[10:0]: Selects the start of the horizontal window, each LSB represents one tp. ***Note:*** *HSTRT[10:0] should be less than HEND[10:0].*
18	HEND	61	RW	Horizontal Window line end most significant 8 bits, 3 LSB in COMM register (see "COMM" on page 15). Bit[10:0]: Selects the end of the horizontal window, each LSB represents one tp. ***Note:*** *HEND[10:0] should be larger than HSTRT[10:0].*
19	VSTRT	01	RW	Vertical Window line start most significant 8 bits, 2 LSB in COMA register (see "COMA" on page 12). Bit[9:0]: Selects the start of the vertical window, each LSB represents two scan lines in CIF or two scan lines in QCIF. ***Note:*** *VSTRT[9:0] should be less than VEND[9:0].*

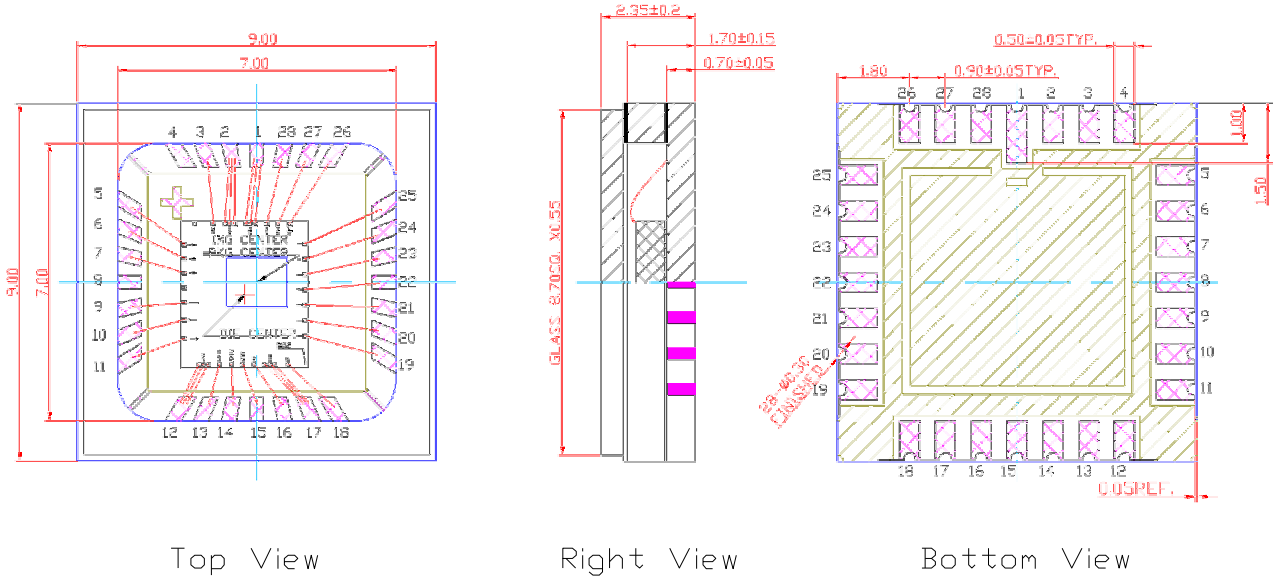
Table 10 Device Control Register List (Sheet 4 of 4)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
1A	VEND	3D	RW	Vertical Window line end most significant 8 bits, 2 LSB in COMA register (see "COMA" on page 12). Bit[9:0]: Selects the end of the vertical window, each LSB represents two scan lines in CIF and two scan lines in QCIF. ***Note:*** *VEND[9:0] should be larger than VSTRT[9:0]. The adjustment range for the vertical window size is from [01] to [12F].*
1B-29	RSVD	XX	–	Reserved
2A	COML	00	RW	Common Control L Bit[7:4]: Line interval adjust value MSB 4 bits Bit[3:2]: HSYNC timing end point adjustment MSB 2 bits Bit[1:0]: HSYNC timing start point adjustment MSB 2 bits
2B	FRARL	00	RW	Line Interval Adjustment Value LSB 8 bits The frame rate will be adjusted by changing the line interval. Each LSB will add 1/594 T_{frame} in CIF and 1/594 T_{frame} in QCIF mode.
2C	RSVD	XX	–	Reserved
2D	ADDVSL	00	RW	VSYNC Pulse Width LSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each LSB count will add 1 x t_{line} to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse width MSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each MSB count will add 256 x t_{line} to the VSYNC active period.
2F	YAVG	00	RW	Luminance Average Average Luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0])/4
30	HSDY	08	RW	HSYNC position and width start point LSB 8 bits This register and COML[1:0] define the HSYNC start position. Each LSB will shift the HSYNC start point by 1 pixel period.
31	HEDY	30	RW	HSYNC position and width end lower 8 bits This register and COML[3:2] define the HSYNC end position. Each LSB will shift the HSYNC end by 1 pixel period.
32	COMM	2D	RW	Common Control M Bit[7]: Reserved Bit[5:3]: Horizontal window end position 3 LSBs Bit[2:0]: Horizontal window start position 3 LSBs
33-47	RSVD	XX	–	Reserved
NOTE:				

Package Specifications

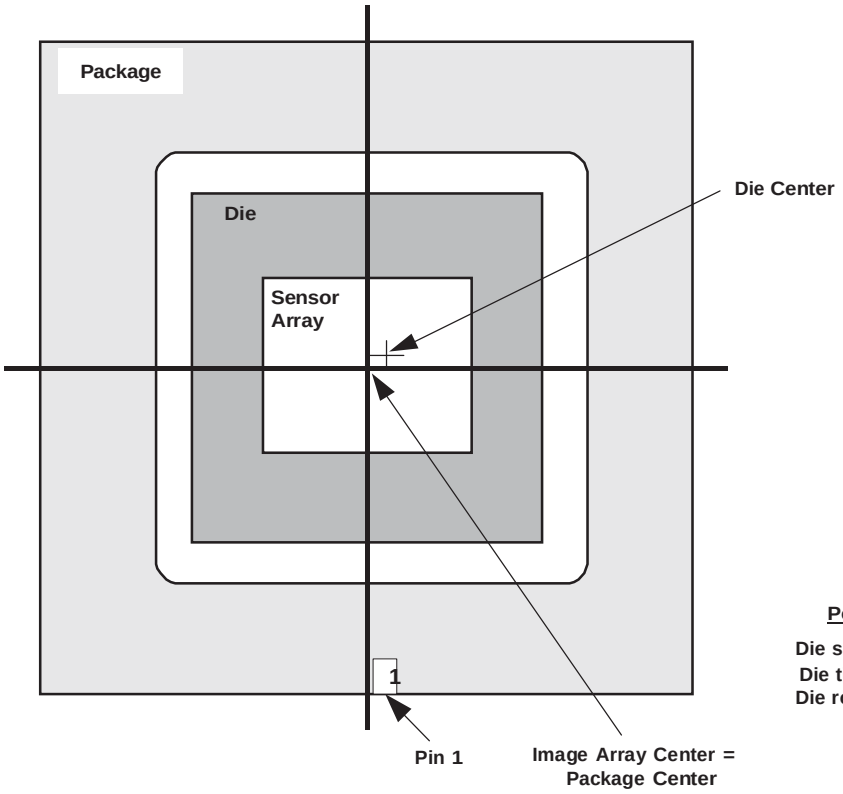
A uses a 28-pin FR5 package (PLCC). Refer to Figure 12 for package information and Figure 13 for the array center on the chip.

Figure 12 A Package Specifications



Sensor Array Center

A Sensor Array Center



Positional Tolerances

Die shift (x,y) = 0.15 mm (6 mils) max.
Die tilt = 1 degrees max.
Die rotation = 3 degrees max.

Important: Most optical systems invert and mirror the image so the chip is usually mounted on the board with pin 1 (AGND) down as shown.

NOTE: Picture is for reference only, not to scale.