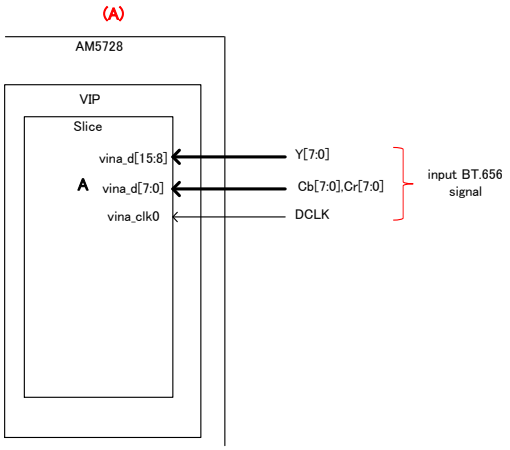
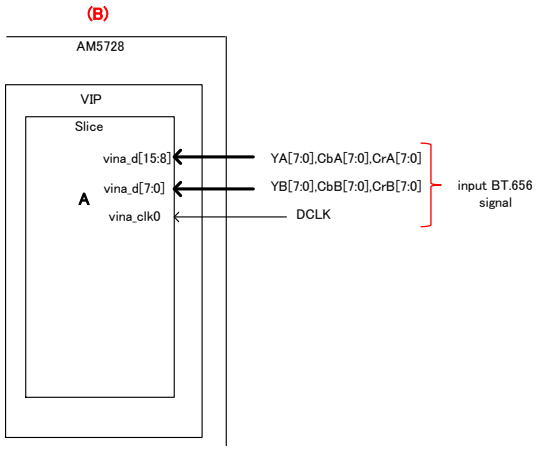
Table 9-13. Multiplexing Configurations and Pixel Clock Rates

	Maximum Channels in Single 16-bit Data Interface Mode (A)	Maximum Channels in Dual 8-bit Data Interface Mode - Interleaved Channels per Single 8-bit Port. One 16-bit VIP can be configured to support two such 8-bit ports. (B)	Interface Clock Rate (MHz)
HD Interlaced	2	1	148.5
D1 Interlaced	8	4	108.1
CIF Interlaced	n/a	n/a	n/a
HD Progressive	1	n/a	148.5
D1 Progressive	4	2	108.1
CIF Progressive (1)	32	16	162.2

(1) Blanking pixels are not used in the CIF clock rate calculations. Addition of blanking pixels would require a slightly higher clock rate.



Is this circut diagram(A) Single 16-bit Data Interface Mode?



Is this circut diagram(B) Dual 8-bit Data Interface Mode –Interleaved Channels per Single 8-bit Port? One 16-bit VIP can be configured to support two such 8-bit ports.