Testing 2xLTE60

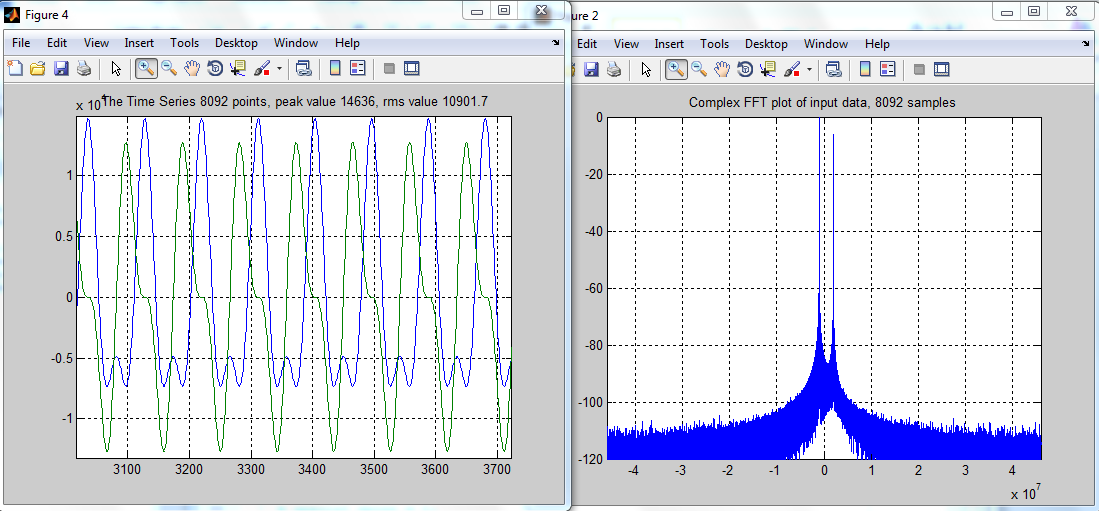
Using Playback code from Ben in NICE with Lamarr EVM Rev2, with FMC loopback card where Tx1 <->Tx2 cables are swapped.

Note: there is a distortion in loading and saving memory, that has not been fixed. For now, this is used to compare the data loaded into tx0Tab, tx1Tab, with the output rx0Tab, rx1Tab after the Capture Request expression is set to 1 in the playback code.

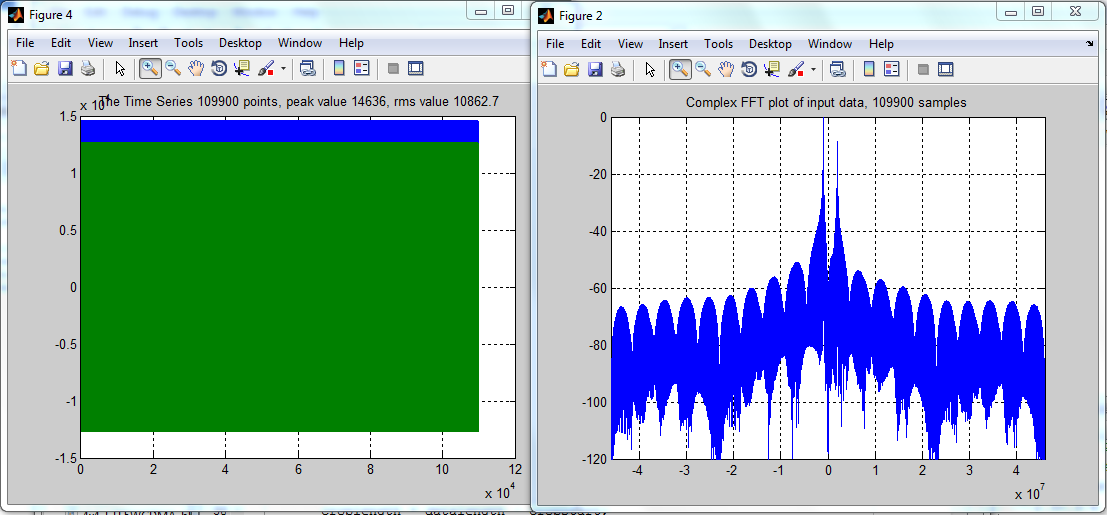
Noted problems:

1. The Rx IMBout test bus is not working yet, can’t get the Rx output signal (minor)
2. The BBRx output requires a special Q delay by 1, this requires post processing before using other complex accelerators in Lamarr. This is a DFE problem.
3. The distorted Tx loading into memory, then reading from memory, can either be a software formatting of another problem, still working on this (it may not be a big problem)
4. Some of the plots after Tx show decimation or resampling images, this will need to be checked with the spectrum analyzer for Tx problems. These show up below -75dbc on the simulation.
5. Eventually the BBRx gain or Rx and Feedback Gain may need to be adjusted for best signal level (minor – not a bug, a calibration step)

Software formatting of the BBTx data, here is the matlab output plotted, and then the output of the BBTx converter software:

Matlab plot, of two tone IQ file

Convert the Matlab file to a .dat, extract the first 5 lines, special 0x and L use matlab to convert .dat back to IQ. Not even loaded to DSP memory yet. I will work on fixing this next. It is a common python file that we used throughout AVV and DFE last year. Somehow its broken now.

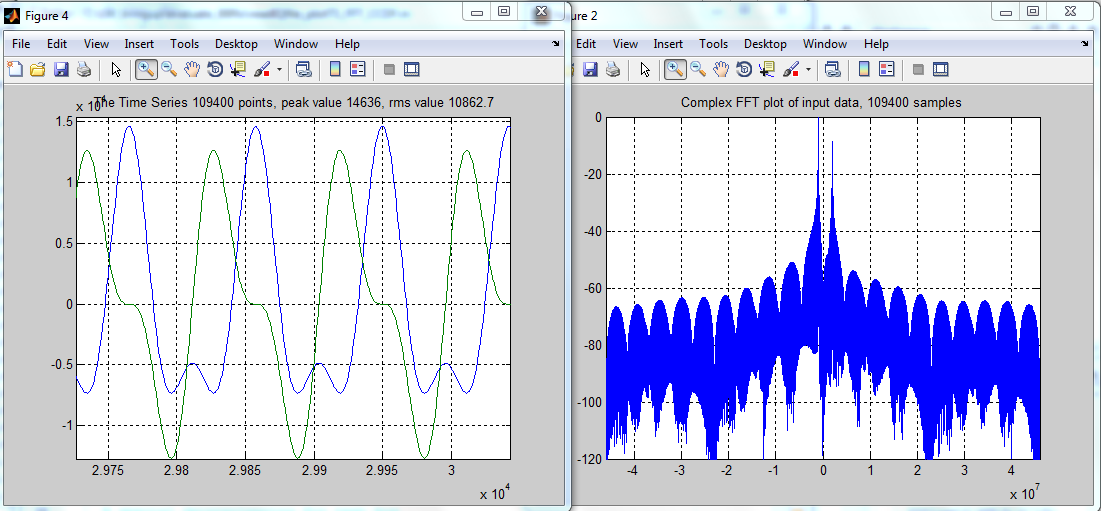


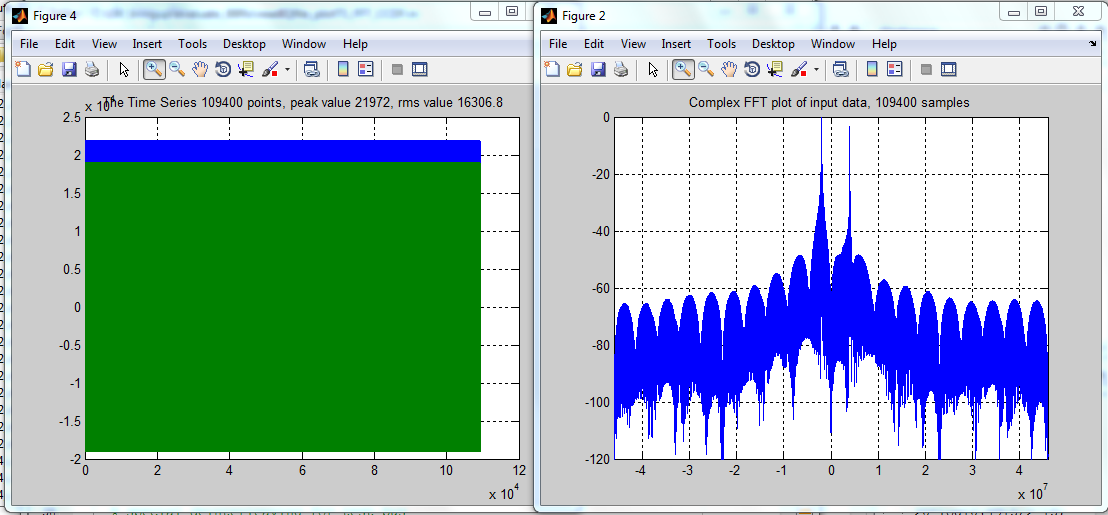
If we use the CCS tool and load the memory and then save it back to a file, we get the distorted waveform above. So its distorted BEFORE it gets to IQN.

Here are the test steps, given the distorted waveforms.

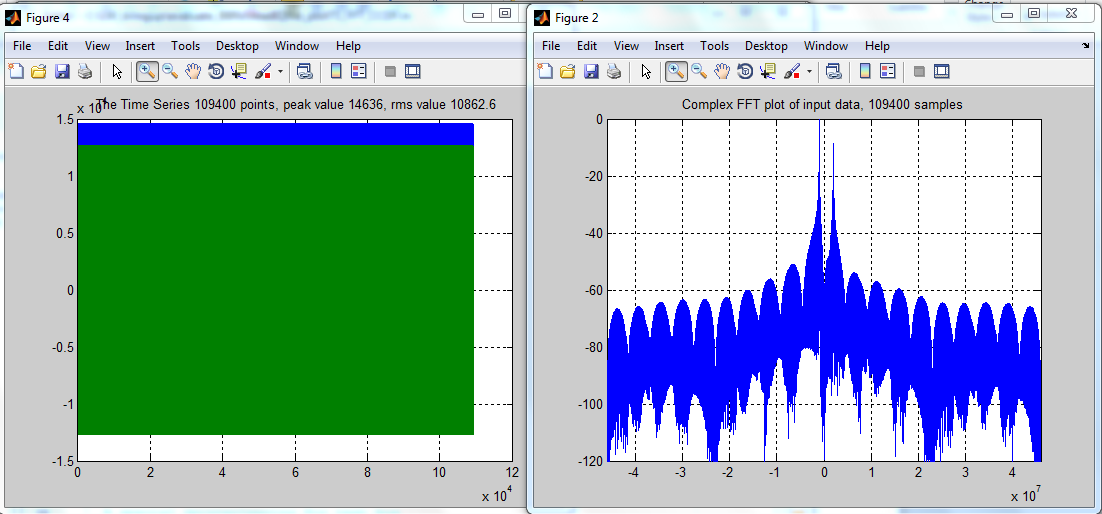
BUFlpbk – in this test there are 2 LTE60 92.16Msps complex carriers. The BBTx0 -> BBRx0, and BBTx1 -> BBRx1.

BBTx0, -2, 1Mhz sampled at 92.16 (saved tx0Tab back to file, and extracted .dat -> iq in matlab, and then plotted in matlab.)

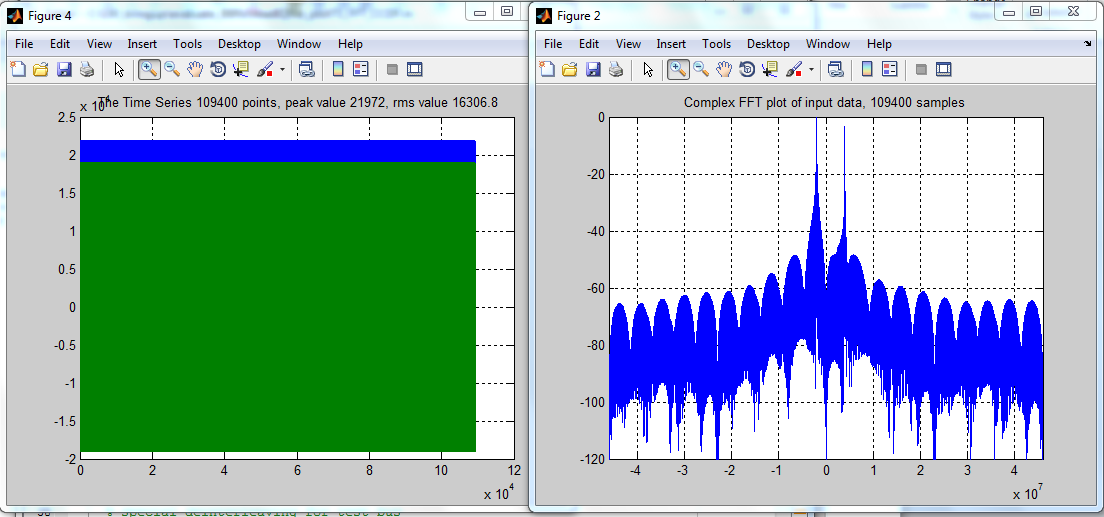


BBtx1, -4, 2Mhz sampled at 92.16Msps

BBrx0 -> loopback from BBTx0



BBrx1 -> loopback from BBTx1

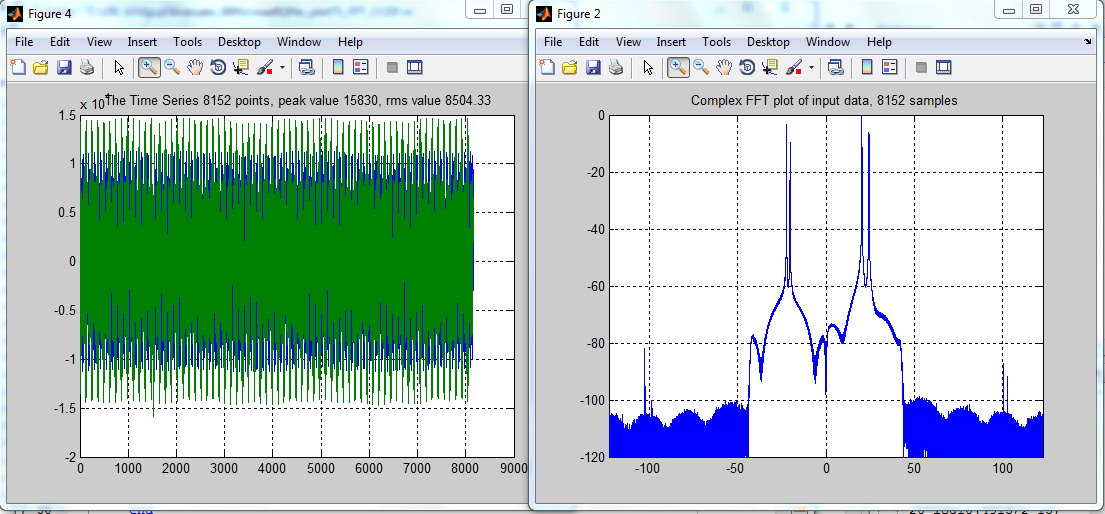


JESDlpk The next test, repeats a stream -> antenna loopback, in this case there is only 1 Tx and 1 Rx stream. The two carriers are mixed and summed, for the Tx. In the Rx the lower carrier is processed. In the Feedback the upper carrier is processed. The expected set of tone processing is expected, with the additional delaying of the Q samples by 1.

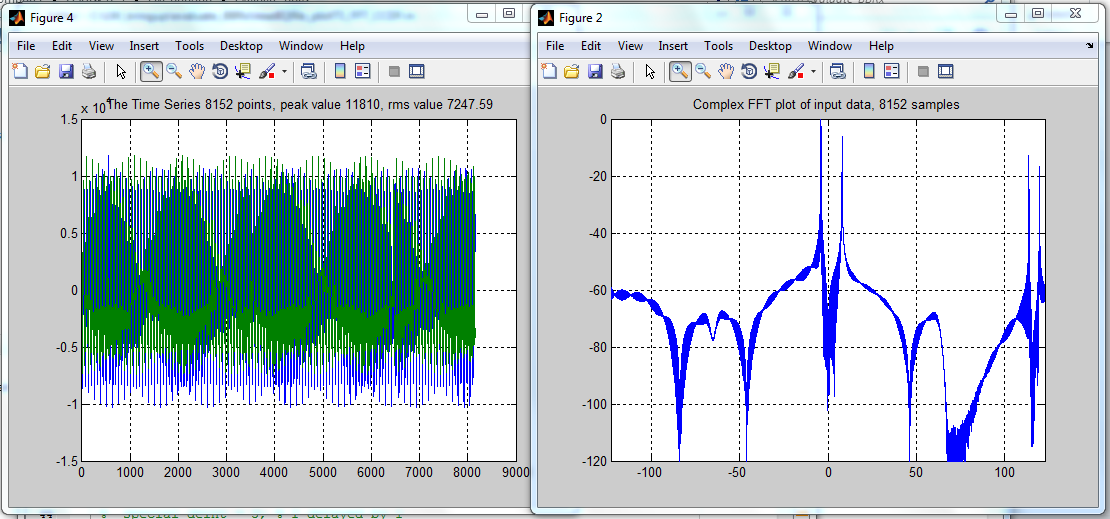
The BBTx is the same set of 2 tone data as the BUFlpbk test.

Some additional plots are taken using the DFE2.gel script.

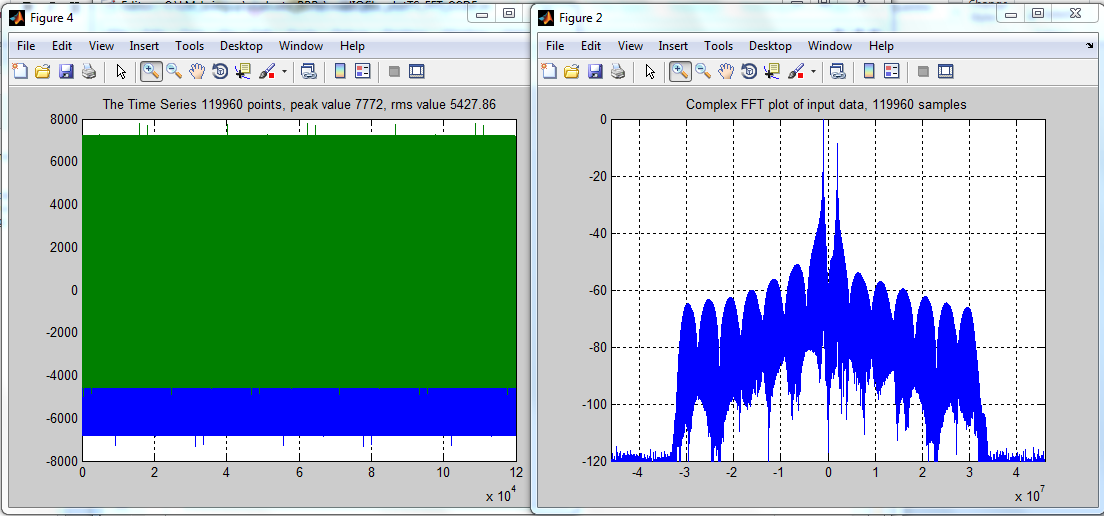
DIDin0 Capture Buffer 8K data, 245.76

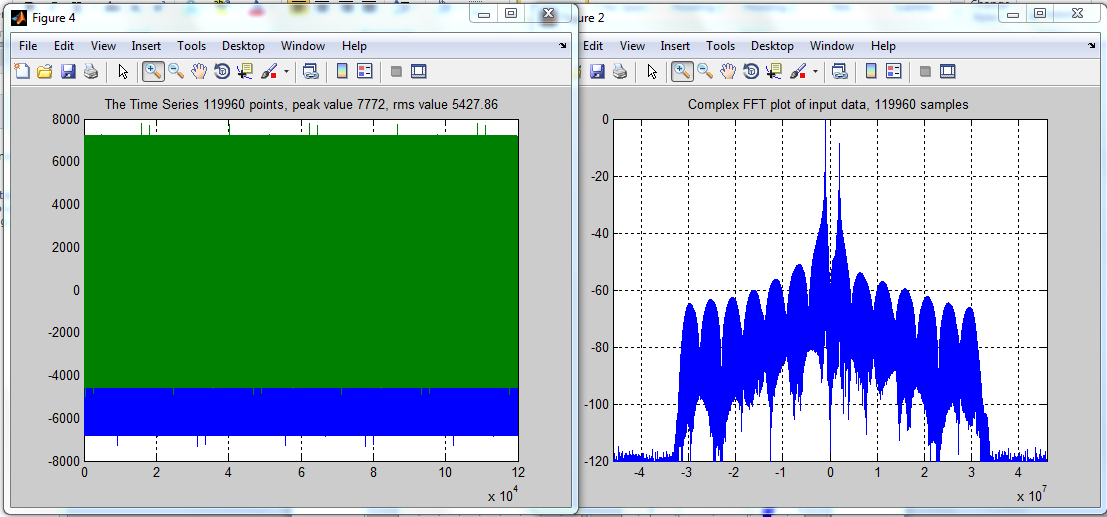


Fdbk NLM Capture Buffer 8K Rx (Upper carrier) 122.88



BBRx0 (lower carrier from Tx0), 92.16 – note: need to delay Q by 1 sample



BBrx1 (upper carrier from Tx1), 92.16 – note: need to delay Q by 1 sample

Nosync (Cable loopback) test - The next section is a cable loopback test, in this case, the difference is instead of the JESD lanes loopback we are using the Serdes, the FMC breakout card, and SMA cables. This does not test the actual ADC and DAC JESD and Synchronization, it is testing a serdes Tx to serdes Rx loopback (so the formats have to be the same).

BBTx0, BBTx1 are the same as discussed in the above tests.

DPDin is still the same as the above JESDlpbk test.

We use the DFE gel file to check the JESD status, noting that JESD Sync is bypassed.

C66xx\_1: GEL Output: ==============

C66xx\_1: GEL Output: JESD\_Check\_All

C66xx\_1: GEL Output: ==============

C66xx\_1: GEL Output: JESDTX Lane 0 enabled, assigned to TX Link 0

C66xx\_1: GEL Output: JESDTX Lane 1 enabled, assigned to TX Link 0

C66xx\_1: GEL Output: JESDRX Lane 0 enabled, assigned to RX Link 0

C66xx\_1: GEL Output: JESDRX Lane 1 enabled, assigned to RX Link 0

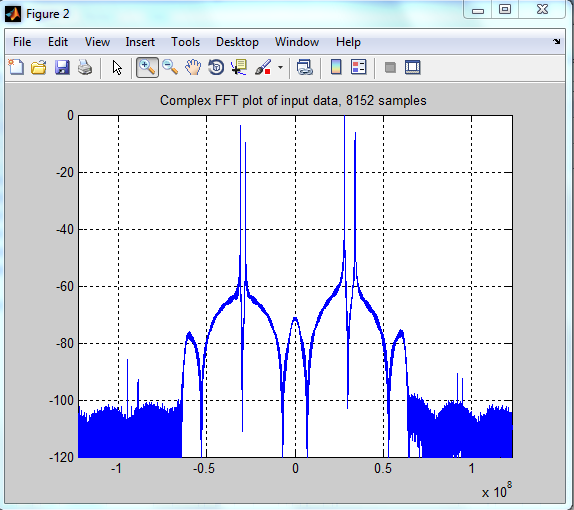
C66xx\_1: GEL Output: JESDTX has no errors.

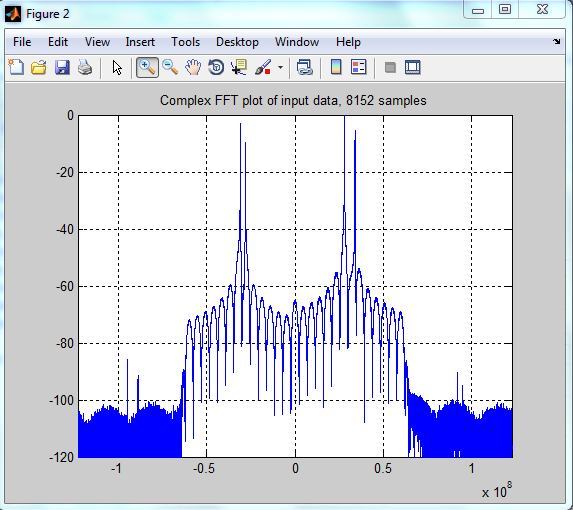
C66xx\_1: GEL Output: JESDRX has no errors.

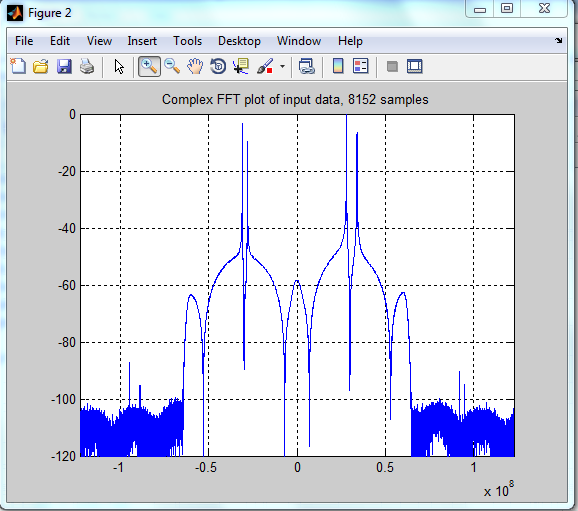
C66xx\_1: GEL Output: INFO: JESDRX Link 0 has a skew of 0 between the earliest and latest lanes.

We can check that the JESD Tx is connected to JESD Rx0 and JESD FdbkA through the test bus connections.

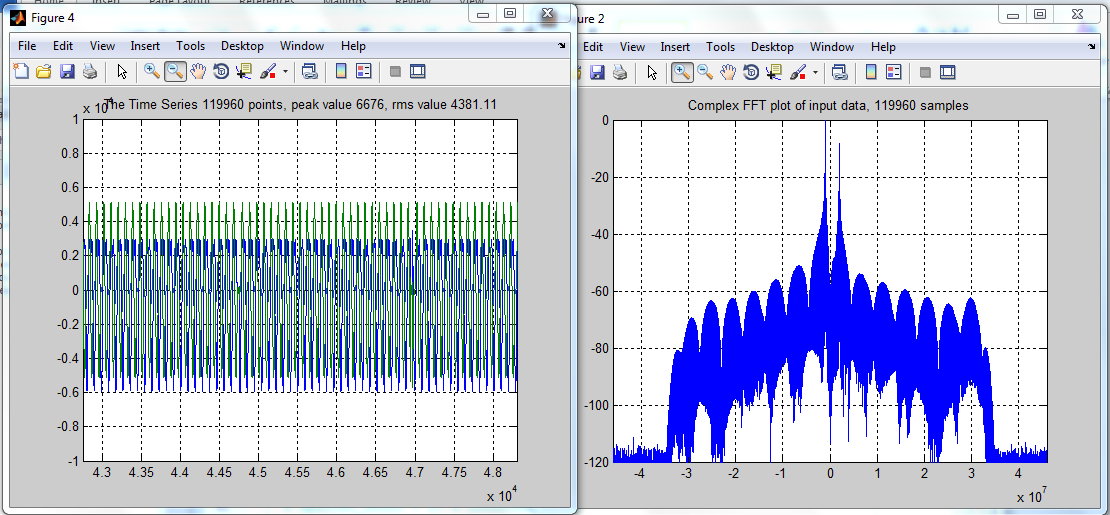
Test Bus JESD Tx0 map (this can be 1 or 2 streams interleaved this is 1 stream/antenna), note the Tx resample images. This may change the configuration, to use a higher DPD rate, to not run into the 40% bandwidth of the resamplers. Currently we resample 2/1. Dec2, 245.76in 245.76 out.



Test Bus JESD Rx map (interleaved 1-2-4, however this is 1 stream/antenna) – should look just like JESD Tx because this is still a digital loopback.

FdbkA test bus

The Rx block downconverts the lower carrier, the Feedback downconverts the upper carrier. This is done to provide 2 wideband Rx paths to the Rx DDUC (channel/antenna container/carrier) processing.

The BBRx0 output should be the lower 2 tone signal. 

The BBRx1 output should be the upper 2 tone signal.

