

DSP RM/CM/DM Decode

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4:19 PM

Search terms: DSPx_PM
CM_DSP
RM_DSP
EMU

Notes:
- DSP2 off all around
- DSP1 mostly off, one reset done
- Set power domains (DSP1, EMU) ON, give SW_WAKE to clock domains, enable module modes, remove reset

Core Registers (Cortex-A15MPCore)

PRCM

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CM_CORE_AON_MPU
CM_MPU_CLKSTCTRL 00000103 CLKACTIVITY_MPU_GCLK ACT CLKTRCTRL HW_AUTO
CM_MPU_STATICDEP 00000010 PCIE_STATDEP DISABLED VPE_STATDEP DISABLED L4PER3_STATDEP DISABLED
L4PER2_STATDEP DISABLED GMAC_STATDEP DISABLED IPU_STATDEP DISABLED
IPU1_STATDEP DISABLED EVE2_STATDEP DISABLED EVE1_STATDEP DISABLED
DSP2_STATDEP DISABLED CUSTEFUSE_STATDEP DISABLED COREAON_STATDEP DISABLED
WKUPAON_STATDEP DISABLED L4SEC_STATDEP DISABLED L4PER_STATDEP DISABLED
L4CFG_STATDEP DISABLED SDMA_STATDEP DISABLED GPU_STATDEP DISABLED
CAM_STATDEP DISABLED DSS_STATDEP DISABLED L3INIT_STATDEP DISABLED
L3MAIN1_STATDEP DISABLED EMIF_STATDEP ENABLED IVA_STATDEP DISABLED
DSP1_STATDEP DISABLED IPU2_STATDEP DISABLED
CM_MPU_DYNAMICDEP 04000030 WINDOWSIZE 4 L3MAIN1_DYNDEP ENABLED EMIF_DYNDEP ENABLED
CM_MPU_MPU_CLKCTRL 01000001 CLKSEL_ABE_DIV_MODE DIV8 CLKSEL_EMIF_DIV_MODE DIV4 STBYST FUNC
IDLEST FUNC MODULEMODE AUTO
CM_MPU_MPU_MPU_DBG_CLKCTRL 00000001 IDLEST FUNC MODULEMODE AUTO
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DSP2_PRM

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PM_DSP2_PWRSTCTRL 003F0000 DSP2_EDMA_ONSTATE MEM_ON DSP2_L2_ONSTATE MEM_ON DSP2_L1_ONSTATE MEM_ON
LOWPOWERSTATECHANGE DIS POWERSTATE OFF
PM_DSP2_PWRSTST 00000000 LASTPOWERSTATEENTERED OFF INTRANSITION NO DSP2_EDMA_STATEST MEM_OFF
DSP2_L2_STATEST MEM_OFF DSP2_L1_STATEST MEM_OFF LOGICSTATEST OFF
POWERSTATEST OFF
RM_DSP2_RSTCTRL 00000003 RST_DSP2 ASSERT RST_DSP2_LRST ASSERT
RM_DSP2_RSTST 0000000B RST_DSP2_EMU_REQ RESET_YES RST_DSP2_EMU RESET_NO RST_DSP2 RESET_YES
RST_DSP2_LRST RESET_YES
RM_DSP2_DSP2_CONTEXT 00000701 LOSTMEM_DSP_EDMA LOST LOSTMEM_DSP_L2 LOST LOSTMEM_DSP_L1 LOST
LOSTCONTEXT_DFF LOST
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WKUPAON_PRM

```
RM_WKUPAON_L4_WKUP_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_WKUPAON_WD_TIMER2_WKDEP 00000000 WKUPDEP_WD_TIMER2_EVE2 DISABLED WKUPDEP_WD_TIMER2_EVE1 DISABLED WKUPDEP_WD_TIMER2_DSP2 DISABLED
WKUPDEP_WD_TIMER2_IPU1 DISABLED WKUPDEP_WD_TIMER2_DSP1 DISABLED WKUPDEP_WD_TIMER2_IPU2 DISABLED
WKUPDEP_WD_TIMER2_MPU DISABLED
RM_WKUPAON_WD_TIMER2_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_WKUPAON_GPIO1_WKDEP 00000000 WKUPDEP_GPIO1_IRQ2_EVE2 DISABLED WKUPDEP_GPIO1_IRQ2_EVE1 DISABLED WKUPDEP_GPIO1_IRQ2_DSP2 DISABLED
WKUPDEP_GPIO1_IRQ2_IPU1 DISABLED WKUPDEP_GPIO1_IRQ2_DSP1 DISABLED WKUPDEP_GPIO1_IRQ2_IPU2 DISABLED
WKUPDEP_GPIO1_IRQ2_MPU DISABLED WKUPDEP_GPIO1_IRQ1_EVE2 DISABLED WKUPDEP_GPIO1_IRQ1_EVE1 DISABLED
WKUPDEP_GPIO1_IRQ1_DSP2 DISABLED WKUPDEP_GPIO1_IRQ1_IPU1 DISABLED WKUPDEP_GPIO1_IRQ1_DSP1 DISABLED
WKUPDEP_GPIO1_IRQ1_IPU2 DISABLED WKUPDEP_GPIO1_IRQ1_MPU DISABLED
RM_WKUPAON_GPIO1_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_WKUPAON_TIMER1_WKDEP 00000000 WKUPDEP_TIMER1_EVE2 DISABLED WKUPDEP_TIMER1_EVE1 DISABLED WKUPDEP_TIMER1_DSP2 DISABLED
WKUPDEP_TIMER1_IPU1 DISABLED WKUPDEP_TIMER1_DSP1 DISABLED WKUPDEP_TIMER1_IPU2 DISABLED
WKUPDEP_TIMER1_MPU DISABLED
RM_WKUPAON_TIMER1_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_WKUPAON_TIMER12_WKDEP 00000000 WKUPDEP_TIMER12_EVE2 DISABLED WKUPDEP_TIMER12_EVE1 DISABLED WKUPDEP_TIMER12_DSP2 DISABLED
WKUPDEP_TIMER12_IPU1 DISABLED WKUPDEP_TIMER12_DSP1 DISABLED WKUPDEP_TIMER12_IPU2 DISABLED
WKUPDEP_TIMER12_MPU DISABLED
RM_WKUPAON_TIMER12_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_WKUPAON_COUNTER_32K_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
RM_WKUPAON_KBD_WKDEP 00000000 WKUPDEP_KBD_EVE2 DISABLED WKUPDEP_KBD_EVE1 DISABLED WKUPDEP_KBD_DSP2 DISABLED
WKUPDEP_KBD_IPU1 DISABLED WKUPDEP_KBD_DSP1 DISABLED WKUPDEP_KBD_IPU2 DISABLED
WKUPDEP_KBD_MPU DISABLED
RM_WKUPAON_KBD_CONTEXT 00000001 LOSTCONTEXT_DFF LOST
PM_WKUPAON_UART10_WKDEP 00000000 WKUPDEP_UART10_EVE2 DISABLED WKUPDEP_UART10_EVE1 DISABLED WKUPDEP_UART10_DSP2 DISABLED
WKUPDEP_UART10_IPU1 DISABLED WKUPDEP_UART10_SDMA DISABLED WKUPDEP_UART10_DSP1 DISABLED
WKUPDEP_UART10_IPU2 DISABLED WKUPDEP_UART10_MPU DISABLED
RM_WKUPAON_UART10_CONTEXT 00000000 LOSTMEM_RETAINED_BANK MAINTAINED LOSTCONTEXT_DFF MAINTAINED
PM_WKUPAON_DCAN1_WKDEP 00000000 WKUPDEP_DCAN1_EVE2 DISABLED WKUPDEP_DCAN1_EVE1 DISABLED WKUPDEP_DCAN1_DSP2 DISABLED
WKUPDEP_DCAN1_IPU1 DISABLED WKUPDEP_DCAN1_SDMA DISABLED WKUPDEP_DCAN1_DSP1 DISABLED
WKUPDEP_DCAN1_IPU2 DISABLED WKUPDEP_DCAN1_MPU DISABLED
RM_WKUPAON_DCAN1_CONTEXT 00000000 LOSTMEM_DCAN_MEM MAINTAINED LOSTCONTEXT_DFF MAINTAINED
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OCP_SOCKET_PRM

```
REVISION_PRM 40000301 SCHEME H08 FUNC 0000 R_RTL 0
X_MAJOR OMAP5430 CUSTOM STANDARD Y_MINOR ES2
PRM_IRQSTATUS_MPU 00000100 ABB_IVA_DONE_ST IRQ_FAL ABB_DSPEVE_DONE_ST IRQ_FAL ABB_GPU_DONE_ST IRQ_FAL
DPLL_EVE_RECAL_ST IRQ_FAL DPLL_DSP_RECAL_ST IRQ_FAL IO_ST IRQ_FAL
TRANSITION_ST IRQ_TRU DPLL_DDR_RECAL_ST IRQ_FAL DPLL_GPU_RECAL_ST IRQ_FAL
DPLL_GMAC_RECAL_ST IRQ_FAL DPLL_ABE_RECAL_ST IRQ_FAL DPLL_PER_RECAL_ST IRQ_FAL
DPLL_IVA_RECAL_ST IRQ_FAL DPLL_MPU_RECAL_ST IRQ_FAL DPLL_CORE_RECAL_ST IRQ_FAL
PRM_IRQSTATUS_MPU_2 00000000 ABB_MPU_DONE_ST IRQ_FAL
PRM_IRQENABLE_MPU 00000200 ABB_IVA_DONE_EN IRQ_FAL ABB_DSPEVE_DONE_EN IRQ_FAL ABB_GPU_DONE_EN IRQ_FAL
DPLL_EVE_RECAL_EN IRQ_MSK DPLL_DSP_RECAL_EN IRQ_MSK IO_EN IRQ_EN
TRANSITION_EN IRQ_MSK DPLL_DDR_RECAL_EN IRQ_MSK DPLL_GPU_RECAL_EN IRQ_MSK
DPLL_GMAC_RECAL_EN IRQ_MSK DPLL_ABE_RECAL_EN IRQ_MSK DPLL_PER_RECAL_EN IRQ_MSK
DPLL_IVA_RECAL_EN IRQ_MSK DPLL_MPU_RECAL_EN IRQ_MSK DPLL_CORE_RECAL_EN IRQ_MSK
PRM_IRQENABLE_MPU_2 00000000 ABB_MPU_DONE_EN IRQ_FAL
PRM_IRQSTATUS_IPU2 F0000500 ABB_MPU_DONE_ST IRQ_TRU ABB_IVA_DONE_ST IRQ_TRU ABB_DSPEVE_DONE_ST IRQ_TRU
ABB_GPU_DONE_ST IRQ_TRU DPLL_EVE_RECAL_ST IRQ_FAL DPLL_DSP_RECAL_ST IRQ_FAL
FORCEWKUP_ST IRQ_TRU IO_ST IRQ_FAL TRANSITION_ST IRQ_TRU
DPLL_DDR_RECAL_ST IRQ_FAL DPLL_GPU_RECAL_ST IRQ_FAL DPLL_GMAC_RECAL_ST IRQ_FAL
DPLL_ABE_RECAL_ST IRQ_FAL DPLL_PER_RECAL_ST IRQ_FAL DPLL_IVA_RECAL_ST IRQ_FAL
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DPLL_MPU_RECAL_ST IRQ_FAL DPLL_CORE_RECAL_ST IRQ_FAL
PRM_IRQENABLE_IPU2 00000000 ABB_MPU_DONE_EN IRQ_FAL ABB_IVA_DONE_EN IRQ_FAL ABB_DSPEVE_DONE_EN IRQ_FAL
ABB_GPU_DONE_EN IRQ_FAL DPLL_EVE_RECAL_EN IRQ_MSK DPLL_DSP_RECAL_EN IRQ_MSK
FORCEWKUP_EN IRQ_MSK IO_EN IRQ_MSK TRANSITION_EN IRQ_MSK
DPLL_DDR_RECAL_EN IRQ_MSK DPLL_GPU_RECAL_EN IRQ_MSK DPLL_GMAC_RECAL_EN IRQ_MSK
DPLL_ABE_RECAL_EN IRQ_MSK DPLL_PER_RECAL_EN IRQ_MSK DPLL_IVA_RECAL_EN IRQ_MSK
DPLL_MPU_RECAL_EN IRQ_MSK DPLL_CORE_RECAL_EN IRQ_MSK
PRM_IRQSTATUS_DSP1 F0000400 ABB_MPU_DONE_ST IRQ_TRU ABB_IVA_DONE_ST IRQ_TRU ABB_DSPEVE_DONE_ST IRQ_TRU
ABB_GPU_DONE_ST IRQ_TRU DPLL_EVE_RECAL_ST IRQ_FAL DPLL_DSP_RECAL_ST IRQ_FAL
FORCEWKUP_ST IRQ_TRU IO_ST IRQ_FAL DPLL_DDR_RECAL_ST IRQ_FAL
DPLL_GPU_RECAL_ST IRQ_FAL DPLL_GMAC_RECAL_ST IRQ_FAL DPLL_ABE_RECAL_ST IRQ_FAL
DPLL_PER_RECAL_ST IRQ_FAL DPLL_IVA_RECAL_ST IRQ_FAL DPLL_MPU_RECAL_ST IRQ_FAL
DPLL_CORE_RECAL_ST IRQ_FAL
PRM_IRQENABLE_DSP1 00000000 ABB_MPU_DONE_EN IRQ_FAL ABB_IVA_DONE_EN IRQ_FAL ABB_DSPEVE_DONE_EN IRQ_FAL
ABB_GPU_DONE_EN IRQ_FAL DPLL_USB_RECAL_EN IRQ_MSK DPLL_EVE_RECAL_EN IRQ_MSK
DPLL_DSP_RECAL_EN IRQ_MSK FORCEWKUP_EN IRQ_MSK IO_EN IRQ_MSK
DPLL_DDR_RECAL_EN IRQ_MSK DPLL_GPU_RECAL_EN IRQ_MSK DPLL_GMAC_RECAL_EN IRQ_MSK
DPLL_ABE_RECAL_EN IRQ_MSK DPLL_PER_RECAL_EN IRQ_MSK DPLL_IVA_RECAL_EN IRQ_MSK
DPLL_MPU_RECAL_EN IRQ_MSK DPLL_CORE_RECAL_EN IRQ_MSK
CM_PRM_PROFILING_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
PRM_IRQENABLE_DSP2 00000000 ABB_MPU_DONE_EN IRQ_FAL ABB_IVA_DONE_EN IRQ_FAL ABB_DSPEVE_DONE_EN IRQ_FAL
ABB_GPU_DONE_EN IRQ_FAL DPLL_EVE_RECAL_EN IRQ_MSK DPLL_DSP_RECAL_EN IRQ_MSK
FORCEWKUP_EN IRQ_MSK IO_EN IRQ_MSK DPLL_DDR_RECAL_EN IRQ_MSK
DPLL_GPU_RECAL_EN IRQ_MSK DPLL_GMAC_RECAL_EN IRQ_MSK DPLL_ABE_RECAL_EN IRQ_MSK
DPLL_PER_RECAL_EN IRQ_MSK DPLL_IVA_RECAL_EN IRQ_MSK DPLL_MPU_RECAL_EN IRQ_MSK
DPLL_CORE_RECAL_EN IRQ_MSK
PRM_IRQENABLE_EVE1 00000000 ABB_MPU_DONE_EN IRQ_FAL ABB_IVA_DONE_EN IRQ_FAL ABB_DSPEVE_DONE_EN IRQ_FAL
ABB_GPU_DONE_EN IRQ_FAL DPLL_EVE_RECAL_EN IRQ_MSK DPLL_DSP_RECAL_EN IRQ_MSK
FORCEWKUP_EN IRQ_MSK IO_EN IRQ_MSK DPLL_DDR_RECAL_EN IRQ_MSK
DPLL_GPU_RECAL_EN IRQ_MSK DPLL_GMAC_RECAL_EN IRQ_MSK DPLL_ABE_RECAL_EN IRQ_MSK
DPLL_PER_RECAL_EN IRQ_MSK DPLL_IVA_RECAL_EN IRQ_MSK DPLL_MPU_RECAL_EN IRQ_MSK
DPLL_CORE_RECAL_EN IRQ_MSK
PRM_IRQENABLE_EVE2 00000000 ABB_MPU_DONE_EN IRQ_FAL ABB_IVA_DONE_EN IRQ_FAL ABB_DSPEVE_DONE_EN IRQ_FAL
ABB_GPU_DONE_EN IRQ_FAL DPLL_EVE_RECAL_EN IRQ_MSK DPLL_DSP_RECAL_EN IRQ_MSK
FORCEWKUP_EN IRQ_MSK IO_EN IRQ_MSK DPLL_DDR_RECAL_EN IRQ_MSK
DPLL_GPU_RECAL_EN IRQ_MSK DPLL_GMAC_RECAL_EN IRQ_MSK DPLL_ABE_RECAL_EN IRQ_MSK
DPLL_PER_RECAL_EN IRQ_MSK DPLL_IVA_RECAL_EN IRQ_MSK DPLL_MPU_RECAL_EN IRQ_MSK
DPLL_CORE_RECAL_EN IRQ_MSK
PRM_IRQENABLE_IPU1 00000000 ABB_MPU_DONE_EN IRQ_FAL ABB_IVA_DONE_EN IRQ_FAL ABB_DSPEVE_DONE_EN IRQ_FAL
ABB_GPU_DONE_EN IRQ_FAL DPLL_EVE_RECAL_EN IRQ_MSK DPLL_DSP_RECAL_EN IRQ_MSK
FORCEWKUP_EN IRQ_MSK IO_EN IRQ_MSK TRANSITION_EN IRQ_MSK
DPLL_DDR_RECAL_EN IRQ_MSK DPLL_GPU_RECAL_EN IRQ_MSK DPLL_GMAC_RECAL_EN IRQ_MSK
DPLL_ABE_RECAL_EN IRQ_MSK DPLL_PER_RECAL_EN IRQ_MSK DPLL_IVA_RECAL_EN IRQ_MSK
DPLL_MPU_RECAL_EN IRQ_MSK DPLL_CORE_RECAL_EN IRQ_MSK
PRM_IRQSTATUS_DSP2 F0000400 ABB_MPU_DONE_ST IRQ_TRU ABB_IVA_DONE_ST IRQ_TRU ABB_DSPEVE_DONE_ST IRQ_TRU
ABB_GPU_DONE_ST IRQ_TRU DPLL_EVE_RECAL_ST IRQ_FAL DPLL_DSP_RECAL_ST IRQ_FAL
FORCEWKUP_ST IRQ_TRU IO_ST IRQ_FAL DPLL_DDR_RECAL_ST IRQ_FAL
DPLL_GPU_RECAL_ST IRQ_FAL DPLL_GMAC_RECAL_ST IRQ_FAL DPLL_ABE_RECAL_ST IRQ_FAL
DPLL_PER_RECAL_ST IRQ_FAL DPLL_IVA_RECAL_ST IRQ_FAL DPLL_MPU_RECAL_ST IRQ_FAL
DPLL_CORE_RECAL_ST IRQ_FAL
PRM_IRQSTATUS_EVE1 F0000400 ABB_MPU_DONE_ST IRQ_TRU ABB_IVA_DONE_ST IRQ_TRU ABB_DSPEVE_DONE_ST IRQ_TRU
ABB_GPU_DONE_ST IRQ_TRU DPLL_EVE_RECAL_ST IRQ_FAL DPLL_DSP_RECAL_ST IRQ_FAL
FORCEWKUP_ST IRQ_TRU IO_ST IRQ_FAL DPLL_DDR_RECAL_ST IRQ_FAL
DPLL_GPU_RECAL_ST IRQ_FAL DPLL_GMAC_RECAL_ST IRQ_FAL DPLL_ABE_RECAL_ST IRQ_FAL
DPLL_PER_RECAL_ST IRQ_FAL DPLL_IVA_RECAL_ST IRQ_FAL DPLL_MPU_RECAL_ST IRQ_FAL
DPLL_CORE_RECAL_ST IRQ_FAL
PRM_IRQSTATUS_EVE2 F0000400 ABB_MPU_DONE_ST IRQ_TRU ABB_IVA_DONE_ST IRQ_TRU ABB_DSPEVE_DONE_ST IRQ_TRU
ABB_GPU_DONE_ST IRQ_TRU DPLL_EVE_RECAL_ST IRQ_FAL DPLL_DSP_RECAL_ST IRQ_FAL
FORCEWKUP_ST IRQ_TRU IO_ST IRQ_FAL DPLL_DDR_RECAL_ST IRQ_FAL
DPLL_GPU_RECAL_ST IRQ_FAL DPLL_GMAC_RECAL_ST IRQ_FAL DPLL_ABE_RECAL_ST IRQ_FAL
DPLL_PER_RECAL_ST IRQ_FAL DPLL_IVA_RECAL_ST IRQ_FAL DPLL_MPU_RECAL_ST IRQ_FAL
DPLL_CORE_RECAL_ST IRQ_FAL
PRM_IRQSTATUS_IPU1 F0000500 ABB_MPU_DONE_ST IRQ_TRU ABB_IVA_DONE_ST IRQ_TRU ABB_DSPEVE_DONE_ST IRQ_TRU
ABB_GPU_DONE_ST IRQ_TRU DPLL_EVE_RECAL_ST IRQ_FAL DPLL_DSP_RECAL_ST IRQ_FAL
FORCEWKUP_ST IRQ_TRU IO_ST IRQ_FAL TRANSITION_ST IRQ_TRU
DPLL_DDR_RECAL_ST IRQ_FAL DPLL_GPU_RECAL_ST IRQ_FAL DPLL_GMAC_RECAL_ST IRQ_FAL
DPLL_ABE_RECAL_ST IRQ_FAL DPLL_PER_RECAL_ST IRQ_FAL DPLL_IVA_RECAL_ST IRQ_FAL
DPLL_MPU_RECAL_ST IRQ_FAL DPLL_CORE_RECAL_ST IRQ_FAL
PRM_DEBUG_CFG1 00000000 SEL1 0000
PRM_DEBUG_CFG2 00000000 SEL2 0000
PRM_DEBUG_CFG3 00000000 SEL3 0000
PRM_DEBUG_CFG 00000000 SELO 0000
PRM_DEBUG_OUT 00000000 OUTPUT 00000000

IPU_PRM
PM_IPU_PWRSTCTRL 00330103 PERIPHEM_ONSTATE MEM_ON AESSMEM_ONSTATE MEM_ON PERIPHEM_RETSTATE MEM_OFF
AESSMEM_RETSTATE MEM_RET LOWPOWERSTATECHANGE DIS LOGICRETSTATE LOGIC_OFF
POWERSTATE ON
PM_IPU_PWRSTST 00000337 LASTPOWERSTATEENTERED OFF INTRANSITION NO PERIPHEM_STATEST MEM_ON
AESSMEM_STATEST MEM_ON LOGICSTATEST ON POWERSTATEST ON
RM_IPU1_RSTCTRL 00000000 RST_IPU CLEAR RST_CPU1 CLEAR RST_CPU0 CLEAR
RM_IPU1_RSTST 00000007 RST_ICCRUSHER_CPU1 RESET_NO RST_ICCRUSHER_CPU0 RESET_NO RST_EMULATION_CPU1 RESET_NO
RST_EMULATION_CPU0 RESET_NO RST_IPU RESET_YES RST_CPU1 RESET_YES
RST_CPU0 RESET_YES
RM_IPU1_IPU1_CONTEXT 00000000 LOSTMEM_IPU_L2RAM MAINTAINED LOSTMEM_IPU_UNICACHE MAINTAINED LOSTCONTEXT_RFF MAINTAINED
LOSTCONTEXT_DFF MAINTAINED
PM_IPU_MCASP1_WKDEP 00000000 WKUPDEP_MCASP1_DMA_DSP2 ENABLED WKUPDEP_MCASP1_DMA_SDMA ENABLED WKUPDEP_MCASP1_DMA_DSP1 ENABLED
WKUPDEP_MCASP1_IRQ_EVE2 DISABLED WKUPDEP_MCASP1_IRQ_EVE1 DISABLED WKUPDEP_MCASP1_IRQ_DSP2 DISABLED
WKUPDEP_MCASP1_IRQ_IPU1 DISABLED WKUPDEP_MCASP1_IRQ_DSP1 DISABLED WKUPDEP_MCASP1_IRQ_IPU2 DISABLED
WKUPDEP_MCASP1_IRQ_MPU DISABLED
RM_IPU_MCASP1_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_IPU_TIMERS5_WKDEP 00000000 WKUPDEP_TIMERS5_EVE2 DISABLED WKUPDEP_TIMERS5_EVE1 DISABLED WKUPDEP_TIMERS5_DSP2 DISABLED
WKUPDEP_TIMERS5_IPU1 DISABLED WKUPDEP_TIMERS5_DSP1 DISABLED WKUPDEP_TIMERS5_IPU2 DISABLED

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WKUPDEP_TIMERS5_MPU DISABLED
RM_IPU_TIMER5_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_IPU_TIMER6_WKDEP 00000000 WKUPDEP_TIMER6_EVE2 DISABLED WKUPDEP_TIMER6_EVE1 DISABLED WKUPDEP_TIMER6_DSP2 DISABLED
WKUPDEP_TIMER6_IPU1 DISABLED WKUPDEP_TIMER6_DSP1 DISABLED WKUPDEP_TIMER6_IPU2 DISABLED
WKUPDEP_TIMER6_MPU DISABLED
RM_IPU_TIMER6_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_IPU_TIMER7_WKDEP 00000000 WKUPDEP_TIMER7_EVE2 DISABLED WKUPDEP_TIMER7_EVE1 DISABLED WKUPDEP_TIMER7_DSP2 DISABLED
WKUPDEP_TIMER7_IPU1 DISABLED WKUPDEP_TIMER7_DSP1 DISABLED WKUPDEP_TIMER7_IPU2 DISABLED
WKUPDEP_TIMER7_MPU DISABLED
RM_IPU_TIMER7_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_IPU_TIMER8_WKDEP 00000000 WKUPDEP_TIMER8_EVE2 DISABLED WKUPDEP_TIMER8_EVE1 DISABLED WKUPDEP_TIMER8_DSP2 DISABLED
WKUPDEP_TIMER8_IPU1 DISABLED WKUPDEP_TIMER8_DSP1 DISABLED WKUPDEP_TIMER8_IPU2 DISABLED
WKUPDEP_TIMER8_MPU DISABLED
RM_IPU_TIMER8_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_IPU_I2C5_WKDEP 0000B000 WKUPDEP_I2C5_DMA_DSP2 ENABLED WKUPDEP_I2C5_DMA_SDMA ENABLED WKUPDEP_I2C5_DMA_DSP1 ENABLED
WKUPDEP_I2C5_IRQ_EVE2 DISABLED WKUPDEP_I2C5_IRQ_EVE1 DISABLED WKUPDEP_I2C5_IRQ_DSP2 DISABLED
WKUPDEP_I2C5_IRQ_IPU1 DISABLED WKUPDEP_I2C5_IRQ_DSP1 DISABLED WKUPDEP_I2C5_IRQ_IPU2 DISABLED
WKUPDEP_I2C5_IRQ_MPU DISABLED
RM_IPU_I2C5_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_IPU_UART6_WKDEP 00000000 WKUPDEP_UART6_EVE2 DISABLED WKUPDEP_UART6_EVE1 DISABLED WKUPDEP_UART6_DSP2 DISABLED
WKUPDEP_UART6_IPU1 DISABLED WKUPDEP_UART6_SDMA DISABLED WKUPDEP_UART6_DSP1 DISABLED
WKUPDEP_UART6_IPU2 DISABLED WKUPDEP_UART6_MPU DISABLED
RM_IPU_UART6_CONTEXT 00000000 LOSTMEM_RETAINED_BANK MAINTAINED LOSTCONTEXT_RFF MAINTAINED

CM_CORE_DSS
CM_DSS_CLKSTRCTL 00000003 CLKACTIVITY_HDMI_PHY_GFCLK INACT CLKACTIVITY_HDMI_CEC_GFCLK INACT CLKACTIVITY_DSS_L4_GICLK INACT
CLKACTIVITY_BB2D_GFCLK INACT CLKACTIVITY_VIDEO2_DPLL_CLK INACT CLKACTIVITY_HDMI_DPLL_CLK INACT
CLKACTIVITY_VIDEO1_DPLL_CLK INACT CLKACTIVITY_DSS_GFCLK INACT CLKACTIVITY_DSS_L3_GICLK INACT
CLKTRCTRL HW_AUTO
CM_DSS_STATICDEP 00000020 L3MAIN1_STATDEP ENABLED EMIF_STATDEP DISABLED IVA_STATDEP DISABLED
CM_DSS_DYNAMICDEP 00000000 L3MAIN1_DYNDEP DISABLED
CM_DSS_DSS_CLKCTRL 00070000 STBYST STANDBY IDLEST DISABLE OPTFCLKEN_VIDEO2_CLK FCLK_DIS
OPTFCLKEN_VIDEO1_CLK FCLK_DIS OPTFCLKEN_32KHZ_CLK FCLK_DIS OPTFCLKEN_HDMI_CLK FCLK_DIS
OPTFCLKEN_48MHZ_CLK FCLK_DIS OPTFCLKEN_DSSECLK FCLK_DIS MODULEMODE DISABLED
CM_DSS_BB2D_CLKCTRL 00070000 STBYST STANDBY IDLEST DISABLE MODULEMODE DISABLED

CM_CORE_AON_CKGEN
CM_CLKSEL_CORE 00000110 CLKSEL_L4 L3_CLK_DIV_2 CLKSEL_L3 CORE_CLK_DIV_2
CM_CLKSEL_ABE 00000000 SLIMBUS1_CLK_GATE GATED PAD_CLKS_GATE GATED CLKSEL_OPP DIV_1
CM_DLL_CTRL 00000000 DLL_OVERRIDE NO_OVR
CM_CLKMODE_DPLL_CORE 00000007 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
DPLL_SSC_EN DISABLED DPLL_REGM4XEN DISABLED DPLL_LPMODE_EN DISABLED
DPLL_RELOCK_RAMP_EN Disabled DPLL_DRIFTGUARD_EN DIASBLED DPLL_RAMP_RATE REFCLKX2
DPLL_RAMP_LEVEL RAMP_DISABLE DPLL_EN DPLL_LOCK_MODE
CM_IDLEST_DPLL_CORE 0000001F ST_DPLL_INIT DPLL_INIT ST_DPLL_MODE 7 ST_DPLL_CLK DPLL_LOCKED
CM_AUTOIDLE_DPLL_CORE 00000001 AUTO_DPLL_MODE AUTO_LP_STOP
CM_CLKSEL_DPLL_CORE 00010A04 DPLL_BYP_CLKSEL CLKINP DCC_EN DISABLED DPLL_CLKOUTHIF_CLKSEL_SEL_DCO
DPLL_MULT 010A DPLL_DIV 04
CM_DIV_M2_DPLL_CORE 00000002 CLKST CLK_GATED DIVHS 2
CM_DIV_H12_DPLL_CORE 00000204 CLKST CLK_ENABLED DIVHS 4
CM_DIV_H13_DPLL_CORE 0000023E CLKST CLK_ENABLED DIVHS 62
CM_DIV_H14_DPLL_CORE 00000005 CLKST CLK_GATED DIVHS 5
CM_SSC_DELTAMSTEP_DPLL_CORE 00000000 DELTAMSTEP 000000
CM_SSC_MODFREQDIV_DPLL_CORE 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00
CM_DIV_H22_DPLL_CORE 00000205 CLKST CLK_ENABLED DIVHS 5
CM_DIV_H23_DPLL_CORE 00000204 CLKST CLK_ENABLED DIVHS 4
CM_DIV_H24_DPLL_CORE 00000006 CLKST CLK_GATED DIVHS 6
CM_CLKMODE_DPLL_MPU 00000007 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
DPLL_SSC_EN DISABLED DPLL_REGM4XEN DISABLED DPLL_LPMODE_EN DISABLED
DPLL_RELOCK_RAMP_EN Disabled DPLL_DRIFTGUARD_EN DIASBLED DPLL_RAMP_RATE REFCLKX2
DPLL_RAMP_LEVEL RAMP_DISABLE DPLL_EN DPLL_LOCK_MODE
CM_IDLEST_DPLL_MPU 0000001F ST_DPLL_INIT DPLL_INIT ST_DPLL_MODE RESERVED3 ST_DPLL_CLK DPLL_LOCKED
CM_AUTOIDLE_DPLL_MPU 00000001 AUTO_DPLL_MODE AUTO_LP_STOP
CM_CLKSEL_DPLL_MPU 00C04B00 DPLL_BYP_CLKSEL Supported DCC_EN ENABLED DPLL_MULT 004B
DPLL_DIV 00
CM_DIV_M2_DPLL_MPU 00000201 CLKST CLK_ENABLED DIVHS 1
CM_SSC_DELTAMSTEP_DPLL_MPU 00000000 DELTAMSTEP 000000
CM_SSC_MODFREQDIV_DPLL_MPU 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00
CM_BYPCLK_DPLL_MPU 00000000 CLKSEL /1
CM_CLKMODE_DPLL_IVA 00000007 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
DPLL_SSC_EN DISABLED DPLL_REGM4XEN DISABLED DPLL_LPMODE_EN DISABLED
DPLL_RELOCK_RAMP_EN Disabled DPLL_DRIFTGUARD_EN DIASBLED DPLL_RAMP_RATE REFCLKX2
DPLL_RAMP_LEVEL RAMP_DISABLE DPLL_EN DPLL_LOCK_MODE
CM_IDLEST_DPLL_IVA 00000012 ST_DPLL_INIT DPLL_INIT ST_DPLL_MODE LP_STOP ST_DPLL_CLK DPLL_UNLOCKED
CM_AUTOIDLE_DPLL_IVA 00000001 AUTO_DPLL_MODE AUTO_LP_STOP
CM_CLKSEL_DPLL_IVA 00010A04 DPLL_BYP_CLKSEL Not_supported DCC_EN DISABLED DPLL_MULT 010A
DPLL_DIV 04
CM_DIV_M2_DPLL_IVA 00000002 CLKST CLK_GATED DIVHS 2
CM_SSC_DELTAMSTEP_DPLL_IVA 00000000 DELTAMSTEP 000000
CM_SSC_MODFREQDIV_DPLL_IVA 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00
CM_BYPCLK_DPLL_IVA 00000000 CLKSEL CORE_X2_CLK_DIV_1
CM_CLKMODE_DPLL_ABE 00000007 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
DPLL_SSC_EN DISABLED DPLL_REGM4XEN DISABLED DPLL_LPMODE_EN DISABLED
DPLL_RELOCK_RAMP_EN Disabled DPLL_DRIFTGUARD_EN DIASBLED DPLL_RAMP_RATE REFCLKX2
DPLL_RAMP_LEVEL RAMP_DISABLE DPLL_EN DPLL_LOCK_MODE
CM_IDLEST_DPLL_ABE 0000001F ST_DPLL_INIT DPLL_INIT ST_DPLL_MODE RESERVED3 ST_DPLL_CLK DPLL_LOCKED
CM_AUTOIDLE_DPLL_ABE 00000001 AUTO_DPLL_MODE Low_Power_Stop
CM_CLKSEL_DPLL_ABE 00080800 DPLL_BYP_CLKSEL Supported DCC_EN DISABLED DPLL_MULT 0008
DPLL_DIV 00
CM_DIV_M2_DPLL_ABE 00000A01 CLKX2ST CLK_ENABLED CLKST CLK_ENABLED DIVHS 1
CM_DIV_M3_DPLL_ABE 00000001 CLKST CLK_GATED DIVHS 1
CM_SSC_DELTAMSTEP_DPLL_ABE 00000000 DELTAMSTEP 000000
CM_SSC_MODFREQDIV_DPLL_ABE 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00

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CM_CLKMODE_DPLL_DDR 00000007 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
DPLL_SSC_EN DISABLED DPLL_REGM4XEN DISABLED DPLL_LPMODE_EN DISABLED
DPLL_RELOCK_RAMP_EN 0 DPLL_DRIFTGUARD_EN DIASBLED DPLL_RAMP_RATE REFCLKX2
DPLL_RAMP_LEVEL RAMP_DISABLE DPLL_EN DPLL_LOCK_MODE
CM_IDLEST_DPLL_DDR 0000001F ST_DPLL_INIT DPLL_INIT ST_DPLL_MODE RESERVED3 ST_DPLL_CLK DPLL_LOCKED
CM_AUTOIDLE_DPLL_DDR 00000001 AUTO_DPLL_MODE AUTO_LP_STOP
CM_CLKSEL_DPLL_DDR 00010A04 DPLL_BYP_CLKSEL 0 DCC_EN DISABLED DPLL_MULT 010A
DPLL_DIV 04
CM_DIV_M2_DPLL_DDR 00000202 CLKST CLK_ENABLED DIVHS 2
CM_DIV_H11_DPLL_DDR 00000208 CLKST CLK_ENABLED DIVHS 8
CM_SSC_DELTAMSTEP_DPLL_DDR 00000000 DELTAMSTEP 000000
CM_SSC_MODFREQDIV_DPLL_DDR 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00
CM_CLKMODE_DPLL_DSP 00000007 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
DPLL_SSC_EN DISABLED DPLL_REGM4XEN DISABLED DPLL_LPMODE_EN DISABLED
DPLL_RELOCK_RAMP_EN 0 DPLL_DRIFTGUARD_EN DIASBLED DPLL_RAMP_RATE REFCLKX2
DPLL_RAMP_LEVEL RAMP_DISABLE DPLL_EN DPLL_LOCK_MODE
CM_IDLEST_DPLL_DSP 00000012 ST_DPLL_INIT DPLL_INIT ST_DPLL_MODE LP_STOP ST_DPLL_CLK DPLL_UNLOCKED
CM_AUTOIDLE_DPLL_DSP 00000001 AUTO_DPLL_MODE AUTO_LP_STOP
CM_CLKSEL_DPLL_DSP 00004B01 DPLL_BYP_CLKSEL 0 DCC_EN DISABLED DPLL_MULT 004B
DPLL_DIV 01
CM_DIV_M2_DPLL_DSP 00000001 CLKST CLK_GATED DIVHS 1
CM_DIV_M3_DPLL_DSP 00000003 CLKST CLK_GATED DIVHS 3
CM_SSC_DELTAMSTEP_DPLL_DSP 00000000 DELTAMSTEP 000000
CM_SSC_MODFREQDIV_DPLL_DSP 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00
CM_BYPCLK_DPLL_DSP 00000000 CLKSEL CORE_X2_CLK_DIV_1
CM_SHADOW_FREQ_CONFIG1 0005080C DPLL_DDR_DPLL_EN DPLL_LP_BYP_MODE DPLL_DDR_M2_DIV 1 DLL_RESET RESET
DLL_OVERRIDE OVR FREQ_UPDATE Not_updated
CM_SHADOW_FREQ_CONFIG2 00000004 DPLL_CORE_H12_DIV 1 CLKSEL_L3 CORE_CLK_DIV_1 GPMC_FREQ_UPDATE DISABLED
CM_DYN_DEP_PRESCAL 00000020 PRESCAL 32
CM_CLKMODE_DPLL_EVE 00000005 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
DPLL_SSC_EN DISABLED DPLL_REGM4XEN DISABLED DPLL_LPMODE_EN DISABLED
DPLL_RELOCK_RAMP_EN 0 DPLL_DRIFTGUARD_EN DIASBLED DPLL_RAMP_RATE REFCLKX2
DPLL_RAMP_LEVEL RAMP_DISABLE DPLL_EN DPLL_LP_BYP_MODE
CM_IDLEST_DPLL_EVE 00000002 ST_DPLL_INIT DPLL_NOTINIT ST_DPLL_MODE LP_STOP ST_DPLL_CLK DPLL_UNLOCKED
CM_AUTOIDLE_DPLL_EVE 00000001 AUTO_DPLL_MODE AUTO_LP_STOP
CM_CLKSEL_DPLL_EVE 00000000 DPLL_BYP_CLKSEL 0 DCC_EN DISABLED DPLL_MULT 0000
DPLL_DIV 00
CM_DIV_M2_DPLL_EVE 00000001 CLKST CLK_GATED DIVHS 1
CM_SSC_DELTAMSTEP_DPLL_EVE 00000000 DELTAMSTEP 000000
CM_SSC_MODFREQDIV_DPLL_EVE 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00
CM_BYPCLK_DPLL_EVE 00000000 CLKSEL 0
CM_CLKMODE_DPLL_GMAC 00000007 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
DPLL_SSC_EN DISABLED DPLL_REGM4XEN DISABLED DPLL_LPMODE_EN DISABLED
DPLL_RELOCK_RAMP_EN 0 DPLL_DRIFTGUARD_EN DIASBLED DPLL_RAMP_RATE REFCLKX2
DPLL_RAMP_LEVEL RAMP_DISABLE DPLL_EN DPLL_LOCK_MODE
CM_IDLEST_DPLL_GMAC 0000001F ST_DPLL_INIT DPLL_INIT ST_DPLL_MODE RESERVED3 ST_DPLL_CLK DPLL_LOCKED
CM_AUTOIDLE_DPLL_GMAC 00000001 AUTO_DPLL_MODE AUTO_LP_STOP
CM_CLKSEL_DPLL_GMAC 0000FA04 DPLL_BYP_CLKSEL 0 DCC_EN DISABLED DPLL_CLKOUTHIF_CLKSEL_SEL_DCO
DPLL_MULT 00FA DPLL_DIV 04
CM_DIV_M2_DPLL_GMAC 00000204 CLKST CLK_ENABLED DIVHS 4
CM_DIV_M3_DPLL_GMAC 0000000A CLKST CLK_GATED DIVHS 10
CM_DIV_H11_DPLL_GMAC 00000228 CLKST CLK_ENABLED DIVHS 40
CM_DIV_H12_DPLL_GMAC 00000208 CLKST CLK_ENABLED DIVHS 8
CM_DIV_H13_DPLL_GMAC 0000000A CLKST CLK_GATED DIVHS 10
CM_SSC_DELTAMSTEP_DPLL_GMAC 00000000 DELTAMSTEP 000000
CM_SSC_MODFREQDIV_DPLL_GMAC 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00
CM_CLKMODE_DPLL_GPU 00000007 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
DPLL_SSC_EN DISABLED DPLL_REGM4XEN DISABLED DPLL_LPMODE_EN DISABLED
DPLL_RELOCK_RAMP_EN 0 DPLL_DRIFTGUARD_EN DIASBLED DPLL_RAMP_RATE REFCLKX2
DPLL_RAMP_LEVEL RAMP_DISABLE DPLL_EN DPLL_LOCK_MODE
CM_IDLEST_DPLL_GPU 00000012 ST_DPLL_INIT DPLL_INIT ST_DPLL_MODE 1 ST_DPLL_CLK DPLL_UNLOCKED
CM_AUTOIDLE_DPLL_GPU 00000001 AUTO_DPLL_MODE AUTO_LP_STOP
CM_CLKSEL_DPLL_GPU 00010A04 DPLL_BYP_CLKSEL 0 DCC_EN DISABLED DPLL_CLKOUTHIF_CLKSEL_SEL_DCO
DPLL_MULT 010A DPLL_DIV 04
CM_DIV_M2_DPLL_GPU 00000002 CLKST CLK_GATED DIVHS 2
CM_SSC_DELTAMSTEP_DPLL_GPU 00000000 DELTAMSTEP 000000
CM_SSC_MODFREQDIV_DPLL_GPU 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00

CM_CORE_AON_RTC
CM_RTC_CLKSTCTRL 00000403 CLKACTIVITY_RTC_AUX_CLK ACT CLKACTIVITY_RTC_L4_GICLK INACT CLKTRCTRL HW_AUTO
CM_RTC_RTCCS_CLKCTRL 00020002 IDLEST IDLE MODULEMODE ENABLED

INSTR_PRM
PMI_IDENTICATION 00000000 SCHEME 0 FUNC 0000 RTL 0
MAJOR 0 CUSTOM 0 MINOR 0
PMI_SYS_CONFIG 00000000 IDLEMODE 0 SOFTRESET 0
PMI_STATUS 00000000 FIFOEMPTY 0
PMI_CONFIGURATION 00000000 CLAIM_3 0 CLAIM_2 0 CLAIM_1 0
EVT_CAPT_EN 0
PMI_CLASS_FILTERING 00000000 SNAP_CAPT_EN_03 0 SNAP_CAPT_EN_02 0 SNAP_CAPT_EN_01 0
SNAP_CAPT_EN_00 0
PMI_TRIGGERING 00000000 TRIG_STOP_EN 0 TRIG_START_EN 0
PMI_SAMPLING 00000000 FCLK_DIV_FACOR 0 SAMP_WIND_SIZE 00

CM_CORE_CORE
CM_L3MAIN1_CLKSTCTRL 00000303 CLKACTIVITY_L3MAIN1_L4_GICLK ACT CLKACTIVITY_L3MAIN1_L3_GICLK ACT CLKTRCTRL
CM_L3MAIN1_DYNAMICDEP F4F4F51F EVE2_DYNDEP ENABLED EVE1_DYNDEP ENABLED WINDOWSIZE
L4PER3_DYNDEP ENABLED L4PER2_DYNDEP ENABLED PCIE_DYNDEP
DSP2_DYNDEP ENABLED IPU1_DYNDEP ENABLED WKUPAON_DYNDEP
L4SEC_DYNDEP ENABLED L4PER_DYNDEP ENABLED L4CFG_DYNDEP
GPU_DYNDEP ENABLED DSS_DYNDEP ENABLED EMIF_DYNDEP
IPU_DYNDEP ENABLED IVA_DYNDEP ENABLED DSP1_DYNDEP
IPU2_DYNDEP ENABLED

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CM_L3MAIN1_L3_MAIN_1_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L3MAIN1_GPMC_CLKCTRL	00030000	IDLEST	DISABLE	MODULEMODE	DISABLED			
CM_L3MAIN1_MMU_EDMA_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L3MAIN1_MMU_PCIESS_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L3MAIN1_OCMC_RAM1_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L3MAIN1_OCMC_RAM2_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L3MAIN1_OCMC_RAM3_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L3MAIN1_TPCC_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L3MAIN1_TPTC1_CLKCTRL	00000001	STBYST	FUNC	IDLEST	FUNC	MODULEMODE		
CM_L3MAIN1_TPTC2_CLKCTRL	00000001	STBYST	FUNC	IDLEST	FUNC	MODULEMODE		
CM_L3MAIN1_VCP1_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L3MAIN1_VCP2_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_IPU2_CLKSTCTRL	00000003	CLKACTIVITY_IPU2_GFLCK	INACT	CLKTRCTRL	HW_AUTO			
CM_IPU2_STATICDEP	00000000	ATL_STATDEP	DISABLED	PCIE_STATDEP	DISABLED	VPE_STATDEP		
	L4PER3_STATDEP	DISABLED	L4PER2_STATDEP	DISABLED	GMAC_STATDEP			
	IPU1_STATDEP	DISABLED	IPU1_STATDEP	DISABLED	EVE2_STATDEP			
	EVE1_STATDEP	DISABLED	DSP2_STATDEP	DISABLED	CUSTEFUSE_STATDEP			
	COREAON_STATDEP	DISABLED	WKUPAON_STATDEP	DISABLED	L4SEC_STATDEP			
	L4PER_STATDEP	DISABLED	L4CFG_STATDEP	DISABLED	SDMA_STATDEP			
	GPU_STATDEP	DISABLED	CAM_STATDEP	DISABLED	DSS_STATDEP			
	L3INIT_STATDEP	DISABLED	L3MAIN1_STATDEP	DISABLED	EMIF_STATDEP			
	IVA_STATDEP	DISABLED	DSP1_STATDEP	DISABLED				
CM_IPU2_DYNAMICDEP	04000020	WINDOWSIZE	4	CAM_DYNDEP	DISABLED	L3MAIN1_DYNDEP		
CM_IPU2_IPU2_CLKCTRL	00070000	STBYST	STANDBY	IDLEST	DISABLE	MODULEMODE		
CM_DMA_CLKSTCTRL	00000103	CLKACTIVITY_DMA_L3_GICLK	ACT	CLKTRCTRL	HW_AUTO			
CM_DMA_STATICDEP	00000020	PCIE_STATDEP	DISABLED	L4PER3_STATDEP	DISABLED	L4PER2_STATDEP		
	IPU1_STATDEP	DISABLED	IPU1_STATDEP	DISABLED	WKUPAON_STATDEP			
	L4SEC_STATDEP	DISABLED	L4PER_STATDEP	DISABLED	L4CFG_STATDEP			
	CAM_STATDEP	DISABLED	DSS_STATDEP	DISABLED	L3INIT_STATDEP			
	L3MAIN1_STATDEP	ENABLED	EMIF_STATDEP	DISABLED	IVA_STATDEP			
	IPU2_STATDEP	DISABLED						
CM_DMA_DYNAMICDEP	00000000	L3MAIN1_DYNDEP	DISABLED					
CM_DMA_DMA_SYSTEM_CLKCTRL	00000001	STBYST	FUNC	IDLEST	FUNC	MODULEMODE		
CM_EMIF_CLKSTCTRL	00000703	CLKACTIVITY_EMIF_PHY_GCLK	ACT	CLKACTIVITY_EMIF_DLL_GCLK	ACT	CLKACTIVITY_EMIF_L3_GICLK		
	CLKTRCTRL	HW_AUTO						
CM_EMIF_DMM_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_EMIF_EMIF_OCP_FW_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_EMIF_EMIF1_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_EMIF_EMIF2_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_EMIF_EMIF_DLL_CLKCTRL	00000000	OPTFCLKEN_DLL_CLK	FCLK_DIS					
CM_ATL_ATL_CLKCTRL	04030000	CLKSEL_SOURCE2	SEL_PER_ABE_X1_CLK	CLKSEL_SOURCE1	SEL_FUNC_32K_CLK	IDLEST		
	MODULEMODE	DISABLED						
CM_ATL_CLKSTCTRL	00000003	CLKACTIVITY_ATL_GFLCK	INACT	CLKACTIVITY_ATL_L3_GICLK	INACT	CLKTRCTRL		
CM_L4CFG_CLKSTCTRL	00000303	CLKACTIVITY_L4CFG_L3_GICLK	ACT	CLKACTIVITY_L4CFG_L4_GICLK	ACT	CLKTRCTRL		
CM_L4CFG_DYNAMICDEP	040B08B0	WINDOWSIZE	4	MPU_DYNDEP	ENABLED	CUSTEFUSE_DYNDEP		
	COREAON_DYNDEP	ENABLED	SDMA_DYNDEP	ENABLED	L3INIT_DYNDEP			
	L3MAIN1_DYNDEP	ENABLED	EMIF_DYNDEP	ENABLED				
CM_L4CFG_L4_CFG_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_SPINLOCK_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX1_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_SAR_ROM_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_OCP2SCP2_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX2_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX3_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX4_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX5_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX6_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX7_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX8_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX9_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX10_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX11_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX12_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L4CFG_MAILBOX13_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L3INSTR_CLKSTCTRL	00000603	CLKACTIVITY_L3INSTR_TS_GCLK	ACT	CLKACTIVITY_L3INSTR_DLL_AGING_GCLK	ACT	CLKACTIVITY_L3INSTR_L3_GICLK		
	CLKTRCTRL	HW_AUTO						
CM_L3INSTR_L3_MAIN_2_CLKCTRL	00030000	IDLEST	DISABLE	MODULEMODE	DISABLED			
CM_L3INSTR_L3_INSTR_CLKCTRL	00030000	IDLEST	DISABLE	MODULEMODE	DISABLED			
CM_L3INSTR_OCP_WP_NOC_CLKCTRL	00030000	IDLEST	DISABLE	MODULEMODE	DISABLED			
CM_L3INSTR_DLL_AGING_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO			
CM_L3INSTR_CTRL_MODULE_BANDGAP_CLKCTRL	01000001	CLKSEL	DIV16	IDLEST	FUNC	MODULEMODE	AUT	
CM_CORE_L3INIT								
CM_L3INIT_CLKSTCTRL	01718F02	CLKACTIVITY_SATA_REF_GFLCK	ACT	CLKACTIVITY_L3INIT_32K_GFLCK	INACT	CLKACTIVITY_L3INIT_960M_GFLCK	ACT	
	CLKACTIVITY_L3INIT_480M_GFLCK	ACT	CLKACTIVITY_USB_OTG_SS_REF_CLK	ACT	CLKACTIVITY_MLB_SYS_L3_GFLCK	INACT		
	CLKACTIVITY_MLB_SPB_L4_GICLK	INACT	CLKACTIVITY_MLB_SHB_L3_GICLK	INACT	CLKACTIVITY_MMC2_GFLCK	ACT		
	CLKACTIVITY_MMC1_GFLCK	ACT	CLKACTIVITY_USB_DPLL_HS_CLK	INACT	CLKACTIVITY_USB_DPLL_CLK	INACT		
	CLKACTIVITY_L3INIT_48M_GFLCK	ACT	CLKACTIVITY_L3INIT_USB_LFPS_TX_GFLCK	ACT	CLKACTIVITY_L3INIT_L4_GICLK	ACT		
	CLKACTIVITY_L3INIT_L3_GICLK	ACT	CLKTRCTRL	SW_WKUP				
CM_L3INIT_STATICDEP	00000020	L4PER3_STATDEP	DISABLED	WKUPAON_STATDEP	DISABLED	L4SEC_STATDEP	DISABL	
	L4PER_STATDEP	DISABLED	L4CFG_STATDEP	DISABLED	L3MAIN1_STATDEP	ENABLE		
	EMIF_STATDEP	DISABLED	IVA_STATDEP	DISABLED				
CM_L3INIT_DYNAMICDEP	00000000	L3MAIN1_DYNDEP	DISABLED					
CM_L3INIT_MMC1_CLKCTRL	01040002	CLKSEL_DIV	DIV1	CLKSEL_SOURCE	SEL_192M	STBYST	STANDBY	
	IDLEST	FUNC	OPTFCLKEN_CLK32K	FCLK_DIS	MODULEMODE	ENABLE		
CM_L3INIT_MMC2_CLKCTRL	01040002	CLKSEL_DIV	DIV1	CLKSEL_SOURCE	SEL_192M	STBYST	STANDBY	
	IDLEST	FUNC	OPTFCLKEN_CLK32K	FCLK_DIS	MODULEMODE	ENABLE		
CM_L3INIT_USB_OTG_SS2_CLKCTRL	00000101	STBYST	FUNC	IDLEST	FUNC	OPTFCLKEN_REFCLK960M	FCLK_E	
	MODULEMODE	AUTO						
CM_L3INIT_USB_OTG_SS3_CLKCTRL	00070000	STBYST	STANDBY	IDLEST	DISABLE	MODULEMODE	DISABL	
CM_L3INIT_USB_OTG_SS4_CLKCTRL	00070000	STBYST	STANDBY	IDLEST	DISABLE	MODULEMODE	DISABL	
CM_L3INIT_MLB_SS_CLKCTRL	00070000	STBYST	STANDBY	IDLEST	DISABLE	MODULEMODE	DISABL	
CM_L3INIT_IEEE1500_2_OCP_CLKCTRL	00040001	STBYST	STANDBY	IDLEST	FUNC	MODULEMODE	AUTO	

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CM_L3INIT_SATA_CLKCTRL 00000102 STBYST FUNC IDLEST FUNC OPTFCKEN_REF_CLK FCLK_E
MODULEMODE ENABLED
CM_PCIE_CLKSTCTRL 00003F02 CLKACTIVITY_PCIE_32K_GFCLK ACT CLKACTIVITY_PCIE_SYS_GFCLK ACT CLKACTIVITY_PCIE_REF_GFCLK ACT
CLKACTIVITY_PCIE_PHY_DIV_GCLK ACT CLKACTIVITY_PCIE_PHY_GCLK ACT CLKACTIVITY_PCIE_L3_GICKL ACT
CLKTRCTRL SW_WKUP
CM_PCIE_STATICDEP 00000000 ATL_STATDEP DISABLED VPE_STATDEP DISABLED L4PER3_STATDEP DISABL
L4PER2_STATDEP DISABLED GMAC_STATDEP DISABLED IPU_STATDEP DISABL
IPU1_STATDEP DISABLED EVE2_STATDEP DISABLED EVE1_STATDEP DISABL
DSP2_STATDEP DISABLED CUSTEFUSE_STATDEP DISABLED COREAON_STATDEP DISABL
L4SEC_STATDEP DISABLED L4PER_STATDEP DISABLED L4CFG_STATDEP DISABL
SDMA_STATDEP DISABLED GPU_STATDEP DISABLED CAM_STATDEP DISABL
DSS_STATDEP DISABLED L3INIT_STATDEP DISABLED EMIF_STATDEP DISABL
IVA_STATDEP DISABLED DSP1_STATDEP DISABLED
CM_PCIE_PCIESS1_CLKCTRL 00000702 STBYST FUNC IDLEST FUNC OPTFCKEN_PCIEPHY_CLK_DIV FCLK_E
OPTFCKEN_PCIEPHY_CLK FCLK_EN OPTFCKEN_32KHZ FCLK_EN MODULEMODE ENABLED
CM_PCIE_PCIESS2_CLKCTRL 00070000 STBYST STANDBY IDLEST DISABLE OPTFCKEN_PCIEPHY_CLK_DIV FCLK_D
OPTFCKEN_PCIEPHY_CLK FCLK_DIS OPTFCKEN_32KHZ FCLK_DIS MODULEMODE DISABL
CM_GMAC_CLKSTCTRL 00001F03 CLKACTIVITY_GMAC_MAIN_CLK ACT CLKACTIVITY_GMAC_RFT_CLK ACT CLKACTIVITY_RMII_50MHZ_CLK ACT
CLKACTIVITY_RGMII_5MHZ_CLK ACT CLKACTIVITY_GMII_250MHZ_CLK ACT CLKTRCTRL HW_AUTO
CM_GMAC_STATICDEP 00000020 L4PER2_STATDEP DISABLED L3MAIN1_STATDEP ENABLED EMIF_STATDEP DISABL
CM_GMAC_DYNAMICDEP 00000000 L3MAIN1_DYNDEP DISABLED
CM_GMAC_GMAC_CLKCTRL 08000002 CLKSEL_RFT 4 CLKSEL_REF SEL_GMAC_RMII_HS_CLK STBYST FUNC
IDLEST 0 MODULEMODE 2
CM_L3INIT_OCP2SCP1_CLKCTRL 00000001 IDLEST FUNC MODULEMODE AUTO
CM_L3INIT_OCP2SCP3_CLKCTRL 00000001 IDLEST FUNC MODULEMODE AUTO
CM_L3INIT_USB_OTG_SS1_CLKCTRL 00040101 STBYST STANDBY IDLEST FUNC OPTFCKEN_REFCLK960M FCLK_E
MODULEMODE AUTO

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```

EMU_CM
CM_EMU_CLKSTCTRL 00000003 CLKACTIVITY_EMU_SYS_CLK INACT CLKTRCTRL HW_AUTO <-- SW_WKUP
CM_EMU_DEBUGSS_CLKCTRL 00060001 STBYST STANDBY IDLEST IDLE MODULEMODE AUTO
CM_EMU_DYNAMICDEP 04000020 WINDOWSIZE 4 L3MAIN1_DYNDEP ENABLED
CM_EMU_MPU_EMU_DBG_CLKCTRL 00020001 IDLEST IDLE MODULEMODE AUTO

```

```

CM_CORE_OCP_SOCKET
REVISION_CM_CORE 40000301 SCHEME H08 FUNC 0000 R_RTL 0
X_MAJOR OMAP5430 CUSTOM STANDARD Y_MINOR E52
CM_CM_CORE_PROFILING_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
CM_CORE_DEBUG_CFG 03020100 SEL3 03 SEL2 02 SEL1 01
SELO 00

```

```

EVE1_PRM
PM_EVE1_PWRSTCTRL 00030000 EVE1_BANK_ONSTATE MEM_ON LOWPOWERSTATECHANGE DIS POWERSTATE OFF
PM_EVE1_PWRSTST 00000000 LASTPOWERSTATEENTERED OFF INTRANSITION NO EVE1_BANK_STATEST MEM_OFF
LOGICSTATEST OFF POWERSTATEST OFF
RM_EVE1_RSTCTRL 00000003 RST_EVE1 ASSERT RST_EVE1_LRST ASSERT
RM_EVE1_RSTST 00000000 RST_EVE1_EMU_REQ RESET_NO RST_EVE1_EMU RESET_NO RST_EVE1 RESET_NO
RST_EVE1_LRST RESET_NO
PM_EVE1_EVE1_WKDEP 00000000 WKUPDEP_EVE1_EVE2 DISABLED WKUPDEP_EVE1_DSP2 DISABLED WKUPDEP_EVE1_IPU1 DISABLED
WKUPDEP_EVE1_SDMA DISABLED WKUPDEP_EVE1_DSP1 DISABLED WKUPDEP_EVE1_IPU2 DISABLED
WKUPDEP_EVE1_MPU DISABLED
RM_EVE1_EVE1_CONTEXT 00000101 LOSTMEM_EVE_BANK LOST LOSTCONTEXT_DFF LOST

```

```

CM_CORE_AON_VPE
CM_VPE_CLKSTCTRL 00000103 CLKACTIVITY_VPE_GCLK ACT CLKTRCTRL HW_AUTO
CM_VPE_VPE_CLKCTRL 00000001 STBYST FUNC IDLEST FUNC MODULEMODE AUTO
CM_VPE_STATICDEP 00000020 L4PER3_STATDEP DISABLED L3MAIN1_STATDEP ENABLED EMIF_STATDEP DISABLED

```

```

CM_CORE_CUSTEFUSE
CM_CUSTEFUSE_CLKSTCTRL 00000003 CLKACTIVITY_CUSTEFUSE_SYS_GFCLK INACT CLKACTIVITY_CUSTEFUSE_L4_GICKL INACT CLKTRCTRL HW_AUTO
CM_CUSTEFUSE_EFUSE_CTRL_CUST_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED

```

```

CM_CORE_AON_EVE1
CM_EVE1_CLKSTCTRL 00000003 CLKACTIVITY_EVE1_GFCLK INACT CLKTRCTRL HW_AUTO
CM_EVE1_STATICDEP 00000020 EVE2_STATDEP DISABLED L3MAIN1_STATDEP ENABLED EMIF_STATDEP DISABLED
IVA_STATDEP DISABLED
CM_EVE1_EVE1_CLKCTRL 00070000 STBYST STANDBY IDLEST DISABLE MODULEMODE DISABLED

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```

CM_CORE_AON_EVE2
CM_EVE2_CLKSTCTRL 00000003 CLKACTIVITY_EVE2_GFCLK INACT CLKTRCTRL HW_AUTO
CM_EVE2_STATICDEP 00000020 EVE1_STATDEP DISABLED L3MAIN1_STATDEP ENABLED EMIF_STATDEP DISABLED
IVA_STATDEP DISABLED
CM_EVE2_EVE2_CLKCTRL 00070000 STBYST STANDBY IDLEST DISABLE MODULEMODE DISABLED

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```

L3INIT_PRM
PM_L3INIT_PWRSTCTRL 000FC617 GMAC_BANK_ONSTATE MEM_ON L3INIT_BANK2_ONSTATE MEM_ON L3INIT_BANK1_ONSTATE MEM_ON
GMAC_BANK_RETSTATE MEM_RET L3INIT_BANK2_RETSTATE MEM_RET L3INIT_BANK1_RETSTATE MEM_OFF
LOWPOWERSTATECHANGE EN LOGICRETSTATE LOGIC_RET POWERSTATE ON
PM_L3INIT_PWRSTST 000003F7 LASTPOWERSTATEENTERED OFF INTRANSITION NO L3INIT_GMAC_STATEST MEM_ON
L3INIT_BANK2_STATEST MEM_ON L3INIT_BANK1_STATEST MEM_ON LOGICSTATEST ON
POWERSTATEST ON
RM_PCIESS_RSTCTRL 00000000 RST_LOCAL_PCIE2 CLEAR RST_LOCAL_PCIE1 CLEAR
RM_PCIESS_RSTST 00000003 RST_LOCAL_PCIE2 RESET_YES RST_LOCAL_PCIE1 RESET_YES
PM_L3INIT_MMC1_WKDEP 00000000 WKUPDEP_MMC1_EVE2 DISABLED WKUPDEP_MMC1_EVE1 DISABLED WKUPDEP_MMC1_DSP2 DISABLED
WKUPDEP_MMC1_IPU1 DISABLED WKUPDEP_MMC1_SDMA DISABLED WKUPDEP_MMC1_DSP1 DISABLED
WKUPDEP_MMC1_IPU2 DISABLED WKUPDEP_MMC1_MPU DISABLED
RM_L3INIT_MMC1_CONTEXT 00000000 LOSTMEM_L3INIT_BANK1 MAINTAINED LOSTCONTEXT_RFF MAINTAINED
PM_L3INIT_MMC2_WKDEP 00000000 WKUPDEP_MMC2_EVE2 DISABLED WKUPDEP_MMC2_EVE1 DISABLED WKUPDEP_MMC2_DSP2 DISABLED
WKUPDEP_MMC2_IPU1 DISABLED WKUPDEP_MMC2_SDMA DISABLED WKUPDEP_MMC2_DSP1 DISABLED
WKUPDEP_MMC2_IPU2 DISABLED WKUPDEP_MMC2_MPU DISABLED
RM_L3INIT_MMC2_CONTEXT 00000000 LOSTMEM_L3INIT_BANK1 MAINTAINED LOSTCONTEXT_RFF MAINTAINED
PM_L3INIT_USB_OTG_SS2_WKDEP 00000000 WKUPDEP_USB_OTG_SS2_EVE2 DISABLED WKUPDEP_USB_OTG_SS2_EVE1 DISABLED WKUPDEP_USB_OTG_SS2_DSP2 DISABLED
WKUPDEP_USB_OTG_SS2_IPU1 DISABLED WKUPDEP_USB_OTG_SS2_DSP1 DISABLED WKUPDEP_USB_OTG_SS2_IPU2 DISABLED

```

```

WKUPDEP_USB_OTG_SS2_MPU DISABLED
RM_L3INIT_USB_OTG_SS2_CONTEXT 00000000 LOSTMEM_L3INIT_BANK1 MAINTAINED LOSTCONTEXT_RFF MAINTAINED
PM_L3INIT_USB_OTG_SS3_WKDEP 00000000 WKUPDEP_USB_OTG_SS3_EVE2 DISABLED WKUPDEP_USB_OTG_SS3_EVE1 DISABLED WKUPDEP_USB_OTG_SS3_DSP2 DISABLED
WKUPDEP_USB_OTG_SS3_IPU1 DISABLED WKUPDEP_USB_OTG_SS3_DSP1 DISABLED WKUPDEP_USB_OTG_SS3_IPU2 DISABLED
WKUPDEP_USB_OTG_SS3_MPU DISABLED
RM_L3INIT_USB_OTG_SS3_CONTEXT 00000000 LOSTMEM_L3INIT_BANK1 MAINTAINED LOSTCONTEXT_RFF MAINTAINED
PM_L3INIT_USB_OTG_SS4_WKDEP 00000000 WKUPDEP_USB_OTG_SS4_EVE2 DISABLED WKUPDEP_USB_OTG_SS4_EVE1 DISABLED WKUPDEP_USB_OTG_SS4_DSP2 DISABLED
WKUPDEP_USB_OTG_SS4_IPU1 DISABLED WKUPDEP_USB_OTG_SS4_DSP1 DISABLED WKUPDEP_USB_OTG_SS4_IPU2 DISABLED
WKUPDEP_USB_OTG_SS4_MPU DISABLED
RM_L3INIT_USB_OTG_SS4_CONTEXT 00000000 LOSTMEM_L3INIT_BANK1 MAINTAINED LOSTCONTEXT_RFF MAINTAINED
RM_L3INIT_MLB_SS_CONTEXT 00000101 LOSTMEM_MLB_BANK LOST LOSTCONTEXT_DFF LOST
RM_L3INIT_IEEE1500_2_OCP_CONTEXT 00000001 LOSTCONTEXT_DFF LOST
PM_L3INIT_SATA_WKDEP 00000000 WKUPDEP_SATA_EVE2 DISABLED WKUPDEP_SATA_EVE1 DISABLED WKUPDEP_SATA_DSP2 DISABLED
WKUPDEP_SATA_IPU1 DISABLED WKUPDEP_SATA_DSP1 DISABLED WKUPDEP_SATA_IPU2 DISABLED
WKUPDEP_SATA_MPU DISABLED
RM_L3INIT_SATA_CONTEXT 00000000 LOSTMEM_L3INIT_BANK1 MAINTAINED LOSTCONTEXT_DFF MAINTAINED
PM_PCIE_PCIESS1_WKDEP 00000000 WKUPDEP_PCIESS1_EVE2 DISABLED WKUPDEP_PCIESS1_EVE1 DISABLED WKUPDEP_PCIESS1_DSP2 DISABLED
WKUPDEP_PCIESS1_IPU1 DISABLED WKUPDEP_PCIESS1_DSP1 DISABLED WKUPDEP_PCIESS1_IPU2 DISABLED
WKUPDEP_PCIESS1_MPU DISABLED
RM_PCIE_PCIESS1_CONTEXT 00000000 LOSTMEM_L3INIT_BANK1 MAINTAINED LOSTCONTEXT_DFF MAINTAINED
PM_PCIE_PCIESS2_WKDEP 00000000 WKUPDEP_PCIESS2_EVE2 DISABLED WKUPDEP_PCIESS2_EVE1 DISABLED WKUPDEP_PCIESS2_DSP2 DISABLED
WKUPDEP_PCIESS2_IPU1 DISABLED WKUPDEP_PCIESS2_DSP1 DISABLED WKUPDEP_PCIESS2_IPU2 DISABLED
WKUPDEP_PCIESS2_MPU DISABLED
RM_PCIE_PCIESS2_CONTEXT 00000101 LOSTMEM_L3INIT_BANK1 LOST LOSTCONTEXT_DFF LOST
RM_GMAC_GMAC_CONTEXT 00000000 LOSTMEM_GMAC_BANK MAINTAINED LOSTCONTEXT_DFF MAINTAINED
RM_L3INIT_OCP2SCP1_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
RM_L3INIT_OCP2SCP3_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_L3INIT_USB_OTG_SS1_WKDEP 00000000 WKUPDEP_USB_OTG_SS1_EVE2 DISABLED WKUPDEP_USB_OTG_SS1_EVE1 DISABLED WKUPDEP_USB_OTG_SS1_DSP2 DISABLED
WKUPDEP_USB_OTG_SS1_IPU1 DISABLED WKUPDEP_USB_OTG_SS1_DSP1 DISABLED WKUPDEP_USB_OTG_SS1_IPU2 DISABLED
WKUPDEP_USB_OTG_SS1_MPU DISABLED
RM_L3INIT_USB_OTG_SS1_CONTEXT 00000000 LOSTMEM_L3INIT_BANK1 MAINTAINED LOSTCONTEXT_RFF MAINTAINED

CM_CORE_CAM
CM_CAM_CLKSTCTRL 00001102 CLKACTIVITY_VIP3_GCLK INACT CLKACTIVITY_VIP2_GCLK INACT CLKACTIVITY_VIP1_GCLK ACT
CLKTRCTRL SW_WKUP
CM_CAM_STATICDEP 00000020 VPE_STATDEP DISABLED L4PER3_STATDEP DISABLED GMAC_STATDEP DISABLED
EVE2_STATDEP DISABLED EVE1_STATDEP DISABLED L4CFG_STATDEP DISABLED
L3MAIN1_STATDEP ENABLED EMIF_STATDEP DISABLED IVA_STATDEP DISABLED
CM_CAM_VIP1_CLKCTRL 00000001 CLKSEL SEL_L3_ICLK STBYST FUNC IDLEST FUNC
MODULEMODE AUTO
CM_CAM_VIP2_CLKCTRL 00070000 CLKSEL SEL_L3_ICLK STBYST STANDBY IDLEST DISABLE
MODULEMODE DISABLED
CM_CAM_VIP3_CLKCTRL 00070000 CLKSEL SEL_L3_ICLK STBYST STANDBY IDLEST DISABLE
MODULEMODE DISABLED

DSS_PRM
PM_DSS_PWRSTCTRL 00030000 DSS_MEM_ONSTATE MEM_ON DSS_MEM_RETSTATE MEM_OFF LOWPOWERSTATECHANGE DIS
LOGICRETSTATE LOGIC_OFF POWERSTATE OFF
PM_DSS_PWRSTST 00000000 LASTPOWERSTATEENTERED OFF INTRANSITION NO DSS_MEM_STATEST MEM_OFF
LOGICSTATEST OFF POWERSTATEST OFF
PM_DSS_DSS_WKDEP 00000000 WKUPDEP_DS11_B_EVE2 DISABLED WKUPDEP_DS11_B_EVE1 DISABLED WKUPDEP_DS11_B_DSP2 DISABLED
WKUPDEP_DS11_B_IPU1 DISABLED WKUPDEP_DS11_B_SDMA DISABLED WKUPDEP_DS11_B_DSP1 DISABLED
WKUPDEP_DS11_B_IPU2 DISABLED WKUPDEP_DS11_B_MPU DISABLED WKUPDEP_DS11_A_EVE2 DISABLED
WKUPDEP_DS11_A_EVE1 DISABLED WKUPDEP_DS11_A_DSP2 DISABLED WKUPDEP_DS11_A_IPU1 DISABLED
WKUPDEP_DS11_A_SDMA DISABLED WKUPDEP_DS11_A_DSP1 DISABLED WKUPDEP_DS11_A_IPU2 DISABLED
WKUPDEP_DS11_A_MPU DISABLED WKUPDEP_DISPC_EVE2 DISABLED WKUPDEP_DISPC_EVE1 DISABLED
WKUPDEP_DISPC_DSP2 DISABLED WKUPDEP_DISPC_IPU1 DISABLED WKUPDEP_DISPC_SDMA DISABLED
WKUPDEP_DISPC_DSP1 DISABLED WKUPDEP_DISPC_IPU2 DISABLED WKUPDEP_DISPC_MPU DISABLED
RM_DSS_DSS_CONTEXT 00000103 LOSTMEM_DSS_MEM LOST LOSTCONTEXT_RFF LOST LOSTCONTEXT_DFF LOST
PM_DSS_DSS2_WKDEP 00000000 WKUPDEP_HDMIDMA_DSP2 DISABLED WKUPDEP_HDMIDMA_SDMA DISABLED WKUPDEP_HDMIDMA_DSP1 DISABLED
WKUPDEP_DS11_C_EVE2 DISABLED WKUPDEP_DS11_C_EVE1 DISABLED WKUPDEP_DS11_C_DSP2 DISABLED
WKUPDEP_DS11_C_IPU1 DISABLED WKUPDEP_DS11_C_SDMA DISABLED WKUPDEP_DS11_C_DSP1 DISABLED
WKUPDEP_DS11_C_IPU2 DISABLED WKUPDEP_DS11_C_MPU DISABLED WKUPDEP_HDMIIRQ_EVE2 DISABLED
WKUPDEP_HDMIIRQ_EVE1 DISABLED WKUPDEP_HDMIIRQ_DSP2 DISABLED WKUPDEP_HDMIIRQ_IPU1 DISABLED
WKUPDEP_HDMIIRQ_DSP1 DISABLED WKUPDEP_HDMIIRQ_IPU2 DISABLED WKUPDEP_HDMIIRQ_MPU DISABLED
RM_DSS_BB2D_CONTEXT 00000101 LOSTMEM_DSS_MEM LOST LOSTCONTEXT_DFF LOST

GPU_PRM
PM_GPU_PWRSTCTRL 00030000 GPU_MEM_ONSTATE MEM_ON LOWPOWERSTATECHANGE DIS POWERSTATE OFF
PM_GPU_PWRSTST 00000000 LASTPOWERSTATEENTERED OFF INTRANSITION NO GPU_MEM_STATEST MEM_OFF
LOGICSTATEST OFF POWERSTATEST OFF
RM_GPU_GPU_CONTEXT 00000101 LOSTMEM_GPU_MEM LOST LOSTCONTEXT_DFF LOST

COREAON_PRM
PM_COREAON_SMARTREFLEX_MPU_WKDEP 00000003 WKUPDEP_SMARTREFLEX_MPU_EVE2 DISABLED WKUPDEP_SMARTREFLEX_MPU_EVE1 DISABLED WKUPDEP_SMARTREFLEX_MPU_DSP2 DISABLED
WKUPDEP_SMARTREFLEX_MPU_IPU1 DISABLED WKUPDEP_SMARTREFLEX_MPU_DSP1 DISABLED WKUPDEP_SMARTREFLEX_MPU_IPU2 ENABLED
WKUPDEP_SMARTREFLEX_MPU_MPU ENABLED
RM_COREAON_SMARTREFLEX_MPU_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_COREAON_SMARTREFLEX_CORE_WKDEP 00000000 WKUPDEP_SMARTREFLEX_CORE_EVE2 DISABLED WKUPDEP_SMARTREFLEX_CORE_EVE1 DISABLED WKUPDEP_SMARTREFLEX_CORE_DSP2 DISABLED
WKUPDEP_SMARTREFLEX_CORE_IPU1 DISABLED WKUPDEP_SMARTREFLEX_CORE_DSP1 DISABLED WKUPDEP_SMARTREFLEX_CORE_IPU2 DISABLED
WKUPDEP_SMARTREFLEX_CORE_MPU DISABLED
RM_COREAON_SMARTREFLEX_CORE_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
PM_COREAON_SMARTREFLEX_GPU_WKDEP 00000000 WKUPDEP_SMARTREFLEX_GPU_EVE2 DISABLED WKUPDEP_SMARTREFLEX_GPU_EVE1 DISABLED WKUPDEP_SMARTREFLEX_GPU_DSP2 DISABLED
WKUPDEP_SMARTREFLEX_GPU_IPU1 DISABLED WKUPDEP_SMARTREFLEX_GPU_DSP1 DISABLED WKUPDEP_SMARTREFLEX_GPU_IPU2 DISABLED
WKUPDEP_SMARTREFLEX_GPU_MPU DISABLED
RM_COREAON_SMARTREFLEX_GPU_CONTEXT 00000001 LOSTCONTEXT_DFF LOST
PM_COREAON_SMARTREFLEX_DSPEVE_WKDEP 00000000 WKUPDEP_SMARTREFLEX_DSPEVE_EVE2 DISABLED WKUPDEP_SMARTREFLEX_DSPEVE_EVE1 DISABLED WKUPDEP_SMARTREFLEX_DSPEVE_DSP2 DISABLED
WKUPDEP_SMARTREFLEX_DSPEVE_IPU1 DISABLED WKUPDEP_SMARTREFLEX_DSPEVE_SDMA DISABLED WKUPDEP_SMARTREFLEX_DSPEVE_DSP1 DISABLED
WKUPDEP_SMARTREFLEX_DSPEVE_IPU2 DISABLED WKUPDEP_SMARTREFLEX_DSPEVE_MPU DISABLED
RM_COREAON_SMARTREFLEX_DSPEVE_CONTEXT 00000001 LOSTCONTEXT_DFF LOST
PM_COREAON_SMARTREFLEX_IVAHD_WKDEP 00000000 WKUPDEP_SMARTREFLEX_IVAHD_EVE2 DISABLED WKUPDEP_SMARTREFLEX_IVAHD_EVE1 DISABLED WKUPDEP_SMARTREFLEX_IVAHD_DSP2 DISABLED
WKUPDEP_SMARTREFLEX_IVAHD_IPU1 DISABLED WKUPDEP_SMARTREFLEX_IVAHD_DSP1 DISABLED WKUPDEP_SMARTREFLEX_IVAHD_IPU2 DISABLED
WKUPDEP_SMARTREFLEX_IVAHD_MPU DISABLED

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RM_COREAON_SMARTREFLEX_IVAHD_CONTEXT 00000001 LOSTCONTEXT_DFF LOST

CM_CORE__RESTORE

CM_L3MAIN1_CLKSTCTRL_RESTORE 00000303 RESTORE 00000303
CM_L4CFG_CLKSTCTRL_RESTORE 00000303 RESTORE 00000303
CM_L4PER_CLKSTCTRL_RESTORE 01A38503 RESTORE 01A38503
CM_L3INIT_CLKSTCTRL_RESTORE 01718F02 RESTORE 01718F02
CM_L3INSTR_L3_MAIN_2_CLKCTRL_RESTORE 00030000 RESTORE 00030000
CM_L3INSTR_L3_INSTR_CLKCTRL_RESTORE 00030000 RESTORE 00030000
CM_L3INSTR_OCP_WP_NOC_CLKCTRL_RESTORE 00030000 RESTORE 00030000
CM_CM_CORE_PROFILING_CLKCTRL_RESTORE 00030000 RESTORE 00030000
CM_L3MAIN1_DYNAMICDEP_RESTORE F4F4F51F RESTORE F4F4F51F
CM_L4CFG_DYNAMICDEP_RESTORE 040B08B0 RESTORE 040B08B0
CM_L4PER_DYNAMICDEP_RESTORE 04004188 RESTORE 04004188
CM_DMA_STATICDEP_RESTORE 00000020 RESTORE 00000020

EVE2_PRM

PM_EVE2_PWRSTCTRL 00030000 EVE2_BANK_ONSTATE MEM_ON LOWPOWERSTATECHANGE DIS POWERSTATE OFF
PM_EVE2_PWRSTST 00000000 LASTPOWERSTATEENTERED OFF INTRANSITION NO EVE2_BANK_STATEST MEM_OFF
LOGICSTATEST OFF POWERSTATEST OFF
RM_EVE2_RSTCTRL 00000003 RST_EVE2 ASSERT RST_EVE2_LRST ASSERT
RM_EVE2_RSTST 00000000 RST_EVE2_EMU_REQ RESET_NO RST_EVE2_EMU RESET_NO RST_EVE2 RESET_NO
RST_EVE2_LRST RESET_NO
PM_EVE2_EVE2_WKDEP 00000000 WKUPDEP_EVE2_EVE1 DISABLED WKUPDEP_EVE2_DSP2 DISABLED WKUPDEP_EVE2_IPU1 DISABLED
WKUPDEP_EVE2_SDMA DISABLED WKUPDEP_EVE2_DSP1 DISABLED WKUPDEP_EVE2_IPU2 DISABLED
WKUPDEP_EVE2_MPU DISABLED
RM_EVE2_EVE2_CONTEXT 00000101 LOSTMEM_EVE_BANK LOST LOSTCONTEXT_DFF LOST

SMARTREFLEX_MPU

SMARTREFLEX_MPU

SRCONFIG 00000000 ACCUMDATA 0000 SRCLKLENGTH 0000 SRENABLE 0
SENENABLE 0 ERRORGENERATORENABLE 0 MINMAXAVGENABLE 0
SENNENABLE 0 SENPENABLE 0
SRSTATUS 00000000 AVGERRVALID 0 MINMAXAVGVALID 0 ERRORGENERATORVALID 0
MINMAXAVGACCUMVALID 0
SENVAL 00000000 SENPVAL 0000 SENNVAL 0000
SENMIN 00000000 SENPMIN 0000 SENNMIN 0000
SENMAX 00000000 SENPMAX 0000 SENNMAX 0000
SENAVG 00000000 SENPAVG 0000 SENNAVG 0000
AVGWEIGHT 00000000 SENPAVGWEIGHT1 0000 SENNAVGWEIGHT 0000
NVALUERECIPROCAL 00000000 SENPGAIN 0 SENNGAIN 0 SENPRN 00
SENNRN 00
IRQ_EOI 00000000 EOI 0
IRQSTATUS_RAW 00000000 MCUACCUMINTSTATRAW 0 MCUVALIDINTSTATRAW 0 MCUBOUNDSINTSTATRAW 0
MCUDISABLEACKINTSTATRAW 0
IRQSTATUS 00000000 MCUACCUMINTSTATENA 0 MCUVALIDINTSTATENA 0 MCUBOUNDSINTSTATENA 0
MCUDISABLEACKINTSTATENA 0
IRQENABLE_SET 00000000 MCUACCUMINTENASET 0 MCUVALIDINTENASET 0 MCUBOUNDSINTENASET 0
MCUDISABLEACKINTENASET 0
IRQENABLE_CLR 00000000 MCUACCUMINTENACL 0 MCUVALIDINTENACL 0 MCUBOUNDSINTENACL 0
MCUDISABLEACKINTENACL 0
SENEROR 00000000 AVGERROR 00 SENEROR 00
ERRCONFIG 00000000 WAKEUPENABLE 0 IDLEMODE 0 VPBOUNDSINTSTATENA 0
VPBOUNDSINTENABLE 0 ERRWEIGHT 0 ERRMAXLIMIT 00
ERRMINLIMIT 00

SMARTREFLEX_CORE

SRCONFIG 00000000 ACCUMDATA 0000 SRCLKLENGTH 0000 SRENABLE 0
SENENABLE 0 ERRORGENERATORENABLE 0 MINMAXAVGENABLE 0
SENNENABLE 0 SENPENABLE 0
SRSTATUS 00000000 AVGERRVALID 0 MINMAXAVGVALID 0 ERRORGENERATORVALID 0
MINMAXAVGACCUMVALID 0
SENVAL 00000000 SENPVAL 0000 SENNVAL 0000
SENMIN 00000000 SENPMIN 0000 SENNMIN 0000
SENMAX 00000000 SENPMAX 0000 SENNMAX 0000
SENAVG 00000000 SENPAVG 0000 SENNAVG 0000
AVGWEIGHT 00000000 SENPAVGWEIGHT1 0000 SENNAVGWEIGHT 0000
NVALUERECIPROCAL 00000000 SENPGAIN 0 SENNGAIN 0 SENPRN 00
SENNRN 00
IRQ_EOI 00000000 EOI 0
IRQSTATUS_RAW 00000000 MCUACCUMINTSTATRAW 0 MCUVALIDINTSTATRAW 0 MCUBOUNDSINTSTATRAW 0
MCUDISABLEACKINTSTATRAW 0
IRQSTATUS 00000000 MCUACCUMINTSTATENA 0 MCUVALIDINTSTATENA 0 MCUBOUNDSINTSTATENA 0
MCUDISABLEACKINTSTATENA 0
IRQENABLE_SET 00000000 MCUACCUMINTENASET 0 MCUVALIDINTENASET 0 MCUBOUNDSINTENASET 0
MCUDISABLEACKINTENASET 0
IRQENABLE_CLR 00000000 MCUACCUMINTENACL 0 MCUVALIDINTENACL 0 MCUBOUNDSINTENACL 0
MCUDISABLEACKINTENACL 0
SENEROR 00000000 AVGERROR 00 SENEROR 00
ERRCONFIG 00000000 WAKEUPENABLE 0 IDLEMODE 0 VPBOUNDSINTSTATENA 0
VPBOUNDSINTENABLE 0 ERRWEIGHT 0 ERRMAXLIMIT 00
ERRMINLIMIT 00

SMARTREFLEX_DSPEVE

SRCONFIG 00000000 ACCUMDATA 0000 SRCLKLENGTH 0000 SRENABLE 0
SENENABLE 0 ERRORGENERATORENABLE 0 MINMAXAVGENABLE 0
SENNENABLE 0 SENPENABLE 0
SRSTATUS 00000000 AVGERRVALID 0 MINMAXAVGVALID 0 ERRORGENERATORVALID 0
MINMAXAVGACCUMVALID 0
SENVAL 00000000 SENPVAL 0000 SENNVAL 0000
SENMIN 00000000 SENPMIN 0000 SENNMIN 0000
SENMAX 00000000 SENPMAX 0000 SENNMAX 0000


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SENAVG      00000000 SENPAVG      0000 SENNAVG      0000
AVGWEIGHT  00000000 SENPAVGWEIGHT1 0000 SENNAVGWEIGHT 0000
NVALUERECIPROCAL 00000000 SENPGAIN 0 SENNGAIN 0 SENPRN 00
SENNRN      00
IRQ_EOI     00000000 EOI 0
IRQSTATUS_RAW 00000000 MCUACCUMINTSTATRAW 0 MCUVALIDINTSTATRAW 0 MCUBOUNDSINTSTATRAW 0
MCUDISABLEACKINTSTATRAW 0
IRQSTATUS  00000000 MCUACCUMINTSTATENA 0 MCUVALIDINTSTATENA 0 MCUBOUNDSINTSTATENA 0
MCUDISABLEACKINTSTATENA 0
IRQENABLE_SET 00000000 MCUACCUMINTENASET 0 MCUVALIDINTENASET 0 MCUBOUNDSINTENASET 0
MCUDISABLEACKINTENASET 0
IRQENABLE_CLR 00000000 MCUACCUMINTENACL 0 MCUVALIDINTENACL 0 MCUBOUNDSINTENACL 0
MCUDISABLEACKINTENACL 0
SENERROR   00000000 AVGERROR 00 SENERROR 00
ERRCONFIG  00000000 WAKEUPENABLE 0 IDLEMODE 0 VPBOUNDSINTSTATENA 0
VPBOUNDSINTENABLE 0 ERRWEIGHT 0 ERRMAXLIMIT 00
ERRMINLIMIT 00

```

SMARTREFLEX_GPU

```

SRCONFIG  00000000 ACCUMDATA 0000 SRCLKLENGTH 0000 SRENABLE 0
SENENABLE 0 ERRORGENERATORENABLE 0 MINMAXAVGENABLE 0
SENNENABLE 0 SENPENABLE 0
SRSTATUS  00000000 AVGERRVALID 0 MINMAXAVGVALID 0 ERRORGENERATORVALID 0
MINMAXAVGACCUMVALID 0
SENVAL    00000000 SENPVAL 0000 SENNVAL 0000
SENMIN    00000000 SENPMIN 0000 SENNMIN 0000
SENMAX    00000000 SENPMAX 0000 SENNMAX 0000
SENAVG    00000000 SENPAVG 0000 SENNAVG 0000
AVGWEIGHT 00000000 SENPAVGWEIGHT1 0000 SENNAVGWEIGHT 0000
NVALUERECIPROCAL 00000000 SENPGAIN 0 SENNGAIN 0 SENPRN 00
SENNRN      00
IRQ_EOI     00000000 EOI 0
IRQSTATUS_RAW 00000000 MCUACCUMINTSTATRAW 0 MCUVALIDINTSTATRAW 0 MCUBOUNDSINTSTATRAW 0
MCUDISABLEACKINTSTATRAW 0
IRQSTATUS  00000000 MCUACCUMINTSTATENA 0 MCUVALIDINTSTATENA 0 MCUBOUNDSINTSTATENA 0
MCUDISABLEACKINTSTATENA 0
IRQENABLE_SET 00000000 MCUACCUMINTENASET 0 MCUVALIDINTENASET 0 MCUBOUNDSINTENASET 0
MCUDISABLEACKINTENASET 0
IRQENABLE_CLR 00000000 MCUACCUMINTENACL 0 MCUVALIDINTENACL 0 MCUBOUNDSINTENACL 0
MCUDISABLEACKINTENACL 0
SENERROR   00000000 AVGERROR 00 SENERROR 00
ERRCONFIG  00000000 WAKEUPENABLE 0 IDLEMODE 0 VPBOUNDSINTSTATENA 0
VPBOUNDSINTENABLE 0 ERRWEIGHT 0 ERRMAXLIMIT 00
ERRMINLIMIT 00

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SMARTREFLEX_IVA

```

SRCONFIG  00000000 ACCUMDATA 0000 SRCLKLENGTH 0000 SRENABLE 0
SENENABLE 0 ERRORGENERATORENABLE 0 MINMAXAVGENABLE 0
SENNENABLE 0 SENPENABLE 0
SRSTATUS  00000000 AVGERRVALID 0 MINMAXAVGVALID 0 ERRORGENERATORVALID 0
MINMAXAVGACCUMVALID 0
SENVAL    00000000 SENPVAL 0000 SENNVAL 0000
SENMIN    00000000 SENPMIN 0000 SENNMIN 0000
SENMAX    00000000 SENPMAX 0000 SENNMAX 0000
SENAVG    00000000 SENPAVG 0000 SENNAVG 0000
AVGWEIGHT 00000000 SENPAVGWEIGHT1 0000 SENNAVGWEIGHT 0000
NVALUERECIPROCAL 00000000 SENPGAIN 0 SENNGAIN 0 SENPRN 00
SENNRN      00
IRQ_EOI     00000000 EOI 0
IRQSTATUS_RAW 00000000 MCUACCUMINTSTATRAW 0 MCUVALIDINTSTATRAW 0 MCUBOUNDSINTSTATRAW 0
MCUDISABLEACKINTSTATRAW 0
IRQSTATUS  00000000 MCUACCUMINTSTATENA 0 MCUVALIDINTSTATENA 0 MCUBOUNDSINTSTATENA 0
MCUDISABLEACKINTSTATENA 0
IRQENABLE_SET 00000000 MCUACCUMINTENASET 0 MCUVALIDINTENASET 0 MCUBOUNDSINTENASET 0
MCUDISABLEACKINTENASET 0
IRQENABLE_CLR 00000000 MCUACCUMINTENACL 0 MCUVALIDINTENACL 0 MCUBOUNDSINTENACL 0
MCUDISABLEACKINTENACL 0
SENERROR   00000000 AVGERROR 00 SENERROR 00
ERRCONFIG  00000000 WAKEUPENABLE 0 IDLEMODE 0 VPBOUNDSINTSTATENA 0
VPBOUNDSINTENABLE 0 ERRWEIGHT 0 ERRMAXLIMIT 00
ERRMINLIMIT 00

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CKGEN_PRM

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CM_CLKSEL_SYSCLK1 00000000 CLKSEL SYSCLK_DIV_6
CM_CLKSEL_WKUPAON 00000000 CLKSEL SEL_SYS_CLK
CM_CLKSEL_ABE_PLL_REF 00000000 CLKSEL SEL_SYS_CLK
CM_CLKSEL_SYS 00000002 SYS_CLKSEL RESERVED
CM_CLKSEL_ABE_PLL_BYPAS 00000000 CLKSEL SEL_SYS_CLK
CM_CLKSEL_ABE_PLL_SYS 00000001 CLKSEL SEL_SYS_CLK2
CM_CLKSEL_ABE_24M 00000000 CLKSEL SYSCLK_DIV_8
CM_CLKSEL_ABE_SYS 00000000 CLKSEL SYSCLK_DIV_1
CM_CLKSEL_HDMI_MCASP_AUX 00000000 CLKSEL CLK_DIV_1
CM_CLKSEL_HDMI_TIMER 00000000 CLKSEL CLK_DIV_1
CM_CLKSEL_MCASP_SYS 00000000 CLKSEL SYSCLK_DIV_8
CM_CLKSEL_MLBP_MCASP 00000000 CLKSEL CLK_DIV_1
CM_CLKSEL_MLB_MCASP 00000000 CLKSEL CLK_DIV_1
CM_CLKSEL_PER_ABE_X1_GFCLK_MCASP_AUX 00000000 CLKSEL CLK_DIV_1
CM_CLKSEL_SYS_CLK1_32K 00000000 CLKSEL SEL_SYS_CLK1
CM_CLKSEL_TIMER_SYS 00000000 CLKSEL SYSCLK_DIV_1
CM_CLKSEL_VIDEO1_MCASP_AUX 00000000 CLKSEL CLK_DIV_1
CM_CLKSEL_VIDEO1_TIMER 00000000 CLKSEL CLK_DIV_1
CM_CLKSEL_VIDEO2_MCASP_AUX 00000000 CLKSEL CLK_DIV_1
CM_CLKSEL_VIDEO2_TIMER 00000000 CLKSEL CLK_DIV_1

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CM_CLKSEL_CLKOUTMUX0 00000000 CLKSEL SEL_SYS_CLK1
 CM_CLKSEL_CLKOUTMUX1 00000000 CLKSEL SEL_SYS_CLK1
 CM_CLKSEL_CLKOUTMUX2 00000000 CLKSEL SEL_SYS_CLK1
 CM_CLKSEL_HDMI_PLL_SYS 00000000 CLKSEL SEL_SYS_CLK1
 CM_CLKSEL_VIDEO1_PLL_SYS 00000000 CLKSEL SEL_SYS_CLK1
 CM_CLKSEL_VIDEO2_PLL_SYS 00000000 CLKSEL SEL_SYS_CLK1
 CM_CLKSEL_ABE_CLK_DIV 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_ABE_GICLK_DIV 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_AESS_FCLK_DIV 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_EVE_CLK 00000000 CLKSEL SEL_EVE_GFCLK
 CM_CLKSEL_USB_OTG_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_CORE_DPLL_OUT_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_DSP_GFCLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_EMIF_PHY_GCLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_EMU_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_FUNC_96M_AON_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_GMAC_250M_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_GPU_GCLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_HDMI_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_IVA_GCLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_L3INIT_480M_GFCLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_MPU_GCLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_PCIE1_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_PCIE2_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_PER_ABE_X1_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_SATA_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_SYS_CLK1_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_SYS_CLK2_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_VIDEO1_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_VIDEO2_CLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1
 CM_CLKSEL_ABE_LP_CLK 00000000 CLKSEL CLK_DIV_16
 CM_CLKSEL_EVE_GFCLK_CLKOUTMUX 00000000 CLKSEL CLK_DIV_1

CAM_PRM

PM_CAM_PWRSTCTRL 00030000 VIP_BANK_ONSTATE MEM_ON LOWPOWERSTATECHANGE DIS POWERSTATE OFF
 PM_CAM_PWRSTST 00000037 LASTPOWERSTATEENTERED OFF INTRANSITION NO VIP_BANK_STATEST MEM_ON
 LOGICSTATEST ON POWERSTATEST ON
 PM_CAM_VIP1_WKDEP 00000000 WKUPDEP_VIP1_EVE2 DISABLED WKUPDEP_VIP1_EVE1 DISABLED WKUPDEP_VIP1_DSP2 DISABLED
 WKUPDEP_VIP1_IPU1 DISABLED WKUPDEP_VIP1_DSP1 DISABLED WKUPDEP_VIP1_IPU2 DISABLED
 WKUPDEP_VIP1_MPU DISABLED
 RM_CAM_VIP1_CONTEXT 00000000 LOSTMEM_VIP_BANK MAINTAINED LOSTCONTEXT_DFF MAINTAINED
 PM_CAM_VIP2_WKDEP 00000000 WKUPDEP_VIP2_EVE2 DISABLED WKUPDEP_VIP2_EVE1 DISABLED WKUPDEP_VIP2_DSP2 DISABLED
 WKUPDEP_VIP2_IPU1 DISABLED WKUPDEP_VIP2_DSP1 DISABLED WKUPDEP_VIP2_IPU2 DISABLED
 WKUPDEP_VIP2_MPU DISABLED
 RM_CAM_VIP2_CONTEXT 00000101 LOSTMEM_VIP_BANK LOST LOSTCONTEXT_DFF LOST
 PM_CAM_VIP3_WKDEP 00000000 WKUPDEP_VIP3_EVE2 DISABLED WKUPDEP_VIP3_EVE1 DISABLED WKUPDEP_VIP3_DSP2 DISABLED
 WKUPDEP_VIP3_IPU1 DISABLED WKUPDEP_VIP3_DSP1 DISABLED WKUPDEP_VIP3_IPU2 DISABLED
 WKUPDEP_VIP3_MPU DISABLED
 RM_CAM_VIP3_CONTEXT 00000101 LOSTMEM_VIP_BANK LOST LOSTCONTEXT_DFF LOST

CM_CORE_L4PER

CM_L4PER_CLKSTCTRL 01A38503 CLKACTIVITY_L4PER_32K_GFCLK INACT CLKACTIVITY_UART5_GFCLK INACT CLKACTIVITY_GPIO_GFCLK ACT
 CLKACTIVITY_MMCM4_GFCLK ACT CLKACTIVITY_MMCM3_GFCLK INACT CLKACTIVITY_PER_96M_GFCLK ACT
 CLKACTIVITY_PER_48M_GFCLK INACT CLKACTIVITY_PER_12M_GFCLK INACT CLKACTIVITY_UART4_GFCLK INACT
 CLKACTIVITY_UART3_GFCLK ACT CLKACTIVITY_UART2_GFCLK ACT CLKACTIVITY_UART1_GFCLK ACT
 CLKACTIVITY_TIMER9_GFCLK INACT CLKACTIVITY_TIMER4_GFCLK INACT CLKACTIVITY_TIMER3_GFCLK INACT
 CLKACTIVITY_TIMER2_GFCLK INACT CLKACTIVITY_TIMER11_GFCLK ACT CLKACTIVITY_TIMER10_GFCLK INACT
 CLKACTIVITY_L4PER_L3_GICLK ACT CLKTRCTRL HW_AUTO
 CM_L4PER_DYNAMICIDEP 04004188 WINDOWSIZE 4 L4SEC_DYNDEP ENABLED DSS_DYNDEP ENABLED
 L3INIT_DYNDEP ENABLED IPU_DYNDEP ENABLED
 CM_L4PER2_L4_PER2_CLKCTRL 00000001 IDLEST FUNC MODULEMODE AUTO
 CM_L4PER3_L4_PER3_CLKCTRL 00020001 IDLEST IDLE MODULEMODE AUTO
 CM_L4PER_TIMER10_CLKCTRL 00030000 CLKSEL SEL_TIMER_SYS_CLK IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_TIMER11_CLKCTRL 00020002 CLKSEL SEL_TIMER_SYS_CLK IDLEST IDLE MODULEMODE ENABLE
 CM_L4PER_TIMER2_CLKCTRL 00030000 CLKSEL SEL_TIMER_SYS_CLK IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_TIMER3_CLKCTRL 00030000 CLKSEL SEL_TIMER_SYS_CLK IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_TIMER4_CLKCTRL 00030000 CLKSEL SEL_TIMER_SYS_CLK IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_TIMER9_CLKCTRL 00030000 CLKSEL SEL_TIMER_SYS_CLK IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_ELM_CLKCTRL 00020001 IDLEST IDLE MODULEMODE AUTO
 CM_L4PER_GPIO2_CLKCTRL 00030000 IDLEST DISABLE OPTFCLKEN_DBCLK FCLK_DIS MODULEMODE DISABLED
 CM_L4PER_GPIO3_CLKCTRL 00030000 IDLEST DISABLE OPTFCLKEN_DBCLK FCLK_DIS MODULEMODE DISABLED
 CM_L4PER_GPIO4_CLKCTRL 00030000 IDLEST DISABLE OPTFCLKEN_DBCLK FCLK_DIS MODULEMODE DISABLED
 CM_L4PER_GPIO5_CLKCTRL 00020001 IDLEST IDLE OPTFCLKEN_DBCLK FCLK_DIS MODULEMODE AUTO
 CM_L4PER_GPIO6_CLKCTRL 00020001 IDLEST IDLE OPTFCLKEN_DBCLK FCLK_DIS MODULEMODE AUTO
 CM_L4PER_HDQ1W_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER2_PWMSS2_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER2_PWMSS3_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_I2C1_CLKCTRL 00020002 IDLEST IDLE MODULEMODE ENABLE
 CM_L4PER_I2C2_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_I2C3_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_I2C4_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_L4_PER1_CLKCTRL 00020001 IDLEST IDLE MODULEMODE AUTO
 CM_L4PER2_PWMSS1_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER3_TIMER13_CLKCTRL 00030000 CLKSEL SEL_TIMER_SYS_CLK IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER3_TIMER14_CLKCTRL 00020002 CLKSEL SEL_TIMER_SYS_CLK IDLEST IDLE MODULEMODE ENABLE
 CM_L4PER3_TIMER15_CLKCTRL 00030000 CLKSEL SEL_TIMER_SYS_CLK IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_MCSPI1_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_MCSPI2_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_MCSPI3_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_MCSPI4_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_L4PER_GPIO7_CLKCTRL 00020101 IDLEST IDLE OPTFCLKEN_DBCLK FCLK_EN MODULEMODE AUTO
 CM_L4PER_GPIO8_CLKCTRL 00030000 IDLEST DISABLE OPTFCLKEN_DBCLK FCLK_DIS MODULEMODE DISABLED
 CM_L4PER_MMCM3_CLKCTRL 00030000 CLKSEL_DIV MMCCCLK_DIV_1 CLKSEL_MUX SEL_FUNC_48M_CLK IDLEST DISABLE

CM_L4PER_MM4_CLKCTRL	00020002	CLKSEL_DIV	MMCCCLK_DIV_1	CLKSEL_MUX	SEL_FUNC_48M_CLK	IDLEST	IDLE
CM_L4PER3_TIMER16_CLKCTRL	07030000	CLKSEL	SEL_PER_ABE_X1_GFCLK	IDLEST	DISABLE	MODULEMODE	DISABLED
CM_L4PER2_QSPI_CLKCTRL	01030000	CLKSEL_DIV	DIV1	CLKSEL_SOURCE	SEL_PER_QSPI_CLK	IDLEST	DISABLE
CM_L4PER_UART1_CLKCTRL	00010002	CLKSEL	SEL_FUNC_48M_CLK	IDLEST	TRANS	MODULEMODE	ENABLE
CM_L4PER_UART2_CLKCTRL	00010002	CLKSEL	SEL_FUNC_48M_CLK	IDLEST	TRANS	MODULEMODE	ENABLE
CM_L4PER_UART3_CLKCTRL	00010002	CLKSEL	SEL_FUNC_48M_CLK	IDLEST	TRANS	MODULEMODE	ENABLE
CM_L4PER_UART4_CLKCTRL	00030000	CLKSEL	SEL_FUNC_48M_CLK	IDLEST	DISABLE	MODULEMODE	DISABLED
CM_L4PER2_MCASP2_CLKCTRL	00030000	CLKSEL_AHCLKR	SEL_ABE_24M_GFCLK	CLKSEL_AHCLKR	SEL_ABE_24M_GFCLK	CLKSEL_AUX_CLK	SEL_PER_ABE
CM_L4PER2_MCASP3_CLKCTRL	04030000	CLKSEL_AHCLKX	SEL_ATL_CLK2	CLKSEL_AUX_CLK	SEL_PER_ABE_X1_GFCLK	IDLEST	DISABLE
CM_L4PER_UART5_CLKCTRL	00030000	CLKSEL	SEL_FUNC_48M_CLK	IDLEST	DISABLE	MODULEMODE	DISABLED
CM_L4PER2_MCASP5_CLKCTRL	00030000	CLKSEL_AHCLKX	SEL_ABE_24M_GFCLK	CLKSEL_AUX_CLK	SEL_PER_ABE_X1_GFCLK	IDLEST	DISABLE
CM_L4SEC_CLKSTCTRL	00000102	CLKACTIVITY_L4SEC_L3_GICLK	ACT	CLKTRCTRL	SW_WKUP		
CM_L4SEC_STATICDEP	00000020	L4PER_STATDEP	DISABLED	L3MAIN1_STATDEP	ENABLED	EMIF_STATDEP	DISABLED
CM_L4SEC_DYNAMICDEP	00000000	L3MAIN1_DYNDEP	DISABLED				
CM_L4PER2_MCASP8_CLKCTRL	00000002	CLKSEL_AHCLKX	SEL_ABE_24M_GFCLK	CLKSEL_AUX_CLK	SEL_PER_ABE_X1_GFCLK	IDLEST	FUNC
CM_L4PER2_MCASP4_CLKCTRL	00030000	CLKSEL_AHCLKX	SEL_ABE_24M_GFCLK	CLKSEL_AUX_CLK	SEL_PER_ABE_X1_GFCLK	IDLEST	DISABLE
CM_L4SEC_AES1_CLKCTRL	00030000	IDLEST	DISABLE	MODULEMODE	DISABLED		
CM_L4SEC_AES2_CLKCTRL	00030000	IDLEST	DISABLE	MODULEMODE	DISABLED		
CM_L4SEC_DES3DES_CLKCTRL	00030000	IDLEST	DISABLE	MODULEMODE	DISABLED		
CM_L4SEC_FPKA_CLKCTRL	00030000	IDLEST	DISABLE	MODULEMODE	DISABLED		
CM_L4SEC_RNG_CLKCTRL	00000001	IDLEST	FUNC	MODULEMODE	AUTO		
CM_L4SEC_SHA2MD51_CLKCTRL	00030000	IDLEST	DISABLE	MODULEMODE	DISABLED		
CM_L4PER2_UART7_CLKCTRL	00030000	CLKSEL	SEL_FUNC_48M_CLK	IDLEST	DISABLE	MODULEMODE	DISABLED
CM_L4SEC_DMA_CRYPTO_CLKCTRL	00040001	STBYST	STANDBY	IDLEST	FUNC	MODULEMODE	AUTO
CM_L4PER2_UART8_CLKCTRL	00030000	CLKSEL	SEL_FUNC_48M_CLK	IDLEST	DISABLE	MODULEMODE	DISABLED
CM_L4PER2_UART9_CLKCTRL	00030000	CLKSEL	SEL_FUNC_48M_CLK	IDLEST	DISABLE	MODULEMODE	DISABLED
CM_L4PER2_DCAN2_CLKCTRL	00030000	IDLEST	DISABLE	MODULEMODE	DISABLED		
CM_L4SEC_SHA2MD52_CLKCTRL	00030000	IDLEST	DISABLE	MODULEMODE	DISABLED		
CM_L4PER2_CLKSTCTRL	C0010002	CLKACTIVITY_MCASP8_AUX_GFCLK	ACT	CLKACTIVITY_MCASP8_AHCLKX	ACT	CLKACTIVITY_MCASP7_AUX_GFCLK	INACT
		CLKACTIVITY_MCASP7_AHCLKX	INACT	CLKACTIVITY_MCASP6_AUX_GFCLK	INACT	CLKACTIVITY_MCASP6_AHCLKX	INACT
		CLKACTIVITY_MCASP5_AHCLKX	INACT	CLKACTIVITY_MCASP5_AUX_GFCLK	INACT	CLKACTIVITY_MCASP4_AUX_GFCLK	INACT
		CLKACTIVITY_MCASP4_AHCLKX	INACT	CLKACTIVITY_MCASP3_AUX_GFCLK	INACT	CLKACTIVITY_MCASP3_AHCLKX	INACT
		CLKACTIVITY_MCASP2_AUX_GFCLK	INACT	CLKACTIVITY_MCASP2_AHCLKR	INACT	CLKACTIVITY_MCASP2_AHCLKX	INACT
		CLKACTIVITY_L4PER2_L3_GICLK	ACT	CLKACTIVITY_DCAN2_SYS_CLK	INACT	CLKACTIVITY_ICSS_IEP_CLK	INACT
		CLKACTIVITY_PER_192M_GFCLK	INACT	CLKACTIVITY_QSPI_GFCLK	INACT	CLKACTIVITY_UART9_GFCLK	INACT
		CLKACTIVITY_UART8_GFCLK	INACT	CLKACTIVITY_UART7_GFCLK	INACT	CLKACTIVITY_ICSS_CLK	INACT
		CLKTRCTRL	SW_WKUP				
CM_L4PER2_DYNAMICDEP	044010C8	WINDOWSIZE	4	GMAC_DYNDEP	ENABLED	L4CFG_DYNDEP	ENABLED
		L3INIT_DYNDEP	ENABLED	ATL_DYNDEP	ENABLED	IPU_DYNDEP	ENABLED
CM_L4PER2_MCASP6_CLKCTRL	00030000	CLKSEL_AHCLKX	SEL_ABE_24M_GFCLK	CLKSEL_AUX_CLK	SEL_PER_ABE_X1_GFCLK	IDLEST	DISABLE
CM_L4PER2_MCASP7_CLKCTRL	00030000	CLKSEL_AHCLKX	SEL_ABE_24M_GFCLK	CLKSEL_AUX_CLK	SEL_PER_ABE_X1_GFCLK	IDLEST	DISABLE
CM_L4PER2_STATICDEP	00000020	IPU1_STATDEP	DISABLED	DSP2_STATDEP	DISABLED	L3MAIN1_STATDEP	ENABLED
		DSP1_STATDEP	DISABLED	IPU2_STATDEP	DISABLED		
CM_L4PER3_CLKSTCTRL	00000403	CLKACTIVITY_TIMER16_GFCLK	INACT	CLKACTIVITY_TIMER15_GFCLK	INACT	CLKACTIVITY_TIMER14_GFCLK	ACT
		CLKACTIVITY_TIMER13_GFCLK	INACT	CLKACTIVITY_L4PER3_L3_GICLK	INACT	CLKTRCTRL	HW_AUTO
CM_L4PER3_DYNAMICDEP	848012A8	VPE_DYNDEP	ENABLED	WINDOWSIZE	4	RTC_DYNDEP	ENABLED
		L4CFG_DYNDEP	ENABLED	CAM_DYNDEP	ENABLED	L3INIT_DYNDEP	ENABLED
		L3MAIN1_DYNDEP	ENABLED	IPU_DYNDEP	ENABLED		
CM_CORE_AON_INSTR							
CMI_IDENTIFICATION	00000000	SCHEME	0	FUNC	0000	RTL	0
		MAJOR	0	CUSTOM	0	MINOR	0
CMI_SYS_CONFIG	00000000	IDLEMODE	0	SOFTRESET	0		
CMI_STATUS	00000000	FIFOEMPTY	0				
CMI_CONFIGURATION	00000000	CLAIM_3	0	CLAIM_2	0	CLAIM_1	0
		MOD_ACT_EN	0	EVT_CAPT_EN	0		
CMI_CLASS_FILTERING	00000000	SNAP_CAPT_EN_1F	0	SNAP_CAPT_EN_1E	0	SNAP_CAPT_EN_1D	0
		SNAP_CAPT_EN_1C	0	SNAP_CAPT_EN_1B	0	SNAP_CAPT_EN_1A	0
		SNAP_CAPT_EN_19	0	SNAP_CAPT_EN_18	0	SNAP_CAPT_EN_17	0
		SNAP_CAPT_EN_16	0	SNAP_CAPT_EN_15	0	SNAP_CAPT_EN_14	0
		SNAP_CAPT_EN_13	0	SNAP_CAPT_EN_12	0	SNAP_CAPT_EN_11	0
		SNAP_CAPT_EN_10	0	SNAP_CAPT_EN_03	0	SNAP_CAPT_EN_02	0
		SNAP_CAPT_EN_01	0	SNAP_CAPT_EN_00	0		
CMI_TRIGGERING	00000000	TRIG_STOP_EN	0	TRIG_START_EN	0		
CMI_SAMPLING	00000000	FCLK_DIV_FACTOR	0	SAMP_WIND_SIZE	00		
IVA_PRM							
PM_IVA_PWRSTCTRL	00FF0003	TCM2_MEM_ONSTATE	MEM_ON	TCM1_MEM_ONSTATE	MEM_ON	SL2_MEM_ONSTATE	MEM_ON
		HWA_MEM_ONSTATE	MEM_ON	TCM2_MEM_RETSTATE	MEM_OFF	TCM1_MEM_RETSTATE	MEM_OFF
		SL2_MEM_RETSTATE	MEM_OFF	HWA_MEM_RETSTATE	MEM_OFF	LOWPOWERSTATECHANGE	DIS
		LOGICRETSTATE	LOGIC_OFF	POWERSTATE	ON		
PM_IVA_PWRSTST	00000FF7	LASTPOWERSTATEENTERED	OFF	INTRANSITION	NO	TCM2_MEM_STATEST	MEM_ON
		TCM1_MEM_STATEST	MEM_ON	SL2_MEM_STATEST	MEM_ON	HWA_MEM_STATEST	MEM_ON
		LOGICSTATEST	ON	POWERSTATEST	ON		
RM_IVA_RSTCTRL	00000000	RST_LOGIC	CLEAR	RST_SEQ2	CLEAR	RST_SEQ1	CLEAR
RM_IVA_RSTST	00000007	RST_ICCCRUSHER_SEQ2	RESET_NO	RST_ICCCRUSHER_SEQ1	RESET_NO	RST_EMULATION_SEQ2	RESET_NO
		RST_EMULATION_SEQ1	RESET_NO	RST_LOGIC	RESET_YES	RST_SEQ2	RESET_YES
		RST_SEQ1	RESET_YES				
RM_IVA_IVA_CONTEXT	00000701	LOSTMEM_HWA_MEM	LOST	LOSTMEM_TCM2_MEM	LOST	LOSTMEM_TCM1_MEM	LOST
		LOSTCONTEXT_DFF	LOST				
RM_IVA_SL2_CONTEXT	00000101	LOSTMEM_SL2_MEM	LOST	LOSTCONTEXT_DFF	LOST		

DSP1_PRM

PM_DSP1_PWRSTCTRL 003F0000 DSP1_EDMA_ONSTATE MEM_ON DSP1_L2_ONSTATE MEM_ON DSP1_L1_ONSTATE MEM_ON
 LOWPOWERSTATECHANGE DIS **POWERSTATE OFF**
PM_DSP1_PWRSTST 00000000 LASTPOWERSTATEENTERED OFF INTRANSITION NO DSP1_EDMA_STATEST MEM_OFF
 DSP1_L2_STATEST MEM_OFF DSP1_L1_STATEST MEM_OFF LOGICSTATEST OFF
POWERSTATEST OFF
RM_DSP1_RSTCTRL 00000003 **RST_DSP1 ASSERT RST_DSP1_LRST ASSERT**
RM_DSP1_RSTST 00000003 **RST_DSP1_EMU_REQ RESET_NO RST_DSP1_EMU RESET_NO RST_DSP1 RESET_YES**
RST_DSP1_LRST RESET_YES
 RM_DSP1_DSP1_CONTEXT 00000701 LOSTMEM_DSP_EDMA LOST LOSTMEM_DSP_L2 LOST LOSTMEM_DSP_L1 LOST
 LOSTCONTEXT_DFF LOST

CORE_PRM

PM_CORE_PWRSTCTRL 03FF0F07 OCP_NRET_BANK_ONSTATE MEM_ON IPU_UNICACHE_ONSTATE MEM_ON IPU_L2RAM_ONSTATE MEM_ON
 CORE_OCMRAM_ONSTATE MEM_ON CORE_OTHER_BANK_ONSTATE MEM_ON OCP_NRET_BANK_RETSTATE MEM_OFF
 IPU_UNICACHE_RETSTATE MEM_RET IPU_L2RAM_RETSTATE MEM_RET CORE_OCMRAM_RETSTATE MEM_RET
 CORE_OTHER_BANK_RETSTATE MEM_RET LOWPOWERSTATECHANGE DIS LOGICRETSTATE LOGIC_RET
 POWERSTATE ON
PM_CORE_PWRSTST 00003FF7 LASTPOWERSTATEENTERED OFF INTRANSITION NO OCP_NRET_BANK_STATEST MEM_ON
 IPU_UNICACHE_STATEST MEM_ON IPU_L2RAM_STATEST MEM_ON CORE_OCMRAM_STATEST MEM_ON
 CORE_OTHER_BANK_STATEST MEM_ON LOGICSTATEST ON POWERSTATEST ON
 RM_L3MAIN1_L3_MAIN_1_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED LOSTCONTEXT_DFF MAINTAINED
 RM_L3MAIN1_GPMC_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L3MAIN1_MMU_EDMA_CONTEXT 00000002 LOSTCONTEXT_RFF LOST
 RM_L3MAIN1_MMU_PCIESS_CONTEXT 00000002 LOSTCONTEXT_RFF LOST
PM_L3MAIN1_OCMC_RAM1_WKDEP 00000000 WKUPDEP_OCMC_RAM1_EVE2 DISABLED WKUPDEP_OCMC_RAM1_EVE1 DISABLED WKUPDEP_OCMC_RAM1_DSP2 DISABLED
 WKUPDEP_OCMC_RAM1_IPU1 DISABLED WKUPDEP_OCMC_RAM1_DSP1 DISABLED WKUPDEP_OCMC_RAM1_IPU2 DISABLED
 WKUPDEP_OCMC_RAM1_MPU DISABLED
 RM_L3MAIN1_OCMC_RAM1_CONTEXT 00000101 LOSTMEM_CORE_OCMRAM LOST LOSTCONTEXT_DFF LOST
PM_L3MAIN1_OCMC_RAM2_WKDEP 00000000 WKUPDEP_OCMC_RAM2_EVE2 DISABLED WKUPDEP_OCMC_RAM2_EVE1 DISABLED WKUPDEP_OCMC_RAM2_DSP2 DISABLED
 WKUPDEP_OCMC_RAM2_IPU1 DISABLED WKUPDEP_OCMC_RAM2_DSP1 DISABLED WKUPDEP_OCMC_RAM2_IPU2 DISABLED
 WKUPDEP_OCMC_RAM2_MPU DISABLED
 RM_L3MAIN1_OCMC_RAM2_CONTEXT 00000101 LOSTMEM_CORE_OCMRAM LOST LOSTCONTEXT_DFF LOST
PM_L3MAIN1_OCMC_RAM3_WKDEP 00000000 WKUPDEP_OCMC_RAM3_EVE2 DISABLED WKUPDEP_OCMC_RAM3_EVE1 DISABLED WKUPDEP_OCMC_RAM3_DSP2 DISABLED
 WKUPDEP_OCMC_RAM3_IPU1 DISABLED WKUPDEP_OCMC_RAM3_DSP1 DISABLED WKUPDEP_OCMC_RAM3_IPU2 DISABLED
 WKUPDEP_OCMC_RAM3_MPU DISABLED
 RM_L3MAIN1_OCMC_RAM3_CONTEXT 00000101 LOSTMEM_CORE_OCMRAM LOST LOSTCONTEXT_DFF LOST
PM_L3MAIN1_TPCC_WKDEP 00000000 WKUPDEP_TPCC_EVE2 DISABLED WKUPDEP_TPCC_EVE1 DISABLED WKUPDEP_TPCC_DSP2 DISABLED
 WKUPDEP_TPCC_IPU1 DISABLED WKUPDEP_TPCC_DSP1 DISABLED WKUPDEP_TPCC_IPU2 DISABLED
 WKUPDEP_TPCC_MPU DISABLED
 RM_L3MAIN1_TPCC_CONTEXT 00000000 LOSTMEM_TPCC_BANK MAINTAINED LOSTCONTEXT_RFF MAINTAINED
PM_L3MAIN1_TPTC1_WKDEP 00000000 WKUPDEP_TPTC1_EVE2 DISABLED WKUPDEP_TPTC1_EVE1 DISABLED WKUPDEP_TPTC1_DSP2 DISABLED
 WKUPDEP_TPTC1_IPU1 DISABLED WKUPDEP_TPTC1_DSP1 DISABLED WKUPDEP_TPTC1_IPU2 DISABLED
 WKUPDEP_TPTC1_MPU DISABLED
 RM_L3MAIN1_TPTC1_CONTEXT 00000000 LOSTMEM_TPTC_BANK MAINTAINED LOSTCONTEXT_RFF MAINTAINED
PM_L3MAIN1_TPTC2_WKDEP 00000000 WKUPDEP_TPTC2_EVE2 DISABLED WKUPDEP_TPTC2_EVE1 DISABLED WKUPDEP_TPTC2_DSP2 DISABLED
 WKUPDEP_TPTC2_IPU1 DISABLED WKUPDEP_TPTC2_DSP1 DISABLED WKUPDEP_TPTC2_IPU2 DISABLED
 WKUPDEP_TPTC2_MPU DISABLED
 RM_L3MAIN1_TPTC2_CONTEXT 00000000 LOSTMEM_TPTC_BANK MAINTAINED LOSTCONTEXT_RFF MAINTAINED
 RM_L3MAIN1_VCP1_CONTEXT 00000000 LOSTMEM_VCP_BANK MAINTAINED LOSTCONTEXT_DFF MAINTAINED
 RM_L3MAIN1_VCP2_CONTEXT 00000000 LOSTMEM_VCP_BANK MAINTAINED LOSTCONTEXT_DFF MAINTAINED
RM_IPU2_RSTCTRL 00000007 **RST_IPU ASSERT RST_CPU1 ASSERT RST_CPU0 ASSERT**
RM_IPU2_RSTST 00000007 **RST_ICCRUSHER_CPU1 RESET_NO RST_ICCRUSHER_CPU0 RESET_NO RST_EMULATION_CPU1 RESET_YES**
RST_EMULATION_CPU0 RESET_NO RST_IPU RESET_YES RST_CPU1 RESET_YES
RST_CPU0 RESET_YES
 RM_IPU2_IPU2_CONTEXT 00000003 LOSTMEM_IPU_L2RAM MAINTAINED LOSTMEM_IPU_UNICACHE MAINTAINED LOSTCONTEXT_RFF LOST
 LOSTCONTEXT_DFF LOST
 RM_DMA_DMA_SYSTEM_CONTEXT 00000000 LOSTMEM_CORE_OTHER_BANK MAINTAINED LOSTCONTEXT_RFF MAINTAINED
 RM_EMIF_DMM_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED LOSTCONTEXT_DFF MAINTAINED
 RM_EMIF_EMIF_OCP_FW_CONTEXT 00000003 LOSTCONTEXT_RFF LOST LOSTCONTEXT_DFF LOST
 RM_EMIF_EMIF1_CONTEXT 00000003 LOSTCONTEXT_RFF LOST LOSTCONTEXT_DFF LOST
 RM_EMIF_EMIF2_CONTEXT 00000003 LOSTCONTEXT_RFF LOST LOSTCONTEXT_DFF LOST
 RM_EMIF_EMIF_DLL_CONTEXT 00000001 LOSTCONTEXT_DFF LOST
 RM_ATL_ATL_CONTEXT 00000000 LOSTMEM_ATL_BANK MAINTAINED LOSTCONTEXT_DFF MAINTAINED
 RM_L4CFG_L4_CFG_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED LOSTCONTEXT_DFF MAINTAINED
 RM_L4CFG_SPINLOCK_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX1_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_SAR_ROM_CONTEXT 00000001 LOSTCONTEXT_DFF LOST
 RM_L4CFG_OCP2SCP2_CONTEXT 00000001 LOSTCONTEXT_DFF LOST
 RM_L4CFG_MAILBOX2_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX3_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX4_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX5_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX6_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX7_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX8_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX9_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX10_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX11_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX12_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L4CFG_MAILBOX13_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
 RM_L3INSTR_L3_MAIN_2_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED LOSTCONTEXT_DFF MAINTAINED
 RM_L3INSTR_L3_INSTR_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED
 RM_L3INSTR_OCP_WP_NOC_CONTEXT 00000103 LOSTMEM_CORE_NRET_BANK LOST LOSTCONTEXT_RFF LOST LOSTCONTEXT_DFF LOST

EMU_PRM

PM_EMU_PWRSTCTRL 00030000 EMU_BANK_ONSTATE MEM_ON POWERSTATE OFF
PM_EMU_PWRSTST 00000000 LASTPOWERSTATEENTERED OFF INTRANSITION NO EMU_BANK_STATEST MEM_OFF
 LOGICSTATEST OFF **POWERSTATEST OFF**
RM_EMU_DEBUGSS_CONTEXT 00000101 LOSTMEM_EMU_BANK LOST LOSTCONTEXT_DFF LOST

CM_CORE_CKGEN

CM_CLKSEL_USB_60MHZ 00000001 CLKSEL SEL_DIV_8
 CM_CLKMODE_DPLL_PER 00000007 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
 DPLL_SSC_EN DISABLED DPLL_REGM4XEN DISABLED DPLL_LP_MODE_EN DISABLED

DPLL_RELOCK_RAMP_EN Disabled DPLL_DRIFTGUARD_EN DIASBLED DPLL_RAMP_RATE REFCLKX2
 DPLL_RAMP_LEVEL RAMP_DISABLE DPLL_EN DPLL_LOCK_MODE
 CM_IDLEST_DPLL_PER 0000001F ST_DPLL_INIT DPLL_INIT ST_DPLL_MODE RESERVED3 ST_DPLL_CLK DPLL_LOCKED
 CM_AUTOIDLE_DPLL_PER 00000001 AUTO_DPLL_MODE AUTO_LP_STOP
 CM_CLKSEL_DPLL_PER 00006004 DPLL_BYP_CLKSEL CLKINP DCC_EN DISABLED DPLL_MULT 0060
 DPLL_DIV 04
 CM_DIV_M2_DPLL_PER 00000804 CLKX2ST CLK_ENABLED CLKST CLK_GATED DIVHS 4
 CM_DIV_H11_DPLL_PER 00000003 CLKST CLK_GATED DIVHS 3
 CM_DIV_H12_DPLL_PER 00000004 CLKST CLK_GATED DIVHS 4
 CM_DIV_H13_DPLL_PER 0000000A CLKST CLK_GATED DIVHS 10
 CM_DIV_H14_DPLL_PER 00000002 CLKST CLK_GATED DIVHS 2
 CM_SSC_DELTAMSTEP_DPLL_PER 00000000 DELTAMSTEP 000000
 CM_SSC_MODFREQDIV_DPLL_PER 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00
 CM_CLKMODE_DPLL_USB 00000007 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
 DPLL_SSC_EN DISABLED DPLL_EN DPLL_LOCK_MODE
 CM_IDLEST_DPLL_USB 0000001F ST_DPLL_INIT DPLL_INIT ST_DPLL_MODE RESERVED7 ST_DPLL_CLK DPLL_LOCKED
 CM_AUTOIDLE_DPLL_USB 00000001 AUTO_DPLL_MODE AUTO_LP_STOP
 CM_CLKSEL_DPLL_USB 0401E009 DPLL_SD_DIV 04 DPLL_BYP_CLKSEL CLKINP DCC_EN DISABLED
 DPLL_SELFREQDQCO LS_CLK DPLL_MULT 01E0 DPLL_DIV 09
 CM_DIV_M2_DPLL_USB 00000202 CLKST CLK_ENABLED DIVHS 02
 CM_SSC_DELTAMSTEP_DPLL_USB 00000000 DELTAMSTEP 000000
 CM_SSC_MODFREQDIV_DPLL_USB 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00
 CM_CLKDCOLDO_DPLL_USB 00000200 ST_DPLL_CLKDCOLDO CLK_ENABLED
 CM_CLKMODE_DPLL_PCIE_REF 00000007 DPLL_SSC_TYPE TRIANGULAR DPLL_SSC_DOWNSPREAD FULL_SPREAD DPLL_SSC_ACK DISABLED
 DPLL_SSC_EN DISABLED DPLL_EN DPLL_LOCK_MODE
 CM_IDLEST_DPLL_PCIE_REF 0000001F ST_DPLL_INIT DPLL_INIT ST_DPLL_MODE RESERVED7 ST_DPLL_CLK DPLL_LOCKED
 CM_AUTOIDLE_DPLL_PCIE_REF 00000001 AUTO_DPLL_MODE AUTO_LP_STOP
 CM_CLKSEL_DPLL_PCIE_REF 04004B00 DPLL_SD_DIV 04 DPLL_BYP_CLKSEL 0 DCC_EN DISABLED
 DPLL_SELFREQDQCO LS_CLK DPLL_MULT 004B DPLL_DIV 00
 CM_DIV_M2_DPLL_PCIE_REF 0000040F CLKLDOST CLK_ENABLED CLKST CLK_GATED DIVHS 0F
 CM_SSC_DELTAMSTEP_DPLL_PCIE_REF 00000000 DELTAMSTEP 000000
 CM_SSC_MODFREQDIV_DPLL_PCIE_REF 00000000 MODFREQDIV_EXPONENT 0 MODFREQDIV_MANTISSA 00
 CM_CLKMODE_APLL_PCIE 00000101 CLKDIV_BYPASS PCIEDIVBY2_BYPASS_1 REFSEL CLKREF_ADPLL INPSEL 0
 MODE PCIE MODE_SELECT APLL_FORCE_LOCK_MODE
 CM_IDLEST_APLL_PCIE 00000001 ST_APLL_CLK APLL_LOCKED
 CM_DIV_M2_APLL_PCIE 00000000 CLKST CLK_GATED DIVHS 00
 CM_CLKVCO_LDO_APLL_PCIE 00000600 CLK_DIVST CLK_ENABLED CLKST CLK_ENABLED

WKUPAON_CM

CM_WKUPAON_CLKSTCTRL 0002D103 CLKACTIVITY_UART10_GFCLK INACT CLKACTIVITY_TIMER1_GFCLK ACT CLKACTIVITY_DCAN1_SYS_CLK INACT
 CLKACTIVITY_SYS_CLK_ALL ACT CLKACTIVITY_SYS_CLK_FUNC ACT CLKACTIVITY_WKUPAON_GICLK ACT
 CLKACTIVITY_WKUPAON_SYS_GFCLK INACT CLKACTIVITY_ABE_LP_CLK INACT CLKACTIVITY_SYS_CLK ACT
 CLKTRCTRL 3
 CM_WKUPAON_L4_WKUP_CLKCTRL 00000001 IDLEST FUNC MODULEMODE AUTO
 CM_WKUPAON_WD_TIMER2_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_WKUPAON_GPIO1_CLKCTRL 00030000 IDLEST DISABLE OPTFCLKEN_DBCLK FCLK_DIS MODULEMODE DISABLED
 CM_WKUPAON_TIMER1_CLKCTRL 01000002 CLKSEL SEL_SYS_CLK1_32K_CLK IDLEST FUNC MODULEMODE ENABLE
 CM_WKUPAON_TIMER12_CLKCTRL 00000001 IDLEST FUNC MODULEMODE AUTO
 CM_WKUPAON_COUNTER_32K_CLKCTRL 00000001 IDLEST FUNC MODULEMODE AUTO
 CM_WKUPAON_KBD_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_WKUPAON_UART10_CLKCTRL 00030000 CLKSEL SEL_FUNC_48M_CLK IDLEST DISABLE MODULEMODE DISABLED
 CM_WKUPAON_DCAN1_CLKCTRL 00030000 CLKSEL SEL_SYS_CLK1 IDLEST DISABLE MODULEMODE DISABLED

CM_CORE_AON_OCP_SOCKET

REVISION_CM_CORE_AON 40000301 SCHEME H08 FUNC 0000 R_RTL 0
 X_MAJOR OMAP5430 CUSTOM STANDARD Y_MINOR E52
 CM_CM_CORE_AON_PROFILING_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_CORE_AON_DEBUG_OUT 00000000 OUTPUT 00000000
 CM_CORE_AON_DEBUG_CFG0 00000000 SEL0 0000
 CM_CORE_AON_DEBUG_CFG1 00000000 SEL1 0000
 CM_CORE_AON_DEBUG_CFG2 00000000 SEL2 0000
 CM_CORE_AON_DEBUG_CFG3 00000000 SEL3 0000

MPU_PRM

PM_MPU_PWRSTCTRL 003C0605 MPU_RAM_ONSTATE MEM_ON MPU_L2_ONSTATE MEM_ON MPU_RAM_RETSTATE MEM_RET
 MPU_L2_RETSTATE MEM_RET LOWPOWERSTATECHANGE DIS LOGICRETSTATE LOGIC_RET
 POWERSTATE RET
 PM_MPU_PWRSTST 030003C7 LASTPOWERSTATEENTERED ON INTRANSITION NO MPU_RAM_STATEST MEM_ON
 MPU_L2_STATEST MEM_ON LOGICSTATEST ON POWERSTATEST ON
 RM_MPU_MPU_CONTEXT 00000000 LOSTMEM_MPU_RAM MAINTAINED LOSTMEM_MPU_L2 MAINTAINED LOSTCONTEXT_RFF MAINTAINED
 LOSTCONTEXT_DFF MAINTAINED

CM_CORE_IVA

CM_IVA_CLKSTCTRL 00000003 CLKACTIVITY_IVA_GCLK INACT CLKTRCTRL HW_AUTO
 CM_IVA_STATICDEP 00000020 L3MAIN1_STATDEP ENABLED EMIF_STATDEP DISABLED
 CM_IVA_DYNAMICDEP 00000000 L3MAIN1_DYNDEP DISABLED
 CM_IVA_IVA_CLKCTRL 00060001 STBYST STANDBY IDLEST IDLE MODULEMODE AUTO
 CM_IVA_SL2_CLKCTRL 00020001 IDLEST IDLE MODULEMODE AUTO

CM_CORE_AON_IPU

CM_IPU1_CLKSTCTRL 00000103 CLKACTIVITY_IPU1_GFCLK ACT CLKTRCTRL HW_AUTO
 CM_IPU1_STATICDEP 00000000 ATL_STATDEP DISABLED PCIE_STATDEP DISABLED VPE_STATDEP DISABLED
 L4PER3_STATDEP DISABLED L4PER2_STATDEP DISABLED GMAC_STATDEP DISABLED
 IPU_STATDEP DISABLED EVE2_STATDEP DISABLED EVE1_STATDEP DISABLED
 DSP2_STATDEP DISABLED CUSTEFUSE_STATDEP DISABLED COREAON_STATDEP DISABLED
 WKUPAON_STATDEP DISABLED L4SEC_STATDEP DISABLED L4PER_STATDEP DISABLED
 L4CFG_STATDEP DISABLED SDMA_STATDEP DISABLED GPU_STATDEP DISABLED
 CAM_STATDEP DISABLED DSS_STATDEP DISABLED L3INIT_STATDEP DISABLED
 L3MAIN1_STATDEP DISABLED EMIF_STATDEP DISABLED IVA_STATDEP DISABLED
 DSP1_STATDEP DISABLED IPU2_STATDEP DISABLED
 CM_IPU1_DYNAMICDEP 04000020 WINDOWSIZE 4 L3MAIN1_DYNDEP ENABLED
 CM_IPU1_IPU1_CLKCTRL 01000001 CLKSEL SEL_CORE_IPU_ISS_BOOST_CLK STBYST FUNC IDLEST FUNC
 MODULEMODE AUTO

CM_IPU_CLKSTCTRL 00001902 CLKACTIVITY_MCASP1_AHCLKR INACT CLKACTIVITY_MCASP1_AHCLKX INACT CLKACTIVITY_MCASP1_AUX_GFCLK INACT
 CLKACTIVITY_UART6_GFCLK INACT CLKACTIVITY_IPU_96M_GFCLK INACT CLKACTIVITY_TIMER8_GFCLK ACT
 CLKACTIVITY_TIMER7_GFCLK ACT CLKACTIVITY_TIMER6_GFCLK INACT CLKACTIVITY_TIMER5_GFCLK INACT
 CLKACTIVITY_IPU_L3_GICLK ACT CLKTRCTRL SW_WKUP

CM_IPU_MCASP1_CLKCTRL 00030000 CLKSEL_AHCLKR SEL_ABE_24M_GFCLK CLKSEL_AHCLKX SEL_ABE_24M_GFCLK CLKSEL_AUX_CLK SEL_PER_ABE_X1_GFCLK
 IDLEST DISABLE MODULEMODE DISABLED

CM_IPU_TIMER5_CLKCTRL 00030000 CLKSEL SEL_TIMER_SYS_CLK IDLEST DISABLE MODULEMODE DISABLED
 CM_IPU_TIMER6_CLKCTRL 00030000 CLKSEL SEL_TIMER_SYS_CLK IDLEST DISABLE MODULEMODE DISABLED
 CM_IPU_TIMER7_CLKCTRL 00000002 CLKSEL SEL_TIMER_SYS_CLK IDLEST FUNC MODULEMODE ENABLE
 CM_IPU_TIMER8_CLKCTRL 00000002 CLKSEL SEL_TIMER_SYS_CLK IDLEST FUNC MODULEMODE ENABLE
 CM_IPU_I2C5_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_IPU_UART6_CLKCTRL 00030000 CLKSEL SEL_FUNC_48M_CLK IDLEST DISABLE MODULEMODE DISABLED

RTC_PRM

PM_RTC_RTCCS_WKDEP 00000003 WKUPDEP_RTC_IRQ2_EVE2 DISABLED WKUPDEP_RTC_IRQ2_EVE1 DISABLED WKUPDEP_RTC_IRQ2_DSP2 DISABLED
 WKUPDEP_RTC_IRQ2_IPU1 DISABLED WKUPDEP_RTC_IRQ2_DSP1 DISABLED WKUPDEP_RTC_IRQ2_IPU2 DISABLED
 WKUPDEP_RTC_IRQ2_MPU DISABLED WKUPDEP_RTC_IRQ1_EVE2 DISABLED WKUPDEP_RTC_IRQ1_EVE1 DISABLED
 WKUPDEP_RTC_IRQ1_DSP2 DISABLED WKUPDEP_RTC_IRQ1_IPU1 DISABLED WKUPDEP_RTC_IRQ1_DSP1 DISABLED
 WKUPDEP_RTC_IRQ1_IPU2 ENABLED WKUPDEP_RTC_IRQ1_MPU ENABLED

RM_RTC_RTCCS_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED

CM_CORE_AON_DSP1

CM_DSP1_CLKSTCTRL 00000003 CLKACTIVITY_DSP1_GFCLK INACT CLKTRCTRL HW_AUTO <- SW_WAKE
 CM_DSP1_STATICDEP 00000020 ATL_STATDEP DISABLED PCIE_STATDEP DISABLED VPE_STATDEP DISABLED
 L4PER3_STATDEP DISABLED L4PER2_STATDEP DISABLED GMAC_STATDEP DISABLED
 IPU_STATDEP DISABLED IPU1_STATDEP DISABLED EVE2_STATDEP DISABLED
 EVE1_STATDEP DISABLED DSP2_STATDEP DISABLED CUSTEFUSE_STATDEP DISABLED
 COREAON_STATDEP DISABLED WKUPAON_STATDEP DISABLED L4SEC_STATDEP DISABLED
 L4PER_STATDEP DISABLED L4CFG_STATDEP DISABLED GPU_STATDEP DISABLED
 CAM_STATDEP DISABLED DSS_STATDEP DISABLED L3INIT_STATDEP DISABLED
 L3MAIN1_STATDEP ENABLED EMIF_STATDEP DISABLED IVA_STATDEP DISABLED
 IPU2_STATDEP DISABLED

CM_DSP1_DYNAMICDEP 04000020 WINDOWSIZE 4 L3MAIN1_DYNDEP ENABLED
 CM_DSP1_DSP1_CLKCTRL 00070000 STBYST STANDBY IDLEST DISABLE MODULEMODE DISABLED

CUSTEFUSE_PRM

PM_CUSTEFUSE_PWRSTCTRL 00000000 LOWPOWERSTATECHANGE DIS POWERSTATE OFF
 PM_CUSTEFUSE_PWRSTST 00000000 LASTPOWERSTATEENTERED OFF INTRANSITION NO LOGICSTATEST OFF
 POWERSTATEST OFF

RM_CUSTEFUSE_EFUSE_CTRL_CUST_CONTEXT 00000001 LOSTCONTEXT_DFF LOST

VPE_PRM

PM_VPE_PWRSTCTRL 00030104 VPE_BANK_ONSTATE MEM_ON VPE_BANK_RETSTATE MEM_RET LOWPOWERSTATECHANGE DIS
 LOGICRETSTATE LOGIC_RET POWERSTATE OFF

PM_VPE_PWRSTST 00000037 LASTPOWERSTATEENTERED OFF INTRANSITION NO VPE_BANK_STATEST MEM_ON
 LOGICSTATEST ON POWERSTATEST ON

PM_VPE_VPE_WKDEP 00000000 WKUPDEP_VPE_EVE2 DISABLED WKUPDEP_VPE_EVE1 DISABLED WKUPDEP_VPE_DSP2 DISABLED
 WKUPDEP_VPE_IPU1 DISABLED WKUPDEP_VPE_DSP1 DISABLED WKUPDEP_VPE_IPU2 DISABLED
 WKUPDEP_VPE_MPU DISABLED

RM_VPE_VPE_CONTEXT 00000000 LOSTMEM_VPE_BANK MAINTAINED LOSTCONTEXT_DFF MAINTAINED

CM_CORE_AON_DSP2

CM_DSP2_CLKSTCTRL 00000003 CLKACTIVITY_DSP2_GFCLK INACT CLKTRCTRL HW_AUTO
 CM_DSP2_STATICDEP 00000020 ATL_STATDEP DISABLED PCIE_STATDEP DISABLED VPE_STATDEP DISABLED
 L4PER3_STATDEP DISABLED L4PER2_STATDEP DISABLED GMAC_STATDEP DISABLED
 IPU_STATDEP DISABLED IPU1_STATDEP DISABLED EVE2_STATDEP DISABLED
 EVE1_STATDEP DISABLED CUSTEFUSE_STATDEP DISABLED COREAON_STATDEP DISABLED
 WKUPAON_STATDEP DISABLED L4SEC_STATDEP DISABLED L4PER_STATDEP DISABLED
 L4CFG_STATDEP DISABLED GPU_STATDEP DISABLED CAM_STATDEP DISABLED
 DSS_STATDEP DISABLED L3INIT_STATDEP DISABLED L3MAIN1_STATDEP ENABLED
 EMIF_STATDEP DISABLED IVA_STATDEP DISABLED DSP1_STATDEP DISABLED
 IPU2_STATDEP DISABLED

CM_DSP2_DYNAMICDEP 04000020 WINDOWSIZE 4 L3MAIN1_DYNDEP ENABLED
 CM_DSP2_DSP2_CLKCTRL 00070000 STBYST STANDBY IDLEST DISABLE MODULEMODE DISABLED

CM_CORE_COREAON

CM_COREAON_CLKSTCTRL 00001002 CLKACTIVITY_ABE_GICLK INACT CLKACTIVITY_SR_IVAHD_SYS_GFCLK INACT CLKACTIVITY_SR_DSPEVE_SYS_GFCLK INACT
 CLKACTIVITY_COREAON_32K_GFCLK ACT CLKACTIVITY_SR_CORE_SYS_GFCLK INACT CLKACTIVITY_SR_GPU_SYS_GFCLK INACT
 CLKACTIVITY_SR_MPU_SYS_GFCLK INACT CLKACTIVITY_COREAON_L4_GICLK INACT CLKTRCTRL SW_WKUP

CM_COREAON_SMARTREFLEX_MPU_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_COREAON_SMARTREFLEX_CORE_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_COREAON_USB_PHY1_CORE_CLKCTRL 00000100 OPTFCLKEN_CLK32K FCLK_EN
 CM_COREAON_SMARTREFLEX_GPU_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_COREAON_SMARTREFLEX_DSPEVE_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_COREAON_SMARTREFLEX_IVAHD_CLKCTRL 00030000 IDLEST DISABLE MODULEMODE DISABLED
 CM_COREAON_USB_PHY2_CORE_CLKCTRL 00000100 OPTFCLKEN_CLK32K FCLK_EN
 CM_COREAON_USB_PHY3_CORE_CLKCTRL 00000100 OPTFCLKEN_CLK32K FCLK_EN

L4PER_PRM

PM_L4PER_PWRSTCTRL 000F0107 NONRETAINED_BANK_ONSTATE MEM_ON RETAINED_BANK_ONSTATE MEM_ON NONRETAINED_BANK_RETSTATE MEM_OFF
 RETAINED_BANK_RETSTATE MEM_RET LOWPOWERSTATECHANGE DIS LOGICRETSTATE LOGIC_RET
 POWERSTATE ON

PM_L4PER_PWRSTST 000000F7 LASTPOWERSTATEENTERED OFF INTRANSITION NO NONRETAINED_BANK_STATEST MEM_ON
 RETAINED_BANK_STATEST MEM_ON LOGICSTATEST ON POWERSTATEST ON

RM_L4PER2_L4PER2_CONTEXT 00000003 LOSTCONTEXT_RFF LOST LOSTCONTEXT_DFF LOST
 RM_L4PER3_L4PER3_CONTEXT 00000003 LOSTCONTEXT_RFF LOST LOSTCONTEXT_DFF LOST

PM_L4PER_TIMER10_WKDEP 00000000 WKUPDEP_TIMER10_EVE2 DISABLED WKUPDEP_TIMER10_EVE1 DISABLED WKUPDEP_TIMER10_DSP2 DISABLED
 WKUPDEP_TIMER10_IPU1 DISABLED WKUPDEP_TIMER10_DSP1 DISABLED WKUPDEP_TIMER10_IPU2 DISABLED
 WKUPDEP_TIMER10_MPU DISABLED

RM_L4PER_TIMER10_CONTEXT 00000000 LOSTCONTEXT_DFF MAINTAINED

PM_L4PER_TIMER11_WKDEP 00000000 WKUPDEP_TIMER11_EVE2 DISABLED WKUPDEP_TIMER11_EVE1 DISABLED WKUPDEP_TIMER11_DSP2 DISABLED
 WKUPDEP_TIMER11_IPU1 DISABLED WKUPDEP_TIMER11_DSP1 DISABLED WKUPDEP_TIMER11_IPU2 DISABLED
 WKUPDEP_TIMER11_MPU DISABLED


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RM_L4SEC_DES3DES_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
RM_L4SEC_FPKA_CONTEXT 0000101 LOSTMEM_NONRETAINED_BANK LOST LOSTCONTEXT_DFF LOST
RM_L4SEC_RNG_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
RM_L4SEC_SHA2MD51_CONTEXT 00000000 LOSTCONTEXT_RFF MAINTAINED
PM_L4PER2_UART7_WKDEP 00000000 WKUPDEP_UART7_EVE1 DISABLED WKUPDEP_UART7_DSP2 DISABLED
WKUPDEP_UART7_IPU1 DISABLED WKUPDEP_UART7_SDMA DISABLED WKUPDEP_UART7_DSP1 DISABLED
WKUPDEP_UART7_IPU2 DISABLED WKUPDEP_UART7_MPU DISABLED
RM_L4PER2_UART7_CONTEXT 00000000 LOSTMEM_RETAINED_BANK MAINTAINED LOSTCONTEXT_RFF MAINTAINED
RM_L4SEC_DMA_CRYPT0_CONTEXT 0000102 LOSTMEM_RETAINED_BANK LOST LOSTCONTEXT_RFF LOST
PM_L4PER2_UART8_WKDEP 00000000 WKUPDEP_UART8_EVE2 DISABLED WKUPDEP_UART8_EVE1 DISABLED WKUPDEP_UART8_DSP2 DISABLED
WKUPDEP_UART8_IPU1 DISABLED WKUPDEP_UART8_SDMA DISABLED WKUPDEP_UART8_DSP1 DISABLED
WKUPDEP_UART8_IPU2 DISABLED WKUPDEP_UART8_MPU DISABLED
RM_L4PER2_UART8_CONTEXT 00000000 LOSTMEM_RETAINED_BANK MAINTAINED LOSTCONTEXT_RFF MAINTAINED
PM_L4PER2_UART9_WKDEP 00000000 WKUPDEP_UART9_EVE2 DISABLED WKUPDEP_UART9_EVE1 DISABLED WKUPDEP_UART9_DSP2 DISABLED
WKUPDEP_UART9_IPU1 DISABLED WKUPDEP_UART9_SDMA DISABLED WKUPDEP_UART9_DSP1 DISABLED
WKUPDEP_UART9_IPU2 DISABLED WKUPDEP_UART9_MPU DISABLED
RM_L4PER2_UART9_CONTEXT 00000000 LOSTMEM_RETAINED_BANK MAINTAINED LOSTCONTEXT_RFF MAINTAINED
PM_L4PER2_DCAN2_WKDEP 00000000 WKUPDEP_DCAN2_EVE2 DISABLED WKUPDEP_DCAN2_EVE1 DISABLED WKUPDEP_DCAN2_DSP2 DISABLED
WKUPDEP_DCAN2_IPU1 DISABLED WKUPDEP_DCAN2_SDMA DISABLED WKUPDEP_DCAN2_DSP1 DISABLED
WKUPDEP_DCAN2_IPU2 DISABLED WKUPDEP_DCAN2_MPU DISABLED
RM_L4PER2_DCAN2_CONTEXT 00000000 LOSTMEM_DCAN_BANK MAINTAINED LOSTCONTEXT_DFF MAINTAINED
RM_L4SEC_SHA2MD52_CONTEXT 00000002 LOSTCONTEXT_RFF LOST

```

```

CM_CORE_AON_RESTORE
CM_CLKSEL_CORE_RESTORE 00000110 RESTORE 00000110
CM_DIV_M2_DPLL_CORE_RESTORE 00000002 RESTORE 00000002
CM_DIV_H12_DPLL_CORE_RESTORE 00000204 RESTORE 00000204
CM_DIV_H13_DPLL_CORE_RESTORE 0000023E RESTORE 0000023E
CM_DIV_H14_DPLL_CORE_RESTORE 00000005 RESTORE 00000005
CM_DIV_H22_DPLL_CORE_RESTORE 00000205 RESTORE 00000205
CM_DIV_H23_DPLL_CORE_RESTORE 00000204 RESTORE 00000204
CM_DIV_H24_DPLL_CORE_RESTORE 00000006 RESTORE 00000006
CM_CLKSEL_DPLL_CORE_RESTORE 00010A04 RESTORE 00010A04
CM_SSC_DELTAMSTEP_DPLL_CORE_RESTORE 00000000 RESTORE 00000000
CM_SSC_MODFREQDIV_DPLL_CORE_RESTORE 00000000 RESTORE 00000000
CM_CLKMODE_DPLL_CORE_RESTORE 00000007 RESTORE 00000007
CM_SHADOW_FREQ_CONFIG2_RESTORE 00000004 RESTORE 00000004
CM_SHADOW_FREQ_CONFIG1_RESTORE 0005080C RESTORE 0005080C
CM_AUTOIDLE_DPLL_CORE_RESTORE 00000001 RESTORE 00000001
CM_MPU_CLKSTCTRL_RESTORE 00000103 RESTORE 00000103
CM_CM_CORE_AON_PROFILING_CLKCTRL_RESTORE 00030000 RESTORE 00030000
CM_DYN_DEP_PRESCAL_RESTORE 00000020 RESTORE 00000020

```

DEVICE_PRM

```

PRM_RSTCTRL 00000000 RST_GLOBAL_COLD_SW _OXO RST_GLOBAL_WARM_SW _OXO
PRM_RSTST 00000001 TSHUT_IVA_RST _OXO TSHUT_DSPEVE_RST _OXO TSHUT_CORE_RST _OXO
TSHUT_MM_RST _OXO TSHUT_MPU_RST _OXO ICEPICK_RST _OXO
EXTERNAL_WARM_RST _OXO MPU_WDT_RST _OXO GLOBAL_WARM_SW_RST _OXO
GLOBAL_COLD_RST _OX1
PRM_RSTTIME 000043FF RSTTIME2 16 RSTTIME1 03FF
PRM_CLKREQCTRL 00000000 CLKREQ_COND NEVER
PRM_PSCON_COUNT 00303017 HG_PONOUT_2_PGOODIN_TIME 30 PONOUT_2_PGOODIN_TIME 30 PCHARGE_TIME 17
PRM_IO_COUNT 0000003A ISO_2_ON_TIME 3A
PRM_IO_PMCCTRL 00010020 GLOBAL_WUEN ENABLED WUCLK_STATUS 0 WUCLK_CTRL LOW
IO_ON_STATUS HIGH ISOOVR_EXTEND NOOVERRIDE ISOCLK_STATUS 0
ISOCLK_OVERRIDE NOOVERRIDE
PRM_SRAM_COUNT 78000017 STARTUP_COUNT 78 SLP_CNT_VALUE 00 VSETUPCNT_VALUE 00
PCHARGE_CNT_VALUE 23
PRM_SLDO_CORE_SETUP 00000006 AIPOFF NO_OVERRIDE ENFUNC5 ONE_STEP ENFUNC4 EXT_CLOCK
ENFUNC3 SUB_REGUL_DISABLED ENFUNC2 EXT_CAP ENFUNC1 SHORT_PROT_DISABLED
ABBOFF_SLEEP SRAMNW_SLP_VDDAR ABBOFF_ACT SRAMNW_ACT_VDDAR ENABLE_RTA RTA_DISABLED
PRM_SLDO_CORE_CTRL 00000000 SRAM_IN_TRANSITION IDLE SRAMLDO_STATUS ACTIVE RETMODE_ENABLE DISABLED
PRM_SLDO_MPU_SETUP 00000006 AIPOFF NO_OVERRIDE ENFUNC5 ONE_STEP ENFUNC4 EXT_CLOCK
ENFUNC3 SUB_REGUL_DISABLED ENFUNC2 EXT_CAP ENFUNC1 SHORT_PROT_DISABLED
ABBOFF_SLEEP SRAMNW_SLP_VDDAR ABBOFF_ACT SRAMNW_ACT_VDDAR ENABLE_RTA RTA_DISABLED
PRM_SLDO_MPU_CTRL 00000000 SRAM_IN_TRANSITION IDLE SRAMLDO_STATUS ACTIVE RETMODE_ENABLE DISABLED
PRM_SLDO_GPU_SETUP 00000006 AIPOFF NO_OVERRIDE ENFUNC5 ONE_STEP ENFUNC4 EXT_CLOCK
ENFUNC3 SUB_REGUL_DISABLED ENFUNC2 EXT_CAP ENFUNC1 SHORT_PROT_DISABLED
ABBOFF_SLEEP SRAMNW_SLP_VDDAR ABBOFF_ACT SRAMNW_ACT_VDDAR ENABLE_RTA RTA_DISABLED
PRM_SLDO_GPU_CTRL 00000000 SRAM_IN_TRANSITION IDLE SRAMLDO_STATUS ACTIVE RETMODE_ENABLE DISABLED
PRM_ABBLDO_MPU_SETUP 00003F05 SR2_WTCNT_VALUE 3F NOCAP CAP ACTIVE_FBB_SEL FBB
SR2EN FUNCTIONAL
PRM_ABBLDO_MPU_CTRL 00000011 SR2_IN_TRANSITION IDLE SR2_STATUS FBB OPP_CHANGE 0
OPP_SEL FASTOPP
PRM_ABBLDO_GPU_SETUP 00003F05 SR2_WTCNT_VALUE 3F NOCAP CAP ACTIVE_FBB_SEL FBB
SR2EN FUNCTIONAL
PRM_ABBLDO_GPU_CTRL 00000011 SR2_IN_TRANSITION IDLE SR2_STATUS FBB OPP_CHANGE 0
OPP_SEL FASTOPP
PRM_BANDGAP_SETUP 00000078 STARTUP_COUNT 78
PRM_DEVICE_OFF_CTRL 00000000 EMIF2_OFFWKUP_DISABLE ENABLED EMIF1_OFFWKUP_DISABLE ENABLED DEVICE_OFF_ENABLE DISABLED
PRM_PHASE1_CNDP 4A05E000 PHASE1_CNDP 4A05E000
PRM_PHASE2A_CNDP 4A05E030 PHASE2A_CNDP 4A05E030
PRM_PHASE2B_CNDP 4A05E060 PHASE2B_CNDP 4A05E060
PRM_MODEM_IF_CTRL 00000000 MODEM_SHUTDOWN_IRQ INACTIVE MODEM_WAKE_IRQ INACTIVE
PRM_SLDO_DSPEVE_SETUP 00000006 AIPOFF NO_OVERRIDE ENFUNC5 ONE_STEP ENFUNC4 EXT_CLOCK
ENFUNC3 SUB_REGUL_DISABLED ENFUNC2 EXT_CAP ENFUNC1 SHORT_PROT_DISABLED
ABBOFF_SLEEP SRAMNW_SLP_VDDAR ABBOFF_ACT SRAMNW_ACT_VDDAR ENABLE_RTA RTA_DISABLED
PRM_SLDO_IVA_SETUP 00000006 AIPOFF NO_OVERRIDE ENFUNC5 ONE_STEP ENFUNC4 EXT_CLOCK
ENFUNC3 SUB_REGUL_DISABLED ENFUNC2 EXT_CAP ENFUNC1 SHORT_PROT_DISABLED
ABBOFF_SLEEP SRAMNW_SLP_VDDAR ABBOFF_ACT SRAMNW_ACT_VDDAR ENABLE_RTA RTA_DISABLED
PRM_ABBLDO_DSPEVE_CTRL 00000011 SR2_IN_TRANSITION IDLE SR2_STATUS FBB OPP_CHANGE 0
OPP_SEL FASTOPP
PRM_ABBLDO_IVA_CTRL 00000011 SR2_IN_TRANSITION IDLE SR2_STATUS FBB OPP_CHANGE 0

```

```

OPP_SEL FASTOPP
PRM_SLDO_DSPEVE_CTRL 00000000 SRAM_IN_TRANSITION IDLE SRAMLDO_STATUS ACTIVE RETMODE_ENABLE DISABLED
PRM_SLDO_IVA_CTRL 00000000 SRAM_IN_TRANSITION IDLE SRAMLDO_STATUS ACTIVE RETMODE_ENABLE DISABLED
PRM_ABBLDO_DSPEVE_SETUP 00003F05 SR2_WTCNT_VALUE 3F NOCAP CAP ACTIVE_FBB_SEL FBB
SR2EN FUNCTIONAL
PRM_ABBLDO_IVA_SETUP 00003F05 SR2_WTCNT_VALUE 3F NOCAP CAP ACTIVE_FBB_SEL FBB
SR2EN FUNCTIONAL

CM_CORE_GPU
CM_GPU_CLKSTCTRL 00000003 CLKACTIVITY_GPU_HYD_GCLK INACT CLKACTIVITY_GPU_CORE_GCLK INACT CLKACTIVITY_GPU_L3_GICK INACT
CLKTRCTRL HW_AUTO
CM_GPU_STATICDEP 00000020 L3MAIN1_STATDEP ENABLED EMIF_STATDEP DISABLED IVA_STATDEP DISABLED
CM_GPU_DYNAMICDEP 00000000 L3MAIN1_DYNDEP DISABLED
CM_GPU_GPU_CLKCTRL 0A070000 CLKSEL_HYD_CLK SEL_GPU_GCLK CLKSEL_CORE_CLK SEL_GPU_GCLK STBYST STANDBY
IDLEST DISABLE MODULEMODE DISABLED

```

Dual_Cortex_A15_MPU_Subsystem

```

MPU_PRCM_OCP_SOCKET
REVISION_PRCM_MPU 00000000 REVISION 00000000

```

```

MPU_PRCM_CM_C0
CM_CPU0_CLKSTCTRL 00000000 CLKTRCTRL NO_SLEEP
CM_CPU0_CPU0_CLKCTRL 00000000 STBYST FUNC

```

```

MPU_PRCM_CM_C1
CM_CPU1_CLKSTCTRL 00000000 CLKTRCTRL NO_SLEEP
CM_CPU1_CPU1_CLKCTRL 00000000 STBYST FUNC

```

```

MPU_AXI2OCP_MISC
MA_PRIORITY 00000000 HIMEM_INTERLEAVE_UN 0 PRIORITY 0

```

```

MPU_PRCM_PRM_C0
PM_CPU0_PWRSTCTRL 00030107 L1_BANK_ONSTATE MEM_ON L1_BANK_RETSTATE MEM_RET LOGICRETSTATE LOGIC_RET
POWERSTATE ON
PM_CPU0_PWRSTST 03000037 LASTPOWERSTATEENTERED ON INTRANSITION NO L1_BANK_STATEST MEM_ON
LOGICSTATEST ON POWERSTATEST ON
RM_CPU0_CPU0_RSTCTRL 00000000 RST CLEAR
RM_CPU0_CPU0_RSTST 00000000 DBGRST_REQ_RSTST CLEAR RSTST CLEAR
RM_CPU0_CPU0_CONTEXT 00000101 LOSTMEM_CPU_L1 LOST LOSTCONTEXT_DFF LOST

```

```

MPU_PRCM_PRM_C1
PM_CPU1_PWRSTCTRL 00030107 L1_BANK_ONSTATE MEM_ON L1_BANK_RETSTATE MEM_RET FORCED_OFF OFF_NOT_FORCED
LOGICRETSTATE LOGIC_RET POWERSTATE ON
PM_CPU1_PWRSTST 03000037 LASTPOWERSTATEENTERED ON INTRANSITION NO L1_BANK_STATEST MEM_ON
LOGICSTATEST ON POWERSTATEST ON
RM_CPU1_CPU1_RSTCTRL 00000000 RST CLEAR
RM_CPU1_CPU1_RSTST 00000000 DBGRST_REQ_RSTST CLEAR RSTST CLEAR
RM_CPU1_CPU1_CONTEXT 00000101 LOSTMEM_CPU_L1 LOST LOSTCONTEXT_DFF LOST

```

```

MPU_WUGEN
WKG_CONTROL_0 00000000 DOMAINRESET 0 MPU_WARM_RESET 0 MPU_COLD_RESET 0
EVENTO 0 STANDBYWFE 0 STANDBYWFI 0
WKG_ENB_A_0 00000000 WKG_ENB_FOR_INTR31 0 WKG_ENB_FOR_INTR30 0 WKG_ENB_FOR_INTR29 0
WKG_ENB_FOR_INTR28 0 WKG_ENB_FOR_INTR27 0 WKG_ENB_FOR_INTR26 0
WKG_ENB_FOR_INTR25 0 WKG_ENB_FOR_INTR24 0 WKG_ENB_FOR_INTR23 0
WKG_ENB_FOR_INTR22 0 WKG_ENB_FOR_INTR21 0 WKG_ENB_FOR_INTR20 0
WKG_ENB_FOR_INTR19 0 WKG_ENB_FOR_INTR18 0 WKG_ENB_FOR_INTR17 0
WKG_ENB_FOR_INTR16 0 WKG_ENB_FOR_INTR15 0 WKG_ENB_FOR_INTR14 0
WKG_ENB_FOR_INTR13 0 WKG_ENB_FOR_INTR12 0 WKG_ENB_FOR_INTR11 0
WKG_ENB_FOR_INTR10 0 WKG_ENB_FOR_INTR9 0 WKG_ENB_FOR_INTR8 0
WKG_ENB_FOR_INTR7 0 WKG_ENB_FOR_INTR6 0 WKG_ENB_FOR_INTR5 0
WKG_ENB_FOR_INTR4 0 WKG_ENB_FOR_INTR3 0 WKG_ENB_FOR_INTR2 0
WKG_ENB_FOR_INTR1 0 WKG_ENB_FOR_INTR0 0
WKG_ENB_B_0 00000000 WKG_ENB_FOR_INTR63 0 WKG_ENB_FOR_INTR62 0 WKG_ENB_FOR_INTR61 0
WKG_ENB_FOR_INTR60 0 WKG_ENB_FOR_INTR59 0 WKG_ENB_FOR_INTR58 0
WKG_ENB_FOR_INTR57 0 WKG_ENB_FOR_INTR56 0 WKG_ENB_FOR_INTR55 0
WKG_ENB_FOR_INTR54 0 WKG_ENB_FOR_INTR53 0 WKG_ENB_FOR_INTR52 0
WKG_ENB_FOR_INTR51 0 WKG_ENB_FOR_INTR50 0 WKG_ENB_FOR_INTR49 0
WKG_ENB_FOR_INTR48 0 WKG_ENB_FOR_INTR47 0 WKG_ENB_FOR_INTR46 0
WKG_ENB_FOR_INTR45 0 WKG_ENB_FOR_INTR44 0 WKG_ENB_FOR_INTR43 0
WKG_ENB_FOR_INTR42 0 WKG_ENB_FOR_INTR41 0 WKG_ENB_FOR_INTR40 0
WKG_ENB_FOR_INTR39 0 WKG_ENB_FOR_INTR38 0 WKG_ENB_FOR_INTR37 0
WKG_ENB_FOR_INTR36 0 WKG_ENB_FOR_INTR35 0 WKG_ENB_FOR_INTR34 0
WKG_ENB_FOR_INTR33 0 WKG_ENB_FOR_INTR32 0
WKG_ENB_C_0 00000000 WKG_ENB_FOR_INTR95 0 WKG_ENB_FOR_INTR94 0 WKG_ENB_FOR_INTR93 0
WKG_ENB_FOR_INTR92 0 WKG_ENB_FOR_INTR91 0 WKG_ENB_FOR_INTR90 0
WKG_ENB_FOR_INTR89 0 WKG_ENB_FOR_INTR88 0 WKG_ENB_FOR_INTR87 0
WKG_ENB_FOR_INTR86 0 WKG_ENB_FOR_INTR85 0 WKG_ENB_FOR_INTR84 0
WKG_ENB_FOR_INTR83 0 WKG_ENB_FOR_INTR82 0 WKG_ENB_FOR_INTR81 0
WKG_ENB_FOR_INTR80 0 WKG_ENB_FOR_INTR79 0 WKG_ENB_FOR_INTR78 0
WKG_ENB_FOR_INTR77 0 WKG_ENB_FOR_INTR76 0 WKG_ENB_FOR_INTR75 0
WKG_ENB_FOR_INTR74 0 WKG_ENB_FOR_INTR73 0 WKG_ENB_FOR_INTR72 0
WKG_ENB_FOR_INTR71 0 WKG_ENB_FOR_INTR70 0 WKG_ENB_FOR_INTR69 0
WKG_ENB_FOR_INTR68 0 WKG_ENB_FOR_INTR67 0 WKG_ENB_FOR_INTR66 0
WKG_ENB_FOR_INTR65 0 WKG_ENB_FOR_INTR64 0
WKG_ENB_D_0 00000000 WKG_ENB_FOR_INTR127 0 WKG_ENB_FOR_INTR126 0 WKG_ENB_FOR_INTR125 0
WKG_ENB_FOR_INTR124 0 WKG_ENB_FOR_INTR123 0 WKG_ENB_FOR_INTR122 0
WKG_ENB_FOR_INTR121 0 WKG_ENB_FOR_INTR120 0 WKG_ENB_FOR_INTR119 0
WKG_ENB_FOR_INTR118 0 WKG_ENB_FOR_INTR117 0 WKG_ENB_FOR_INTR116 0
WKG_ENB_FOR_INTR115 0 WKG_ENB_FOR_INTR114 0 WKG_ENB_FOR_INTR113 0
WKG_ENB_FOR_INTR112 0 WKG_ENB_FOR_INTR111 0 WKG_ENB_FOR_INTR110 0
WKG_ENB_FOR_INTR109 0 WKG_ENB_FOR_INTR108 0 WKG_ENB_FOR_INTR107 0

```

```

WKG_ENB_FOR_INTR106 0   WKG_ENB_FOR_INTR105 0 WKG_ENB_FOR_INTR104 0
WKG_ENB_FOR_INTR103 0   WKG_ENB_FOR_INTR102 0 WKG_ENB_FOR_INTR101 0
WKG_ENB_FOR_INTR100 0   WKG_ENB_FOR_INTR99 0  WKG_ENB_FOR_INTR98 0
WKG_ENB_FOR_INTR97 0    WKG_ENB_FOR_INTR96 0
WKG_ENB_E_0 00000000 WKG_ENB_FOR_INTR159 0 WKG_ENB_FOR_INTR158 0 WKG_ENB_FOR_INTR157 0
WKG_ENB_FOR_INTR156 0   WKG_ENB_FOR_INTR155 0 WKG_ENB_FOR_INTR154 0
WKG_ENB_FOR_INTR153 0   WKG_ENB_FOR_INTR152 0 WKG_ENB_FOR_INTR151 0
WKG_ENB_FOR_INTR150 0   WKG_ENB_FOR_INTR149 0 WKG_ENB_FOR_INTR148 0
WKG_ENB_FOR_INTR147 0   WKG_ENB_FOR_INTR146 0 WKG_ENB_FOR_INTR145 0
WKG_ENB_FOR_INTR144 0   WKG_ENB_FOR_INTR143 0 WKG_ENB_FOR_INTR142 0
WKG_ENB_FOR_INTR141 0   WKG_ENB_FOR_INTR140 0 WKG_ENB_FOR_INTR139 0
WKG_ENB_FOR_INTR138 0   WKG_ENB_FOR_INTR137 0 WKG_ENB_FOR_INTR136 0
WKG_ENB_FOR_INTR135 0   WKG_ENB_FOR_INTR134 0 WKG_ENB_FOR_INTR133 0
WKG_ENB_FOR_INTR132 0   WKG_ENB_FOR_INTR131 0 WKG_ENB_FOR_INTR130 0
WKG_ENB_FOR_INTR129 0   WKG_ENB_FOR_INTR128 0
WKG_CONTROL_1 00000000 DOMAINRESET 0 MPU_WARM_RESET 0 MPU_COLD_RESET 0
EVENTO 0 STANDBYWFE 0 STANDBYWFI 0
WKG_ENB_A_1 00000000 WKG_ENB_FOR_INTR31 0 WKG_ENB_FOR_INTR30 0 WKG_ENB_FOR_INTR29 0
WKG_ENB_FOR_INTR28 0   WKG_ENB_FOR_INTR27 0 WKG_ENB_FOR_INTR26 0
WKG_ENB_FOR_INTR25 0   WKG_ENB_FOR_INTR24 0 WKG_ENB_FOR_INTR23 0
WKG_ENB_FOR_INTR22 0   WKG_ENB_FOR_INTR21 0 WKG_ENB_FOR_INTR20 0
WKG_ENB_FOR_INTR19 0   WKG_ENB_FOR_INTR18 0 WKG_ENB_FOR_INTR17 0
WKG_ENB_FOR_INTR16 0   WKG_ENB_FOR_INTR15 0 WKG_ENB_FOR_INTR14 0
WKG_ENB_FOR_INTR13 0   WKG_ENB_FOR_INTR12 0 WKG_ENB_FOR_INTR11 0
WKG_ENB_FOR_INTR10 0   WKG_ENB_FOR_INTR9 0  WKG_ENB_FOR_INTR8 0
WKG_ENB_FOR_INTR7 0    WKG_ENB_FOR_INTR6 0  WKG_ENB_FOR_INTR5 0
WKG_ENB_FOR_INTR4 0    WKG_ENB_FOR_INTR3 0  WKG_ENB_FOR_INTR2 0
WKG_ENB_FOR_INTR1 0    WKG_ENB_FOR_INTR0 0
WKG_ENB_B_1 00000000 WKG_ENB_FOR_INTR63 0 WKG_ENB_FOR_INTR62 0 WKG_ENB_FOR_INTR61 0
WKG_ENB_FOR_INTR60 0   WKG_ENB_FOR_INTR59 0 WKG_ENB_FOR_INTR58 0
WKG_ENB_FOR_INTR57 0   WKG_ENB_FOR_INTR56 0 WKG_ENB_FOR_INTR55 0
WKG_ENB_FOR_INTR54 0   WKG_ENB_FOR_INTR53 0 WKG_ENB_FOR_INTR52 0
WKG_ENB_FOR_INTR51 0   WKG_ENB_FOR_INTR50 0 WKG_ENB_FOR_INTR49 0
WKG_ENB_FOR_INTR48 0   WKG_ENB_FOR_INTR47 0 WKG_ENB_FOR_INTR46 0
WKG_ENB_FOR_INTR45 0   WKG_ENB_FOR_INTR44 0 WKG_ENB_FOR_INTR43 0
WKG_ENB_FOR_INTR42 0   WKG_ENB_FOR_INTR41 0 WKG_ENB_FOR_INTR40 0
WKG_ENB_FOR_INTR39 0   WKG_ENB_FOR_INTR38 0 WKG_ENB_FOR_INTR37 0
WKG_ENB_FOR_INTR36 0   WKG_ENB_FOR_INTR35 0 WKG_ENB_FOR_INTR34 0
WKG_ENB_FOR_INTR33 0   WKG_ENB_FOR_INTR32 0
WKG_ENB_C_1 00000000 WKG_ENB_FOR_INTR95 0 WKG_ENB_FOR_INTR94 0 WKG_ENB_FOR_INTR93 0
WKG_ENB_FOR_INTR92 0   WKG_ENB_FOR_INTR91 0 WKG_ENB_FOR_INTR90 0
WKG_ENB_FOR_INTR89 0   WKG_ENB_FOR_INTR88 0 WKG_ENB_FOR_INTR87 0
WKG_ENB_FOR_INTR86 0   WKG_ENB_FOR_INTR85 0 WKG_ENB_FOR_INTR84 0
WKG_ENB_FOR_INTR83 0   WKG_ENB_FOR_INTR82 0 WKG_ENB_FOR_INTR81 0
WKG_ENB_FOR_INTR80 0   WKG_ENB_FOR_INTR79 0 WKG_ENB_FOR_INTR78 0
WKG_ENB_FOR_INTR77 0   WKG_ENB_FOR_INTR76 0 WKG_ENB_FOR_INTR75 0
WKG_ENB_FOR_INTR74 0   WKG_ENB_FOR_INTR73 0 WKG_ENB_FOR_INTR72 0
WKG_ENB_FOR_INTR71 0   WKG_ENB_FOR_INTR70 0 WKG_ENB_FOR_INTR69 0
WKG_ENB_FOR_INTR68 0   WKG_ENB_FOR_INTR67 0 WKG_ENB_FOR_INTR66 0
WKG_ENB_FOR_INTR65 0   WKG_ENB_FOR_INTR64 0
WKG_ENB_D_1 00000000 WKG_ENB_FOR_INTR127 0 WKG_ENB_FOR_INTR126 0 WKG_ENB_FOR_INTR125 0
WKG_ENB_FOR_INTR124 0   WKG_ENB_FOR_INTR123 0 WKG_ENB_FOR_INTR122 0
WKG_ENB_FOR_INTR121 0   WKG_ENB_FOR_INTR120 0 WKG_ENB_FOR_INTR119 0
WKG_ENB_FOR_INTR118 0   WKG_ENB_FOR_INTR117 0 WKG_ENB_FOR_INTR116 0
WKG_ENB_FOR_INTR115 0   WKG_ENB_FOR_INTR114 0 WKG_ENB_FOR_INTR113 0
WKG_ENB_FOR_INTR112 0   WKG_ENB_FOR_INTR111 0 WKG_ENB_FOR_INTR110 0
WKG_ENB_FOR_INTR109 0   WKG_ENB_FOR_INTR108 0 WKG_ENB_FOR_INTR107 0
WKG_ENB_FOR_INTR106 0   WKG_ENB_FOR_INTR105 0 WKG_ENB_FOR_INTR104 0
WKG_ENB_FOR_INTR103 0   WKG_ENB_FOR_INTR102 0 WKG_ENB_FOR_INTR101 0
WKG_ENB_FOR_INTR100 0   WKG_ENB_FOR_INTR99 0  WKG_ENB_FOR_INTR98 0
WKG_ENB_FOR_INTR97 0   WKG_ENB_FOR_INTR96 0
WKG_ENB_E_1 00000000 WKG_ENB_FOR_INTR159 0 WKG_ENB_FOR_INTR158 0 WKG_ENB_FOR_INTR157 0
WKG_ENB_FOR_INTR156 0   WKG_ENB_FOR_INTR155 0 WKG_ENB_FOR_INTR154 0
WKG_ENB_FOR_INTR153 0   WKG_ENB_FOR_INTR152 0 WKG_ENB_FOR_INTR151 0
WKG_ENB_FOR_INTR150 0   WKG_ENB_FOR_INTR149 0 WKG_ENB_FOR_INTR148 0
WKG_ENB_FOR_INTR147 0   WKG_ENB_FOR_INTR146 0 WKG_ENB_FOR_INTR145 0
WKG_ENB_FOR_INTR144 0   WKG_ENB_FOR_INTR143 0 WKG_ENB_FOR_INTR142 0
WKG_ENB_FOR_INTR141 0   WKG_ENB_FOR_INTR140 0 WKG_ENB_FOR_INTR139 0
WKG_ENB_FOR_INTR138 0   WKG_ENB_FOR_INTR137 0 WKG_ENB_FOR_INTR136 0
WKG_ENB_FOR_INTR135 0   WKG_ENB_FOR_INTR134 0 WKG_ENB_FOR_INTR133 0
WKG_ENB_FOR_INTR132 0   WKG_ENB_FOR_INTR131 0 WKG_ENB_FOR_INTR130 0
WKG_ENB_FOR_INTR129 0   WKG_ENB_FOR_INTR128 0
AUX_CORE_BOOT_0 00000000 AUX_CORE_BOOT_0 00000000
AUX_CORE_BOOT_1 00000000 AUX_CORE_BOOT_1 00000000
STM_HWEVENTS_INV 00000000 STM_HWEVENT_INV_31 0 STM_HWEVENT_INV_30 0 STM_HWEVENT_INV_29 0
STM_HWEVENT_INV_28 0   STM_HWEVENT_INV_27 0 STM_HWEVENT_INV_26 0
STM_HWEVENT_INV_25 0   STM_HWEVENT_INV_24 0 STM_HWEVENT_INV_23 0
STM_HWEVENT_INV_22 0   STM_HWEVENT_INV_21 0 STM_HWEVENT_INV_20 0
STM_HWEVENT_INV_19 0   STM_HWEVENT_INV_18 0 STM_HWEVENT_INV_17 0
STM_HWEVENT_INV_16 0   STM_HWEVENT_INV_15 0 STM_HWEVENT_INV_14 0
STM_HWEVENT_INV_13 0   STM_HWEVENT_INV_12 0 STM_HWEVENT_INV_11 0
STM_HWEVENT_INV_10 0   STM_HWEVENT_INV_9 0  STM_HWEVENT_INV_8 0
STM_HWEVENT_INV_7 0    STM_HWEVENT_INV_6 0  STM_HWEVENT_INV_5 0
STM_HWEVENT_INV_4 0    STM_HWEVENT_INV_3 0  STM_HWEVENT_INV_2 0
STM_HWEVENT_INV_1 0    STM_HWEVENT_INV_0 0
AMBA_IF_MODE 00000000 ES2_PM_MODE 0 APB_FENCE_EN 0 BI 0
BO 0 BCM 0 SBD 0
TIMESTAMPCYCLE0 00000000 COUNTER_31_0 00000000
TIMESTAMPCYCLEHI 00000000 COUNTER_47_32 0000
MPU_WD_TIMER
REG_Bundle_0

```

```

WDT_CONTROL_REGISTER_i_0 00000000 WARNEN 0 MPUSSRSTEN 0 INTREN 0
ENABLE 0
WDT_COUNT_REGISTER_i_0 00000000 CURRENTCOUNT 00000000
WDT_LOAD_REGISTER_i_0 00000000 NEWCOUNT 00000000
WDT_PRESCALER_REGISTER_i_0 00000000 PRESCALER 0000
WDT_RESET_STATUS_REGISTER_i_0 00000000 WARN 0 TO 0
WDT_WARNING_REGISTER_i_0 00000000 WARNING_WATERMARK 00000000

```

REG_Bundle_1

```

WDT_CONTROL_REGISTER_i_1 00000000 WARNEN 0 MPUSSRSTEN 0 INTREN 0
ENABLE 0
WDT_COUNT_REGISTER_i_1 00000000 CURRENTCOUNT 00000000
WDT_LOAD_REGISTER_i_1 00000000 NEWCOUNT 00000000
WDT_PRESCALER_REGISTER_i_1 00000000 PRESCALER 0000
WDT_RESET_STATUS_REGISTER_i_1 00000000 WARN 0 TO 0
WDT_WARNING_REGISTER_i_1 00000000 WARNING_WATERMARK 00000000

```

MPU_PRCM_DEVICE

```

PRM_RSTST 00000000 GLOBAL_WARM_RST _0x0 GLOBAL_COLD_RST _0x0
PRM_PSCON_COUNT 00000000 HG_RAMPUP SLOW HG_EN HG_DISABLE HG_PONOUT_2_PGDODDIN_TIME 00
PCHARGE_TIME 00
PRM_FRAC_INCREMENTER_NUMERATOR 00000000 ABE_LP_MODE_NUMERATOR 0000 SYS_MODE_NUMERATOR 0000
PRM_FRAC_INCREMENTER_DENOMINATOR_RELOAD 00000000 RELOAD 0 DENOMINATOR 0000

```

DSP_Subsystem

DSP_SYSTEM

```

DSP_SYSTEM
DSP_SYS_REVISION 00000000 REVISION 00000000
DSP_SYS_HWINFO 00000000 INFO 00000000 NUM 0
DSP_SYS_SYSCONFIG 00000000 DSP_IDLREQ NOREQ STANDBYMODE 0 IDLEMODE 0
DSP_SYS_STAT 00000000 OCPI_DISC_STAT 0 TC1_STAT IDLE TCO_STAT IDLE
C6GX_STAT IDLE
DSP_SYS_DISC_CONFIG 00000000 OCPI_DISC No_effect.
DSP_SYS_BUS_CONFIG 00000000 SDMA_PRI 0 NOPOSTOVERRIDE MIX SDMA_L2PRES 0
CFG_L2PRES 0 TC1_L2PRES 0 TCO_L2PRES 0
TC1_DBS 0 TCO_DBS 0
DSP_SYS_MMU_CONFIG 00000000 MMU1_ABORT NOABORT MMU0_ABORT NOABORT MMU1_EN DISABLED
MMU0_EN DISABLED
DSP_SYS_IRQWAKEEN0 00000000 ENABLE 00000000
DSP_SYS_IRQWAKEEN1 00000000 ENABLE 00000000
DSP_SYS_DMAWAKEEN0 00000000 ENABLE 00000000
DSP_SYS_DMAWAKEEN1 00000000 ENABLE 00000000
DSP_SYS_EVTOUT_SET 00000000 EVENT 00000000
DSP_SYS_EVTOUT_CLR 00000000 EVENT 00000000
DSP_SYS_ERRINT_IRQSTATUS_RAW 00000000 EVENT 000000
DSP_SYS_ERRINT_IRQSTATUS 00000000 EVENT 000000
DSP_SYS_ERRINT_IRQENABLE_SET 00000000 ENABLE 000000
DSP_SYS_ERRINT_IRQENABLE_CLR 00000000 ENABLE 000000
DSP_SYS_EDMAWAKE0_IRQSTATUS_RAW 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE0_IRQSTATUS 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE0_IRQENABLE_SET 00000000 ENABLE 00000000
DSP_SYS_EDMAWAKE0_IRQENABLE_CLR 00000000 ENABLE 00000000
DSP_SYS_EDMAWAKE1_IRQSTATUS_RAW 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE1_IRQSTATUS 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE1_IRQENABLE_SET 00000000 ENABLE 00000000
DSP_SYS_EDMAWAKE1_IRQENABLE_CLR 00000000 ENABLE 00000000
DSP_SYS_HW_DBGOUT_SEL 00000000 GROUP 0
DSP_SYS_HW_DBGOUT_VAL 00000000 VALUE 00000000

```

DSP1_SYSTEM

```

DSP1_SYSTEM
DSP_SYS_REVISION 00000000 REVISION 00000000
DSP_SYS_HWINFO 00000000 INFO 00000000 NUM 0
DSP_SYS_SYSCONFIG 00000000 DSP_IDLREQ NOREQ STANDBYMODE 0 IDLEMODE 0
DSP_SYS_STAT 00000000 OCPI_DISC_STAT 0 TC1_STAT IDLE TCO_STAT IDLE
C6GX_STAT IDLE
DSP_SYS_DISC_CONFIG 00000000 OCPI_DISC No_effect.
DSP_SYS_BUS_CONFIG 00000000 SDMA_PRI 0 NOPOSTOVERRIDE MIX SDMA_L2PRES 0
CFG_L2PRES 0 TC1_L2PRES 0 TCO_L2PRES 0
TC1_DBS 0 TCO_DBS 0
DSP_SYS_MMU_CONFIG 00000000 MMU1_ABORT NOABORT MMU0_ABORT NOABORT MMU1_EN DISABLED
MMU0_EN DISABLED
DSP_SYS_IRQWAKEEN0 00000000 ENABLE 00000000
DSP_SYS_IRQWAKEEN1 00000000 ENABLE 00000000
DSP_SYS_DMAWAKEEN0 00000000 ENABLE 00000000
DSP_SYS_DMAWAKEEN1 00000000 ENABLE 00000000
DSP_SYS_EVTOUT_SET 00000000 EVENT 00000000
DSP_SYS_EVTOUT_CLR 00000000 EVENT 00000000
DSP_SYS_ERRINT_IRQSTATUS_RAW 00000000 EVENT 000000
DSP_SYS_ERRINT_IRQSTATUS 00000000 EVENT 000000
DSP_SYS_ERRINT_IRQENABLE_SET 00000000 ENABLE 000000
DSP_SYS_ERRINT_IRQENABLE_CLR 00000000 ENABLE 000000
DSP_SYS_EDMAWAKE0_IRQSTATUS_RAW 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE0_IRQSTATUS 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE0_IRQENABLE_SET 00000000 ENABLE 00000000
DSP_SYS_EDMAWAKE0_IRQENABLE_CLR 00000000 ENABLE 00000000
DSP_SYS_EDMAWAKE1_IRQSTATUS_RAW 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE1_IRQSTATUS 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE1_IRQENABLE_SET 00000000 ENABLE 00000000
DSP_SYS_EDMAWAKE1_IRQENABLE_CLR 00000000 ENABLE 00000000
DSP_SYS_HW_DBGOUT_SEL 00000000 GROUP 0
DSP_SYS_HW_DBGOUT_VAL 00000000 VALUE 00000000

```

DSP2_SYSTEM

DSP_SYS_REVISION 00000000 REVISION 00000000
DSP_SYS_HWINFO 00000000 INFO 00000000 NUM 0
DSP_SYS_SYSCONFIG 00000000 DSP_IDLREQ NOREQ STANDBYMODE 0 IDLEMODE 0
DSP_SYS_STAT 00000000 OCP1_DISC_STAT 0 TC1_STAT IDLE TCO_STAT IDLE
C66X_STAT IDLE
DSP_SYS_DISC_CONFIG 00000000 OCP1_DISC No_effect.
DSP_SYS_BUS_CONFIG 00000000 SDMA_PRI 0 NOPOSTOVERRIDE MIX SDMA_L2PRES 0
CFG_L2PRES 0 TC1_L2PRES 0 TCO_L2PRES 0
TC1_DBS 0 TCO_DBS 0
DSP_SYS_MMU_CONFIG 00000000 MMU1_ABORT NOABORT MMU0_ABORT NOABORT MMU1_EN DISABLED
MMU0_EN DISABLED
DSP_SYS_IRQWAKEEN0 00000000 ENABLE 00000000
DSP_SYS_IRQWAKEEN1 00000000 ENABLE 00000000
DSP_SYS_DMAWAKEEN0 00000000 ENABLE 00000000
DSP_SYS_DMAWAKEEN1 00000000 ENABLE 00000000
DSP_SYS_EVTOUT_SET 00000000 EVENT 00000000
DSP_SYS_EVTOUT_CLR 00000000 EVENT 00000000
DSP_SYS_ERRINT_IRQSTATUS_RAW 00000000 EVENT 00000000
DSP_SYS_ERRINT_IRQSTATUS 00000000 EVENT 00000000
DSP_SYS_ERRINT_IRQENABLE_SET 00000000 ENABLE 00000000
DSP_SYS_ERRINT_IRQENABLE_CLR 00000000 ENABLE 00000000
DSP_SYS_EDMAWAKE0_IRQSTATUS_RAW 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE0_IRQSTATUS 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE0_IRQENABLE_SET 00000000 ENABLE 00000000
DSP_SYS_EDMAWAKE0_IRQENABLE_CLR 00000000 ENABLE 00000000
DSP_SYS_EDMAWAKE1_IRQSTATUS_RAW 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE1_IRQSTATUS 00000000 EVENT 00000000
DSP_SYS_EDMAWAKE1_IRQENABLE_SET 00000000 ENABLE 00000000
DSP_SYS_EDMAWAKE1_IRQENABLE_CLR 00000000 ENABLE 00000000
DSP_SYS_HW_DBGOUT_SEL 00000000 GROUP 0
DSP_SYS_HW_DBGOUT_VAL 00000000 VALUE 00000000

DSP_FW_L2_NOC_CFG

DSP_FW_L2_NOC_CFG

L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_ERROR_LOG_0 00000000 BLK_BURST_VIOLATION 0 REGION_START_ERRLOG 0 REGION_END_ERRLOG 0
REQINFO_ERRLOG 0000
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_LOGICAL_ADDR_ERRLOG_0 00000000 SLVOFS_LOGICAL 00000000
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_REGUPDATE_CONTROL 00000000 FW_LOAD_REQ 0 FW_UPDATE_REQ 0
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_LOW_0 00000000 PUB_PRIV_DEBUG 0 PUB_USR_DEBUG 0 PUB_PRIV_READ 0
PUB_PRIV_WRITE 0 PUB_PRIV_EXE 0 PUB_USR_READ 0
PUB_USR_WRITE 0 PUB_USR_EXE 0
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_HIGH_0 00000000 W15 0 R15 0 W14 0
R14 0 W13 0 R13 0
W12 0 R12 0 W11 0
R11 0 W10 0 R10 0
W9 0 R9 0 W8 0
R8 0 W7 0 R7 0
W6 0 R6 0 W5 0
R5 0 W4 0 R4 0
W3 0 R3 0 W2 0
R2 0 W1 0 R1 0
W0 0 R0 0
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_START_REGION_1 00000000 START_REGION_1 0
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_END_REGION_1 00000000 END_REGION_1_ENABLE 0 END_REGION_1 0
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_LOW_1 00000000 PUB_PRIV_DEBUG 0 PUB_USR_DEBUG 0 PUB_PRIV_READ 0
PUB_PRIV_WRITE 0 PUB_PRIV_EXE 0 PUB_USR_READ 0
PUB_USR_WRITE 0 PUB_USR_EXE 0
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_HIGH_1 00000000 W15 0 R15 0 W14 0
R14 0 W13 0 R13 0
W12 0 R12 0 W11 0
R11 0 W10 0 R10 0
W9 0 R9 0 W8 0
R8 0 W7 0 R7 0
W6 0 R6 0 W5 0
R5 0 W4 0 R4 0
W3 0 R3 0 W2 0
R2 0 W1 0 R1 0
W0 0 R0 0
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_ERROR_LOG_0 00000000 BLK_BURST_VIOLATION 0 REGION_START_ERRLOG 0 REGION_END_ERRLOG 0
REQINFO_ERRLOG 0000
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_LOGICAL_ADDR_ERRLOG_0 00000000 SLVOFS_LOGICAL 00000000
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_REGUPDATE_CONTROL 00000000 FW_LOAD_REQ 0 FW_UPDATE_REQ 0
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_MRM_PERMISSION_REGION_LOW_0 00000000 PUB_PRIV_DEBUG 0 PUB_USR_DEBUG 0 PUB_PRIV_READ 0
PUB_PRIV_WRITE 0 PUB_PRIV_EXE 0 PUB_USR_READ 0
PUB_USR_WRITE 0 PUB_USR_EXE 0
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_MRM_PERMISSION_REGION_HIGH_0 00000000 W15 0 R15 0 W14 0
R14 0 W13 0 R13 0
W12 0 R12 0 W11 0
R11 0 W10 0 R10 0
W9 0 R9 0 W8 0
R8 0 W7 0 R7 0
W6 0 R6 0 W5 0
R5 0 W4 0 R4 0
W3 0 R3 0 W2 0
R2 0 W1 0 R1 0
W0 0 R0 0
DSPNOC_FLAGMUX_ID_COREID 00000000 CORECHECKSUM 000000 CORETYPEID 00
DSPNOC_FLAGMUX_ID_REVISION 00000000 REVISION 00000000
DSPNOC_FLAGMUX_FAULTEN 00000000 FAULTEN 0
DSPNOC_FLAGMUX_FAULTSTATUS 00000000 FAULTSTATUS 0

```

DSPNOC_FLAGMUX_FLAGINENO          00000000 FLAGINENO          0
DSPNOC_FLAGMUX_FLAGINSTAUSO        00000000 FLAGINSTAUSO        0
DSPNOC_ERRORLOG_ID_COREID           00000000 CORECHECKSUM    000000    CORETYPEID    00
DSPNOC_ERRORLOG_ID_REVISIONID       00000000 REVISION          00000000
DSPNOC_ERRORLOG_FAULTEN             00000000 FAULTEN          0
DSPNOC_ERRORLOG_ERRVLD              00000000 ERRVLD          0
DSPNOC_ERRORLOG_ERRCLR              00000000 ERRCLR          0
DSPNOC_ERRORLOG_ERRLOGO             00000000 FORMAT          0    LEN1          0000    ERRCODE    0
OPC                                  0    LOCK          0
DSPNOC_ERRORLOG_ERRLOG1              00000000 ERRLOG1         0000
DSPNOC_ERRORLOG_ERRLOG3              00000000 ERRLOG3         00000000
DSPNOC_ERRORLOG_ERRLOG5              00000000 ERRLOG5         000000

```

DSP1_FW_L2_NOC_CFG

```

L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_ERROR_LOG_0          00000000 BLK_BURST_VIOLATION 0    REGION_START_ERRLOG 0    REGION_END_ERRLOG 0
REQINFO_ERRLOG    0000
L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_LOGICAL_ADDR_ERRLOG_0    00000000 SLVOFS_LOGICAL    00000000
L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_REGUPDATE_CONTROL    00000000 FW_LOAD_REQ    0    FW_UPDATE_REQ    0
L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_LOW_0    00000000 PUB_PRV_DEBUG    0    PUB_USR_DEBUG    0    PUB_PRV_READ    0
PUB_PRV_WRITE    0    PUB_PRV_EXE    0    PUB_USR_READ    0
PUB_USR_WRITE    0    PUB_USR_EXE    0
L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_HIGH_0    00000000 W15          0    R15          0    W14          0
R14    0    W13          0    R13          0
W12    0    R12          0    W11          0
R11    0    W10          0    R10          0
W9     0    R9           0    W8           0
R8     0    W7           0    R7           0
W6     0    R6           0    W5           0
R5     0    W4           0    R4           0
W3     0    R3           0    W2           0
R2     0    W1           0    R1           0
W0     0    R0           0

```

```

L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_START_REGION_1    00000000 START_REGION_1    0
L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_END_REGION_1    00000000 END_REGION_1_ENABLE 0    END_REGION_1    0
L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_LOW_1    00000000 PUB_PRV_DEBUG    0    PUB_USR_DEBUG    0    PUB_PRV_READ    0
PUB_PRV_WRITE    0    PUB_PRV_EXE    0    PUB_USR_READ    0
PUB_USR_WRITE    0    PUB_USR_EXE    0
L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_HIGH_1    00000000 W15          0    R15          0    W14          0
R14    0    W13          0    R13          0
W12    0    R12          0    W11          0
R11    0    W10          0    R10          0
W9     0    R9           0    W8           0
R8     0    W7           0    R7           0
W6     0    R6           0    W5           0
R5     0    W4           0    R4           0
W3     0    R3           0    W2           0
R2     0    W1           0    R1           0
W0     0    R0           0

```

```

L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_ERROR_LOG_0          00000000 BLK_BURST_VIOLATION 0    REGION_START_ERRLOG 0    REGION_END_ERRLOG 0
REQINFO_ERRLOG    0000
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_LOGICAL_ADDR_ERRLOG_0    00000000 SLVOFS_LOGICAL    00000000
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_REGUPDATE_CONTROL    00000000 FW_LOAD_REQ    0    FW_UPDATE_REQ    0
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_MRM_PERMISSION_REGION_LOW_0    00000000 PUB_PRV_DEBUG    0    PUB_USR_DEBUG    0    PUB_PRV_READ    0
PUB_PRV_WRITE    0    PUB_PRV_EXE    0    PUB_USR_READ    0
PUB_USR_WRITE    0    PUB_USR_EXE    0
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_MRM_PERMISSION_REGION_HIGH_0    00000000 W15          0    R15          0    W14          0
R14    0    W13          0    R13          0
W12    0    R12          0    W11          0
R11    0    W10          0    R10          0
W9     0    R9           0    W8           0
R8     0    W7           0    R7           0
W6     0    R6           0    W5           0
R5     0    W4           0    R4           0
W3     0    R3           0    W2           0
R2     0    W1           0    R1           0
W0     0    R0           0

```

```

DSPNOC_FLAGMUX_ID_COREID           00000000 CORECHECKSUM    000000    CORETYPEID    00
DSPNOC_FLAGMUX_ID_REVISIONID       00000000 REVISION          00000000
DSPNOC_FLAGMUX_FAULTEN             00000000 FAULTEN          0
DSPNOC_FLAGMUX_FAULTSTATUS         00000000 FAULTSTATUS      0
DSPNOC_FLAGMUX_FLAGINENO          00000000 FLAGINENO          0
DSPNOC_FLAGMUX_FLAGINSTAUSO        00000000 FLAGINSTAUSO        0
DSPNOC_ERRORLOG_ID_COREID           00000000 CORECHECKSUM    000000    CORETYPEID    00
DSPNOC_ERRORLOG_ID_REVISIONID       00000000 REVISION          00000000
DSPNOC_ERRORLOG_FAULTEN             00000000 FAULTEN          0
DSPNOC_ERRORLOG_ERRVLD              00000000 ERRVLD          0
DSPNOC_ERRORLOG_ERRCLR              00000000 ERRCLR          0
DSPNOC_ERRORLOG_ERRLOGO             00000000 FORMAT          0    LEN1          0000    ERRCODE    0
OPC                                  0    LOCK          0
DSPNOC_ERRORLOG_ERRLOG1              00000000 ERRLOG1         0000
DSPNOC_ERRORLOG_ERRLOG3              00000000 ERRLOG3         00000000
DSPNOC_ERRORLOG_ERRLOG5              00000000 ERRLOG5         000000

```

DSP2_FW_L2_NOC_CFG

```

L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_ERROR_LOG_0          00000000 BLK_BURST_VIOLATION 0    REGION_START_ERRLOG 0    REGION_END_ERRLOG 0
REQINFO_ERRLOG    0000
L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_LOGICAL_ADDR_ERRLOG_0    00000000 SLVOFS_LOGICAL    00000000
L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_REGUPDATE_CONTROL    00000000 FW_LOAD_REQ    0    FW_UPDATE_REQ    0
L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_LOW_0    00000000 PUB_PRV_DEBUG    0    PUB_USR_DEBUG    0    PUB_PRV_READ    0
PUB_PRV_WRITE    0    PUB_PRV_EXE    0    PUB_USR_READ    0
PUB_USR_WRITE    0    PUB_USR_EXE    0
L3_DSPSS_INIT_OCP_MMUO_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_HIGH_0    00000000 W15          0    R15          0    W14          0
R14    0    W13          0    R13          0

```

W12	0	R12	0	W11	0
R11	0	W10	0	R10	0
W9	0	R9	0	W8	0
R8	0	W7	0	R7	0
W6	0	R6	0	W5	0
R5	0	W4	0	R4	0
W3	0	R3	0	W2	0
R2	0	W1	0	R1	0
W0	0	R0	0		
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_START_REGION_1			00000000	START_REGION_1	0
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_END_REGION_1			00000000	END_REGION_1_ENABLE	0
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_LOW_1			00000000	PUB_PRV_DEBUG	0
				PUB_USR_DEBUG	0
				PUB_PRV_READ	0
				PUB_USR_READ	0
				PUB_USR_WRITE	0
				PUB_USR_EXE	0
L3_DSPSS_INIT_OCP_MMU0_CTRL_TARG_OCP_FW_503000_MRM_PERMISSION_REGION_HIGH_1			00000000	W15	0
				R15	0
				W14	0
R14	0	W13	0	R13	0
W12	0	R12	0	W11	0
R11	0	W10	0	R10	0
W9	0	R9	0	W8	0
R8	0	W7	0	R7	0
W6	0	R6	0	W5	0
R5	0	W4	0	R4	0
W3	0	R3	0	W2	0
R2	0	W1	0	R1	0
W0	0	R0	0		
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_ERROR_LOG_0			00000000	BLK_BURST_VIOLATION	0
				REGION_START_ERRLOG	0
				REGION_END_ERRLOG	0
				REQINFO_ERRLOG	0000
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_LOGICAL_ADDR_ERRLOG_0			00000000	SLVOFS_LOGICAL	00000000
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_REGUPDATE_CONTROL			00000000	FW_LOAD_REQ	0
				FW_UPDATE_REQ	0
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_MRM_PERMISSION_REGION_LOW_0			00000000	PUB_PRV_DEBUG	0
				PUB_USR_DEBUG	0
				PUB_PRV_READ	0
				PUB_USR_READ	0
				PUB_USR_WRITE	0
				PUB_USR_EXE	0
L3_DSPSS_INIT_OCP_MMU1_CTRL_TARG_OCP_FW_504000_MRM_PERMISSION_REGION_HIGH_0			00000000	W15	0
				R15	0
				W14	0
R14	0	W13	0	R13	0
W12	0	R12	0	W11	0
R11	0	W10	0	R10	0
W9	0	R9	0	W8	0
R8	0	W7	0	R7	0
W6	0	R6	0	W5	0
R5	0	W4	0	R4	0
W3	0	R3	0	W2	0
R2	0	W1	0	R1	0
W0	0	R0	0		
DSPNOC_FLAGMUX_ID_COREID			00000000	CORECHECKSUM	000000
				CORETYPEID	00
DSPNOC_FLAGMUX_ID_REVISIONID			00000000	REVISION	00000000
DSPNOC_FLAGMUX_FAULTEN			00000000	FAULTEN	0
DSPNOC_FLAGMUX_FAULTSTATUS			00000000	FAULTSTATUS	0
DSPNOC_FLAGMUX_FLAGINENO			00000000	FLAGINENO	0
DSPNOC_FLAGMUX_FLAGINSTATUS0			00000000	FLAGINSTATUS0	0
DSPNOC_ERRORLOG_ID_COREID			00000000	CORECHECKSUM	000000
				CORETYPEID	00
DSPNOC_ERRORLOG_ID_REVISIONID			00000000	REVISION	00000000
DSPNOC_ERRORLOG_FAULTEN			00000000	FAULTEN	0
DSPNOC_ERRORLOG_ERRVLD			00000000	ERRVLD	0
DSPNOC_ERRORLOG_ERRCLR			00000000	ERRCLR	0
DSPNOC_ERRORLOG_ERRLOG0			00000000	FORMAT	0
				LEN1	0000
				ERRCODE	0
OPC			0	LOCK	0
DSPNOC_ERRORLOG_ERRLOG1			00000000	ERRLOG1	0000
DSPNOC_ERRORLOG_ERRLOG3			00000000	ERRLOG3	00000000
DSPNOC_ERRORLOG_ERRLOG5			00000000	ERRLOG5	000000

IVA_Overview

IVA_Video_Direct_Memory_Access

IVA_Synchronization_Box

IVA_Load_and_Store_Engine

IVA_Motion_Estimation

IVA_Intra_Prediction_Estimation

IVA_Loop_Filter

IVA_Motion_Compensation

IVA_CALCulation_Engine_3

IVA_Entropy_Coder_Decoder

VIP

VPE

Display_Subsystem_Overview

Display_Controller

GPU

BB2D_Overview

L3_MAIN_Interconnect

L4_Interconnects
Dynamic_Memory_Manager
EMIF_Controller
General_Purpose_Memory_Controller
Error_Location_Module
On_Chip_Memory_OCM_Subsystem
System_DMA
Enhanced_DMA
Control_Module
Mailbox
MMU
Spinlock
General_Purpose_Timers
Watchdog_Timers
_32_kHz_Synchronized_Timer
RTC
Multimaster_High_Speed_I2C_Controller
HDQ_1_Wire
UART_IrDA_CIR
Multichannel_Serial_Peripheral_Interface
Quad_Serial_Peripheral_Interface
Multichannel_Audio_Serial_Ports
SuperSpeed_USB_DRD
SATA_Controller
PCIe_Controllers
DCAN
Gigabit_Ethernet_Switch_GMAC_SW
Media_Local_Bus_MLB
eMMC_SD_SDIO
SATA_PHY_Subsystem
USB3_PHY_Subsystem
PCIe_Shared_PHY_Subsystem
General_Purpose_Interface
Keyboard_Controller
PWM_Subsystem_Resources
VCP_Overview
ATL
Embedded_Vision_Engine_EVE_Subsystem
VCOP_CPU_and_Instruction_Set